ECE 651 Project Presentation

Custom IC Design Utilizing Silicon Ensemble, ProGenesis, and Full Custom Layout

Robert Greenwell

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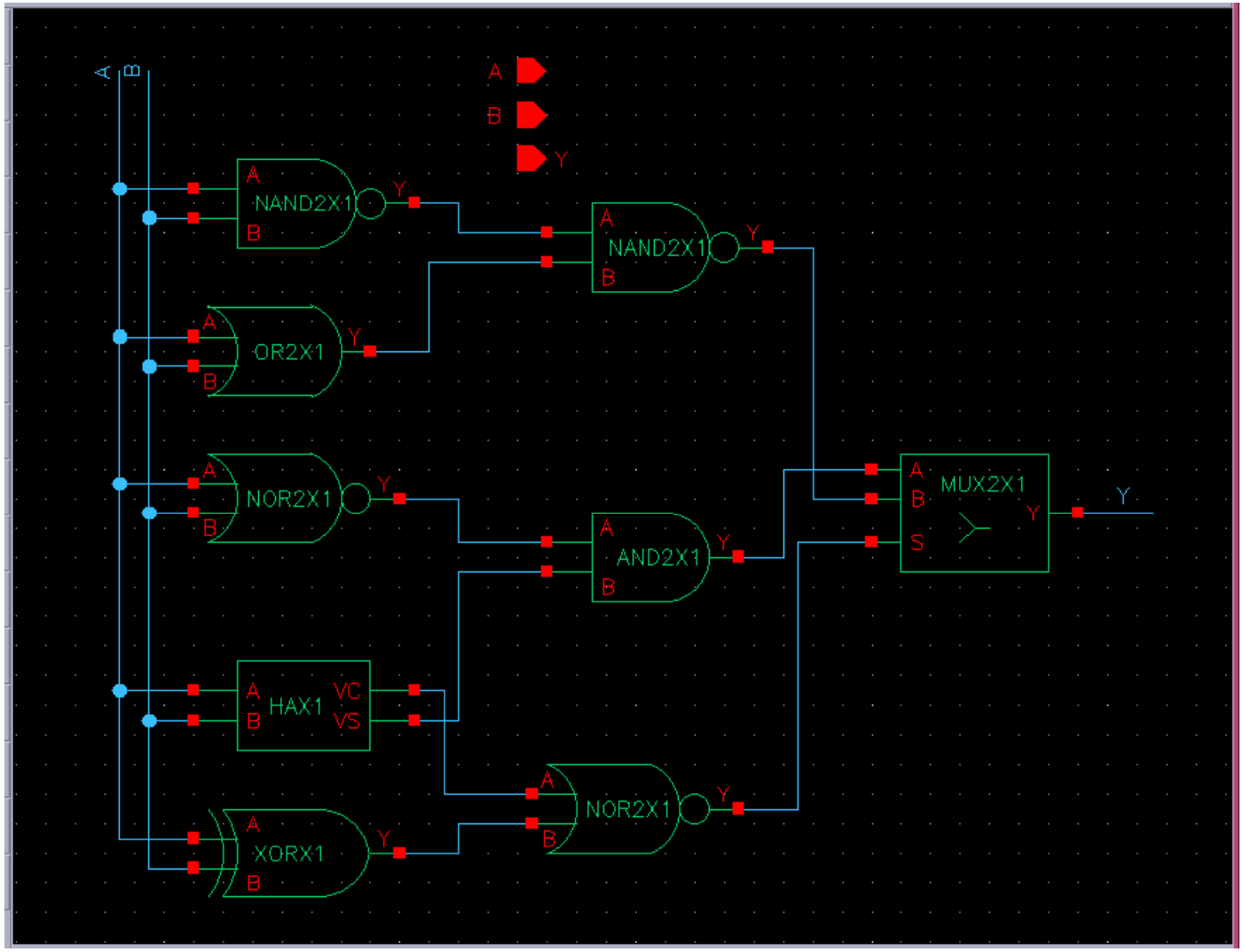
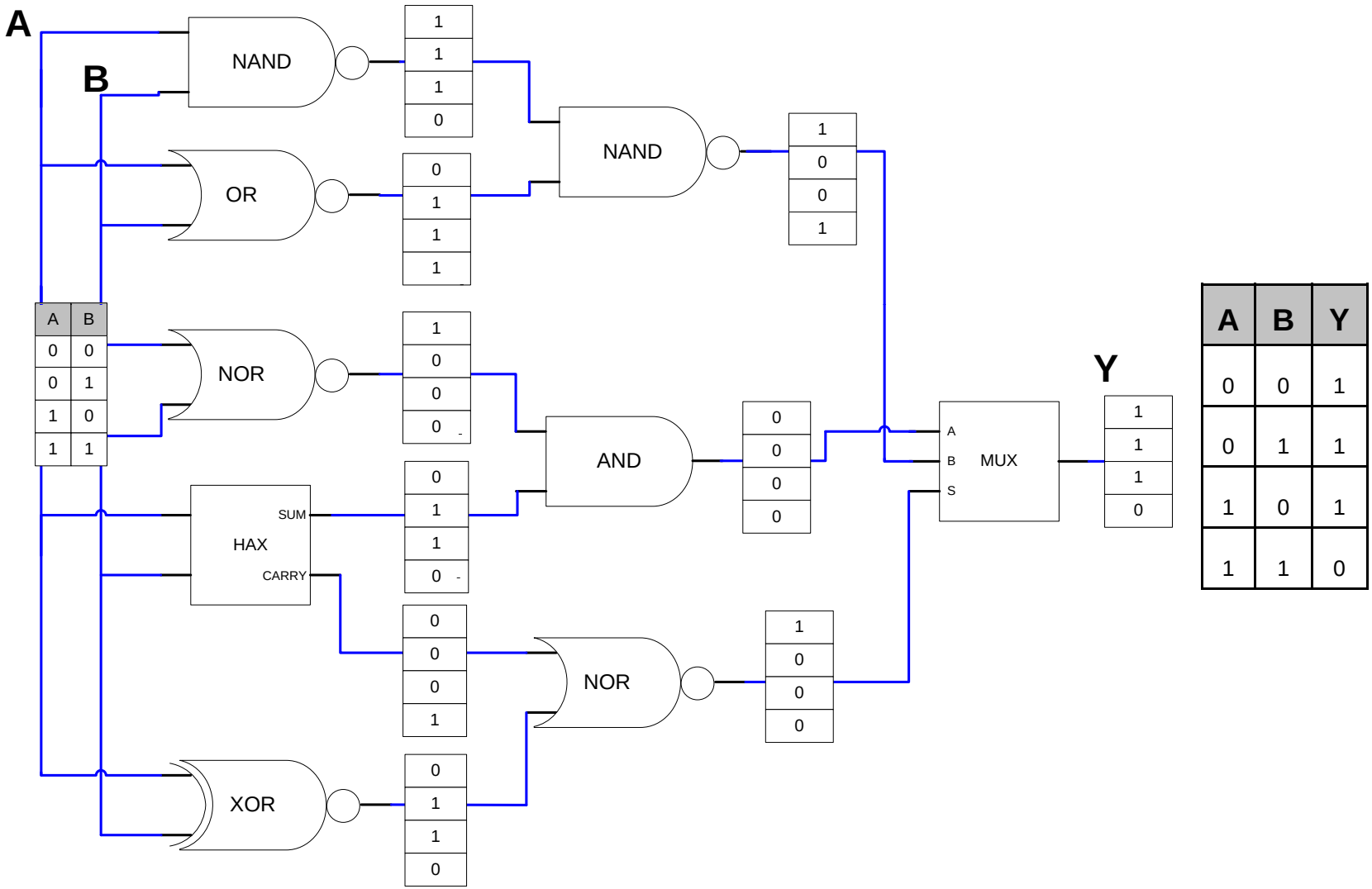
Schematic



GATE	Count
AND2	1
NAND2	2
OR2	1
XOR2	1
NOR2	2
HAX	1
MUX2	1

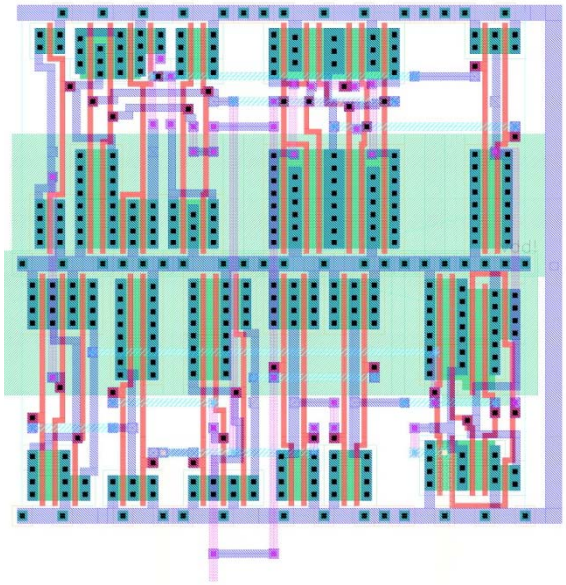
Truth Table



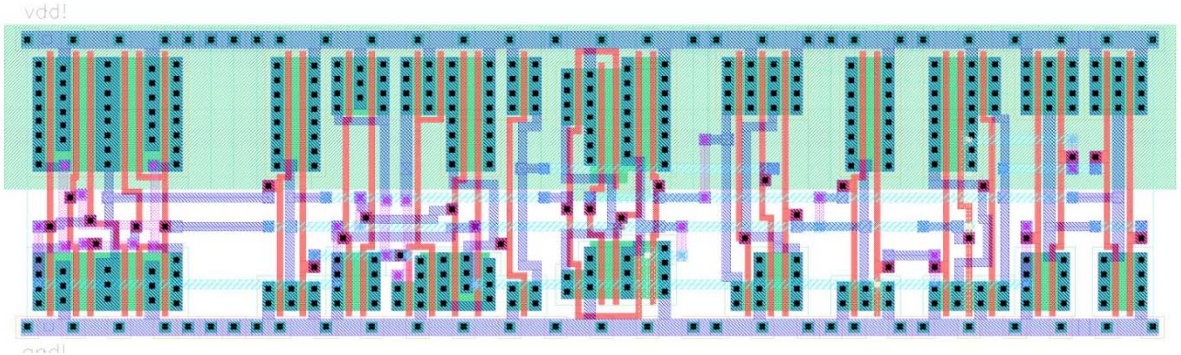
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Silicon Ensemble

- Using Silicon Ensemble two layouts were generated
  - A two-row layout (40 µm x 40 µm)
  - A single-row layout (20 µm x 78.4 µm)



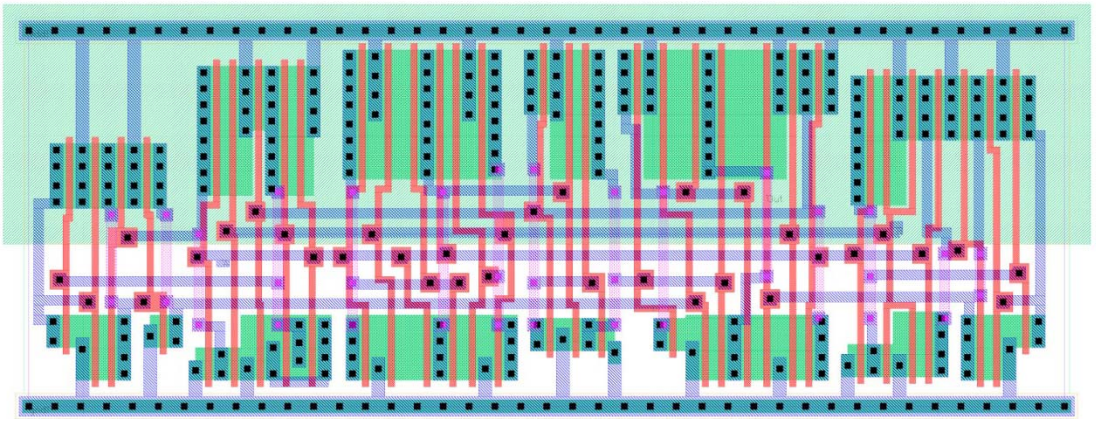
Dual-Row Layout



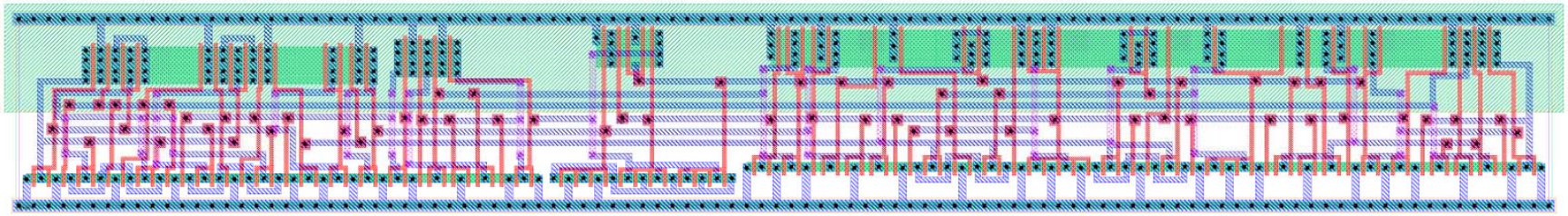
Single-Row Layout

ProGenesis

- Using ProGenesis two layouts were generated
  - An unfolded layout (23.2 µm x 64 µm)
  - A folded layout (20 µm x 164.8 µm)
- Note that ProGenesis folds *every* transistor, causing a substantial increase in area



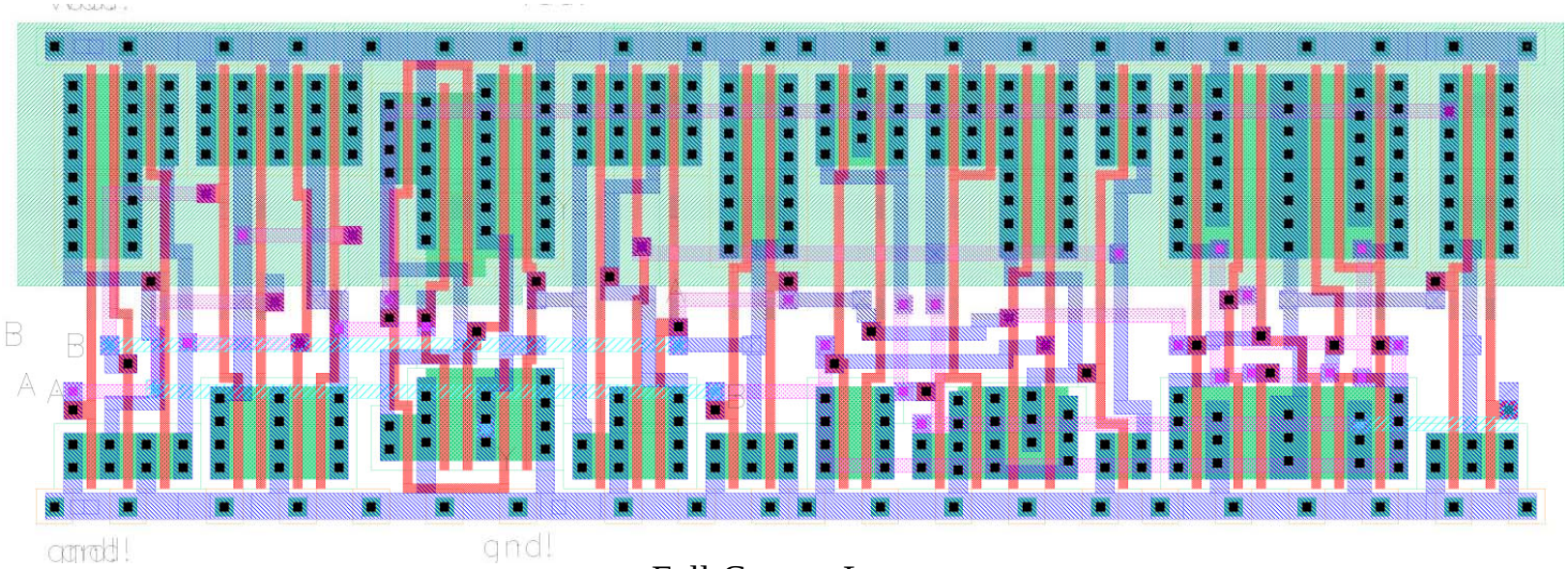
Unfolded Layout



Folded Layout

Full Custom

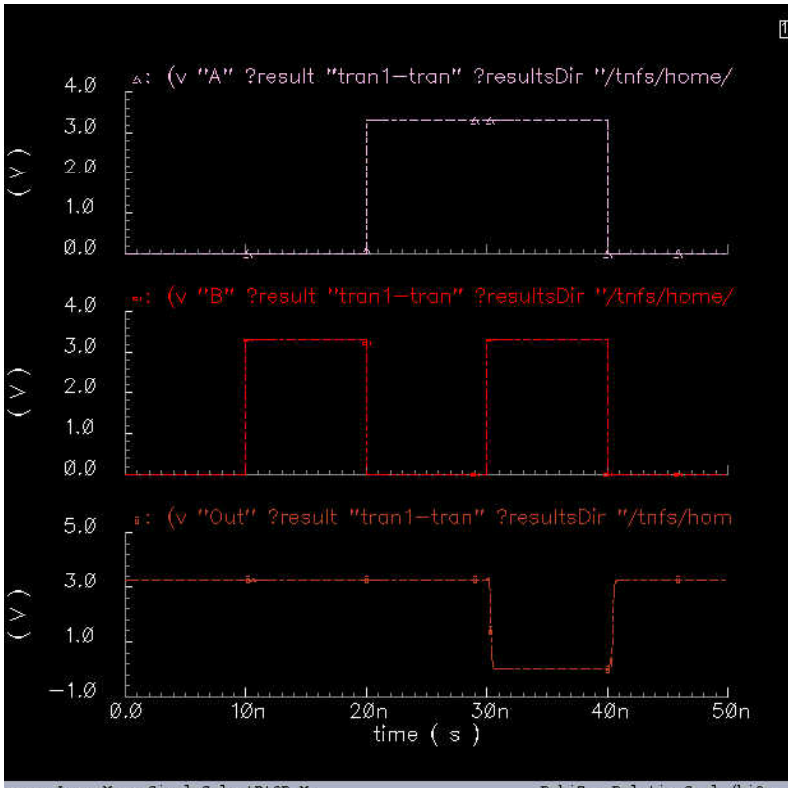
- Utilizing full custom one layout was generated
  - A single-row layout (20 µm x 64 µm) was created



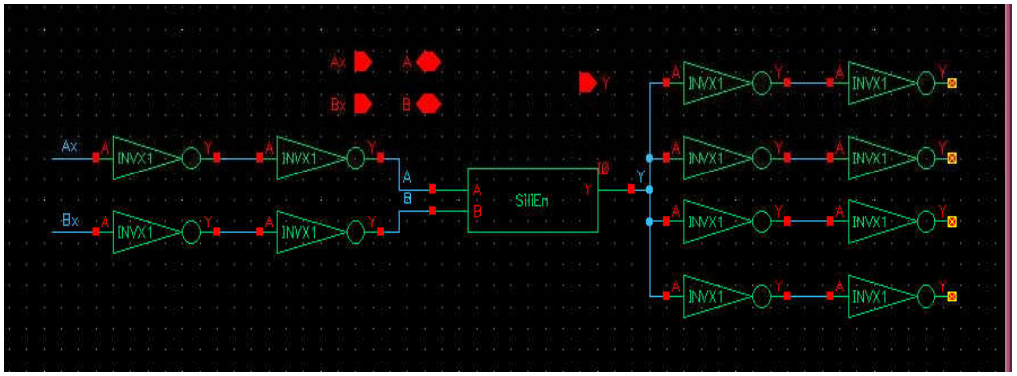
Full-Custom Layout

Simulations

- Load shaping inverters and 4 load-chains are simulated with each layout and the resulting delay is measured



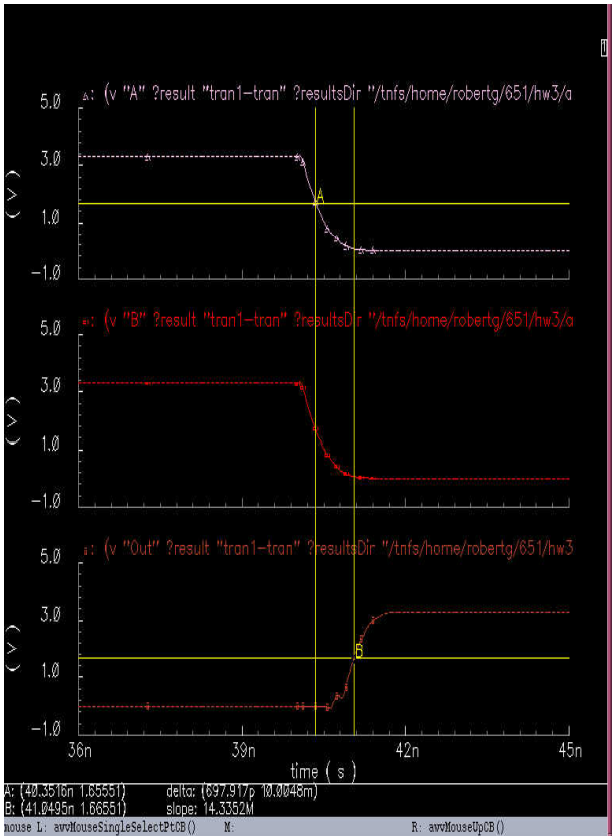
Representative of unloaded simulations



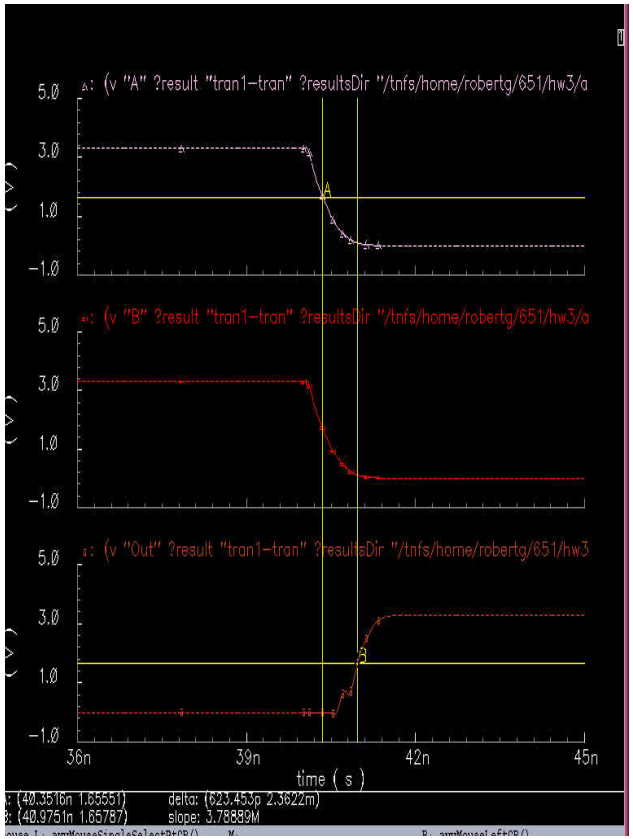
Schematic w/ Load

Simulations

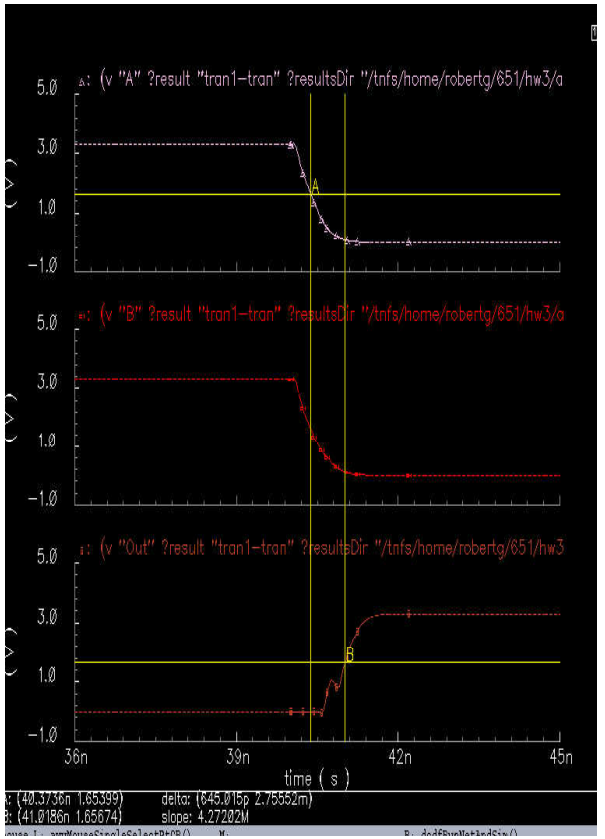
- Load shaping inverters and 4 load-chains



Folded ProGenesis Simulation (w/ load)



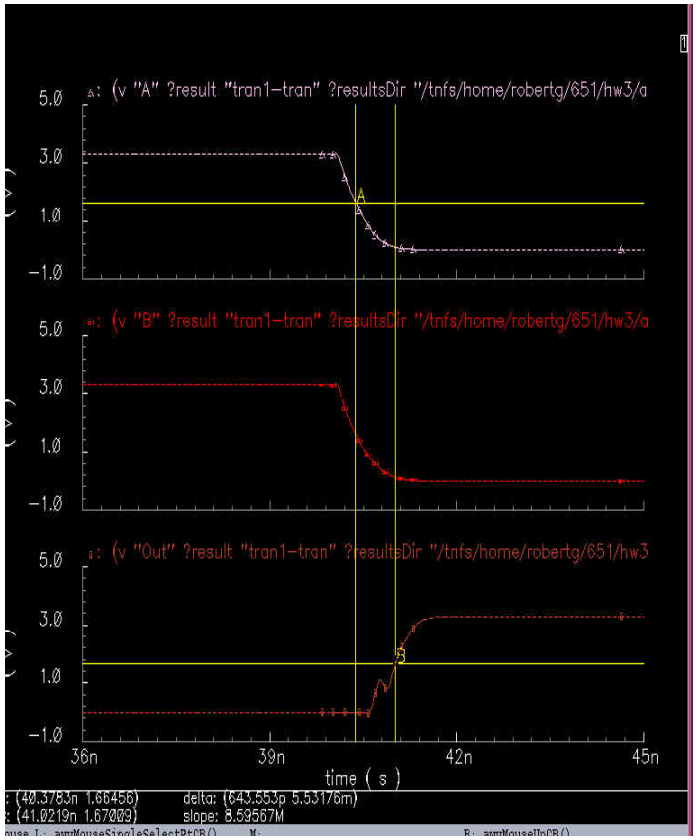
Unfolded ProGenesis Simulation (w/ load)



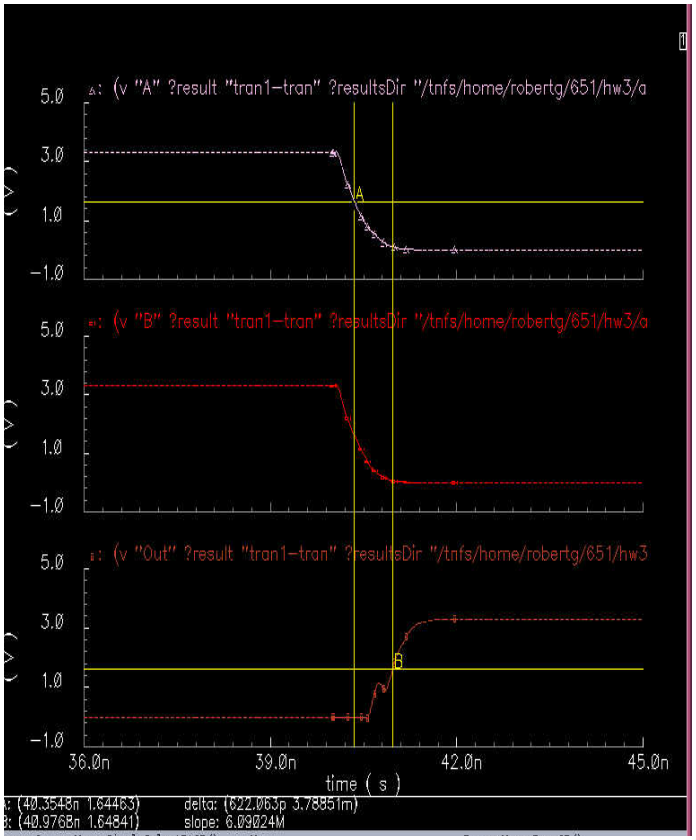
Two-Row Silicon Ensemble (w/ load)

Simulations

- Load shaping inverters and 4 load-chains



Single-Row Silicon Ensemble (w/ load)



Full-Custom (w/ load)

Figures of Merit

- Table comparing the width, length, Area, and Delay for each of the layouts

Layout Type	W (µm)	L (µm)	A (µm)^2	Delay (ps)
Progenesis (folded)	**20**	164.8	3296	697.9
Progenesis (unfolded)	23.2	**64**	1484.8	623.5
Silicon Ensemble (two rows)	40	40	1716	645.0
Silicon Ensemble (one row)	**20**	78.4	1568	643.6
Full Custom	**20**	**64**	**1280**	**622.1**

Conclusions/Lessons Learned

- ProGenesis is slow when tasked with generating [relatively] large layouts.
- When folding is activated in ProGenesis, all transistors are folded, resulting in a larger than expected layout
- Silicon Ensemble is sensitive when generating layout to scale factors that are not square

- The quickest method for generating layout is Silicon Ensemble, though it is also the largest (when ProGenesis is not folded)
- While custom layout takes longer than Silicon Ensemble, it is much quicker than ProGenesis, and the smallest of all the layouts