Data Sheet

SYNOPSYS®

DesignWare
SystemC Libraries

Overview

Leading-edge telecommunications applications today require the integration of DSPs and CPUs with dedicated ASIC circuitry. This is especially important in advanced wireless applications that rely on portable, battery-powered designs. Additionally, the explosion of broadband wired networking applications has introduced the concept of network processor designs that contain multiple CPU cores in tailored architectures. In all cases, software development is becoming a dominant part of the application and design effort.

CoCentric® System Studio is the ideal system-level verification tool for SoC and multiprocessor systems. It simulates algorithms and architectures. It addresses system aspects such as hardware and software tradeoffs, transactional analysis of the architecture, and end-to-end algorithm performance analysis using C/SystemC™. System Studio is tightly integrated with VCS™ to enable smart verification of the RTL implementation.

Off-the-shelf processor and bus models are convenient, easy-to-use and save time compared to writing your own models. ARM® processors and the AMBA On-Chip Bus architectures have captured a significant number of designs. The DesignWare SystemC libraries makes these popular models available to the System Studio customer base.

Verification of system-on-chip (SoC) architectures by RTL simulation is becoming increasingly difficult. This is partly due to increased complexity, but mainly due to the inability to efficiently simulate a processor executing application code in sufficient amounts such that design bottlenecks or longer-term errors can be exposed and repaired. Specifically, engineers need the ability to analyze and optimize architecture performance in real-world, multi-processor, software-centric applications. Doing this with RTL simulation would be inherently slow.

Cycle-accurate, transaction-level simulation is the best way to design and verify software-centric SoC architectures. The goal is to quickly and confidently confirm that the hardware architecture and software partitioning are correct, even before the RTL and software coding is complete.

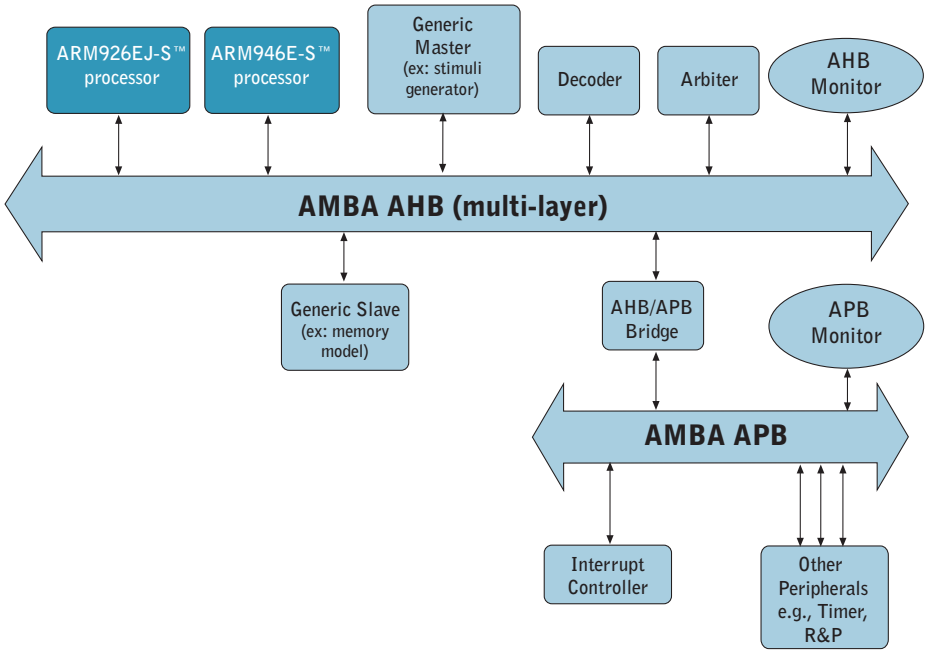

Figure 1. Typical AMBA bus architecture with ARM CPUs

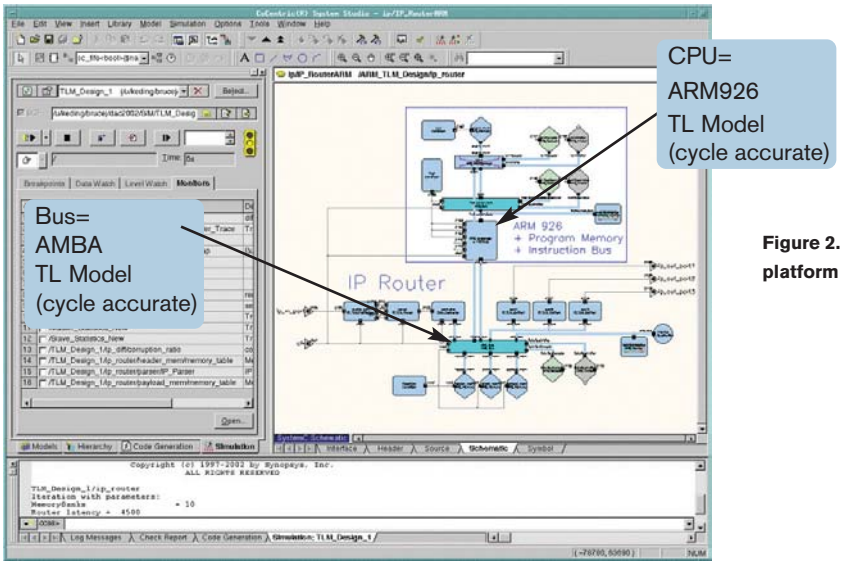

Figure 2. Typical example of ARM-AMBA platform design within CoCentric System Studio

Synopsys now offers the DesignWare ARM Processors SystemC Library and the DesignWare AMBA SystemC Library for designers using CoCentric System Studio. This results, not only in the ability to confirm the SoC architecture early in the design cycle, but also in the availability of a cycle-accurate execution model. This enables the software developers to begin their development well before the RTL is written and before a chip is taped out.

Benefits of Transaction-Level Modeling

Certain verification questions are best answered via RTL simulation, but there are other SoC architecture questions, such as bus loading or cache performance in real-world application scenarios, that cannot be answered with RTL simulation. In such cases, higher levels of design abstraction are required. Specifically for architecture design and verification, transaction-level modeling is about 100x – 2000x faster than equivalent RTL methods. Therefore, users can test 100x more application code in the same amount of time. This allows the detection and debug of system-related effects such as the build-up of errors or bottlenecks over the span of many frames of data.

The DesignWare ARM Processors SystemC Library and the DesignWare AMBA SystemC Library consist of these transaction-level models. By simply dropping them into SystemC designs, users can focus on architecture experiments instead of trying to figure out how to properly model the CPUs and buses.

Design Flow Options

There are many ways to design an SoC, but consider the relative merits of two popular methods. One technique is “successive refinement” of IP blocks, culminating in synthesis via CoCentric SystemC Compiler. The other technique is “IP block swap-out” where, for example, the AMBA bus models used for architecture design at a transactional level are swapped with equivalent RTL implementation IP(IIP), for example, the DesignWare AMBA On-Chip Bus IIP.

DesignWare ARM Processors SystemC Library

The ARM946E-S™ core is a popular member of the ARM 9E Thumb® family. The ARM926EJ-S™ additionally supports the Jazelle™ architecture for Java bytecode operations. Both processors are used in many microcontroller, DSP and Java applications today. The processors are delivered as pre-compiled SystemC transaction-level models that simulate in a cycle-accurate fashion. They are shipped with working examples. The designer uses these models within CoCentric System Studio and also in conjunction with the ADS software development system from ARM, Ltd. The ADU debugger runs together with System Studio, thereby providing full visibility during development.

DesignWare AMBA SystemC Library

The AMBA library is designed to the AMBA v.2.0 specifications. It consists of the AMBA High Performance Bus (AHB) and multi-layer AHB bus elements, as well as the AMBA Advanced Peripheral Bus (APB) elements. In addition to the standard elements, auxiliary models and timing models are included, as well as working design examples. The blocks are pre-compiled SystemC blocks for cycle-accurate transaction-level modeling. Adapters are included for cases when users require pin-accurate simulation and interface.

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