Analog Design Resource Kit Tutorial 2

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CMOS TWO TRANSISTOR CURRENT MIRRORS

Simulation and Measurement

Objective: To study the operation of simple two transistor CMOS current mirrors by simulation and measurement.

Introduction

All active circuits, whether employed on an integrated circuit or composed of discrete components, are usually DC biased in an operating region that takes full advantage of the circuit's unique characteristics. Circuits composed of discrete devices usually are DC biased using some type of resistive network such as you have studied in your first electronics course. On-chip circuits, however, are usually DC biased using active devices because of the relative ease in matching devices from one portion of the chip to the next. A widely used scheme for these types of biasing circuits is through the use of current mirrors. There are a wide variety of current mirrors that are used, each of which have advantages over the other. Simple current mirrors usually contain the fewest transistors and have relatively low constant current output voltages, but usually suffer from poor current matching due to process variations and a low output resistance. More complex current mirrors (such as the Wilson current mirror or cascode current mirrors) contain more transistors that improve the output impedance and current matching, but at the expense of increasing the constant current voltage [1]. The simplest of these current mirrors is the two transistor current mirror, illustrated Figure 1.

Transistors M1 and M2 are used to set the current in the left branch to some value. This current is then "mirrored" in device M3 since its gate voltage is identical to the gate voltage on M2. The component R can be a resistor or, more typically, the on-chip circuit to be DC biased by current I_2. The current in the right branch of the circuit (I_2) can be simply written in terms of the "set branch" current (I_1) as:

$$I_2 = \left(\frac{W}{L}\right)_1 \left(\frac{L}{W}\right)_2 I_1 \qquad (1)$$

where the aspect ratio is defined as (W/L).

A bias voltage can be used to control the current I_1 by varying the gate-source voltage on transistor M1. The set branch current I_1 can be written, assuming transistor M1 is in saturation, as:

$$I_1 = \frac{K_P}{2}\left(\frac{W}{L}\right)_P (V_{BIAS} - V_{DD} - V_{TP})^2 \tag{2}$$

The current flowing through transistor M2 and its gate-source voltage are related by the following expression:

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_1}{K_N (W/L)_N}} \tag{3}$$

assuming transistor M2 is in saturation. This gate voltage is identical to the gate voltage on M3, giving rise to Equation 1. The output impedance of transistor M3 prevents ideal current sink performance, and is governed by the DC current and the channel length modulation parameter, λ [1]. This output impedance also governs the output impedance of the current mirror, which may be written as [1]:

$$r_{OUT} = \frac{1}{\lambda I_2} \tag{4}$$

The typical operating region of the current mirror is governed by a voltage known as V_{MIN}, or the minimum voltage necessary for constant current, and is the minimum voltage needed to keep M3 in saturation; namely,

$$V_{MIN} \cong V_{GS} - V_{TN} \tag{5}$$

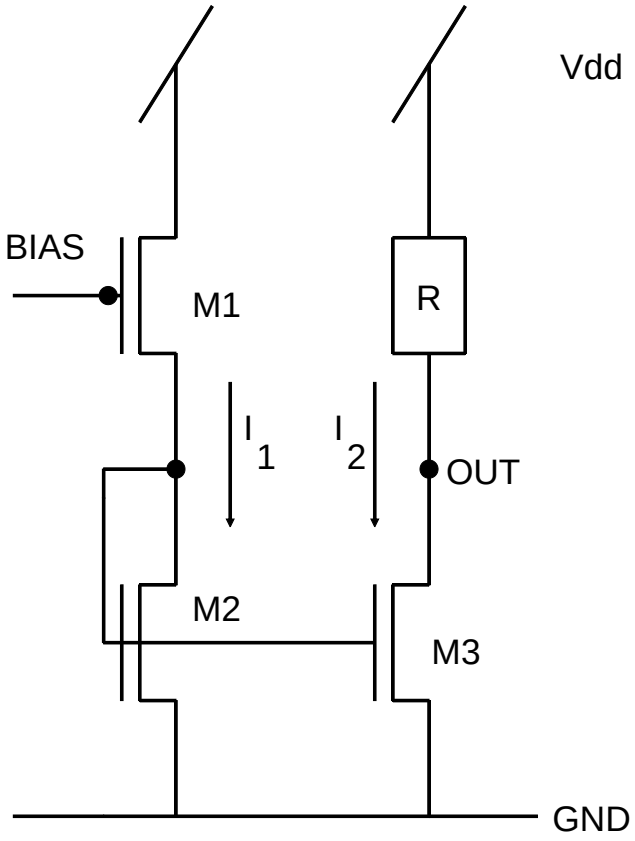


Figure 1

EQUIPMENT and PINOUT

Equipment

1. Design board with chip set IC
2. Function generator set for sawtooth wave generation
3. Multimeter and/or oscilloscope
4. 5.0 volt power supply (if not included on design board)
5. Resistors in the range of 1KΩ to 500 KΩ

Important Pins for this experiment

PIN 2 Adjustable Current Mirror Output
PIN 3 Non Adjustable Current Mirror Output
PIN 10 **GROUND**
PIN 16 Adjustable Current Mirror Bias
PIN 30 **V_{DD} (+5 volts)**

NOTE: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

DO NOT APPLY SIGNALS TO THE CHIP WITHOUT POWER AND GROUND APPLIED TO THE IC. TO DO SO MAY SET UP UNWANTED LATCH-UP PATHS THAT COULD RESULT IN IMMEDIATE DESTRUCTION OF THE IC!

PROCEDURE

Simulation

1. The first step in understanding the operation and simulation results of the current mirror is to compute the DC operating point of the circuit from the design equations listed earlier. Using the transistor aspect ratios listed in the SPICE file, compute the node voltages in the circuit and determine a resistance value R for 0.5 mA maximum current in the right branch of the circuit. Using this value of resistor, determine the output current versus input bias voltage. Comment on any differences in the results. Verify the current mirror action in this circuit by observing currents I_1 and I_2. Note any discrepancies between these two currents and explain possible causes.

2. Next, simulate the circuit using values of the external load resistance ranging from 1 KΩ to 500 KΩ. Simulate and determine the relationship between the output branch current at the input control voltage on the current mirror. A typical SPICE file for this simulation is listed later in this tutorial. Note that this SPICE file takes advantage of the sub-circuit command (.subckt) in SPICE as a way to simplify the SPICE file.

3. The output resistance and minimum output voltage at current saturation of the current are important parameters and can be determined from simulation. Using SPICE, determine these two parameters as a function of bias voltage. A typical SPICE file for this simulation is listed later in this tutorial. Note that this SPICE file takes advantage of the sub-circuit command (.subckt) in SPICE as a way to simplify the SPICE file.

Measurements

1. This next section describes in-laboratory measurements of the current-voltage characteristics of the simple two transistor current mirror.

First, adjust the dc power supply for 5.0 volts and verify **before** applying the DC supply to the IC using either a voltmeter or oscilloscope. Connect the power supply to the chip and to a 10 KΩ output resistance at the appropriate pins (see above pinout table).

Next, prepare an input signal using the function generator. This signal will be used to sweep the bias control voltage on the current set branch of the current mirror circuit. The signal from the function generator should exhibit the following specifications: a 0 to 5.0

volt 1 KHz sawtooth wave (or, alternately, a triangular wave with low duty cycle). Verify using the oscilloscope that the generator's output is within specifications **before** applying the signal to the appropriate pin.

After verifying that the power supply is energized, apply the bias control voltage to the current mirror circuit on the appropriate pin. Record the current waveform displayed on the oscilloscope. If available, use a digital storage oscilloscope to record one of the transfer curves and plot the curve. From the information given in this current transfer characteristic, determine the output conductance and V_{MIN} of the current mirror.

Repeat the measurements for load resistances of 1 KΩ, 100KΩ and 500 KΩ.

Questions

1. Determine the output load impedance and V_{MIN} as a function of bias voltage and output current. Compare these results with the design equations listed earlier.

2. Discuss the reasons why the constant current region and output resistance are functions of the bias voltage on the current mirror pFET.

References

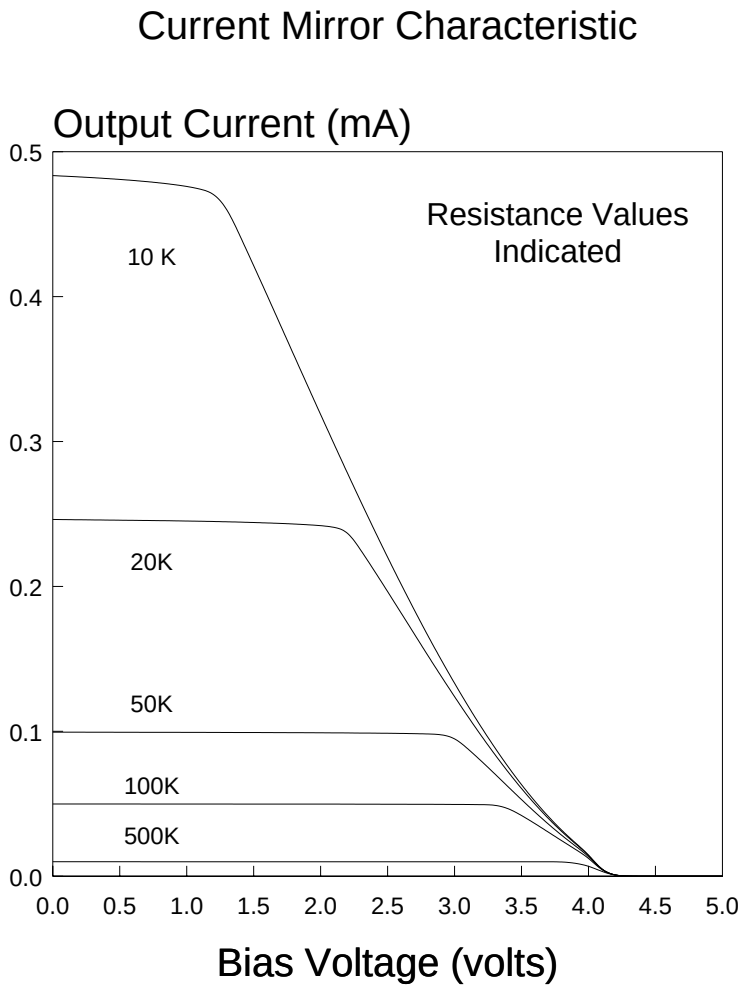
1. Geiger, R., P. Allen and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill Publishing Co., New York, 1990.

SPICE File for Simulating the Two Transistor CMOS Current Mirror

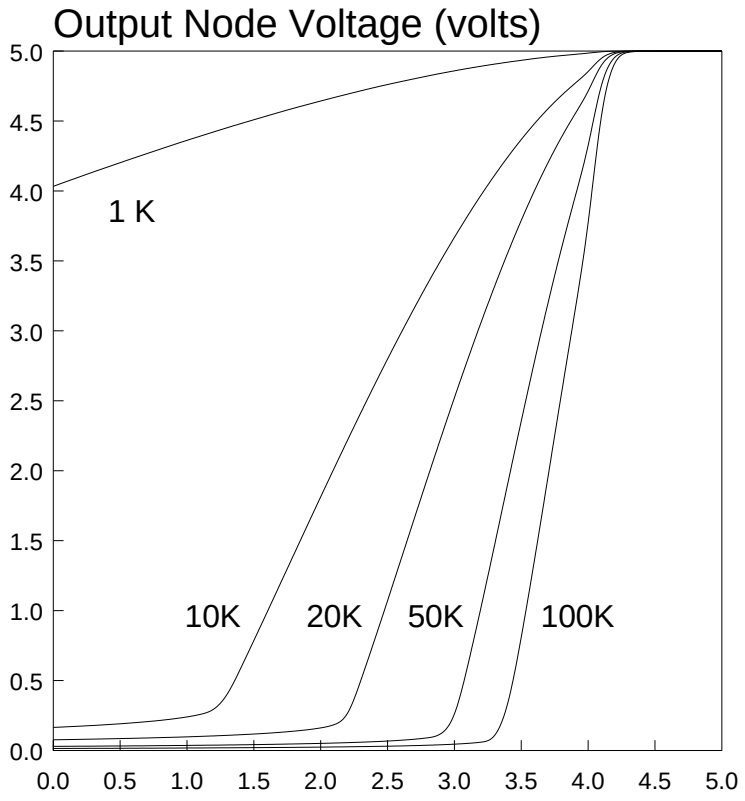
```
*** SPICE DECK created from mirr2.sim, tech=scmos
.subckt mirror 1  6   4
*   Node order:  vdd out vbias
*  This subcircuit defines the two transistor CMOS current mirror on the test chip
M1 1 4 5 1 CMOSP L=5.0U W=25.0U
M2 6 5 0 0 CMOSN L=2.0U W=220.0U
M3 5 5 0 0 CMOSN L=2.0U W=122.0U
C4 5 0 0.353000PF
C5 6 0 0.471000PF
C6 4 0 0.011000PF
*  GND  0
*  OUT  6
*  Vdd   1
*  Vin    4
.ends
vdd 1 0 dc 5
* The "xi" calls are subcircuit calls
*  Current mirrors with varying resistance values
x1 1 3 2 mirror
r100k 1 3 100k
x2 1 4 2 mirror
r500k 1 4 500k
x3 1 5 2 mirror
r1k 1 5 1k
x4 1 6 2 mirror
r10k 1 6 10k
x5 1 7 2 mirror
r50k 1 7 50k
vbias 2 0
.dc vbias 0 5 .1
*  The following "probe" line is for those using PSPICE with PROBE Option
.probe
*  Plot the currents from 0 to 0.5 mA
.plot  dc i(r10k) i(r20k) i(r50k) i(r100k) i(r500k) (0,0.5e-3)
.print  dc i(r10k) i(r20k) i(r50k) i(r100k) i(r500k) (0,0.5e-3)
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
.end
```

Results of SPICE Simulations

The SPICE file listed in the tutorial contains simulations of the two transistor current mirror for values of load resistance ranging from 10 KΩ to 500 KΩ, and for a control bias voltage varying between 0 and 5 volts DC. The models and components used in the simulation are the same as those used in the experiments discussed in the text. The figure below shows the results of the SPICE simulation listed on the previous page. The results show that increased load resistance causes a corresponding decrease in overall current that can be supplied by the current mirror. Note also that the current curves are not quite "flat" in the constant current region; this is a consequence of the finite output conductance associated with transistor M3. Note also that the a change in load resistance causes a change in constant-current bias voltage on M1.



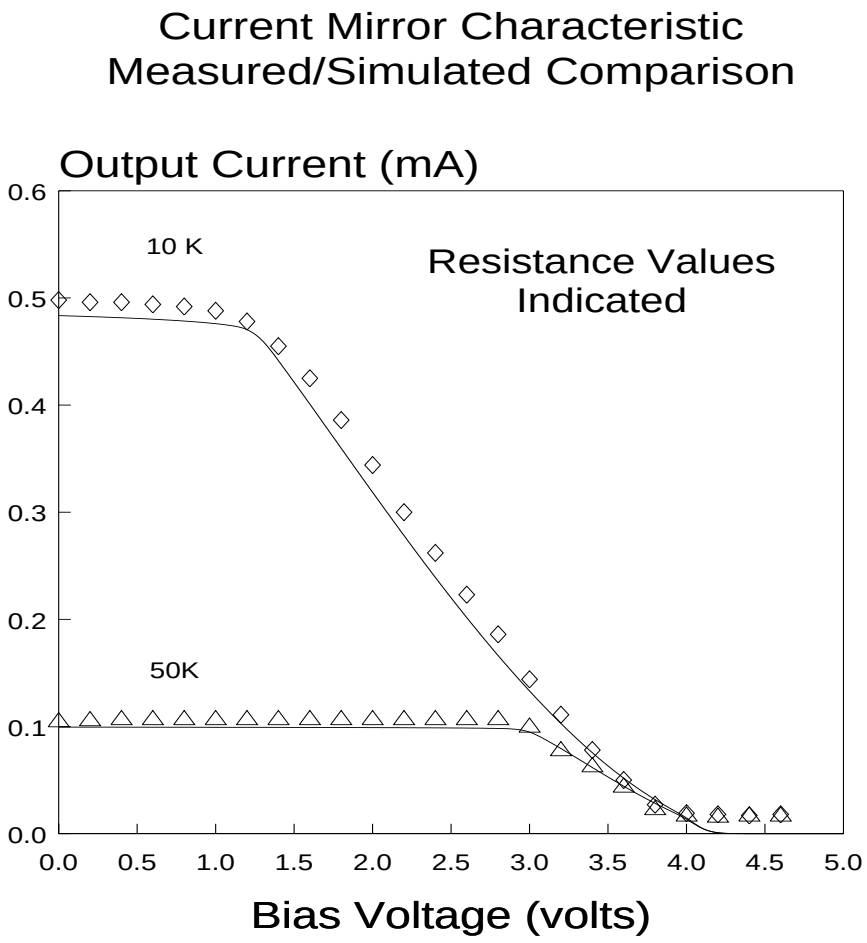
The output node voltage also shows a dependence on load resistance and this dependence is indicated below. Note that the output voltage is constant and near zero in the constant current region of the circuit.



Output Node Resistance Indicated

Measured Response of the Current Mirror

The current-voltage response of the current mirror was measured using swept bias voltage on the current source FET and a 10KΩ and 50KΩ resistive load. The equipment used for this set of measurements was an HP-3314A function generator and a Tektronix 2230 Digital Storage Oscilloscope. The simulated results, shown in the figure below, are repeated from the figure on the previous page. The simulated results are indicated by the solid line and the measured results by points. The two results are in quite good agreement for all values of current source control voltage.



Current Mirror SPICE Simulation: Output Resistance

```
*** SPICE DECK created from mirr2.sim, tech=scmos
* subcircuit definition for two transistor current mirror
.subckt mirror   3        6          1
*                  bias    mirout    set   :subcircuit node definitions
M1 1 3 5 1 CMOSP L=5.0U W=25.0U
M2 6 5 0 0 CMOSN L=2.0U W=220.0U
M3 5 5 0 0 CMOSN L=2.0U W=122.0U
.ends
x1 3 6 1 mirror
vbias 3 0
vout 6 0
vdd 1 0 dc 5
* sweep output voltage and bias voltage to pFET/current source
.dc vout 0 5 0.1 vbias 0 4 0.5
.width out=80
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
*  The following "probe" line is for those using PSPICE with PROBE Option
* .probe
.end
```

Simulation Results

The results of the output resistance simulation are shown below. Notice that beyond the current knee, the output current rather shows a slight dependence on the output voltage. This is caused by the finite output resistance of the current mirror. This value of output resistance can be estimated by computing the slope of the curve (for the conductance) and inverting the result. Theoretically, the output resistance is given by Eqn. 4, which should be approximately 40 KΩ for a current of 1 mA.