Analog Design Resource Kit Tutorial 3

Robert H. Caverly
Department of Electrical and Computer Engineering
University of Massachusetts Dartmouth
N. Dartmouth, MA 02747-2300
caverly@micron.ece.umassd.edu

CMOS OPERATIONAL AMPLIFIERS

Simulation and Measurement

The operational amplifier (op-amp) is one of the major building blocks used in analog circuit design. Besides its use as an amplifier or gain block, it is frequently used as a circuit buffer that provides a high input and output impedance with enhanced drive capability. The op-amp can be fabricated using bipolar junction transistors, MOSFETs or a combination of the two (BiCMOS) to name just a few possibilities. Typical specifications for CMOS op-amps include open loop gain of 60 dB, a 1 MHz unity gain bandwidth, a 100 KΩ output resistance, a 1V/μsec slew rate, a nearly infinite input differential resistance and a few milliwatts power consumption [1].

General purpose op-amps will usually consist of many, sometimes complex stages so that they may be used in fulfilling stringent requirements in a variety of applications. The basic op-amp, however, is relatively simple, and a simple two-stage op-amp can provide modest performance, especially if the application is on-chip or driving light off-chip loads. Study of simple architectures helps in the designer's understanding of the circuit and allows the designer to more easily modify the basic circuit to fit their specific needs. The simplest op-amp circuit contains just two stages, a differential input amplifier stage and a single-ended output stage. A simple 9 transistor CMOS op-amp is shown in Figure 1. The overall voltage gain of the op-amp is a function of the voltage gains of the two stages: the input differential amplifier stage (M4 through M7) and the output stage (M8 and M9). The first stage has a single-ended voltage gain governed by the transconductance of M4 and M6 and the output loading by the output drain conductance of transistors M6 and M7 [2]:

$$A_{v1} = -\frac{g_{m4}}{g_{o6} + g_{o7}} \tag{1}$$

where g_m is the transistor transconductance and g_o is the small signal output conductance. The expression also assumes that M4 and M6 are identical and M5 and M7 are as well. The second stage voltage gain is of similar form to the gain expression of the simple

inverting amplifier discussed in Tutorial 1. However, note that the gate of M8 does not vary with the input voltage, hence there is no transconductance term contributed by this device. The output conductance does, however, contribute to the overall output conductance of the circuit. With this in mind, the voltage gain in this stage can be written as:

$$A_{v2} = -\frac{g_{m9}}{g_{o9} + g_{o8}} \tag{2}$$

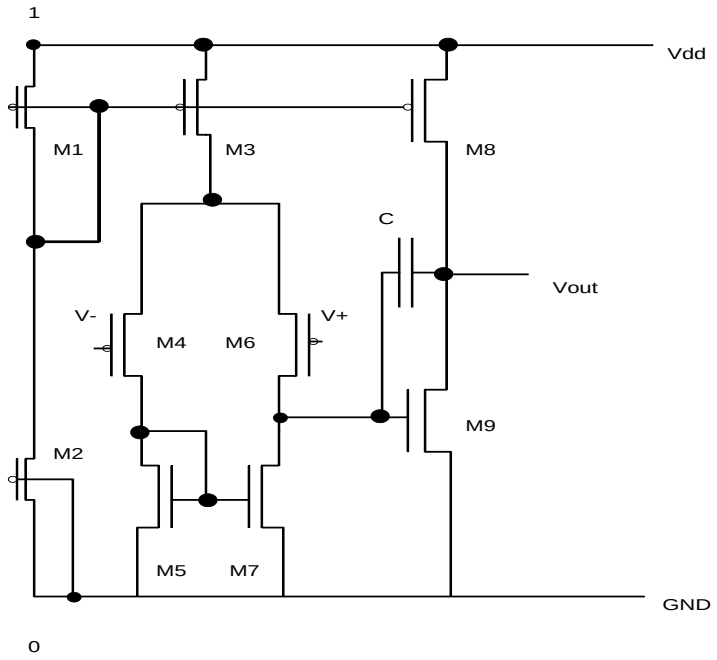


Figure 1

Transistors M1, M2, M3 and M8 are part of the bias network that provides dc bias throughout the operational amplifier. Transistor M2 sets the bias current for the entire circuit. To keep the transconductance, and hence the gain, of the CMOS op-amp as large as possible, the devices should be operated at low currents. This implies that the aspect ratio of M2 will be have a small aspect ratio (i.e., W/L less than unity). The resulting gate voltage on M1 is repeated on devices M3 and M8. The currents through these devices are set by their respective aspect ratios.

Frequency compensation of the op-amp is accomplished by means of the capacitor C shown in Figure 1. Because of the relatively low transconductance of FETs (compared with bipolar transistors), however, a right-half plane zero is created at a frequency low enough to cause degraded op-amp stability [2]:

$$s_z = +\frac{g_{m6}}{C} \tag{3}$$

The right-half plane zero described above is caused by the input signal propagating through compensation capacitor C at high frequencies (Figure 1). The simplest way to reduce the effect of this low frequency zero is to insert a "nulling" resistor in series with the compensation capacitor [2]. This resistor can be created using the inherent sheet resistance of the polysilicon layer in polysilicon-metal1 overlay capacitors, or by the addition of an active transmission gate in series with compensation capacitor C [1]. The addition of some series resistance R_Z shifts the zero to the location given by [2]:

$$s_z = +\frac{1}{C(g_{m6}^{-1} - R_z)} \tag{4}$$

The slew rate (SR) of the CMOS op-amp is dependent on the bandwidth, bias current, compensation capacitor C, and device transconductance [2]:

$$SR = \frac{I_{D3}}{C} \tag{5}$$

The slew rate is governed by the rate that the compensation capacitor C can charged or discharged by transistor M3. To increase SR, the circuit should be biased to increase the current handling capability of M3.

The laboratory exercises described in this tutorial cover simulation and measurements of the simple CMOS op-amp. Open and closed loop gain, bandwidth, offset voltage, and slew rate measurements are included in this tutorial.

EQUIPMENT and PINOUT

Equipment

1. Design board with chip set IC
2. Function generator set for sawtooth (or square) wave generation
3. Multimeter and/or oscilloscope
4. 5.0 volt power supply (if not included on design board)
5. 100 KHz Spectrum Analyzer (if available)

Important Pins for this experiment

PIN 10	**GROUND**
PIN 20	AMP1 OUT
PIN 21	AMP1 IN+
PIN 22	AMP1 IN-
PIN 23	AMP2 IN+
PIN 24	AMP2 IN-
PIN 29	AMP2 OUT
PIN 30	**V_{DD} (+5 Volts)**

NOTE: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

ALSO, DO NOT APPLY ANY VOLTAGE TO THE TEST CHIP WITH THE POWER TO THE CHIP OFF. THIS COULD CAUSE LATCH-UP TO OCCUR, WITH THE POSSIBLE CONSEQUENCE OF CHIP DESTRUCTION.

PROCEDURE

Simulation

1. The first step in testing the operational amplifier's operation is to simulate the ac and dc response of the amplifier, then compare it with the actual fabricated amplifier's response. Determine the dc transfer function of the inverting amplifiers with aspect ratios listed in the SPICE file at the end of this tutorial. Also determine a value of bias voltage that will bias the inverting amplifier into a region of operation that allows for reasonable gain and output voltage swing. Simulate the dc response using a circuit simulator such as SPICE. An example file showing all the necessary input sources and other command/control statements is presented at the end of the tutorial.

In this command file, the command shown causes a sweep of the input voltage "V_{in}" over the range of 0 to 5 volts in 0.1 volt steps. The input voltage and the results of the dc voltage sweep should be plotted on one graph. Obtain a plot of these responses.

2. Another simulation case study that is of interest to op-amp designers is its operation as a feedback circuit element. A typical usage is as a fixed gain resistive feedback amplifier. Simulate the ac response of this op-amp for a fixed design gain of -100 using 10KΩ, 100KΩ, and 1 MΩ resistors in the feedback loop. Have the amplifier drive a typical 10 pF load capacitance (a typical CMOS off-chip load). Also simulate the transient response of the circuit with the 1 MΩ feedback resistor at frequencies of 10 KHz and 100 KHz.

Measurements

1. Open Loop Measurements

1. A convenient circuit for measuring the open loop response of an op-amp is shown in Figure 2 [1]. This circuit configuration provides the necessary feedback to DC stabilize the amplifier while allowing the high gain of the open loop circuit to be measured. The RC cutoff frequency required for this circuit must be much less (factor of 10 to 100 or more) than the anticipated -3dB point of the amplifier open loop response; hence, the values indicated in the figure. You can configure either of the op-amps on the test chip; they both are identical.

OPERATIONAL AMPLIFIER
Open Loop Measurements

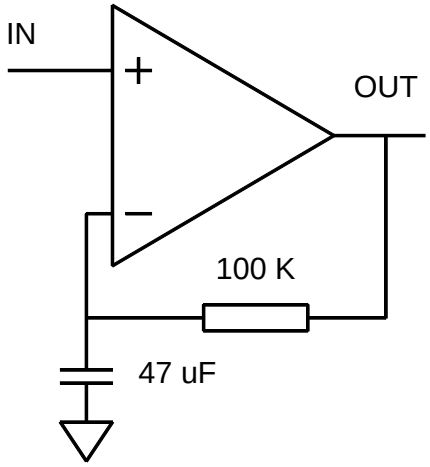


Figure 2

After wiring the circuit, adjust the dc power supply for 5.0 volts and verify **before** applying the dc supply to the IC using either a voltmeter or oscilloscope. Connect the power supply to the chip at the appropriate pins (V_{dd} and Ground).

Next, prepare an input signal using the function generator. This signal should exhibit the following specifications: a 0.5 mV peak sinusoidal signal with a 2 volt DC offset. Verify using the oscilloscope that the generator's output is within specifications **before** applying the signal to the appropriate pin of the IC.

After verifying that the power supply is energized, apply the ac signal to the amplifier. Observe the output of the circuit and record the output voltage response over a frequency range of 0.1 KHz to 25 KHz. Record enough data to determine the frequency response.

2. Remove the input signal and the capacitor from the circuit under test. Replace the feedback resistor with a wire jumper to configure the op-amp as a unity gain circuit. Prepare a square wave input signal using the function generator that exhibits a 0 to 5 volt swing at 50 KHz. **Verify** using the oscilloscope that the generator's output is within specifications **before** applying the signal to the circuit input. Place the input signal at the appropriate pin and observe the output voltage swing from the op-amp on an oscilloscope. Determine the positive and negative slew rates of the op-amp, based on the output voltage rise and fall times. If possible, determine the settling time of the op-amp as well.

2. Closed Loop Measurements

1. The next step in the measurement process is to determine the closed loop frequency response of the op-amp, using several different combinations of resistors to set the closed loop gain. Use the circuit shown in Figure 3. Connect the op-amp and resistors so that design gains of 11 and 101 are achieved using resistors of 100KΩ and 1 MΩ in the feedback loop (R_F). Place a nominal 2 volt offset, 50 mV peak signal (5 mV for the gain of 101) at the input to the amplifier. Determine the mid-band closed loop response (assume 1 KHz is mid-band) and verify that it agrees with the design goal. Increase the frequency and observe the amplitude of the output waveform. Record enough data to determine and plot the frequency response out to at least 100 KHz.

OPERATIONAL AMPLIFIER
Closed Loop Measurements

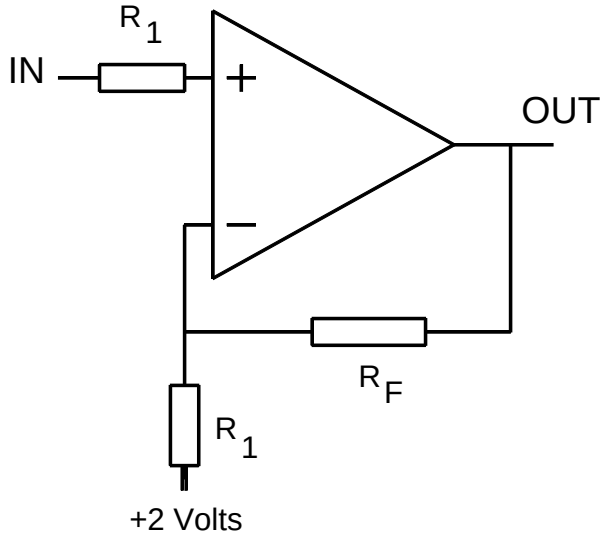


Figure 3

Questions

1. If there are any differences between the designed versus measured ac responses of the feedback amplifier, comment on the possible origins.

2. This operational amplifier has a relatively low slew rate. Comment on how one might improve (at the circuit level) the slew rate of the amplifier. Also comment on the origin of the differences between the rising edge and falling edge slew rates.

REFERENCES

1. Geiger, R., P. Allen and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill Publishing Co., New York, p. 478, 1990.

2. Gray, P. and R. Meyer, "MOS Operational Amplifier Design-A Tutorial Overview", IEEE J. Solid-State Circuits, vol. SC-17(6), pp. 969-982, Dec., 1982.

SPICE Deck for Simulating the 9 Transistor CMOS Operational Amplifier

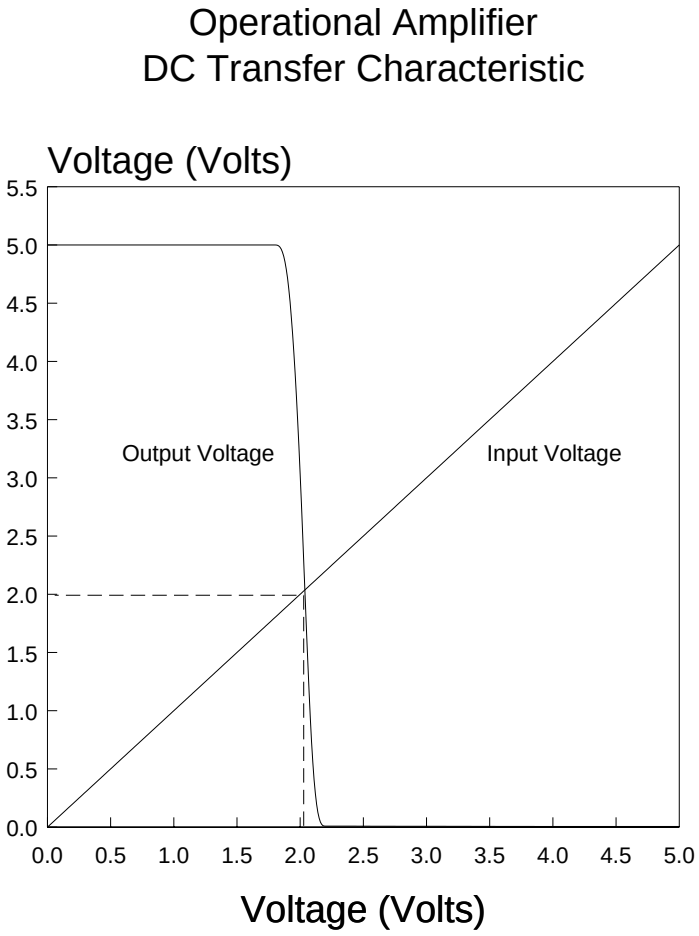
```
* Low current dual stage operational amplifier
M1 2 2 1 1 CMOSP L=5U  W=25U
M2 0 0 2 1 CMOSP L=50U  W=5U
M3 3 2 1 1 CMOSP L=5U  W=25U
M4 4 9 3 1 CMOSP L=5U  W=75U
M6 5 10 3 1 CMOSP L=5U  W=75U
M5 4 4 0 0 CMOSN L=5U  W=10U
M7 5 4 0 0 CMOSN L=5U  W=10U
M8 6 2 1 1 CMOSP L=5U  W=50U
M9 6 5 0 0 CMOSN L=5U  W=40U
C1 5 6 0.5PF
* CLOAD 6 0 10PF
VDD 1 0 DC 5.0
*  v-  9
*  v+ 10
*  vout 6
*  Vdd 1
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
* To run the specific set of simulations, edit out the appropriate
* section's comment columns (*).
* DC Transfer Characteristic:  2.0 Volt Offset
vplus 10 0 dc 2.0
vminus 9 0
.dc vminus 0 5 0.1
* AC Transfer Characteristic:  2.0 Volt Offset
*vplus 10 0 dc 2.0
*vminus 9 0 dc 2.0 ac 1e-6
*.ac dec 10 100 1e9
* The following "probe" line is for those using PSPICE with PROBE Option
* .probe
 .end
```

Results of SPICE Simulations

The SPICE file listed in the tutorial contains two different simulations of the 9 transistor CMOS operational amplifier: a dc transfer analysis, and an ac frequency response analysis. The models and components used in these analyses are typical of those used in most measurements. The following set of figures shows the results of each one of the simulations.

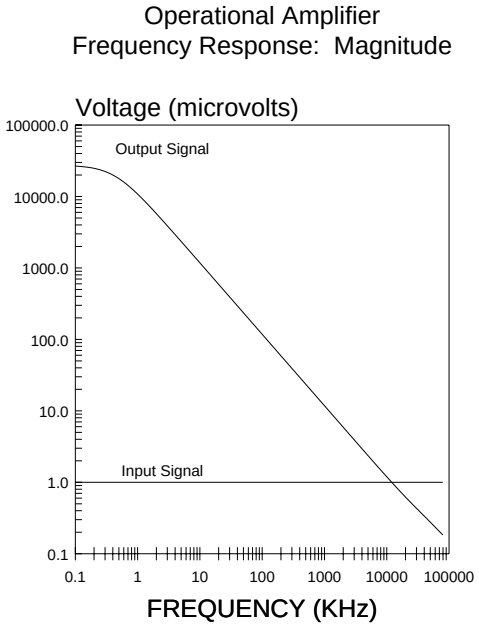
DC Transfer Characteristic

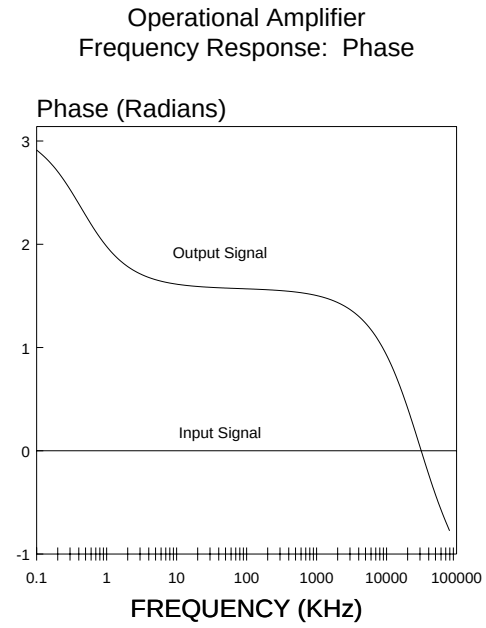
The DC Transfer Characteristic plot shows the input voltage ramp [v(9] and the resulting output signal [v(6)] with a 2.0 volt dc offset at the non-inverting terminal [v(10)]. The simulated transfer characteristic used a compensation capacitor of 0.5 pF. The figure indicates that the op-amp transitions rapidly near an input of 2.0 volts with an input dc offset of 2.0 volts.



AC Frequency Response

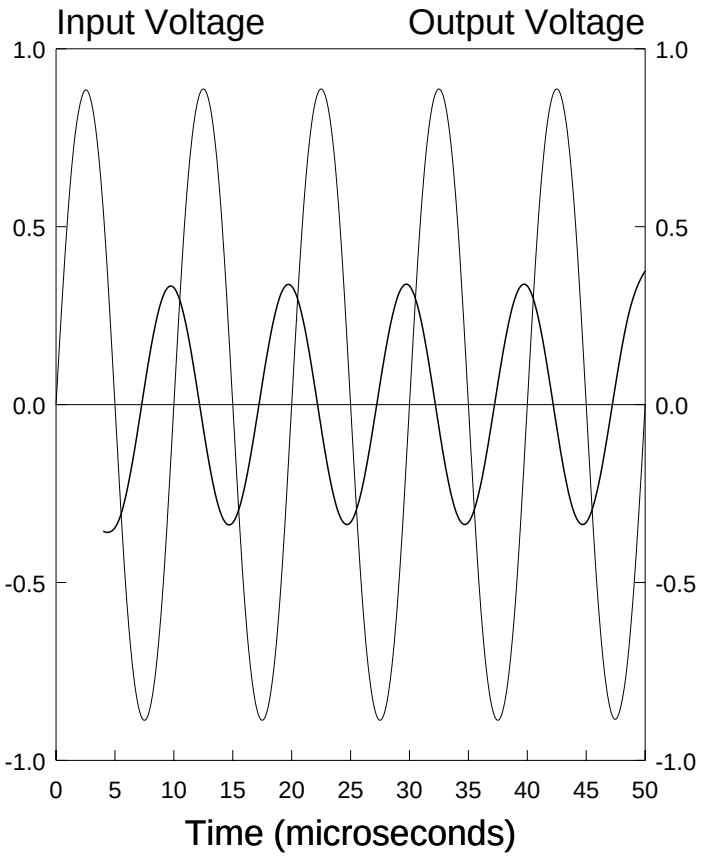
The AC Frequency Response output has been divided into two plots, a magnitude and phase plot. The magnitude plot shows that an input signal of 1 microvolt [vm(9)] provides an output amplitude of approximately 30 millivolts [vm(6)], yielding a low frequency gain magnitude of approximately 30,000. The -3dB point (gain of 21,200) occurs at a frequency of approximately 500 Hz. The phase plot [vp(6), vp(9)] shows a phase of 3.14 (or π) radians at low frequencies, rolling off to 2.355 ($3\pi/4$ radians or 135 degrees) at approximately 500 Hz. Note that the compensating zero flattens the phase response in the frequency range of approximately 10KHz to 1 MHz. The unity gain frequency occurs at approximately 12 MHz; the gain-3dB bandwidth product is approximately 12 MHz as well. The phase margin at 12 MHz is approximately 0.6 radians (or about 35 degrees); the gain of the op-amp at zero phase is approximately -10 dB.





Transient Response

The Transient Response shows the amplification properties of the fedback op-amp (1 MΩ feedback resistor) set for a gain of -100. The excitation is a 10 mV, 100 KHz sinusoid with a 2 volt dc offset. The plot below shows this waveform with the DC offset removed and the amplitude scaled by a factor of 100. The output waveform (**bold**) does not show the expected 2 volt swing, nor does it show the expected 180 degree phase shift. Inspection of the open loop transfer function explains this behavior, however. The gain bandwidth product of the circuit operation (approximately 10 MHz) is nearly that of the open loop op-amp. The op-amp is limiting the gain of the overall circuit by approximately 6 dB with the corresponding 90 degree phase shift evident on the output signal. A simulation at 10 KHz will show more ideal behavior.



Output Voltage Bold

Measurement Results

Measurements of several different operational amplifier parameters were performed on the as-fabricated circuits. This data set included measurements of open loop gain, gain bandwidth product (GBW), slew rate (SR) and gain in a non-inverting amplifier. The equipment used for this set of measurements was an HP-3314A function generator and a Tektronix 2230 Digital Storage Oscilloscope. The spectrum was computed from these samples using software developed at UMass Dartmouth. GBW and open loop gain were measured using the circuit shown in Figure A1. A 0.5 mV peak AC voltage with a 2 volt DC offset was applied to the input. The resulting AC frequency response measurements were compiled and are illustrated in Figure A2. The open loop gain of the op-amp is approximately 1300 with a -3 dB point of approximately 10 KHz, yielding a GBW of 13 MHz.

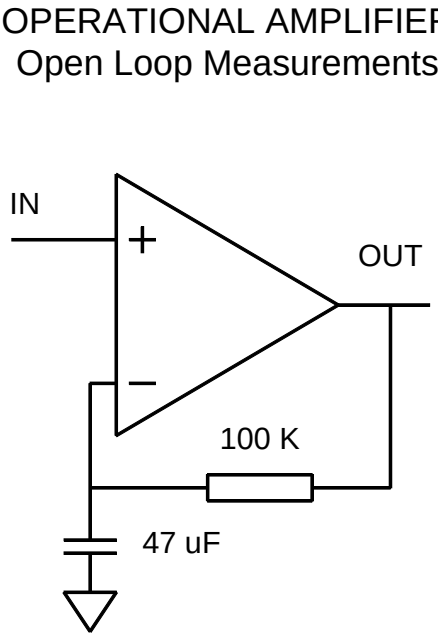


Figure A1

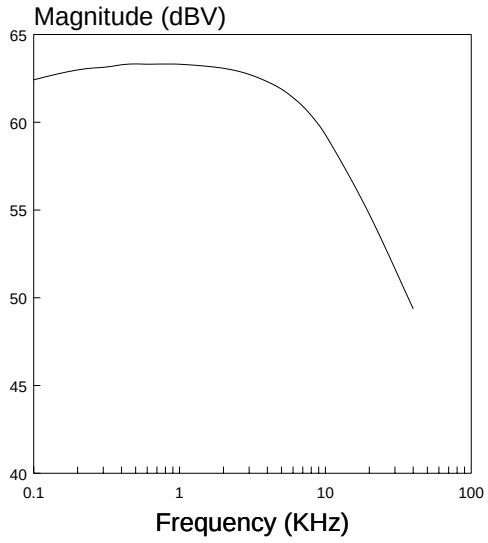


Figure A2

Figure A3 shows the results of frequency response measurements of a non-inverting feedback amplifier using feedback resistances of 100 KΩ and 1.2 MΩ (circuit diagram shown in Figure A4). The feedback amplifier results show the expected low frequency gain response as well as the expected gain roll off at higher frequencies. This roll off in gain also verifies the GBW previously measured.

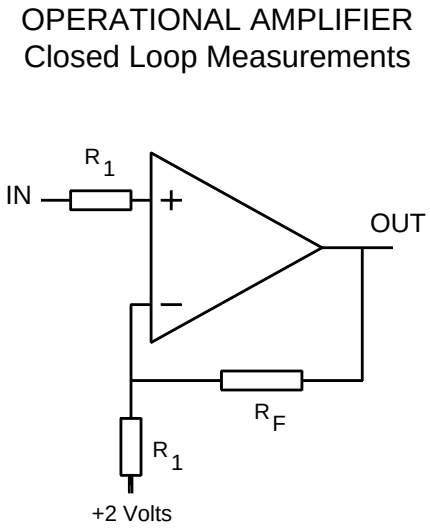


Figure A3

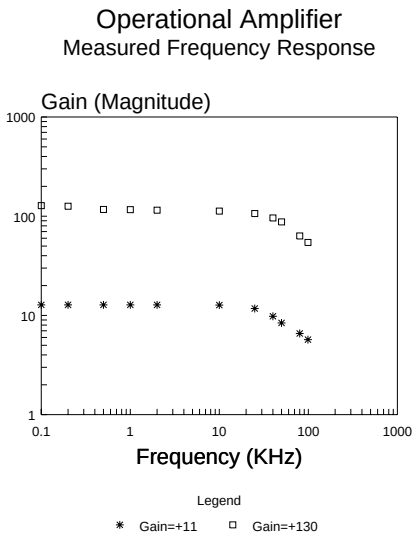


Figure A4

A separate measurement of slew rate was performed using a 0 to 5 volt 50 KHz square wave input. The resulting output exhibited an approximately 0.3 volt rise at the output over 1 μsec, yielding a SR of 0.3 volt/μsec. A higher SR can be achieved by biasing the differential amplifier with a higher current (this particular op-amp was designed for low current drain).