Analog Design Resource Kit Tutorial 4

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SINGLE POLE SWITCHED CAPACITOR FILTER

Simulation and Measurement

Objective: To observe the operation of a switched capacitor network, to compute a number of parameters of the switched capacitor network, and to observe the sampled data nature of this circuit.

Introduction

One of the most widely used circuits in the analog domain utilizes the switched capacitor. These switched capacitors act as continuous time "resistors", but in the discrete time domain, and rely on transfer of charge between two nodes to provide a change in voltage. Because of the sampled data nature of switched capacitor networks, the frequency response of these circuits is a function of the sample rate and ratio of the capacitors that make up the switched capacitor circuit. The circuit that you will be investigating in this tutorial is a single pole network that uses a switched capacitor for the series "resistor" and a lumped capacitor. The output of the switched capacitor circuit contains a buffer amplifier to provide charge transfer isolation and output signal drive.

The sampled data nature of the switched capacitor network is seen by looking at the circuit shown in Figure 1 during each individual phase of the clock. During the input phase of the clock Φ_1 (PHI1), the input capacitor charges up to V_{in} and the output capacitor retains the output potential V_{out} at the end of Φ_2 (PHI2). The total charge at the end of Φ_1 can be written as

$$Q_{\Phi_1} = C_1 V_{IN}(t - \Delta T) + C_2 V_{OUT}(t - \Delta T) \qquad (1)$$

where T is the clock period. During the next phase of the clock (Φ_1), the charge on the input capacitor is transferred to the output capacitor, with the total charge remaining the same at the end of Φ_2 as at the end of Φ_1; namely,

$$Q_{\Phi_1} = Q_{\Phi_2} = (C_1 + C_2)V_{OUT}(t) \tag{2}$$

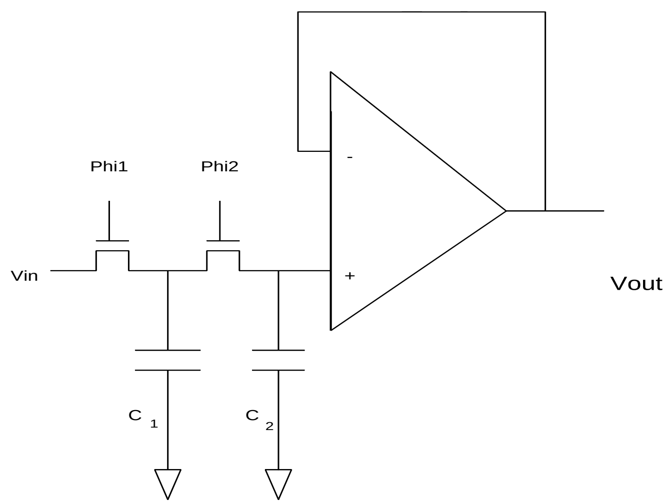

FIGURE 1

If the assumption is made that the samples during each phase of the clock are constant in value (sample and hold approximation), then the samples delayed by time ΔT are delayed in the discrete time domain by a single time unit (namely, n-1) with respect to time t (namely, discrete time unit n). The following is the discrete time equation for the switched capacitor network:

$$(C_1 + C_2)V_{OUT}[n] = C_2 V_{OUT}[n-1] + C_1 V_{IN}[n-1] \tag{3}$$

Equation 3 indicates that the total charge during the second phase of the clock is equal to the sum of the charges on C_1 and C_2 during the first phase of the clock.

Taking the Z-transform of Equation 3 and computing the ratio $V_{OUT}(z)/V_{IN}(z)$ gives the transfer characteristic of the network, H(z):

$$H(z) = \frac{C_1}{z(C_1 + C_2) - C_2} \qquad (4)$$

This transfer function describes a single pole network with the pole at

$$z_P = \frac{C_2}{C_1 + C_2} \qquad (5)$$

The depth of the stop band increases as the pole z_P approaches unity, implying that a large value of C_2 (with respect to C_1) increases the stop-band attenuation of the filter.

At low frequencies (z near unity), the transfer function exhibits a near unity value. As the frequency approaches $f_S/2$ (z nearly -1), the transfer function approaches a value of

$$H(z) = -\frac{1}{1 + 2\frac{C_2}{C_1}} \quad . \qquad (6)$$

This equation defines the depth of the filter stop band and is dependent on the ratio of capacitors C_2/C_1. The -3 dB point of the filter can be computed by replacing z by $e^{j\omega t}$ and forcing the magnitude of the transfer function to be 0.707 ($1/\sqrt{2}$) at the -3 dB point. This yields an expression for the -3 dB point in terms of the clock rate and capacitor ratio:

$$f_{-3\,dB} = \frac{1}{2\pi T} \cos^{-1}\left[1 - \frac{1}{2\alpha(1+\alpha)}\right] \qquad (7)$$

where $\alpha = C_2/C_1$. Large values of α yield high stop-band attenuation values, but also yield lower -3 dB frequencies.

EQUIPMENT and PINOUT

Equipment

1. Design board with test IC
2. DC power supply (5.0 volt minimum)
3. Function generator for use as a clock pulse generator
4. Function generator set for sinusoidal wave generation
5. Oscilloscope (voltmeter if available)
6. Signal/Spectrum Analyzer (if available)

Important Pins for this experiment

PIN 4 SCF#2 Output
PIN 6 SCF#2 Clock
PIN 7 SCF#2 In
PIN 10 **GROUND**
PIN 17 SCF#1 Output
PIN 18 SCF#1 In
PIN 19 SCF#1 Clock
PIN 30 $\mathbf{V_{DD}}$ (+5 Volts)

NOTE: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

DO NOT APPLY SIGNALS TO THE CHIP WITHOUT POWER AND GROUND APPLIED TO THE IC. TO DO SO MAY SET UP UNWANTED LATCH-UP PATHS THAT COULD RESULT IN IMMEDIATE DESTRUCTION OF THE IC!

PROCEDURE

Simulation

1. Simulation of the circuit is the first step toward understanding the actual operation of the switched capacitor circuit, and hence understanding the outcome of the measurements. The switched capacitor network should be simulated with an identical set of model parameters compared with those to be measured. As a prelude to the actual measurements, the simulation conditions are to be set for a 2.0 volt peak to peak 1.0 KHz sinusoidal input signal with a 1.0 volt dc offset. To place the output of the filter response well within the passband of the characteristic, the clock frequency for this circuit can be set to 50 KHz. The input clock should exhibit a 0 to 5 volt swing with 1 microsecond rise and fall times and a 50% duty cycle. The pulse width and duration should be appropriate for a 50 KHz clock frequency. The duration of the simulation should be at least three

clock cycles to observe the resulting waveform in a steady-state condition (that is, free from any numerical start-up conditions). Repeat the simulation for input frequencies of 5.0 KHz and 20 KHz. Observe the output waveform response both in magnitude and phase.

Measurement

NOTE*: You can use either of the circuits for measurement; they are identical.*

2. **Adjust** the dc power supply for a +5.0 volt output. **Verify** using either an oscilloscope or a voltmeter the correct output voltage (+5.0) **before** applying the power supply leads to the IC.

Configure the input clock function generator so that it provides a 0 to 5.0 volt square wave signal at 50 KHz. **Verify** using the oscilloscope that you have the correct amplitude signal. Be sure that the power supply is energized **before** applying the input clock signal. Apply the clock signal to the appropriate pin on the test IC.

Prepare a signal from the function generator that will be used as input to the switched capacitor network. This signal from the function generator should be a 1 volt peak (with a 1 volt dc offset) 0.5 KHz sinusoid. **Verify** using the oscilloscope that you have the correct amplitude signal before applying the input to the circuit. Be sure the power supply is energized **before** applying this signal. This input signal should place you well within the passband of the filter. Connect the signal from the function generator to the circuit and observe the waveform on the oscilloscope. Record the amplitude and sketch the output waveform. While observing the oscilloscope, decrease the clock frequency from 50 KHz to 10 KHz. You should see a dramatic change in the shape of the output waveform. Sketch one cycle of this waveform (with a 10 KHz clock rate), then return the clock frequency to 50 KHz.

3. Connect the output of the switched capacitor network to both the oscilloscope and the signal analyzer. Keeping the amplitude of the input signal the same (clock at 50 KHz), slowly increase the frequency of the input signal from 0.5 KHz while observing both the oscilloscope and the signal analyzer traces. The signal analyzer should indicate a variety of signal components, some changing as the input signal changes, others remaining constant. The oscilloscope trace shows a decrease in the number of samples per cycle as the input frequency increases.

Continue to increase the input signal frequency and observe the output of the filter. Record the - 3dB frequency of the network, and enough data so that you can sketch the magnitude response of the network. At some frequency, the stationary frequency component (clock) and the dynamic frequency component (input) will become equal. Sketch the output trace of the oscilloscope and make a note of the frequency where this occurs. Now, continue increasing the input signal frequency and observe the output waveform on the oscilloscope. Continue to record enough information to determine the magnitude response of the circuit. Sketch the magnitude response of the network for frequencies between 1 Hz and 50 KHz.

4. Adjust the frequency generator for a 0.5 KHz input signal and the clock for a 10 KHz sampling rate. Reduce the input ac component of the input signal to its minimum value, keeping the dc offset at 1 volt. Observe the output waveform on the oscilloscope. Determine the origin of the signal observed on the oscilloscope.

5. Increase the amplitude of the input signal to 1 volt peak (with a 1 volt offset). Adjust the signal frequency to 0.5 KHz and determine the -3 dB point of the filter using the same procedure as above (clock at 10 KHz). Record this cutoff frequency.

QUESTIONS

1. Describe why the 0.5 KHz input waveform observed in Section 2 changed so dramatically when the clock frequency varied from 50 KHz to 10 KHz. Refer to your waveform sketch in your explanation.

2. Determine the ratio C_2/C_1 for the single pole filter from the information introduced in the Introduction.

3. Describe the waveform that you observe as the input signal approaches the stop band of the filter in Section 3.

4. What is the relationship between the frequency of minimum filter output and the clock frequency (Section 3)?

5. Determine the ratio of the - 3dB frequency to the clock frequency for all the data taken in Section 5. Comment on the results.

SPICE Listing for Switched Capacitor Filter

```
*** SPICE DECK created from scfilt4a.sim, tech=scmos
M1 5 4 5 0 CMOSN L=2.0U W=10.0U
M2 7 6 5 0 CMOSN L=4.0U W=10.0U
M3 9 8 7 0 CMOSN L=4.0U W=10.0U
M4 9 10 9 0 CMOSN L=2.0U W=10.0U
M5 12 11 13 0 CMOSN L=2.0U W=10.0U
M6 14 11 15 0 CMOSN L=2.0U W=10.0U
M7 15 8 5 0 CMOSN L=4.0U W=10.0U
M8 15 10 15 0 CMOSN L=2.0U W=10.0U
M9 15 4 15 0 CMOSN L=2.0U W=10.0U
M10 9 6 15 0 CMOSN L=4.0U W=10.0U
M11 1 16 17 1 CMOSP L=2.0U W=4.0U
M12 17 6 8 1 CMOSP L=2.0U W=4.0U
M13 1 8 18 1 CMOSP L=2.0U W=4.0U
M14 1 6 4 1 CMOSP L=2.0U W=4.0U
M15 18 19 6 1 CMOSP L=2.0U W=4.0U
M16 8 16 0 0 CMOSN L=2.0U W=3.0U
M17 8 6 0 0 CMOSN L=2.0U W=3.0U
M18 6 8 0 0 CMOSN L=2.0U W=3.0U
M19 6 19 0 0 CMOSN L=2.0U W=3.0U
M20 1 16 19 1 CMOSP L=2.0U W=4.0U
M21 1 8 10 1 CMOSP L=2.0U W=4.0U
M22 4 6 0 0 CMOSN L=2.0U W=4.0U
M23 19 16 0 0 CMOSN L=2.0U W=4.0U
M24 10 8 0 0 CMOSN L=2.0U W=4.0U
M25 1 20 20 1 CMOSP L=3.0U W=10.0U
M26 1 20 21 1 CMOSP L=3.0U W=66.0U
M27 1 20 22 1 CMOSP L=3.0U W=66.0U
M28 1 20 23 1 CMOSP L=3.0U W=133.0U
M29 20 0 0 1 CMOSP L=45.0U W=3.0U
M30 21 24 25 1 CMOSP L=3.0U W=92.0U
M31 26 9 21 1 CMOSP L=3.0U W=92.0U
M32 22 23 0 1 CMOSP L=3.0U W=183.0U
M33 23 26 0 0 CMOSN L=3.0U W=267.0U
M34 25 25 0 0 CMOSN L=3.0U W=67.0U
M35 26 25 0 0 CMOSN L=3.0U W=67.0U
C36 9 0 1.755000PF
C37 13 0 0.111000PF
C38 19 0 0.051000PF
C39 6 0 0.312000PF
C40 8 0 0.288000PF
C41 12 0 0.277000PF
C42 16 0 0.038000PF
C43 18 0 0.004000PF
C44 17 0 0.004000PF
C45 15 0 0.189000PF
C46 20 0 0.062000PF
C47 7 0 0.053000PF
C48 26 0 1.840000PF
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C49 22 0 0.519000PF
C50 21 0 0.463000PF
C51 14 0 0.199000PF
C52 25 0 0.416000PF
C53 23 0 0.888000PF
C54 5 0 0.146000PF
C55 11 0 0.077000PF
C56 24 0 0.104000PF
C57 4 0 0.216000PF
C58 10 0 0.200000PF
* This resistor models the non-zero resistance of the operational
* amplifier feedback loop in polysilicon
RFEED 24 23 10
* This is an abbreviated node table
*  CMOSN         0
*  CMOSP         1
*  phi1   6
*  phi2   8
*  clock  16
*  GND  0
*  Vdd   1
*  out    23
*  vin    5
*  Control 11
*  rfeedin        24
*  phi1b 4
*  phi2b 10
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
Vdd 1 0 dc 5.0
Vin 5 0 sin(2 1 1e4)
Vclock 16 0 pulse(0 5 0 1u 1u 10u 20u)
Vctrl 11 0 dc 5.0
.width out=80
.tran 3e-4 1e-6
.plot tran v(5) v(16) v(23)
* The following "probe" line is for those using PSPICE with PROBE Option
* .probe
.end
```
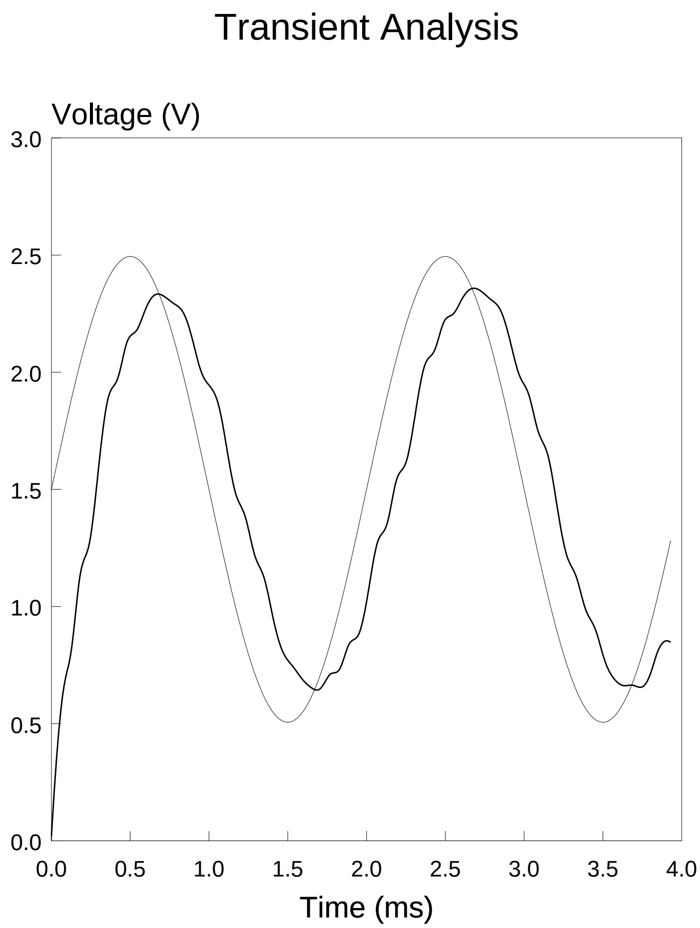

TRANSIENT ANALYSIS EXAMPLE

The following plot shows a SPICE simulation similar to the one described above, but using a 0.5 KHz input signal with a 1.5 volt DC offset and a 1 volt peak amplitude. Note the corresponding DC offset on the output voltage as well as the reduced amplitude and phase shift, indicating that the signal is being attenuated by the switched capacitor network.

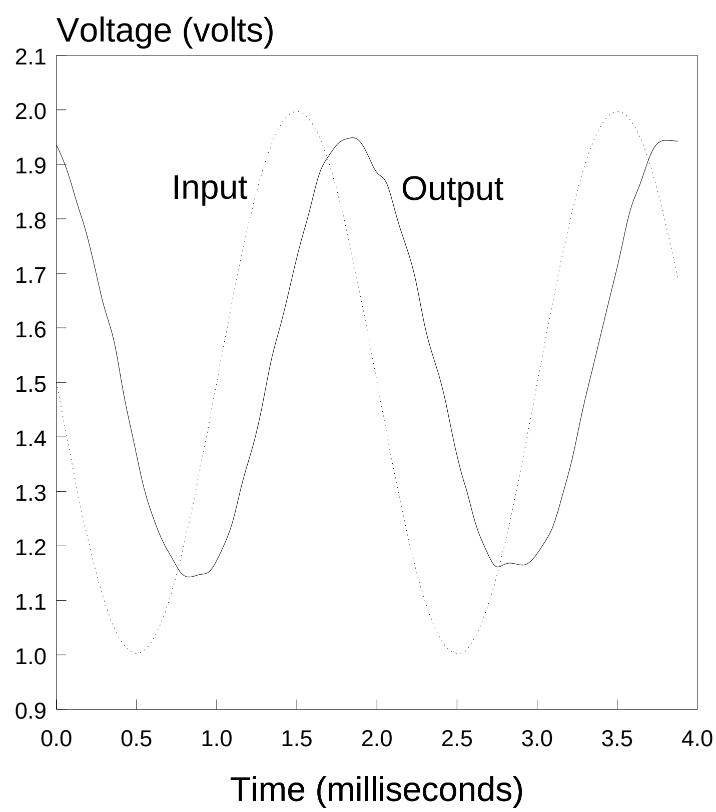


Filter Output Bold

Measured Transient Response

The following figure illustrates the time response of the switched capacitor filter. The input signal is designated with the dashed line, the output signal with the solid line. The input conditions are similar to those used in the simulated response discussed previously. Note that in both the measured and simulated response the the input signal is below the -3dB frequency, but the amplitude is still affected by the switched capacitor network. In addition, there is a small phase shift evident on the output signal. The signal was measured using an HP-3314A function generator and a Tektronix 2230 Digital Storage Oscilloscope.

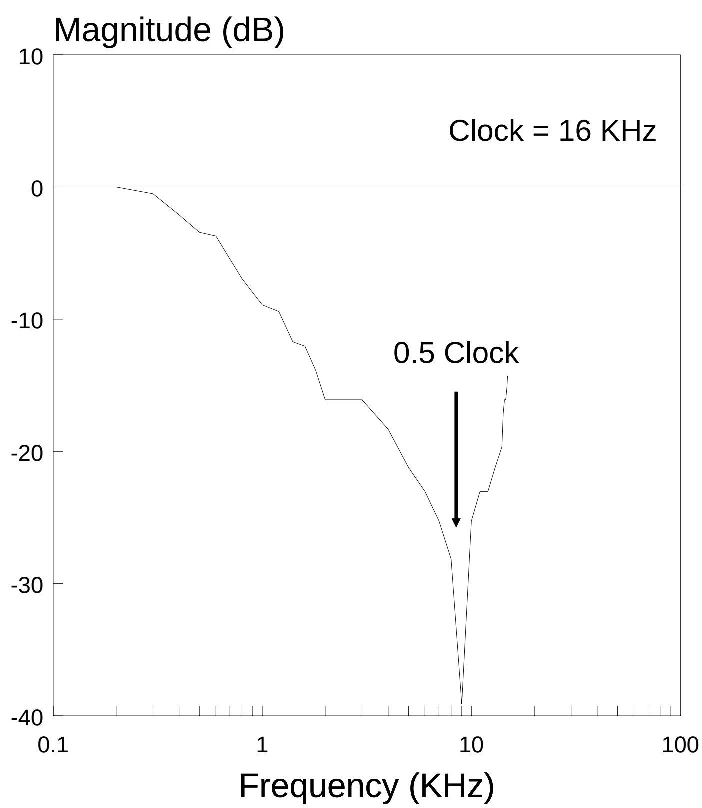
Switched Capacitor Filter
Measured Response



Measured ac Frequency Response

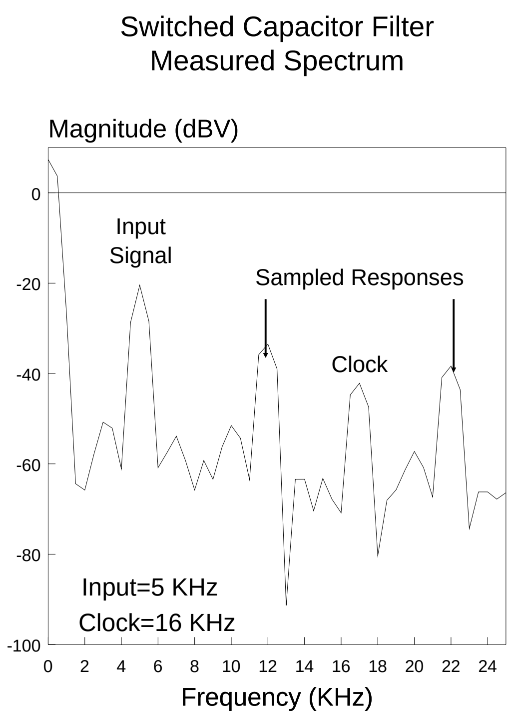
The input was swept in frequency from 10 Hz to 14 KHz to determine the frequency response of the switched capacitor network. An HP-3314A function generator (in sweep mode) and an HP-3561A Dynamic Signal Analyzer was used for these measurements. The measured spectrum is shown in the figure below. Notice the stop band for the filter occurs at one-half the clock frequency and that the ac response begins to increase as the frequency increases beyond this point. The -3dB frequency is approximately 1 KHz. The stop band is approximately 40 dB down from the passband.

Switched Capacitor Filter
Measured Transfer Function

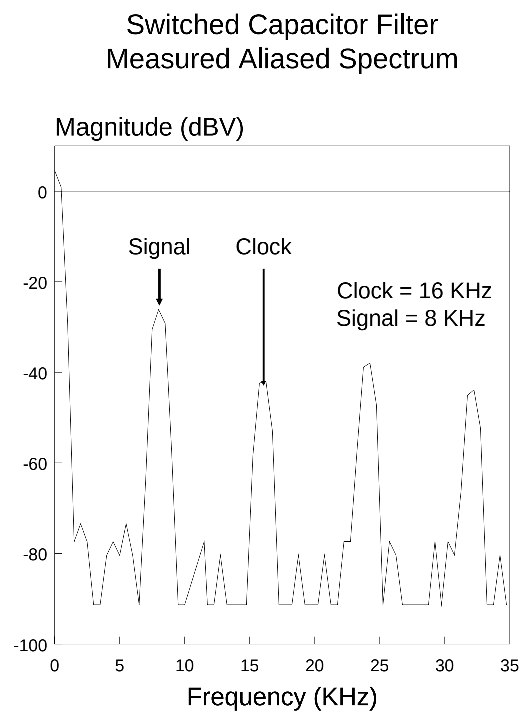


Measured Spectral Response
Unaliased and Aliased Output Responses

Measurements of the output response of the switched capacitor network with the input signal frequency below the Nyquist frequency and at the Nyquist frequency were made. An HP-3314A function generator and an HP-3561A Dynamic Signal Analyzer were used for these measurements. The results, indicated in the figures below, show the effect of aliasing on the signal. The unaliased signal shows the input signal component at 5 KHz (clock at 16 KHz) as well as the sampled responses at 16 KHz ± 5 KHz. The aliased signal shows both the sampled response as well as the original signal at 8 KHz (16 KHz ± 8 KHz), showing the overall effects of aliasing on the output of the filter.



Unaliased Signal



Aliased Signal