Analog Design Resource Kit Tutorial 5

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CMOS RING OSCILLATORS

Simulation and Measurement

Objective: To simulate and observe the operation of a CMOS adjustable ring oscillator.

Introduction

A. The simple ring oscillator

Ring oscillators are used for a variety of purposes. One application of ring oscillators is to determine inverter time delays as a means to evaluate the CMOS fabrication process. Other applications are for use as an internally generated clocking source, or as a stage in a more complex system such as a voltage controlled oscillator (VCO) or a phase locked loop (PLL).

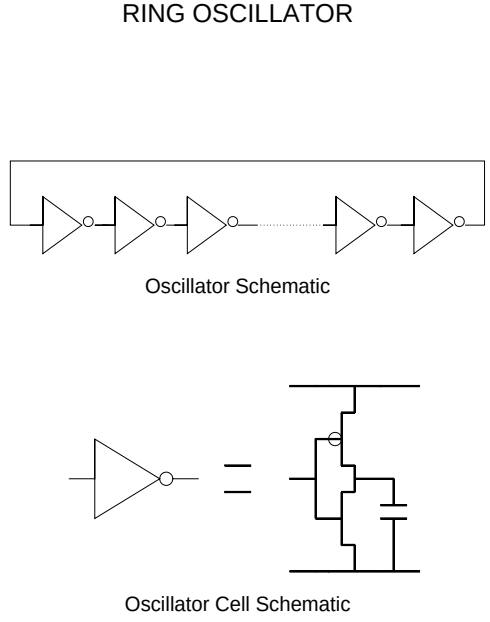


Figure 1

The simplest ring oscillator contains an odd number of cascaded inverters, with the output of the cascade fed back to the input of the inverter chain (Figure 1). In this configuration, the oscillator frequency is completely dependent on the inherent inverter time delay and is therefore not externally controllable. This feature can be seen using the following simple explanation for an N stage ring oscillator. The inverter pair delay is a function of the charge and discharge rate of the driving circuit and the capacitive load C (driven circuit) that it sees [1]:

$$\tau_R = \frac{4C}{K_P (\frac{W}{L})_P V_{DD}} \tag{1}$$

for the rise time and

$$\tau_F = \frac{4C}{K_N (\frac{W}{L})_N V_{DD}} \tag{2}$$

for the fall time, where $K_{N,P}$ is the N(P) intrinsic transconductance and $(\frac{W}{L})_{N,P}$ is the N(P) aspect ratio. The frequency of oscillation for odd-N of such inverters is simply the inverse of the sum of the inverter pair delays $(\tau_R + \tau_F)$ for each inverter:

$$f_{osc} = \frac{1}{N(\tau_R + \tau_F)} \tag{3}$$

If the aspect ratios of the each inverter are adjusted so that $K_N(\frac{W}{L})_N = K_P(\frac{W}{L})_P$ (symmetric switching), then the oscillation frequency can be written simply as:

$$f_{osc} = \frac{V_{DD} K_N (\frac{W}{L})_N}{8NC} \tag{4}$$

Typical 2 micron CMOS inverters exhibit an input capacitance C of about 0.1 pF and, using a unity aspect ratio for the nFET, a 19-stage ring oscillator would oscillate at approximately 16 MHz. Increasing the number of stages or increasing the load

capacitance will lower the oscillator frequency. Figure 2 shows the results of a SPICE simulation on a 19 stage ring oscillator, showing the shape of the output waveform.

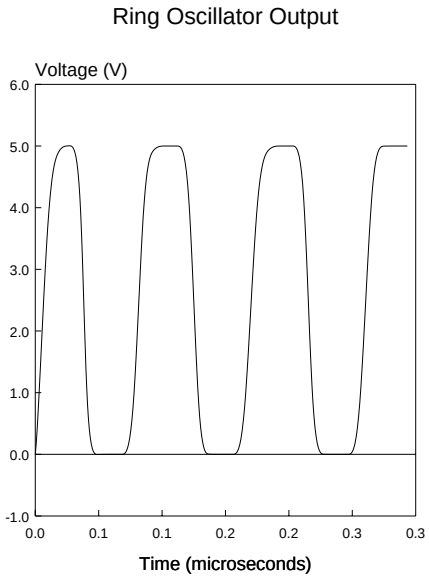


Figure 2

B. Adjustable Ring Oscillator

The oscillation frequency of a ring oscillator can be controlled in several ways, but all are based on controlling the rise and fall times of the inverters in the cascade. One of the simplest means to adjust these times is by adding an nFET in series with the output of each inverter (Figure 3).

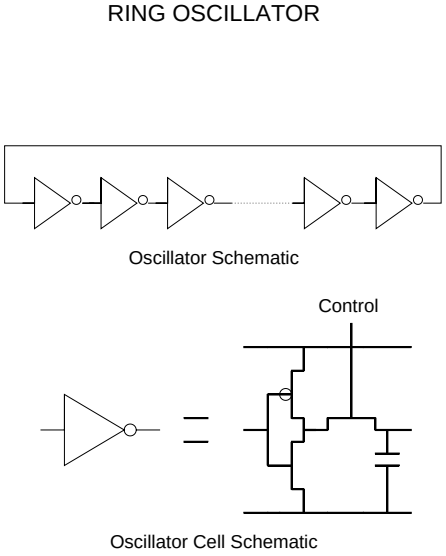


Figure 3

By controlling the gate voltage on this series transistor, the rise and fall times will increase or decrease (depending on the controlling gate voltage), thereby effectively varying the frequency of oscillation. The SPICE listing in the Appendix of this tutorial describes a 19 stage ring oscillator with frequency adjust (control line labeled "Vbias" on node 8).

Figure 4 shows the output of this 19 stage ring oscillator, plotted with the bias control on the series nFET. The maximum frequency of oscillation occurs for a control voltage of 5.0 volts (minimum time delay), and the oscillation frequency decreases with decreasing control voltage. The minimum frequency of oscillation is determined by the loop gain, which is controlled by the series nFET [2]. Therefore, there will be some minimum level of control voltage that must be achieved for oscillator self start-up.

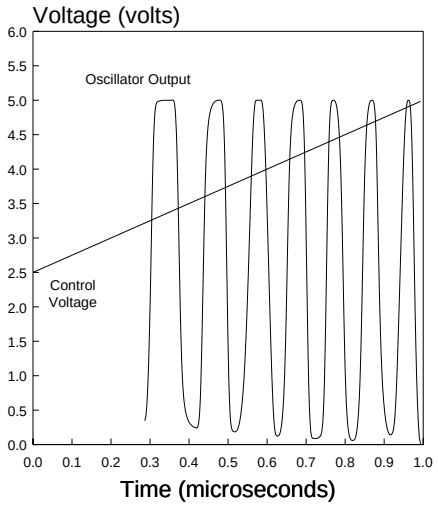


Figure 4

EQUIPMENT and PINOUT

Equipment

1. Design board with test IC
2. DC power supply (5.0 volt minimum)
3. DC power source (0 to 5.0 volts for bias control voltage)
4. Oscilloscope (voltmeter if available)
5. Frequency Counter (if available)

Important Pins for this experiment

PIN 10 **GROUND**
PIN 26 Ring Oscillator Output
PIN 27 Ring Oscillator Frequency Adjust
PIN 30 **V_{DD} (+5 Volts)**

NOTE: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

DO NOT APPLY SIGNALS TO THE CHIP WITHOUT POWER AND GROUND APPLIED TO THE IC. TO DO SO MAY SET UP UNWANTED LATCH-UP PATHS THAT COULD RESULT IN IMMEDIATE DESTRUCTION OF THE IC!

PROCEDURE

Simulation

1. The circuit "ringosc" is a 19-stage adjustable ring oscillator connected to the digital output driver pad of the chip set. The simulation of the adjustable ring oscillator differs from simulations in the previous tutorials in several ways. First, there are no time-varying inputs that must be specified (although the nFET control voltage must be specified). Secondly, because of the feedback nature of the oscillator, initial conditions must be set in order that the simulator achieve DC convergence during bias-point calculations. Only the input voltage of one of the inverters need be specified (see sample SPICE file in the Appendix), and it can be either 0.0 or 5.0 volts. The bias voltage on the series FET must also be specified, either as a DC source or some time-varying waveform (i.e., pulse or piece-wise linear). The output of the ring oscillator is taken from a buffer inverter not in the oscillator inverter chain. This buffer inverter isolates the ring oscillator so that the large capacitance associated with the interconnection between the oscillator and the output pad does not significantly affect the oscillation frequency.

For the oscillator on the test chip, determine the oscillation frequency for bias voltages of 3, 4 and 5 volts using SPICE. Also, determine the minimum control voltage necessary for oscillator self-start.

Measurement

1. **Adjust** the dc power supply for a +5.0 volt output. **Verify** using either an oscilloscope or a voltmeter the correct output voltage (+5.0) **before** applying the power supply leads to the IC.

Configure the bias control line so that it provides a +5.0 volt DC level to the series FET control pin. **Verify** using a voltmeter that you have the correct DC level. Be sure that the power supply is energized **before** applying the control signal to the IC.

2. Connect the output of the adjustable ring oscillator to both the oscilloscope and the frequency counter. Record the output oscillator frequency and duty cycle with the 5.0 volt control voltage. Slowly **decrease** the control DC level while observing both the oscilloscope and the frequency counter. Record the output frequency and duty cycle as

you decrease the DC control level in 0.1 volt increments. Note the DC control voltage that causes the ring oscillator to cease oscillation. Sketch the output trace of the oscilloscope for a DC voltage of 4.0 volts and make a note of the frequency of oscillation.

Questions

1. Plot the output frequency as a function of DC control voltage. Determine the dc control voltage the causes the oscillator loop gain to fall below unity. How does this compare with simulated results?

2. Determine the time delay per ring oscillator cell for a DC control voltage of 5.0 volts. Compare this result with the simulation results. Identify and explain the differences, if any, between the two sets of data.

REFERENCES

1. Weste, N. and K. Eshraghian, *Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed.*, Addison-Wesley Publishing Co., Reading, MA., pp. 207-211, 1993.

2. Shoji, M., *CMOS Digital Circuit Technology,* Prentice Hall, Inc., Englewood Cliffs, NJ., pp. 174-177, 1988.

Ring Oscillator SPICE Deck

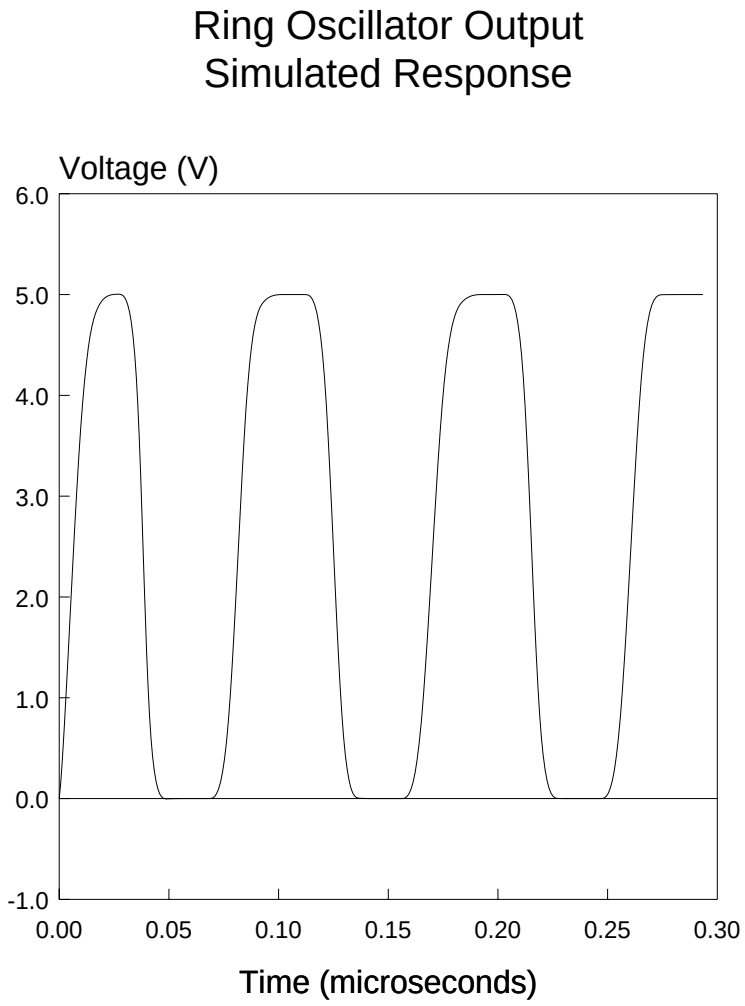
*** *SPICE file created from ringosc.sim, tech=scmos*
M1 1 4 212 1 CMOSP L=2.0U W=3.0U
M2 212 4 0 0 CMOSN L=2.0U W=3.0U
M3 208 8 212 0 CMOSN L=3.0U W=4.0U
M4 1 208 206 1 CMOSP L=2.0U W=3.0U
M5 206 208 0 0 CMOSN L=2.0U W=3.0U
M6 202 8 206 0 CMOSN L=3.0U W=4.0U
M7 1 202 200 1 CMOSP L=2.0U W=3.0U
M8 200 202 0 0 CMOSN L=2.0U W=3.0U
M9 196 8 200 0 CMOSN L=3.0U W=4.0U
M10 1 196 194 1 CMOSP L=2.0U W=3.0U
M11 194 196 0 0 CMOSN L=2.0U W=3.0U
M12 190 8 194 0 CMOSN L=3.0U W=4.0U
M13 1 190 188 1 CMOSP L=2.0U W=3.0U
M14 188 190 0 0 CMOSN L=2.0U W=3.0U
M15 184 8 188 0 CMOSN L=3.0U W=4.0U
M16 1 184 182 1 CMOSP L=2.0U W=3.0U
M17 182 184 0 0 CMOSN L=2.0U W=3.0U
M18 178 8 182 0 CMOSN L=3.0U W=4.0U
M19 1 178 176 1 CMOSP L=2.0U W=3.0U
M20 176 178 0 0 CMOSN L=2.0U W=3.0U
M21 172 8 176 0 CMOSN L=3.0U W=4.0U
M22 1 172 170 1 CMOSP L=2.0U W=3.0U
M23 170 172 0 0 CMOSN L=2.0U W=3.0U
M24 166 8 170 0 CMOSN L=3.0U W=4.0U
M25 1 166 164 1 CMOSP L=2.0U W=3.0U
M26 164 166 0 0 CMOSN L=2.0U W=3.0U
M27 160 8 164 0 CMOSN L=3.0U W=4.0U
M28 1 160 158 1 CMOSP L=2.0U W=3.0U
M29 158 160 0 0 CMOSN L=2.0U W=3.0U
M30 133 8 158 0 CMOSN L=3.0U W=4.0U
M31 1 133 131 1 CMOSP L=2.0U W=3.0U
M32 131 133 0 0 CMOSN L=2.0U W=3.0U
M33 1 133 68 1 CMOSP L=2.0U W=3.0U
M34 68 133 0 0 CMOSN L=2.0U W=3.0U
M35 65 8 68 0 CMOSN L=3.0U W=4.0U
M36 1 65 63 1 CMOSP L=2.0U W=3.0U
M37 63 65 0 0 CMOSN L=2.0U W=3.0U
M38 60 8 63 0 CMOSN L=3.0U W=4.0U
M39 1 60 58 1 CMOSP L=2.0U W=3.0U
M40 58 60 0 0 CMOSN L=2.0U W=3.0U
M41 55 8 58 0 CMOSN L=3.0U W=4.0U
M42 1 55 53 1 CMOSP L=2.0U W=3.0U
M43 53 55 0 0 CMOSN L=2.0U W=3.0U
M44 50 8 53 0 CMOSN L=3.0U W=4.0U
M45 1 50 48 1 CMOSP L=2.0U W=3.0U
M46 48 50 0 0 CMOSN L=2.0U W=3.0U
M47 45 8 48 0 CMOSN L=3.0U W=4.0U
M48 1 45 43 1 CMOSP L=2.0U W=3.0U
M49 43 45 0 0 CMOSN L=2.0U W=3.0U
M50 40 8 43 0 CMOSN L=3.0U W=4.0U

```
M51 1 40 38 1 CMOSP L=2.0U W=3.0U
M52 38 40 0 0 CMOSN L=2.0U W=3.0U
M53 35 8 38 0 CMOSN L=3.0U W=4.0U
M54 1 35 33 1 CMOSP L=2.0U W=3.0U
M55 33 35 0 0 CMOSN L=2.0U W=3.0U
M56 30 8 33 0 CMOSN L=3.0U W=4.0U
M57 1 30 28 1 CMOSP L=2.0U W=3.0U
M58 28 30 0 0 CMOSN L=2.0U W=3.0U
M59 4 8 28 0 CMOSN L=3.0U W=4.0U
C60 172 0 0.038000PF
C61 170 0 0.043000PF
C62 48 0 0.043000PF
C63 50 0 0.037000PF
C64 190 0 0.040000PF
C65 188 0 0.043000PF
C66 133 0 0.128000PF
C67 33 0 0.043000PF
C68 35 0 0.037000PF
C69 200 0 0.043000PF
C70 202 0 0.040000PF
C71 160 0 0.038000PF
C72 158 0 0.043000PF
C73 58 0 0.043000PF
C74 60 0 0.037000PF
C75 178 0 0.038000PF
C76 176 0 0.043000PF
C77 68 0 0.043000PF
C78 43 0 0.043000PF
C79 45 0 0.037000PF
C80 196 0 0.040000PF
C81 194 0 0.043000PF
C82 28 0 0.043000PF
C83 30 0 0.037000PF
C84 212 0 0.043000PF
C85 4 0 0.084000PF
C86 131 0 0.090000PF
C87 166 0 0.038000PF
C88 164 0 0.043000PF
C89 53 0 0.043000PF
C90 55 0 0.037000PF
C91 184 0 0.040000PF
C92 182 0 0.043000PF
C93 38 0 0.043000PF
C94 40 0 0.037000PF
C95 206 0 0.043000PF
C96 208 0 0.040000PF
C97 8 0 0.232000PF
C98 63 0 0.043000PF
C99 65 0 0.037000PF
*  CMOSN          0
*  CMOSP          1
*  GND  0
*  OUT  131
*  Vdd   1
```

```
*  Vbias  8
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
Vdd 1 0 dc 5
Vbias 8 0 pulse(5 4 .2u 1n 1n .8u 1.2u)
* Initial conditions set on input capacitor to one inverter to aid dc convergence
* of the initial or start-up state of the ring oscillator
.ic v(160)=0.0
.tran 1n 0.75u uic
.plot v(160) v(8)
* The following "probe" line is for those using PSPICE with PROBE Option
*.probe
.end
```

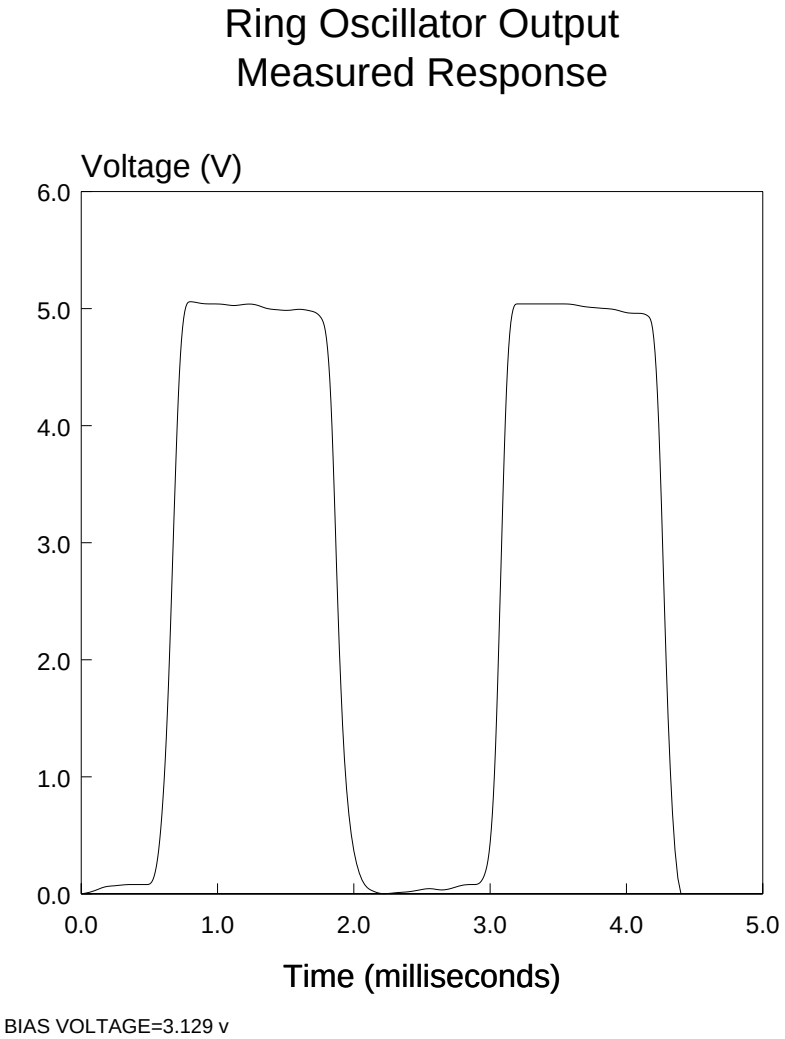
Simulated Response of the Ring Oscillator

The following figure shows the simulated response of the ring oscillator. The bias control voltage is approximately 5 volts, with a corresponding oscillator of approximately 13 MHz. This result agrees favorably with the maximum frequency of oscillation measured on the fabricated chip.



Measured Response of the Ring Oscillator

The response of the ring oscillator at a particular bias control voltage was measured using a Tektronix 2230 Digital Storage Oscilloscope. A bias voltage of 3.129 V was applied to the series transistor. The resulting oscillator frequency is approximately 450 Hz. Changing the bias voltage to 3.03 V yields a 125 Hz signal; a 4.2 volt bias voltage a 6.8 MHz signal. The graph on the next page summarizes the oscillator frequency-bias control voltage relationship.



Measured Ring Oscillator Frequency
Effect of Bias Control Voltage

The output frequency of the ring oscillator as a function of bias control voltage was measured to determine the range of the oscillator. The figure below shows that the oscillator functioned between approximately 0.2 KHz to over 20 MHz. The bias voltages between 3.0 and 4 volts governed the output frequency over the widest range. The voltage variation over this range forces the series nFET into a high resistance (as well as nonlinear) mode of operation, causing the charge/discharge rate of the shunt capacitance to slow dramatically, thereby decreasing the oscillation frequency of the circuit.