# Analog Design Resource Kit Tutorial 6

*Robert H. Caverly*
*Department of Electrical and Computer Engineering*
*University of Massachusetts Dartmouth*
*N. Dartmouth, MA 02747-2300*
*caverly@micron.ece.umassd.edu*

## 4 BIT CMOS CHARGE SCALING DIGITAL TO ANALOG CONVERTER

**Objective:** To observe the operation of a 4-bit digital to analog converter (DAC) using CMOS charge scaling techniques.

**Introduction:**

Data conversion devices are used to convert real world analog signals into a digital representation, a useful technique in a number of areas of signal processing. The basic circuit in the data conversion field is the digital to analog converter (DAC) which translates a digital representation of a signal into its analog equivalent. Many analog to digital converter (ADC) circuits use the DAC as a component in the overall system.

DAC circuits are characterized by a number of parameters such as *dynamic range* (DR), *resolution* (RES), *full scale range* (FSR), *signal to noise ratio* (SNR), *offset error*, *gain error* and *nonlinearity* [1]. Many of these parameters are functions of the number of bits used to represent the analog signal (namely DR and SNR), others are based on the actual circuit construction (errors and linearity). Figure 1 shows an idealized example of the various static errors (offset, gain and linearity) that can be encountered with a DAC [1]. In the figure, the **bold line** represents the ideal DAC transfer characteristic. Gain error, as the name implies, causes an increase (or a decrease) in the full scale output value of the circuit. Offset error describes a shift in the transfer characteristic from its ideal case. Linearity describes the deviation from the ideal case.

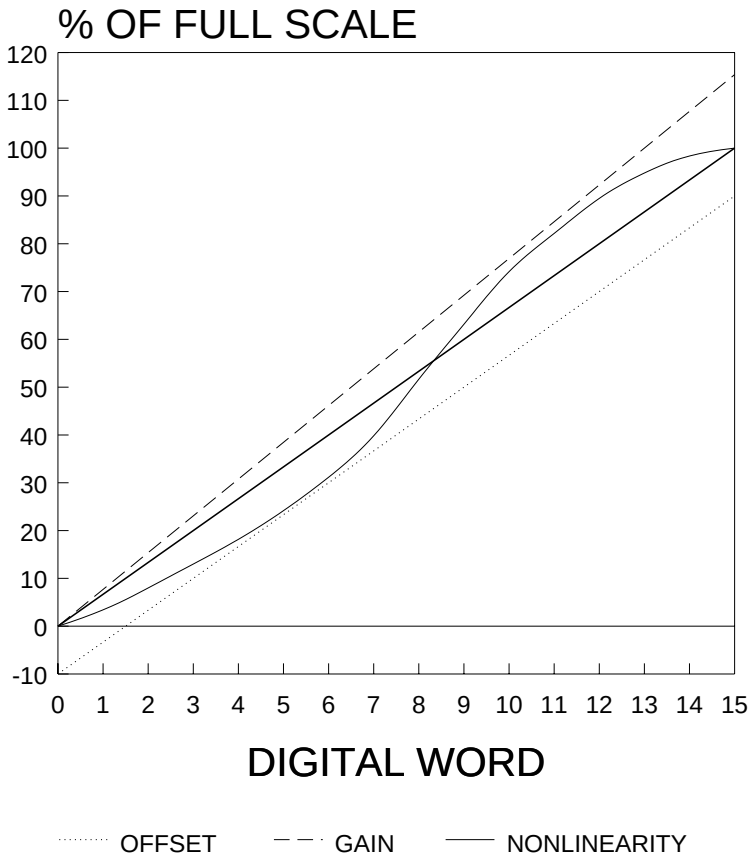



**Figure 1**

There are a variety of methods for accomplishing digital to analog conversion, usually by applying a scaling technique to current, voltage or charge (or some combination of techniques) [1,2]. One widely used technique for an integrated DAC uses the charge scaling technique employing switched capacitors. In this technique, capacitors are conditionally charged or discharged (depending on the digital status word) on one phase of the clock, then the charge redistributes throughout the circuit on the second phase of the clock, resulting in voltage developed that is dependent on the digital status word. As an example, consider the 4 bit DAC shown in Figure 2 where the digital status word is represented by the digital coefficients $a_i$. On the first phase of the clock (ph1 or $\Phi_1$) the capacitors are either charged to the reference voltage $V_{REF}$ ($a_i$ equal a logic 1) or discharged to ground ($a_i$ equal a logic 0). The total charge stored on the capacitors at the end of the first clock phase may be written as:

# 4 Bit Switched Capacitor Digital to Analog Converter

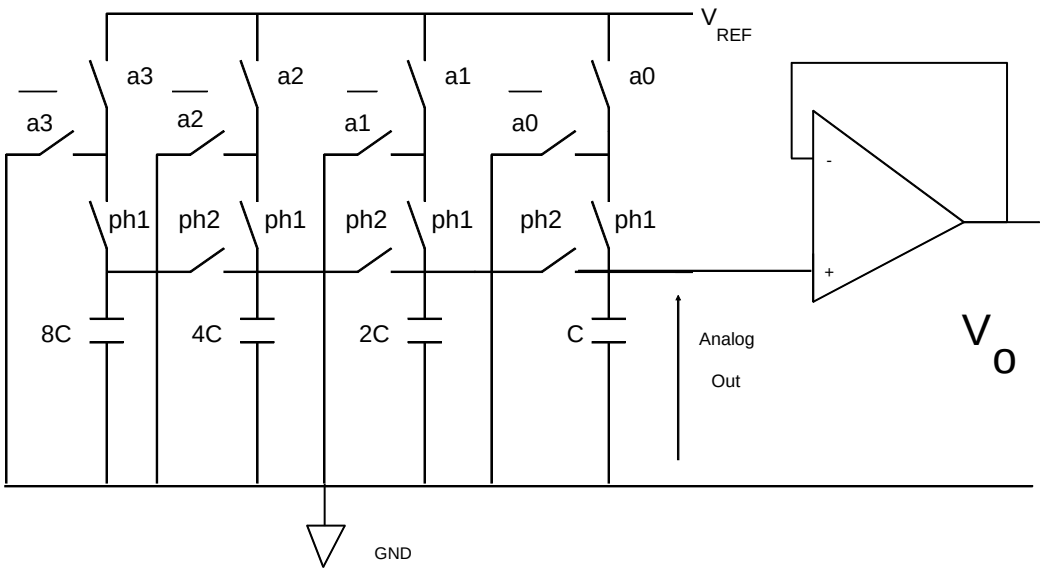



**Figure 2**

$$Q(\varphi_1) = CV_{REF}[8a_3 + 4a_2 + 2a_1 + a_0] = CV_{REF}\sum_{i=0}^{3} 2^i a_i \qquad (1)$$

On the second phase of the clock (ph2 or $\Phi_2$), the capacitors are then connected in parallel by the switches. The charge redistributes among the parallel capacitors so that at the end of the second phase, the total charge is

$$Q(\varphi_2) = 15CV_O \qquad (2)$$

For the ideal DAC, there is no charge loss from phase to phase of the clock $[Q(\varphi_1) = Q(\varphi_2)]$ so that the output voltage $V_O$ may be written as

$$V_O = \frac{V_{REF}}{2^4 - 1}\sum_{i=0}^{3} 2^i a_i \qquad (3)$$

Equation 3 has been written assuming that the capacitors are scaled exactly as shown in Figure 2. In practice, however, these capacitors are closely, but not exactly, matched. This capacitance mismatch affects the DAC linearity, and ultimately limits the number of bits and hence the analog resolution. Most of the possible errors of the DAC are to some degree influenced by this capacitance mismatch. A good process will have component matching in the range of 0.1% to 1%, sufficient for reasonably accurate 8 bit DACs [1]. The ideal response for a 4 bit switch capacitor or charge scaling DAC is shown in Figure 3. This tutorial is based on a switched capacitor or charge scaling DAC of this type. This DAC has been laid out and is available on the test integrated circuit.

4 BIT DAC
Ideal DAC Response

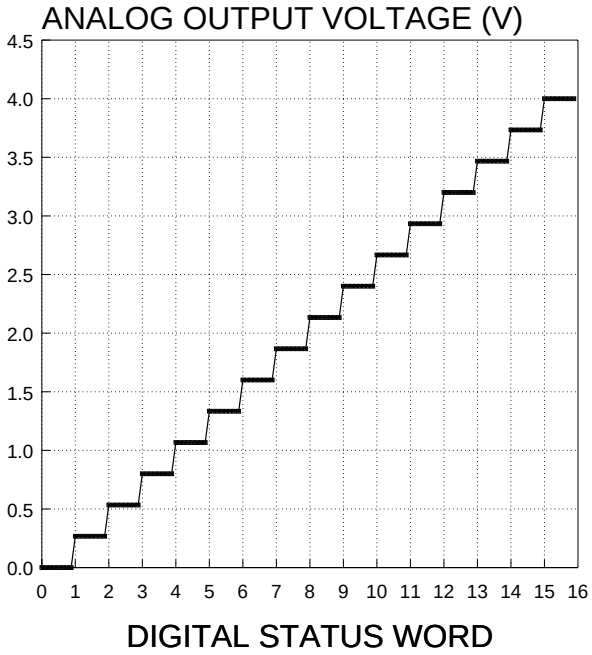



**Figure 3**

## EQUIPMENT and PINOUT

### Equipment

1. Design board with chip set IC
2. 4 Bit Counter Chip (TTL or CMOS for toggling inputs)
3. Oscilloscope
4. 5.0 volt power supply (if not included on design board)
5. Function Generator set for square wave modulation

### Important Pins for this experiment

| | |
|---|---|
| **PIN 10** | **GROUND** |
| **PIN 30** | **$V_{DD}$ (+5 Volts)** |
| PIN 31 | DAC Clock Input |
| PIN 32 | DAC Analog Output |
| PIN 34 | DAC a0 Input (LSB) |
| PIN 36 | DAC a1 Input |
| PIN 37 | DAC a2 Input |
| PIN 38 | DAC a3 Input (MSB) |

***NOTE***: **DO NOT EXCEED 5 VOLTS OR GO BELOW 0 VOLTS ON ANY PIN ON THE TEST IC. TO DO SO CAN RESULT IN IMMEDIATE DESTRUCTION OF THE IC!!**

**ALSO, DO NOT APPLY ANY VOLTAGE TO THE TEST CHIP WITH THE POWER TO THE CHIP OFF. THIS COULD CAUSE LATCH-UP TO OCCUR, WITH THE POSSIBLE CONSEQUENCE OF CHIP DESTRUCTION.**

## PROCEDURE

### Measurements

1. **Adjust** the dc power supply for a +5.0 volt output. **Verify** using either an oscilloscope or a voltmeter the correct output voltage (+5.0) **before** applying the power supply leads to the IC.

Configure the clock function generator so that it provides a 0 to 5.0 volt square wave signal at 50 KHz. **Verify** using the oscilloscope that you have the correct amplitude signal. Be sure that the test chip's power supply is energized **before** applying the input clock signal to the test chip. Apply the clock signal to the appropriate pin on the test IC.

Configure the 4 bit counter chip to provide a count up signal of 0000 to 1111, assuming a logic "0" is ground and a logic "1" is 5.0 volts. Clock the counter chip with a 1.0 KHz signal. Refer to the appropriate data book for the counter chip that you are using (TTL, CMOS) for the proper pin configuration. A sample circuit configuration is shown below. Do not apply the digital lines to the test chip at this time **unless** the test chip power supply is energized.

2. Apply the 50 KHz clock signal and the digital word lines to the appropriate pins on the test IC. Be sure that the test chip power supply is energized **before** applying the digital signals and the 50 KHz clock to the test chip. Connect the oscilloscope to the analog output of the 4 bit DAC.

Record the output levels for each digital word. From these data, determine the SNR (in dB), dynamic range (in dB), offset error (percentage of full scale), the gain error (percentage of full scale) and the integral nonlinearity (in terms of LSBs) of the DAC. Assume a full scale value of 4.0 volts. Definitions for these DAC parameters may be found in various textbooks [see, for example, Ref. 1].

Sample DAC Circuit Configuration

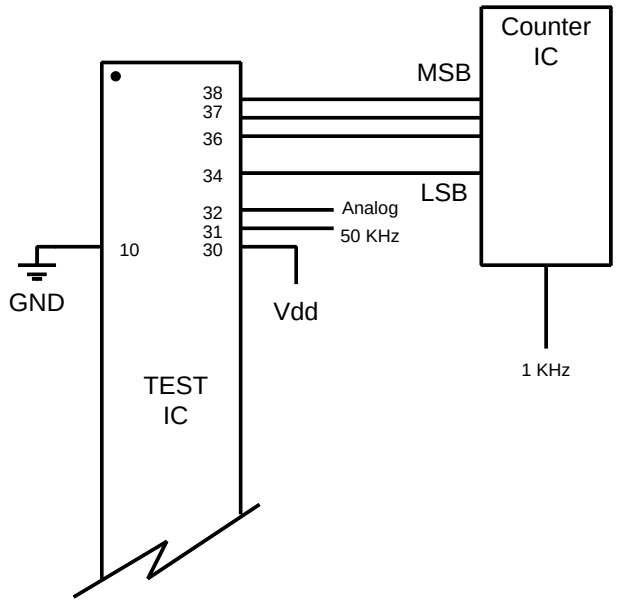



**FIGURE 4**

## REFERENCES

1. Geiger, R., P. Allen and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill Publishing Co., New York, 1990.

2. Haskard, M. and I. May, *Analog VLSI Design: nMOS and CMOS*, Prentice Hall, New York, 1988.

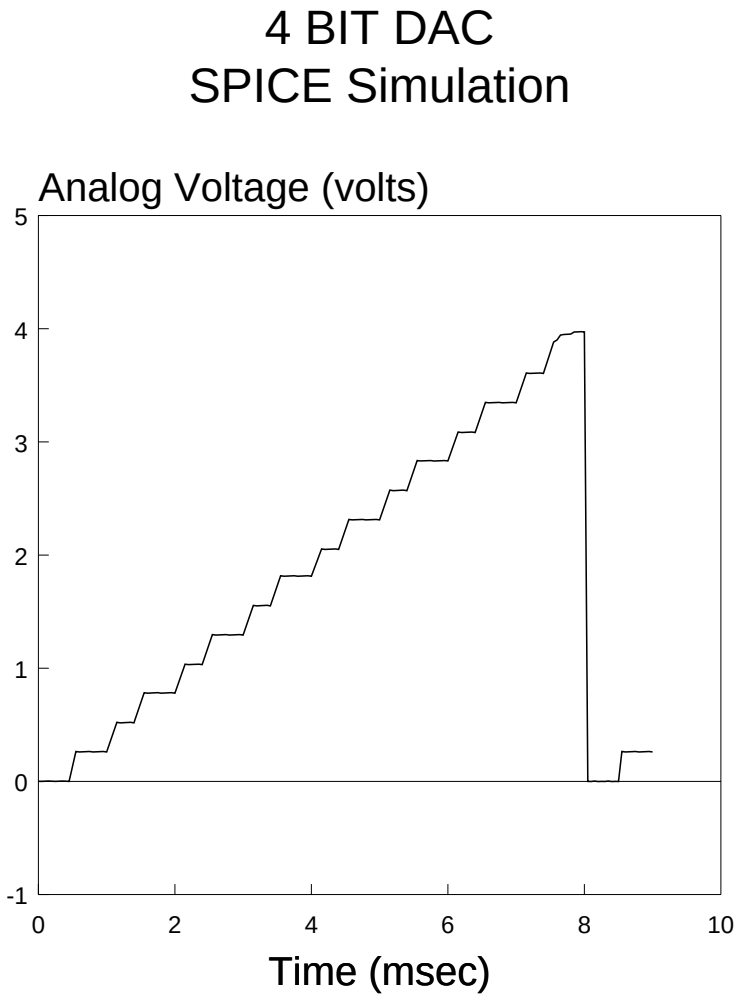
**SPICE Deck for Simulating the Switched Capacitor 4 Bit Digital to Analog Converter**

```
*** 4 Bit DAC W/O BUFFER
M1 1 13 2 0 CMOSN L=2U W=2U
M2 1 12 4 0 CMOSN L=2U W=2U
M3 1 11 6 0 CMOSN L=2U W=2U
M4 1 10 8 0 CMOSN L=2U W=2U
M5 2 23 0 0 CMOSN L=2U W=2U
M6 4 22 0 0 CMOSN L=2U W=2U
M7 6 21 0 0 CMOSN L=2U W=2U
M8 8 20 0 0 CMOSN L=2U W=2U
M9 2 31 3 0 CMOSN L=2U W=2U
M10 4 31 5 0 CMOSN L=2U W=2U
M11 6 31 7 0 CMOSN L=2U W=2U
M12 8 31 9 0 CMOSN L=2U W=2U
M13 3 32 5 0 CMOSN L=2U W=2U
M14 5 32 7 0 CMOSN L=2U W=2U
M15 9 32 7 0 CMOSN L=2U W=2U
C1 9 0 1PF
C2 7 0 2PF
C3 5 0 4PF
C4 3 0 8PF
* Vref  1
* phi1
* phi1 31
* phi2 32
* a0 10
* a1 11
* a2 12
* a3 13
* Out   9
*  These SCN-2.0um parameters taken from MOSIS
.MODEL CMOSN NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5
+ DELTA=1.000000E-06 VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03
+ NFS=2.06E+11 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=31.020000 CGDO=3.173845E-10 CGSO=3.173845E-10 CGBO=4.260832E-10
+ CJ=1.038500E-04 MJ=0.649379 CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000
.MODEL CMOSP PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2
+ DELTA=7.31456 VMAX=17079.4 XJ=0.250000U LAMBDA=1.427309E-02
+ NFS=2.77E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=88.940000 CGDO=2.712940E-10 CGSO=2.712940E-10 CGBO=3.651103E-10
+ CJ=2.375000E-04 MJ=0.532556 CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
* Set up reference voltage, 2 phase clocks and input digital word status
VREF 1 0 DC 5
```

```
VPHI1 31 0 PULSE(0 5 0 1U 1U 8U 40U)
VPHI2 32 0 PULSE(0 5 20U 1U 1U 8U 40U)
VA0 10 0 PULSE(5 0 0 1U 1U 500U 1000U)
VA1 11 0 PULSE(5 0 0 1U 1U 1000U 2000U)
VA2 12 0 PULSE(5 0 0 1U 1U 2000U 4000U)
VA3 13 0 PULSE(5 0 0 1U 1U 4000U 8000U)
VA0BAR 20 0 PULSE(0 5 0 1U 1U 500U 1000U)
VA1BAR 21 0 PULSE(0 5 0 1U 1U 1000U 2000U)
VA2BAR 22 0 PULSE(0 5 0 1U 1U 2000U 4000U)
VA3BAR 23 0 PULSE(0 5 0 1U 1U 4000U 8000U)
.options itl5=0
.tran 50U 10000U
* .plot tran v(13) v(12) v(11) v(10) v(9)
.print tran v(13) v(12) v(11) v(10) v(9)
* The following "probe" line is for those using PSPICE with PROBE Option
* .probe
.end
```

## Results of SPICE Simulations

The SPICE file listed in the tutorial contains the commands for simulating the 4 bit digital to analog converter assuming a digital status word $a_i$ that changes state every 500 μs. The simulation results, shown below, show the classic "staircase" nature of the DAC as the digital word increases from 0000 to 1111. Note the output voltage increase from zero to approximately 4 volts (switching transients have been removed). The reference voltage $V_{REF}$ is set for 5 volts, but due to threshold voltage degrading of the output voltage by the use of n-channel devices, the output will be limited to about the four volt level. Some clock feedthrough on the output signal can also be seen from the simulation. The use of a transmission gate rather than a single switching transistor would reduce both the threshold voltage degradation as well as reduce some of the clock feedthrough since the pFET (of the transmission gate) would be clocked on the complement of the switching signal.



**Measured Results**

The 4 bit DAC was measured using similar conditions as listed in the tutorial. An HP-3314A function generator was used for the 2 KHz clock signal. These collected data (**bold line**), exhibited in the figure below, were obtained using a Tektronix 2230 Digital Storage Oscilloscope. These data are compared with the ideal response of the DAC (thin line) as shown in Figure 3. The measured results show the step nature of the DAC, but with a number of nonidealities that are noticeable when compared to the ideal case. Note also that the full scale value of the DAC is not at $V_{REF}$. Accurately quantifying these nonidealities is one of the problems in the tutorial, but the DAC exhibits an approximate ±1 LSB integral linearity and a ±1.2 LSB differential linearity for the simple layout DAC. The maximum nonlinearity occurs near the maximum input digital word (1110 and 1111) at approximately 23 milliseconds (see below). If the maximum theoretical analog output is 4.0 volts, there is a gain error of 6.25% or less than 0.5 LSB.