# Getting Started with Seamless CVE

Software Version 4.3

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# Table of Contents

# Table of Contents [continued]

# List of Figures

# List of Figures [continued]

# About This Manual

The *Getting Started With Seamless Co-Verification Environment* manual contains short tutorials on how to use the Seamless Co-Verification Environment (Seamless CVE) in cosimulation with several supported simulators. To use this manual, you need to have a basic knowledge of electronic design and design-automation processes.

This manual contains hypertext links that are visible when the document is viewed online with compatible online document browsers. You can use hypertext links to access information at another location in this document.

The hypertext links appear in a contrasting color and may be underlined also. When you position the graphic pointer over the hypertext link, you can click the Select (left) mouse button on the hypertext link to go to its destination.

## Manual Organization

The first chapter, "Introduction," is a an overview of the design used in the tutorials in this manual. Subsequent chapters each contain a tutorial that guides you through a Seamless CVE session with a particular hardware simulator.

## Related Publications

Seamless CVE documentation is located in $CVE_HOME/doc. The following Mentor Graphics manuals contain important information on related topics:

- The *Seamless Co-Verification Environment Installation Instructions* explain how to install the Seamless CVE product.
- The *Seamless Co-Verification Environment User's and Reference Manual* contains an overview of the product, explains how to prepare designs for

cosimulation, and provides procedures for workstation and design configuration and cosimulation.

- The *Seamless CVE PSP Data Manuals* contain the relatively unchanging information on configuration, setup and usage of the Processor Support Packages.

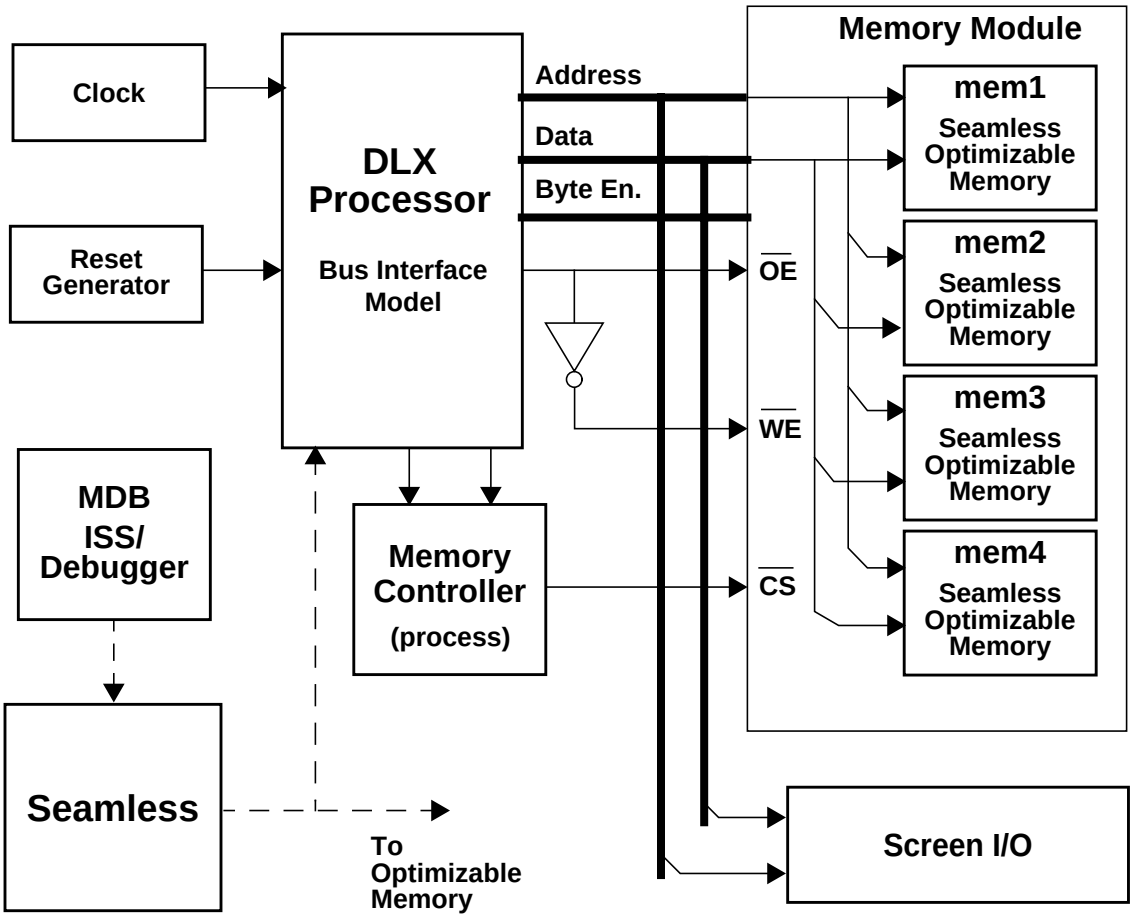
- The *Seamless CVE PSP Release Notes* contain changes and enhancements, known problems and workarounds, and corrected problems for Seamless CVE Processor Support Packages.

- The *Seamless CVE General Release Notes* contains changes and enhancements, known problems and workarounds, and corrected problems for the Seamless CVE product as a whole.

# Chapter 1
# Introduction

The tutorials in the following chapters use the demonstration design shown in Figure 1-1 to explain how to configure and cosimulate a design with Seamless CVE.

**Figure 1-1. Demonstration Design**



The demonstration design consists of the following major components:

- DLX Processor bus-interface model, through which the DLX target software running in the MDB instruction-set simulator (ISS) interacts with the hardware design.
- Memory Module, which consists of four Seamless optimizable memory instances.
- Clock Generator, which provides the system clock.
- Reset Generator, which initializes the processor.
- Screen I/O, which acts as a terminal, allowing direct user input and output through a display window.

Seamless CVE controls communications between the ISS, bus-interface model, and Seamless optimizable memory models. In Seamless optimizable memory models, memory access can take place either through hardware bus cycles, which are simulated in the hardware simulator, or through direct access from the ISS, without hardware bus cycles.

# Cosimulation with Hardware Simulators

The following chapters contain tutorials demonstrating cosimulation with these supported hardware simulators.

- Seamless CVE and ModelSim VHDL Tutorial
- Seamless CVE and NC-Verilog Tutorial

# Chapter 2
# Seamless CVE and ModelSim VHDL Tutorial

This tutorial consists of several sections designed to be performed in sequence, as follows:

- "Setting Up Your Environment" explains how to set up your workstation to run the tutorial.
- "Setting Up the Design Files" explains how to prepare the design components for cosimulation.
- "Invoking Seamless CVE" explains how to invoke Seamless CVE on the design.
- "Invoking the Hardware Simulator" explains how to set up the hardware simulator invocation. You invoke the simulator and allow the Seamless CVE models to register themselves with Seamless CVE.
- "Configuring the Processor" explains how to set up the software simulator invocation for the processor and how to configure the processor's address space and memory instances.
- "Saving the Configuration" explains how to save a Seamless CVE configuration in a file.
- "Starting the Cosimulation" explains how to start the cosimulation process.
- "Enabling Address-Range Optimization" explains how to perform Seamless CVE memory-access optimizations.

- "Exiting from the Cosimulation" explains how to exit from a cosimulation session.
- "Restarting Seamless CVE using the Configuration File" explains how to start up Seamless CVE using a previously saved configuration. It also shows how to use Seamless CVE time optimization to eliminate unnecessary hardware bus cycles.
- "Enabling Time Optimization" explains how to use Seamless CVE time optimization to eliminate unnecessary hardware bus cycles.
- "Enabling Instruction Fetch Optimization" describes a convenient way to enable data-access optimizations for all instruction fetches.

# Setting Up Your Environment

This tutorial assumes that Seamless CVE and ModelSim VHDL are installed and that proper license files and servers are set up as described in the product installation instructions. (See "Related Publications.")

Before starting the tutorial, set the following environment variables:

- CVE_HOME points to the top of the Seamless CVE installation tree for your platform (ss5 or hpu).
- MGLS_HOME points to *$CVE_HOME/mgls* (or to another appropriate location for the license server).
- MGLS_LICENSE_FILE points to the location of your license file.
- MODELTECH points to the installation directory for the ModelSim simulator.

# Setting Up the Design Files

Copy and set up the design files for the tutorial as follows:

1. Create a directory in which you can place the design files and run the tutorial.

2. Change directories to your tutorial directory.

3. Compile the VHDL design files into your tutorial directory by running the *build_design* script:

```
$CVE_HOME/example/tutorial/vsim_vhdl/build_design
```

   This compiles the DLX processor, SRAM, screen, reset generator, memory module, clock generator, and top-level tutorial design into a *work* directory.

4. Set the COMPILER_PATH environment variable:

```
setenv COMPILER_PATH $CVE_HOME/isms/dlxtools/bin
```

5. Compile and link the assembly-language program:

```
$CVE_HOME/isms/dlxtools/bin/dlx-gcc -g \
       $CVE_HOME/example/tutorial/common/sw/crt_tutorial.S \
          -c -I. -o crt_tutorial.o

$CVE_HOME/isms/dlxtools/bin/dlx-ld crt_tutorial.o -Ttext 0x0000 \
        -o crt_tutorial.elf
```

6. Copy the debugger “include” file to your tutorial directory:

```
cp $CVE_HOME/example/tutorial/common/sw/tutorial_int.inc .
```

# Invoking Seamless CVE

Invoke Seamless CVE using the following command:

```
$CVE_HOME/bin/cve
```

Figure 2-1 shows the Seamless CVE session window that appears after invocation. The main features of this window are as follows:

- File Menu—allows you to open configurations for editing, save configurations, and exit from Seamless CVE.

- Setup Menu—allows you to perform hardware-simulator setup as well as the CPU Setup operations described below.
- Optimize Menu—allows you to set up optimizations and optimization sets.
- View Menu—allows you to perform configuration and version checks and to view simulator output.
- Preference Menu—allows you to setup online help format, and enable help balloons or Auto Check as well as to save these preferences.
- Help Menu— allows you to gain access to online help.
- Tool bar—contains clickable icons that provide short cuts to all the major setup operations that you need when configuring a Seamless CVE cosimulation. The tool bar is divided into four major sections:

  **General Setup**
  contains icons for opening a configuration file, saving a configuration file, and starting the hardware simulator.

  **CPU Setup**
  contains icons for setting up software-simulator execution, defining memory access ranges, and mapping memory instances.

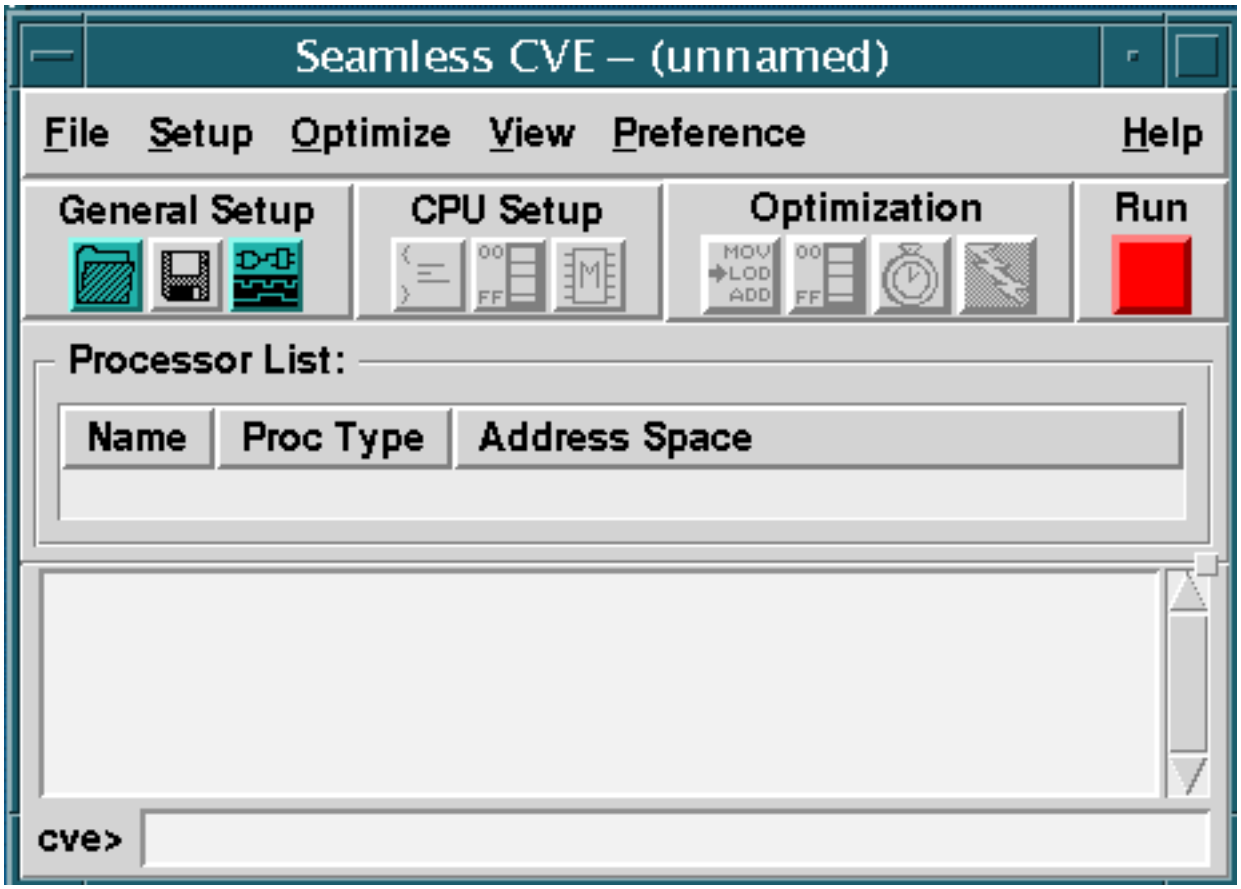
  **Optimization**
  contains icons for optimizing instruction fetches, optimizing accesses to address ranges, and optimizing time.

  **Run**
  contains the Run button, which starts a cosimulation session.

- Processor List window—lists all the registered processors in the design. (There are none registered now.)
- Transcript window— displays Seamless CVE command activity.

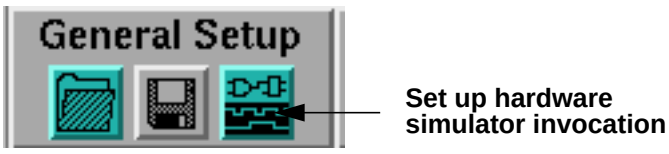
- Command line— allows you enter Seamless CVE commands.

**Figure 2-1. Seamless CVE Session Window**




# Invoking the Hardware Simulator

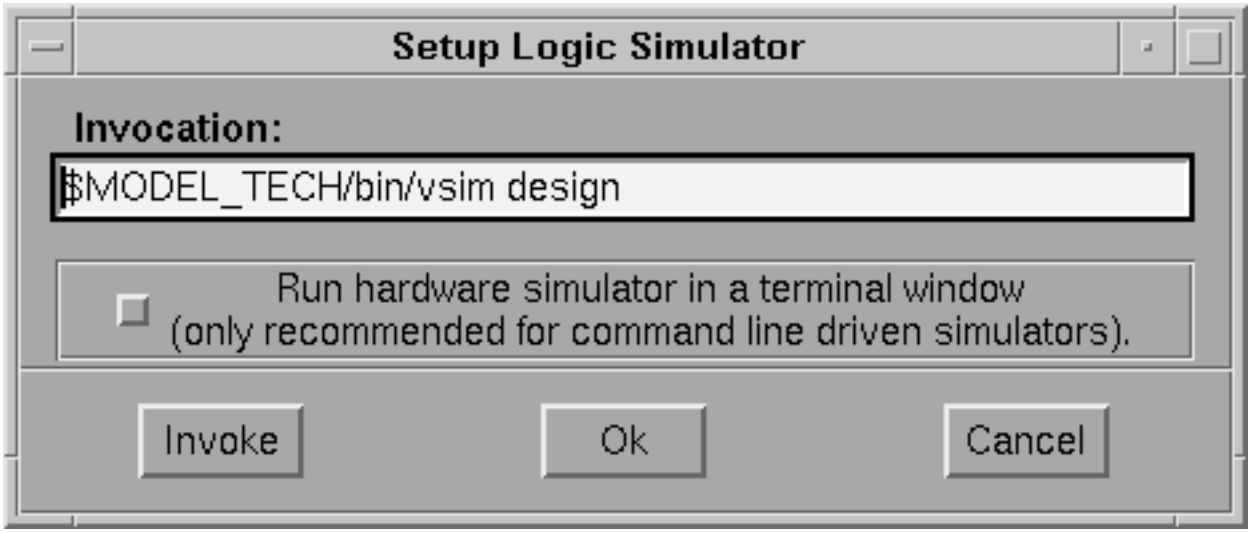
1. Click the Logic Simulation icon in the Session window (as shown below). This activates the Setup Logic Simulator dialog box.




2. Enter the following simulator invocation string in the text-entry box in the Setup Logic Simulator dialog box:

**$MODELTECH/bin/vsim design**

The variable MODELTECH points to the installation directory for the ModelSim VHDL simulator, as set up at the beginning of this tutorial. Do not enable the “Run hardware simulator in a terminal window” button because ModelSim VHDL runs from a GUI.




3. Click the Invoke button in the Setup Logic Simulator dialog box. This invokes the simulator and allows Seamless CVE memory models and processor models within the design to register themselves with the Seamless CVE. (The Ok button allows setup without invocation.)

   The ModelSim VHDL session window comes up. As the simulator loads the design, a listing for the processor model appears in the Processor List window, showing that the model has registered itself.

   Notice that once you set up the invocation, the Logic Simulation icon in the Session window is no longer highlighted, indicating that this step is done. If you wish to view the contents of the hardware simulator terminal window, select the **View > Hardware Output** menu item in the Seamless CVE window.

4. Select the **View > Run Status** menu item in the Seamless CVE window to display the Run Status message box. The indicator lists the hardware simulator as Vsim Uninitialized.

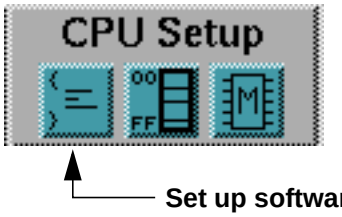
# Configuring the Processor

Setting up a Seamless CVE processor instance for cosimulation is a three-part process consisting of the following steps:

- Setting up the software simulator invocation.
- Mapping memory instances.
- Mapping memory-access ranges.

Set up the software simulator invocation as follows:

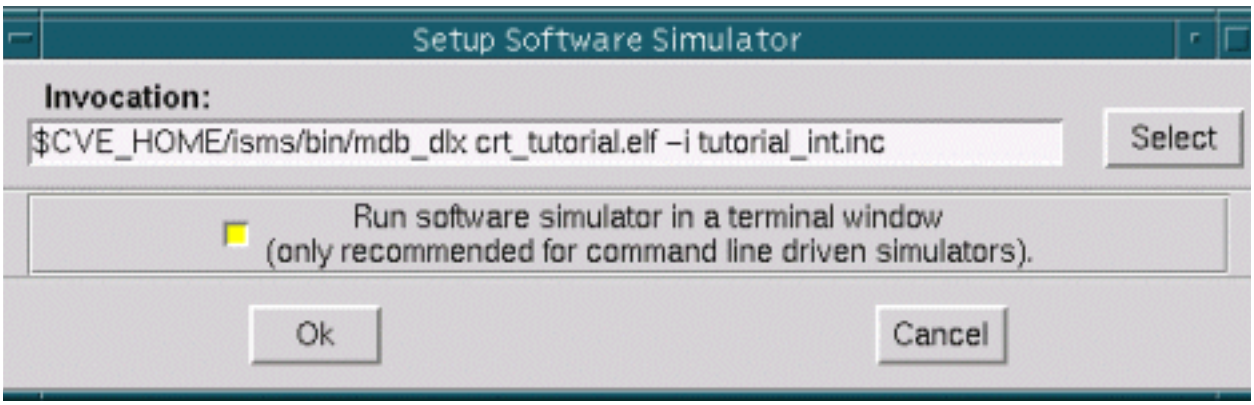
1. Click the Software Simulation icon in the Seamless CVE Session window (shown below). This activates the Setup Software Simulator dialog box.




2. Enter the following simulator invocation string under “Invocation:” in the Setup Software Simulator dialog box:

   **$CVE_HOME/isms/bin/mdb_dlx crt_tutorial.elf -i tutorial_int.inc**

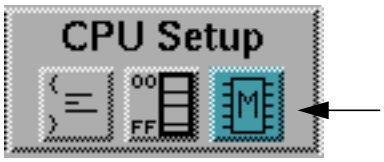
3. Click the button next to “Run software simulator in a terminal window” in the Setup Software Simulator dialog box, as shown below. You do this because the software simulator is not GUI driven.



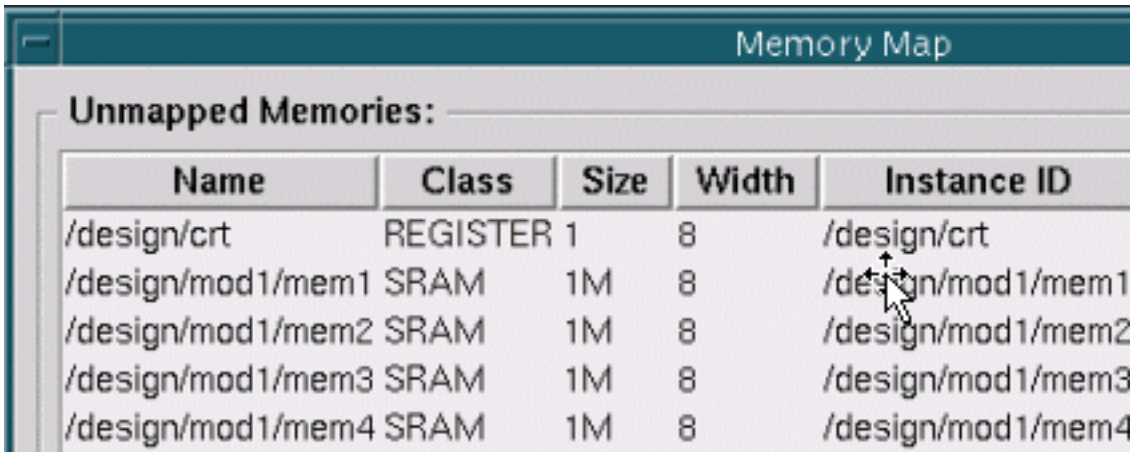
4. Click the Ok button. Notice that the Software Simulation icon in the Session window is no longer highlighted, indicating that setup is done.

You need to map the Seamless optimizable memory instances into the processor's address space. Do this by performing the following steps:

1. Click the Map Memory Instances icon in the CVE Session window (shown below). This activates the Memory Map dialog box.

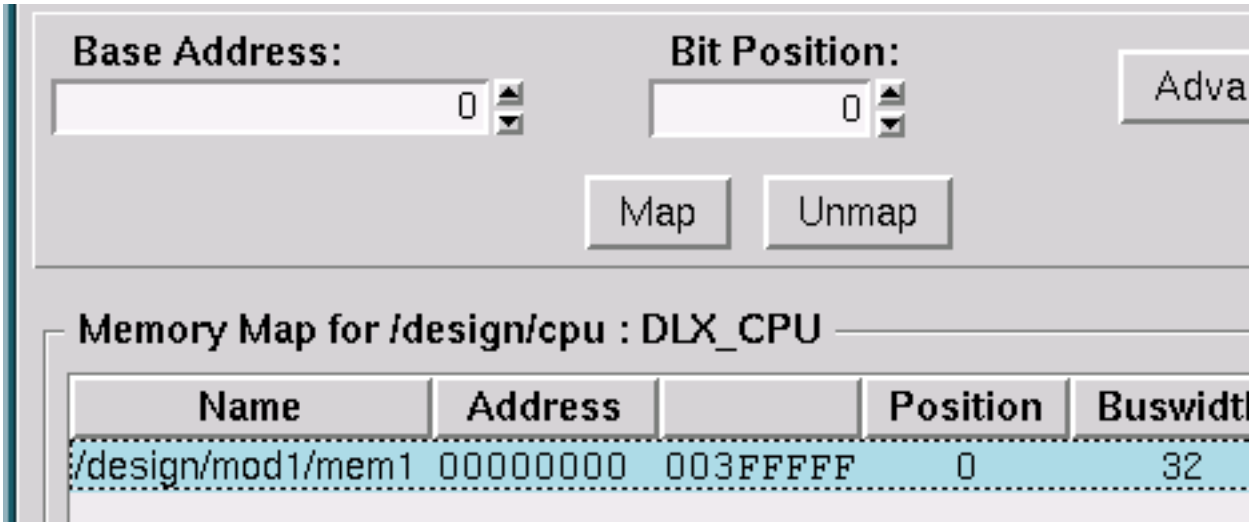



Each of the four memory instances in the memory module is 1Mbyte long and 8 bits wide. These instances will be mapped across the processor's 32-bit data bus such that each instance occupies 8 bits of the bus. As shown below, the logical names of the instances are listed on the far left side and the design instance identifiers are on the right side (and they are the same).




2. Select the *mem1* memory instance by clicking on that instance's entry in the Unmapped Memories list. The instance entry is highlighted when selected. Notice that the Base Address and Bit Position entries are both 0, as shown below.

3. Click the Map button to map *mem1* into the processor address space. The entry for *mem1* appears in the Memory Map list, as shown below.




4. Select the *mem2* memory instance by clicking on that instance's entry in the Unmapped Memories list.

5. Specify the bit position for the *mem2* instance by clicking on the up arrow button to increment the value in the box to 8. This maps the *mem2* instance into bits 8 through 15 of the processor's 32-bit word.

6. Click the Map button to map *mem2* into the processor address space. The entry for *mem2* appears in the Memory Map list with a bit position of 8.

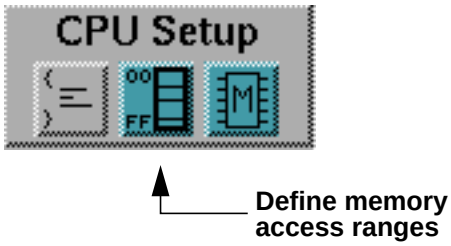
7. Map the *mem3* and *mem4* instances into bit positions 16 and 24, respectively.

8. Select the *crt* entry in the Unmapped Memories list. Enter an address of 3FFFFFF0 in the Base Address box. Set the bit position to 0 and click the Map button to map the instance into the processor address space.

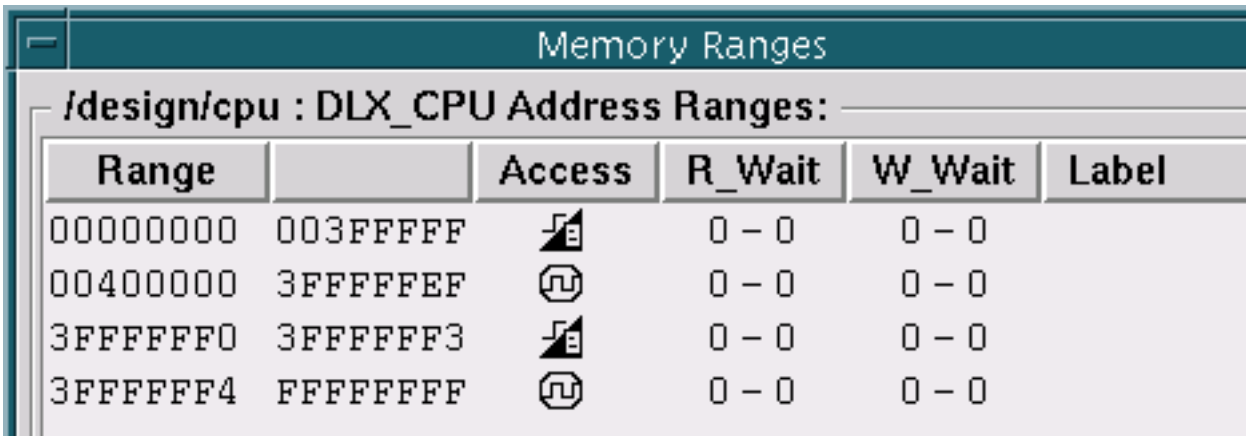
9. Click the Close button to dismiss the Memory Map dialog box.

Set up the memory-access ranges for the processor as follows:

1. Click the Memory Access Ranges icon in the Seamless CVE Session window (shown below).




   The Memory Ranges dialog box appears. The Address Ranges list box contains four entries, as shown below.



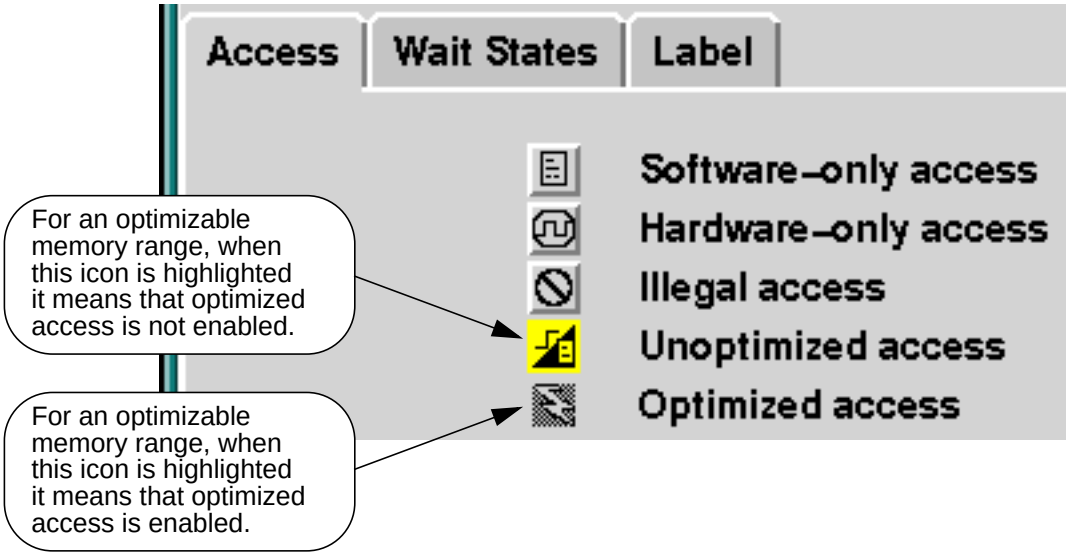

| Range | | Access | R_Wait | W_Wait | Label |
|---|---|---|---|---|---|
| 00000000 | 003FFFFF | | 0 – 0 | 0 – 0 | |
| 00400000 | 3FFFFFEF | | 0 – 0 | 0 – 0 | |
| 3FFFFFF0 | 3FFFFFF3 | | 0 – 0 | 0 – 0 | |
| 3FFFFFF4 | FFFFFFFF | | 0 – 0 | 0 – 0 | |

   Notice that the first entry, for addresses 0 through 3FFFFF, is the address range of the memory module in the hardware design. Since these instances are Seamless memory models, this address range is optimizable.

2. Select the first entry (0 to 3FFFFF) in the Address Ranges list box. The start and end addresses appear in the Start Address and End Address entry boxes.

   Notice the icon under the Access heading in the list box and the corresponding icon on the Access tab in the lower portion of the Memory Ranges dialog box (shown below). Optimized access to this range has not

been enabled yet, meaning that all accesses to this memory range generate hardware bus cycles.




3. Create a label for the optimizable address range as follows:

   a. Click the Label tab.

   b. Enter a label of “optimizable” in the Range Label box, then press Return or click the Apply button. The label appears in the optimizable entry in the Address Ranges list box.

4. Set up wait-state values for the optimizable memory:

   a. Click the Wait States tab.

   b. Enter values of 2 in the Read and Write boxes under Initial, then press Return or click the Apply button. (Leave the Burst boxes blank.) The wait-state values appear in the Address Ranges list box.

5. Select the next unlabeled range (400000 - 3FFFFFFF) listed in the Address Ranges box. Notice that the listed range values appear in the Start and End address boxes.

6. Replace the End Address value by double-clicking on the entry box and entering 4000FF.


**Note**

There are no memory instances, either Seamless CVE or otherwise, in this address range. This and the remaining steps in this section simply demonstrate how to set up memory-access ranges.

7. Make sure the Label tab is on top and enter “hardware” in the Range Label entry box.

8. Click the Apply button. A new entry, at addresses 400000 - 40000FF, with the label “hardware” appears in in the Address Ranges list box. The former hardware-only range is now split into two ranges.

9. Select the next range on the list and label it “hardware2.”

10. Select the *screen* entry, which is next in the list. Although the *screen* is actually based on an optimizable register memory (hence the “optimizable” icon under the Access column), we will pretend it is hardware-only for the present. Enter a label of “screen” for this range then click Apply.

11. Select the unlabeled range at the bottom of the list in the Address Ranges list box (3FFFFFF4 to FFFFFFFF).

12. Enter “illegal” in the Range Label text-entry box, then click the Apply button.

13. Select the Access tab and then click the Illegal access button. This makes addresses 400100 to FFFFFFFF an “illegal” range, as indicated by the icon in the Address Ranges list.

14. Click the Close button to close the window. Notice that the Memory Access Ranges icon in the Session window is no longer highlighted, indicating that this step has been done.

# Saving the Configuration

Save the current configuration by performing the following steps:

1. Click the Save Configuration icon in the Seamless CVE Session window (shown below) or select the **File > Save As** menu item.


**Save Configuration**

2. In the Save As dialog box, enter a configuration filename (and path, if necessary).

3. Click Ok to save the configuration.

# Starting the Cosimulation

1. Click the **Run** button in the Seamless CVE main window. The button changes to yellow and remains pressed, indicating that cosimulation can start. In addition, a terminal window appears showing a software simulator startup message:

   **CVE NOTE: Waiting to connect to hardware process ...**

2. Move the cursor to the ModelSim VHDL simulator's main window and enter the following command at the VSIM prompt:

   **view signals**

3. In the Signals window select **View > Wave > Signals in Region** to bring up the ModelSim VHDL waveform window. If necessary, minimize the Waveform and Signals windows to free some display space.

4. Enter the following at the ModelSim VHDL session window prompt:

   **run -all**

The **run** command starts the hardware simulation (but the simulation cannot run until its software begins to execute). Notice that the Run button turns green, indicating that cosimulation has begun. The Seamless CVE models in the design cause Seamless CVE to start up the software simulator. The software simulator terminal window displays a series of messages followed by this prompt:

**(mdb)**

The Run Status window indicates that the hardware simulator is waiting (for the software simulation to start) and the software simulator is interactive (that is, waiting for you to enter a command to start the software simulation). Neither hardware nor software simulation can proceed until you respond to the software simulator prompt.


5. Enter ***run*** at the **(mdb)** prompt. The Screen window appears and displays the following message.

```
Welcome to the Seamless Tutorial!!
Using the DLX Processor and the MDB Debugger.
```

Notice that the Run Status for both of the simulators changes to “Running” then back to “Interactive” for both simulators. The software simulator runs to a breakpoint and displays a message similar (not necessarily identical) to the following one:

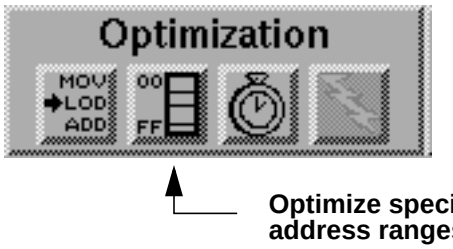
```
25 secs; 656 instr; 26 instr/sec
Hit Breakpoint 1 at 0x00000000 (begin+0x00000000)
(0x00000000) begin              nop
(mdb)
```

In addition, waveforms appear in the hardware simulator waveform window, showing the bus activity that takes place during the simulation run. At this point, the run status of both simulators is interactive.

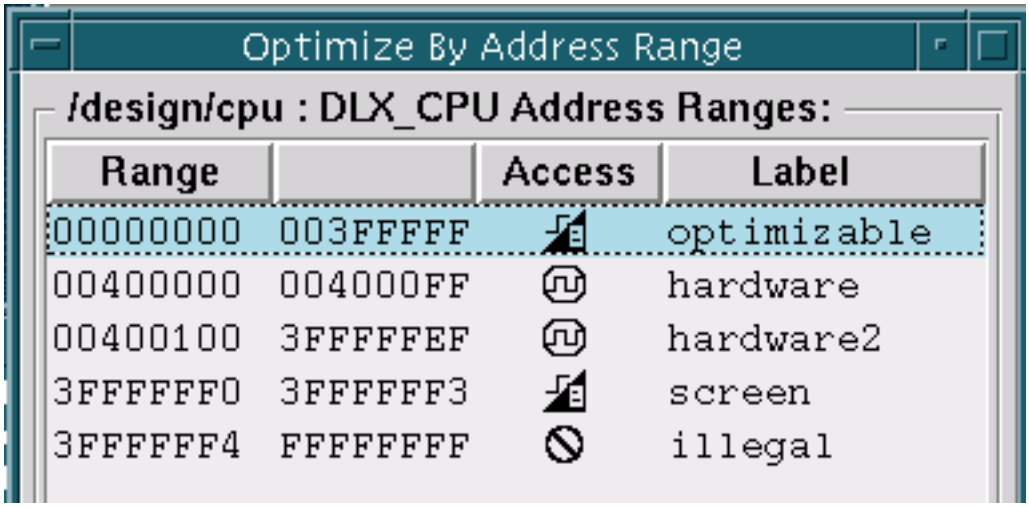
# Enabling Address-Range Optimization

Enable address-range optimization for the optimizable addresses in the processor address space by performing the following steps:

1. Click the Optimize Address Ranges icon in the Seamless CVE Session window (shown below). This activates the Optimize by Address Range dialog box.

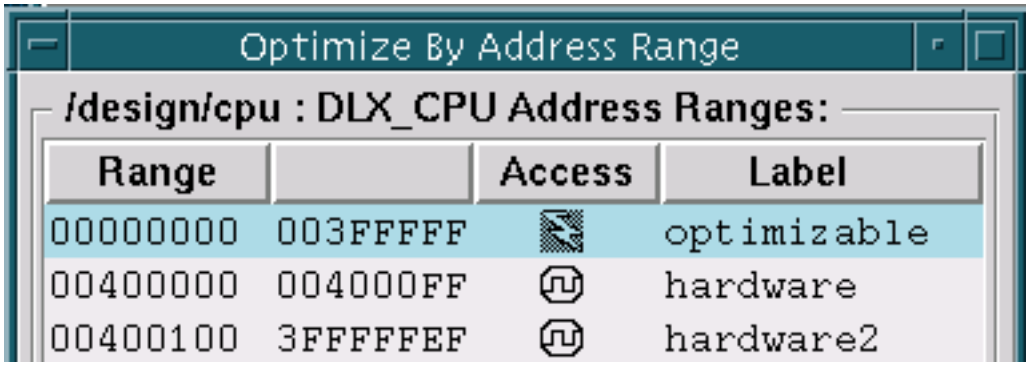



The Address Ranges list contains the ranges you set up in the previous section, as shown below.




2. Click the range labeled “optimizable.” The start and end addresses of the range appear in the entry boxes under Optimization Entry.

3. Click the On button. This modifies the optimizable range in the Address Ranges list as shown below. The “lightning bolt” icon indicates that processor accesses to this range can take place directly through software rather than generating hardware bus cycles.




   You can enable optimized access to any portion of an optimizable address range.

4. Click the Close button to dismiss the Optimize By Address Range dialog box. The Optimize Address Ranges icon in the Seamless CVE session window is now highlighted.

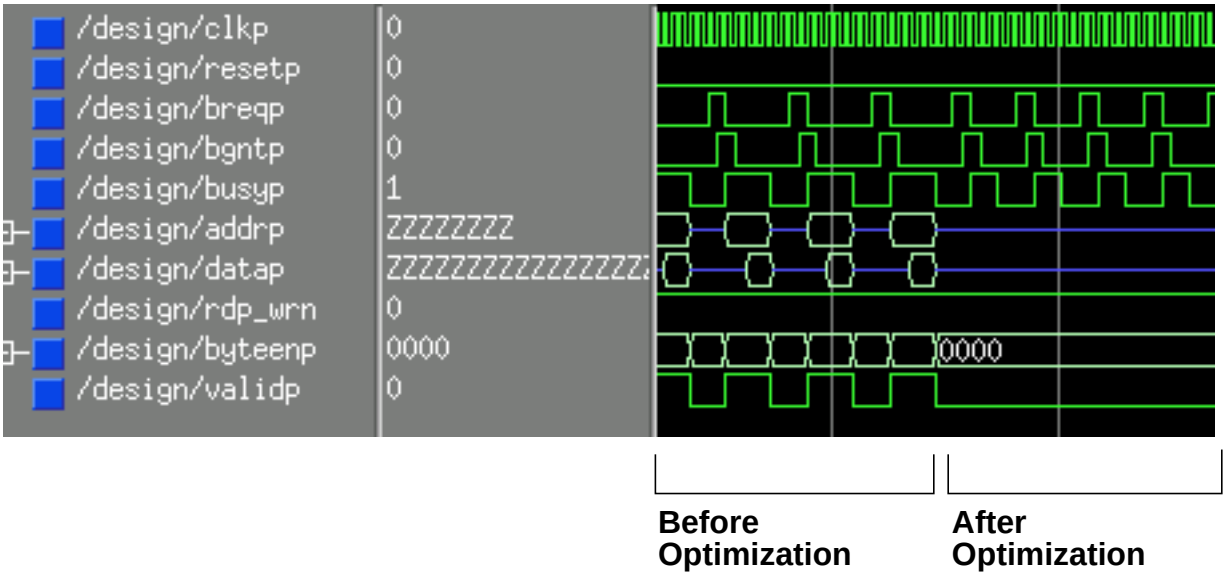
5. Move the cursor to the transcript window in the ModelSim simulator’s session window and enter the following command:

   **run -all**

   This time, the simulation runs faster. A portion of the waveform display that overlaps the first and second runs is shown below. Notice the relative lack of address- and data-bus activity during the second run. The clock runs in the hardware simulation as before. However, the software simulator now accesses memory directly except when writes to the screen, in which case it needs to generate bus activity in the hardware simulation. You can confirm

this by noting that a value of 0x3FFFFFF0 is present on the address bus during these write cycles. (Use the cursor.)

**Figure 2-2. ModelSim Waveform Window**




6. Select the **Optimize > Name Optimization** menu item. This activates the Optimization Set dialog box. This dialog box allows you to save the current optimization state for later recall.

7. Type in a name such as *opt1* in the text-entry box in the Optimization Set dialog box then click Ok to save the optimization set. Notice that the Optimization Set Enable ("lightning bolt") icon under Optimization group in the main Seamless CVE window becomes pressed and is highlighted yellow, meaning that a named optimization set is active.


8. Click the Optimization Set Enable icon to disable the optimization set. The icon becomes "unpressed" and is no longer highlighted. (You can also use the **Optimize > Unoptimize** menu item.) Click the icon again to re-enable the optimization set.

9. Save the current configuration by selecting the **File > Save** menu item.

# Exiting from the Cosimulation

1. Select the **File > Exit** menu item in the Seamless CVE session window or enter “exit” at the command-line. A message box appears saying “Simulator is running. Exit anyway?”

2. Click Yes to exit from the ModelSim VHDL simulator. The Seamless CVE Session window and simulator windows disappear.

# Restarting Seamless CVE using the Configuration File

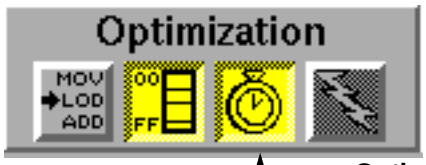
Invoke Seamless CVE using the following command:

```
$CVE_HOME/bin/cve   my_config
```

where *my_config* is the name of the configuration file you saved previously. Seamless CVE, ModelSim VHDL simulator, and software simulator all start up. Notice that the configuration in *my_config* is restored and the cosimulation is ready to start. You can confirm this by clicking on the appropriate CPU Setup and Optimization icons and checking the values that appear in the corresponding dialog boxes.

# Enabling Time Optimization

1. Click the Optimize time icon to activate Seamless time optimizations. The Time Optimizations icon button (shown below) is now “pressed” and highlighted yellow.




**Optimize time by allowing software to run ahead of hardware (using Time Optimization dialog box settings)**

2. Move the cursor to the transcript window in the ModelSim VHDL simulator’s session window and enter the following commands:

   **add wave ***
   **run -all**

   The Run button on the Seamless CVE session window turns green, indicating that cosimulation has begun.

3. Enter ***run*** at the (mdb) prompt in the software simulator’s terminal, as you did earlier in “Starting the Cosimulation.”

   Notice that the same number of instructions are executed as before, but in much less time. The software has run at full speed, decoupled from the hardware simulation, and far fewer clock cycles have occurred in the hardware simulation. The only time hardware clock cycles are required is when the program accesses the screen to print out the message. Although the tutorial program is too simple to show the full effect, usually over 99 percent of hardware clock cycles can be eliminated without affecting simulation results.

4. Select the **Optimize > Name Optimization** menu item. The Optimization Set dialog box appears.

5. Enter a name (different than the one you used previously) for the current optimization set, then click Ok.

6. Select the **Optimize > Recall Optimization** menu item. The Optimization Sets dialog box appears.

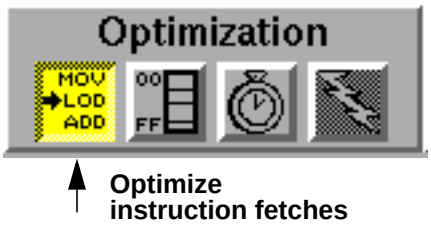
7. Select the first optimization set you saved by clicking on its name, then click the Apply button. Now select the optimization set you saved in this section and click Apply. Notice the effect on the Optimizaton icons.

8. Click the Close button to dismiss the Optimization Set dialog box.

9. Select the **Optimize > Unoptimize** menu item to clear the current optimization set.

# Enabling Instruction Fetch Optimization

1. Click in on the Instruction Fetch Optimizations icon. The icon becomes highlighted as shown below.




   Instruction fetch optimization is a convenient way to automatically enable optimizations for all instruction-fetch bus cycles. This eliminates hardware bus-cycle activity for instruction fetches, allowing the ISS to fetch the instructions directly from memory.

2. Run the hardware and software simulators as before.

3. Select the **Optimize > Unoptimize** menu item.

4. Run the hardware and software simulators again. Notice the difference in run time and bus activity with and without instruction fetch optimizations enabled.

This concludes the *Seamless CVE and ModelSim VHDL Tutorial.* You can experiment with different combinations of optimization settings to see how they

affect cosimulation. For example, try turning on optimizations for single addresses or ranges of addresses to see how they affect simulation speed and bus cycle activity.

# Chapter 3
# Seamless CVE and NC-Verilog Tutorial

This tutorial consists of several sections designed to be performed in sequence, as follows:

- "Setting Up Your Environment" explains how to set up your workstation to run the tutorial.
- "Setting Up the Design Files" explains how to prepare the design components for cosimulation.
- "Invoking Seamless CVE" explains how to invoke Seamless CVE on the design.
- "Invoking the Hardware Simulator" explains how to set up the hardware simulator invocation. You invoke the simulator and allow the Seamless CVE models to register themselves with Seamless CVE.
- "Configuring the Processor" explains how to set up the software simulator invocation for the processor and how to configure the processor's address space and memory instances.
- "Saving the Configuration" explains how to save a Seamless CVE configuration in a file.
- "Starting the Cosimulation" explains how to start the cosimulation process.
- "Enabling Address-Range Optimization" explains how to perform Seamless CVE memory-access optimizations.

- "Exiting from the Cosimulation" explains how to exit from a cosimulation session.
- "Restarting Seamless CVE using the Configuration File" explains how to start up Seamless CVE using a previously saved configuration. It also shows how to use Seamless CVE time optimization to eliminate unnecessary hardware bus cycles.
- "Enabling Time Optimization" explains how to use Seamless CVE time optimization to eliminate unnecessary hardware bus cycles.
- "Enabling Instruction Fetch Optimization" describes a convenient way to enable data-access optimizations for all instruction fetches.

# Setting Up Your Environment

This tutorial assumes that Seamless CVE and NC Verilog are installed and that proper license files and servers are set up as described in the product installation instructions. (See "Related Publications.")

Before starting the tutorial, set the following environment variables:

- CVE_HOME points to the top of the Seamless CVE installation tree for your platform (ss5 or hpu).
- MGLS_HOME points to *$CVE_HOME/mgls* (or to another appropriate location for the license server).
- MGLS_LICENSE_FILE points to the location of your license file.
- CDS_INST_DIR points to the top of the installation directory for the NC Verilog application. (Refer to the product documentation for detailed information.)
- CDS_ROOT points to the top of the installation directory for the NC Verilog application. (Refer to the product documentation for detailed information.)

- SHLIB_PATH (for HPUX): add the current directory as well as $CVE_HOME/lib and $CDS_INST_DIR/tools/lib to the SHLIB_PATH setting.

- LD_LIBRARY_PATH (for Solaris): add the current directory as well as $CVE_HOME/lib and $CDS_INST_DIR/tools/lib to the LD_LIBRARY_PATH setting.

# Setting Up the Design Files

Copy and set up the design files for the tutorial as follows:

1. Create a directory in which you can place the design files and run the tutorial.

2. Change directories to your tutorial directory.

3. Compile the Verilog design files into your tutorial directory by running the *build_design* script:

   ```
   $CVE_HOME/example/tutorial/ncvlog/build_design
   ```

   This compiles the DLX processor, SRAM, screen, reset generator, memory module, clock generator, and top-level tutorial design into your local directory.

4. Set the COMPILER_PATH environment variable:

   ```
   setenv COMPILER_PATH $CVE_HOME/isms/dlxtools/bin
   ```

5. Compile and link the assembly-language program:

   ```
   $CVE_HOME/isms/dlxtools/bin/dlx-gcc -g \
          $CVE_HOME/example/tutorial/common/sw/crt_tutorial.S \
      -c -I. -o crt_tutorial.o

   $CVE_HOME/isms/dlxtools/bin/dlx-ld crt_tutorial.o -Ttext 0x0000 \
           -o crt_tutorial.elf
   ```

6. Copy the debugger “include” file to your tutorial directory:

```
cp $CVE_HOME/example/tutorial/common/sw/tutorial_int.inc .
```

# Invoking Seamless CVE

Invoke Seamless CVE using the following command:

```
$CVE_HOME/bin/cve
```

Figure 3-1 shows the Seamless CVE session window that appears after invocation. The main features of this window are as follows:

- File Menu—allows you to open configurations for editing, save configurations, and exit from Seamless CVE.
- Setup Menu—allows you to perform hardware-simulator setup as well as the CPU Setup operations described below.
- Optimize Menu—allows you to set up optimizations and optimization sets.
- View Menu—allows you to perform configuration and version checks and to view simulator output.
- Preference Menu—allows you to setup online help format, and enable help balloons or Auto Check as well as to save these preferences.
- Help Menu— allows you to gain access to online help.
- Tool bar—contains clickable icons that provide short cuts to all the major setup operations that you need when configuring a Seamless CVE cosimulation. The tool bar is divided into four major sections:

  **General Setup**
  contains icons for opening a configuration file, saving a configuration file, and starting the hardware simulator.

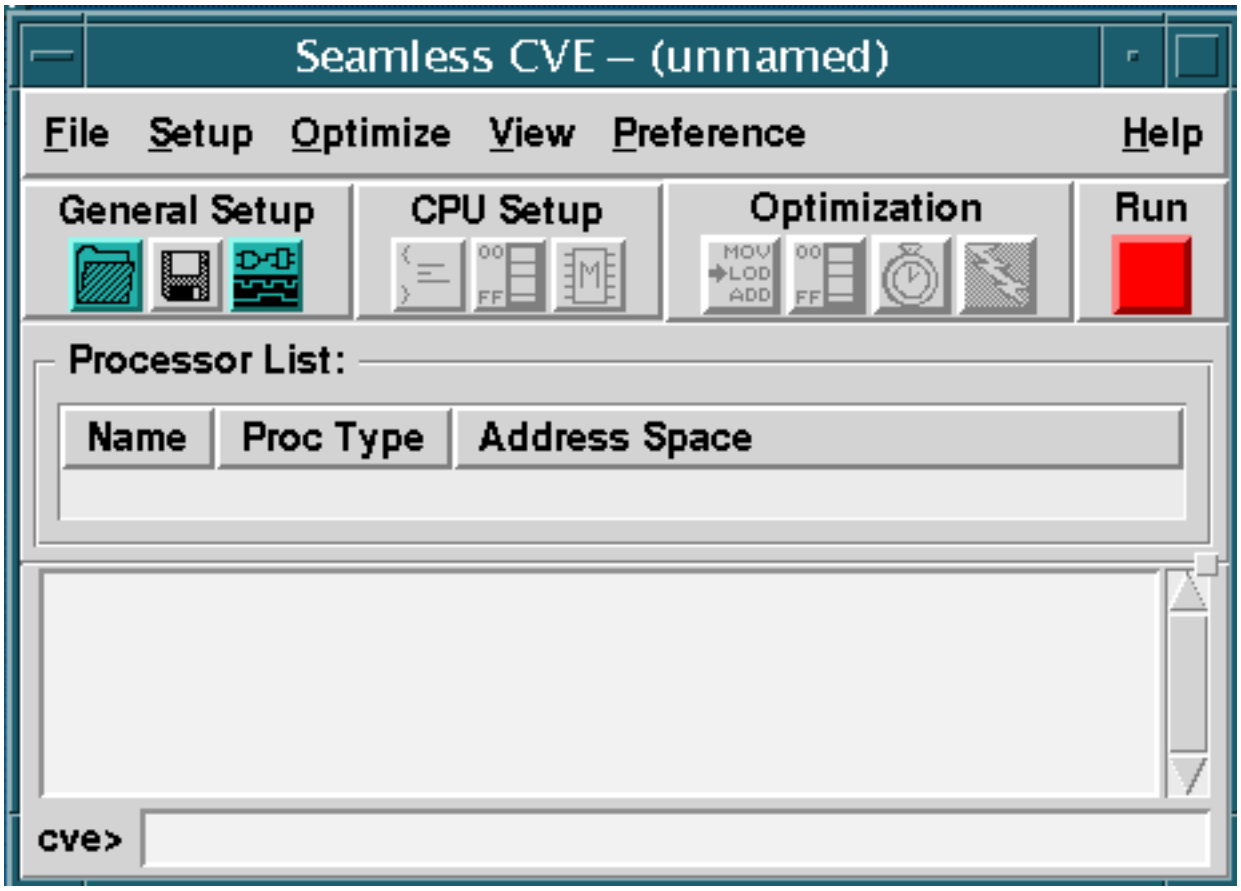
  **CPU Setup**
  contains icons for setting up software-simulator execution, defining memory access ranges, and mapping memory instances.

**Optimization**
contains icons for optimizing instruction fetches, optimizing accesses to address ranges, and optimizing time.

**Run**
contains the Run button, which starts a cosimulation session.

- Processor List window—lists all the registered processors in the design. (There are none registered now.)
- Transcript window— displays Seamless CVE command activity.
- Command line— allows you enter Seamless CVE commands.

**Figure 3-1. Seamless CVE Session Window**



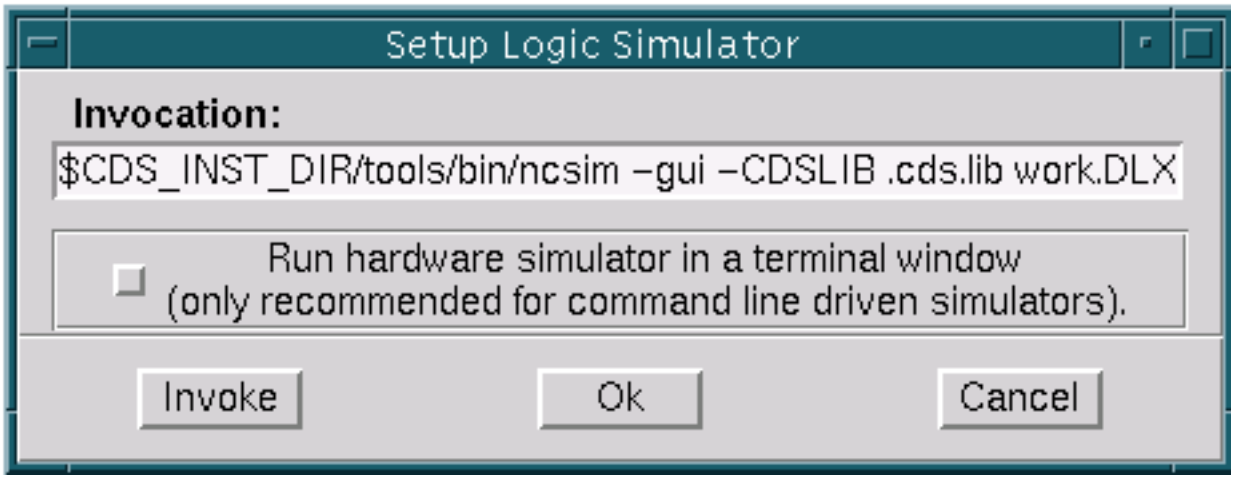
# Invoking the Hardware Simulator

1. Click the Logic Simulation icon in the Session window (as shown below). This activates the Setup Logic Simulator dialog box.


2. Enter the following simulator invocation string in the text-entry box in the Setup Logic Simulator dialog box:

   **$CDS_INST_DIR/tools/bin/ncsim -gui -CDSLIB cds.lib work.DLX_design:snap**

   The variable MODELTECH points to the installation directory for the ModelSim VHDL simulator, as set up at the beginning of this tutorial. Do not enable the “Run hardware simulator in a terminal window” button because NC Verilog runs from a GUI.




3. Click the Invoke button in the Setup Logic Simulator dialog box. This invokes the simulator and allows Seamless CVE memory models and processor models within the design to register themselves with the Seamless CVE. (The Ok button allows setup without invocation.)

The ModelSim VHDL session window comes up. As the simulator loads the design, a listing for the processor model appears in the Processor List window, showing that the model has registered itself.

Notice that once you set up the invocation, the Logic Simulation icon in the Session window is no longer highlighted, indicating that this step is done. If you wish to view the contents of the hardware simulator terminal window, select the **View > Hardware Output** menu item in the Seamless CVE window.

4. Select the **View > Run Status** menu item in the Seamless CVE window to display the Run Status message box. The indicator lists the hardware simulator as Vsim Uninitialized.

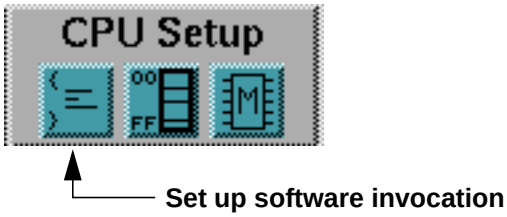
# Configuring the Processor

Setting up a Seamless CVE processor instance for cosimulation is a three-part process consisting of the following steps:

- Setting up the software simulator invocation.
- Mapping memory instances.
- Mapping memory-access ranges.

Set up the software simulator invocation as follows:

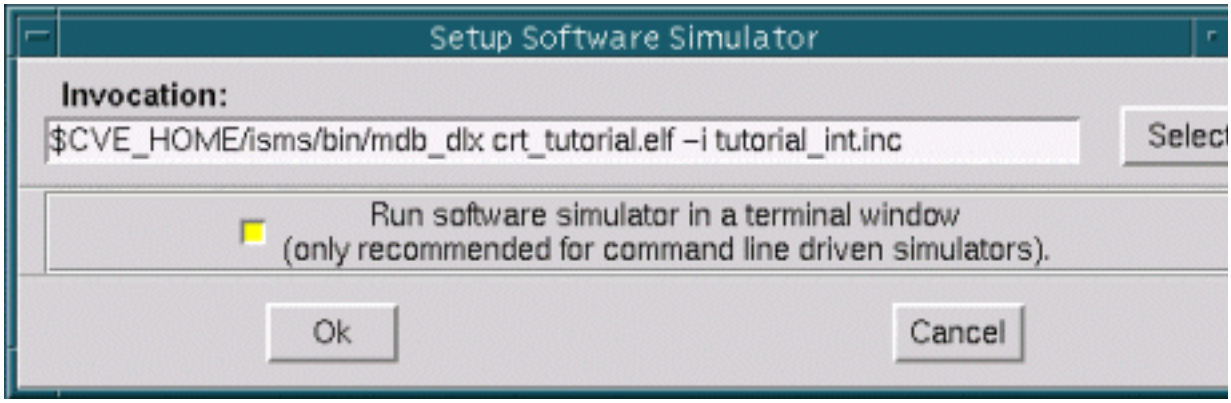
1. Click the Software Simulation icon in the Seamless CVE Session window (shown below). This activates the Setup Software Simulator dialog box.




2. Enter the following simulator invocation string under “Invocation:” in the Setup Software Simulator dialog box:

**$CVE_HOME/isms/bin/mdb_dlx crt_tutorial.elf -i tutorial_int.inc**

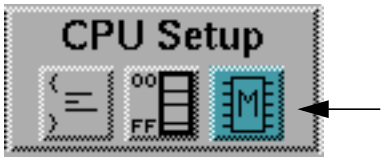
3. Click the button next to “Run software simulator in a terminal window” in the Setup Software Simulator dialog box, as shown below. You do this because the software simulator is not GUI driven.




4. Click the Ok button. Notice that the Software Simulation icon in the Session window is no longer highlighted, indicating that setup is done.

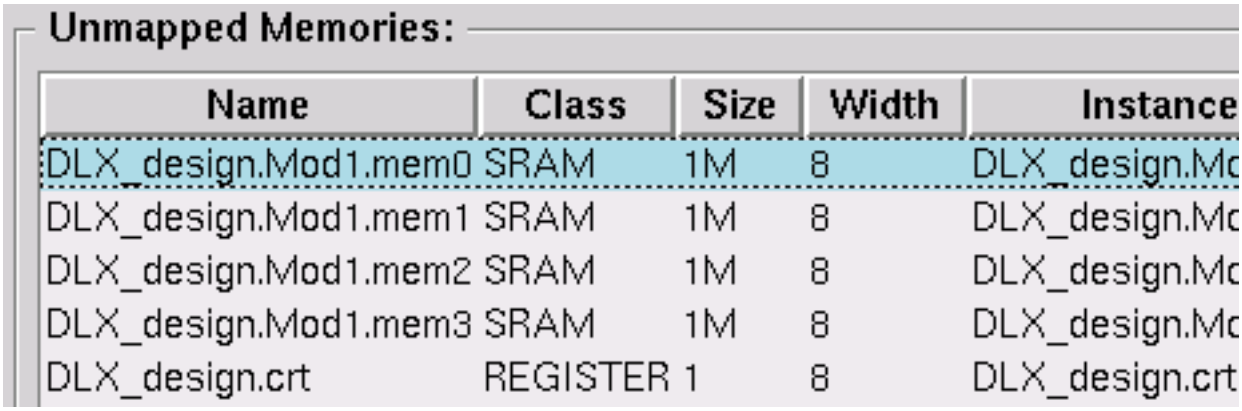
You need to map the Seamless optimizable memory instances into the processor’s address space. Do this by performing the following steps:

1. Click the Map Memory Instances icon in the CVE Session window (shown below). This activates the Memory Map dialog box.



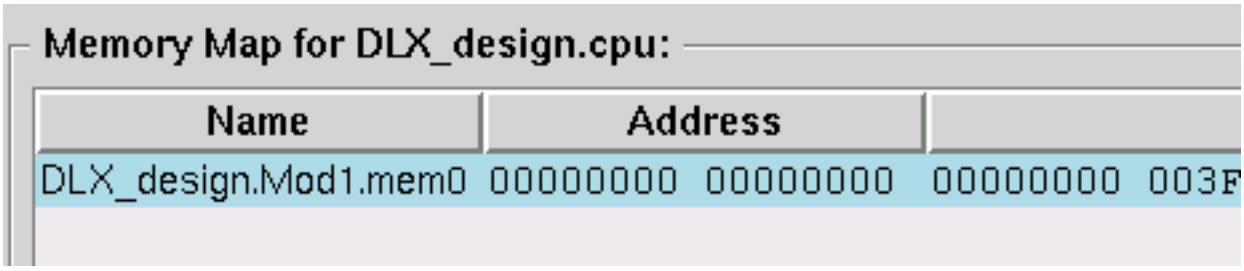

   Each of the four memory instances in the memory module is 1Mbyte long and 8 bits wide. These instances will be mapped across the processor’s 32-bit data bus such that each instance occupies 8 bits of the bus. As shown

below, the logical names of the instances are listed on the far left side and the design instance identifiers are on the right side (and they are the same).




2. Select the *mem0* memory instance by clicking on that instance's entry in the Unmapped Memories list. The instance entry is highlighted when selected. Notice that the Base Address and Bit Position entries are both 0, as shown below.

3. Click the Map button to map *mem0* into the processor address space. The entry for *mem0* appears in the Memory Map list, as shown below.




4. Select the *mem1* memory instance by clicking on that instance's entry in the Unmapped Memories list.

5. Specify the bit position for the *mem1* instance by clicking on the up arrow button to increment the value in the box to 8. This maps the *mem1* instance into bits 8 through 15 of the processor's 32-bit word.

6. Click the Map button to map *mem1* into the processor address space. The entry for *mem1* appears in the Memory Map list with a bit position of 8.

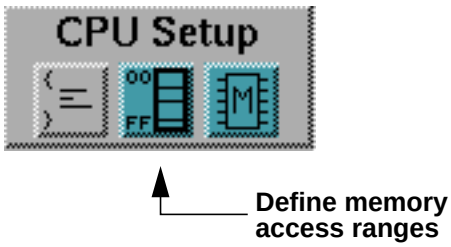
7. Map the *mem2* and *mem3* instances into bit positions 16 and 24, respectively.

8. Select the *crt* entry in the Unmapped Memories list. Enter a base address of 3FFFFFF0 and bit position of 0 then click the Map button to map the instance the processor address space.

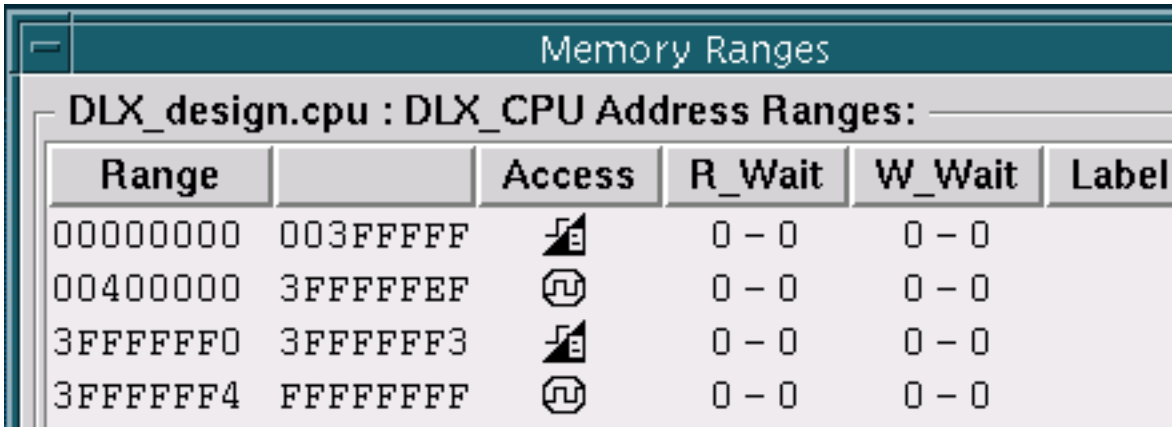
9. Click the Close button to dismiss the Memory Map dialog box.

Set up the memory-access ranges for the processor as follows:

1. Click the Memory Access Ranges icon in the Seamless CVE Session window (shown below).



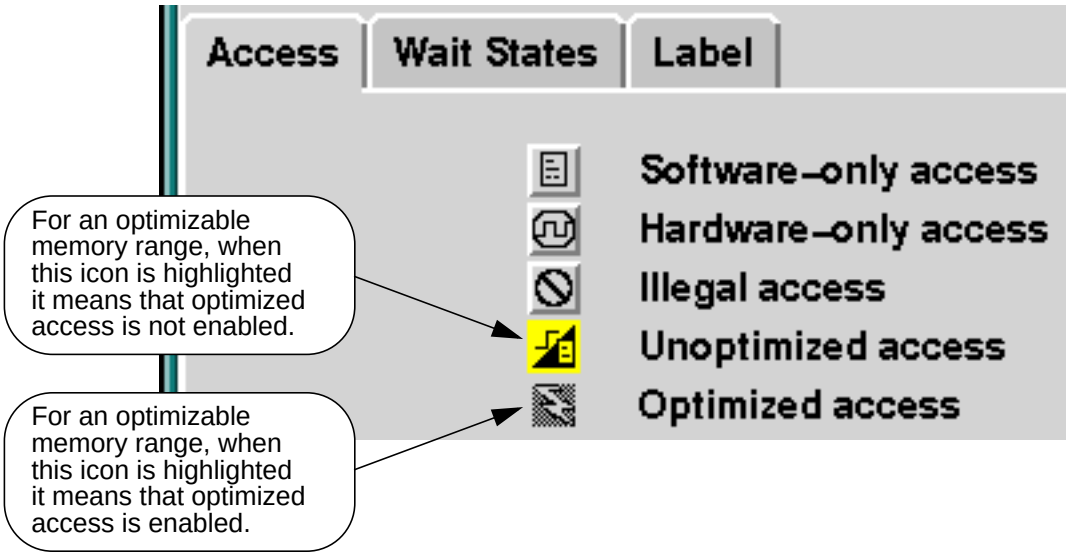

The Memory Ranges dialog box appears. The Address Ranges list box contains four entries, as shown below.




Notice that the first entry, for addresses 0 through 3FFFFF, is the address range of the memory module in the hardware design. Since these instances are Seamless memory models, this address range is optimizable. The icon under “Access” indicates this.

2. Select the first entry (0 to 3FFFFF) in the Address Ranges list box. The start and end addresses appear in the Start Address and End Address entry boxes.

   Notice the icon under the Access heading in the list box and the corresponding icon on the Access tab in the lower portion of the Memory Ranges dialog box (shown below). Optimized access to this range has not been enabled yet, meaning that all accesses to this memory range generate hardware bus cycles.




3. Create a label for the optimizable address range as follows:

   a. Click the Label tab.

   b. Enter a label of “optimizable” in the Range Label box, then press Return or click the Apply button. The label appears in the optimizable entry in the Address Ranges list box.

4. Set up wait-state values for the optimizable memory:

   a. Click the Wait States tab.

   b. Enter values of 2 in the Read and Write boxes under “Initial,” then press Return or click the Apply button. (Leave the Burst boxes blank.) The wait-state values appear in the Address Ranges list box.

5. Select the next unlabeled range (400000 - 3FFFFFFF) listed in the Address Ranges box. Notice that the listed range values appear in the Start and End address boxes.

6. Replace the End Address value by double-clicking on the entry box and entering 4000FF.


**Note**

There are no memory instances, either Seamless CVE or otherwise, in this address range. This and the remaining steps in this section simply demonstrate how to set up memory-access ranges.

7. Click the Label tab and enter “hardware” in the Range Label entry box.

8. Click the Apply button. A new entry, at addresses 400000 - 40000FF, with the label “hardware” appears in in the Address Ranges list box. The former hardware-only range is now split into two ranges.

9. Select the next range on the list and label it “hardware2.”

10. Select the *screen* entry (3FFFFFF0 - 3FFFFFF3), which is next in the list. Although the *screen* is actually based on an optimizable register memory (hence the “optimizable” icon under the Access column), we will pretend it is hardware-only for the present. Enter a label of “screen” for this range then click Apply.

11. Select the unlabeled range at the bottom of the list in the Address Ranges list box (3FFFFFF4 to FFFFFFFF).

12. Enter “illegal” in the Range Label text-entry box, then click the Apply button.

13. Select the Access tab and then click the Illegal access button. This makes addresses 400100 to FFFFFFFF an “illegal” range, as indicated by the icon in the Address Ranges list.

14. Click the Close button to close the window. Notice that the Memory Access Ranges icon in the Session window is no longer highlighted, indicating that this step has been done.

# Saving the Configuration

Save the current configuration by performing the following steps:

1. Click the Save Configuration icon in the Seamless CVE Session window (shown below) or select the **File > Save As** menu item.


**Save Configuration**

2. In the Save As dialog box, enter a configuration filename (and path, if necessary).

3. Click Ok to save the configuration.

# Starting the Cosimulation

1. Click the **Run** button in the Seamless CVE main window. The button changes to yellow and remains pressed, indicating that cosimulation can start. In addition, a terminal window appears showing a software simulator startup message:

   **CVE NOTE: Waiting to connect to hardware process ...**

2. Go to the NC Verilog simulator's main window, activate the Navigator, and set up a waveform display window. Display the signals at the top level of the design, as well as register R30, which is one level down, in the *cpu* module.

3. Click the run button on NC Verilog main window.

   This starts the hardware simulation, but the simulation cannot run until its software begins to execute. Notice that the Run button turns green, indicating that cosimulation has begun. The Seamless CVE models in the design cause Seamless CVE to start up the software simulator. The

software simulator terminal window displays a series of messages followed by this prompt:

**(mdb)**

The Run Status window indicates that the hardware simulator is waiting (for the software simulation to start) and the software simulator is interactive (that is, waiting for you to enter a command to start the software simulation). Neither hardware nor software simulation can proceed until you respond to the software simulator prompt.


4. Enter ***run*** at the **(mdb)** prompt. The Screen window appears and displays the following message.

```
Welcome to the Seamless Tutorial!!
Using the DLX Processor and the MDB Debugger.
```

Notice that the Run Status for both of the simulators changes to “Running” then back to “Interactive” for both simulators. The software simulator runs to a breakpoint and displays a message similar to the following one (the timing may vary):

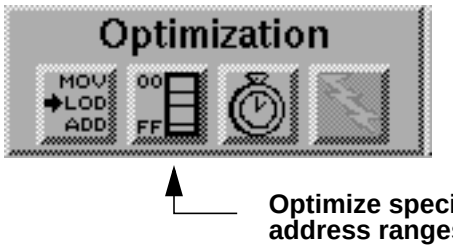
```
14 secs; 656 instr; 46 instr/sec
Hit Breakpoint 1 at 0x00000000 (begin+0x00000000)
(0x00000000) begin              nop
(mdb)
```

At this point, the run status of both simulators is interactive. In addition, waveforms appear in the hardware simulator’s waveform window, showing the bus activity that takes place during the simulation run. Values in register R30, an internal cpu register are also displayed. Display of internal registers as signals is a feature of most PSPs.

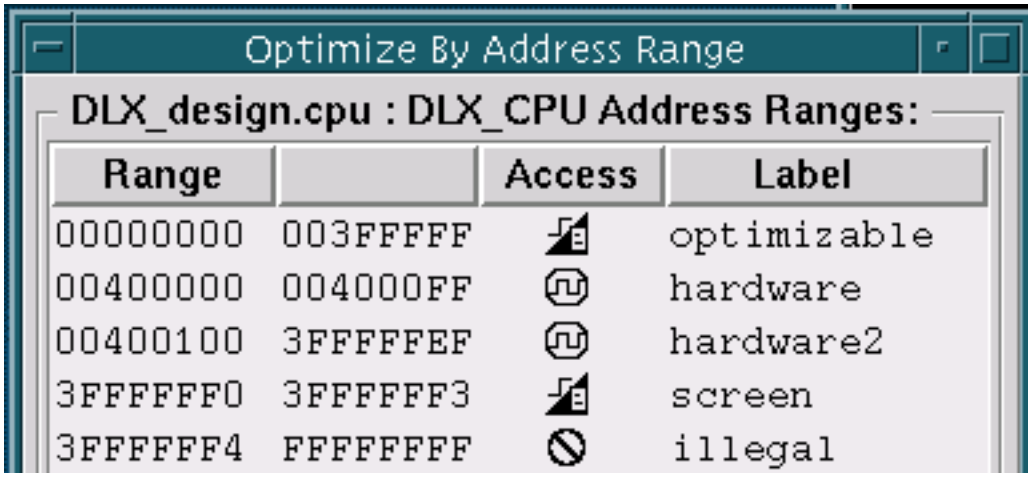
# Enabling Address-Range Optimization

Enable address-range optimization for the optimizable addresses in the processor address space by performing the following steps:

1. Click the Optimize Address Ranges icon in the Seamless CVE Session window (shown below). This activates the Optimize by Address Range dialog box.



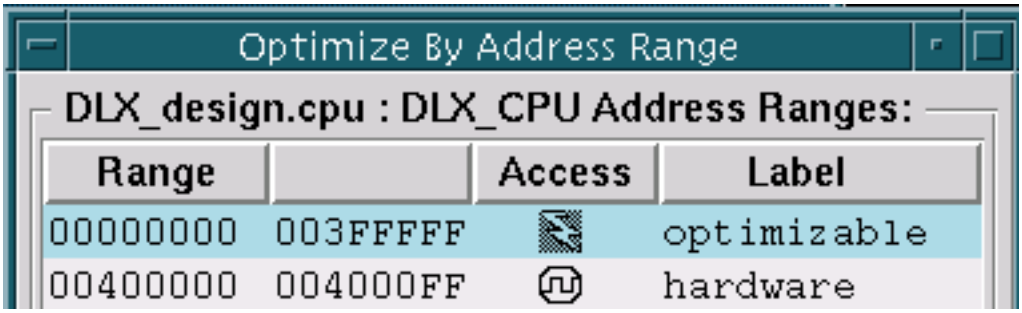

   The Address Ranges list contains the ranges you set up in the previous section, as shown below.




2. Click the range labeled “optimizable.” The start and end addresses of the range appear in the entry boxes under Optimization Entry.

3. Click the On button. This modifies the optimizable range in the Address Ranges list as shown below. The “lightning bolt” icon indicates that

processor accesses to this range can take place directly through software rather than generating hardware bus cycles.




You can enable optimized access to any portion of an optimizable address range.

4. Click the Close button to dismiss the Optimize By Address Range dialog box. The Optimize Address Ranges icon in the Seamless CVE session window is now highlighted.

5. Click the Run button in the NC Verilog simulator session window.

   This time, the simulation runs faster. In the waveform display, notice the relative lack of address- and data-bus activity during the second run. The clock runs in the hardware simulation as before. However, the software simulator now accesses memory directly except when writes to the screen, in which case it needs to generate bus activity in the hardware simulation. You can confirm this by noting that a value of 0x3FFFFFF0 is present on the address bus during these write cycles.

6. Select the **Optimize > Name Optimization** menu item. This activates the Optimization Set dialog box. This dialog box allows you to save the current optimization state for later recall.

7. Type in a name such as *opt1* in the text-entry box in the Optimization Set dialog box then click Ok to save the optimization set. Notice that the Optimization Set Enable (“lightning bolt”) icon under Optimization group

in the main Seamless CVE window becomes pressed and is highlighted yellow, meaning that a named optimization set is active.


8. Click the Optimization Set Enable icon to disable the optimization set. The icon becomes “unpressed” and is no longer highlighted. (You can also use the **Optimize > Unoptimize** menu item.) Click the icon again to re-enable the optimization set.

9. Save the current configuration by selecting the **File > Save** menu item.

# Exiting from the Cosimulation

1. Select the **File > Exit** menu item in the Seamless CVE session window or enter “exit” at the command-line. A message box appears saying “Simulator is running. Exit anyway?”

2. Click Yes to exit from the ModelSim VHDL simulator. The Seamless CVE Session window and simulator windows disappear.

# Restarting Seamless CVE using the Configuration File

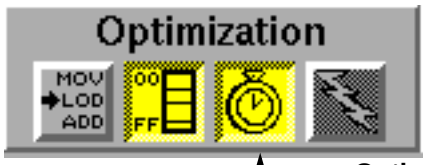
Invoke Seamless CVE using the following command:

```
$CVE_HOME/bin/cve    my_config
```

where *my_config* is the name of the configuration file you saved previously. Seamless CVE, ModelSim VHDL simulator, and software simulator all start up. Notice that the configuration in *my_config* is restored and the cosimulation is ready to start. You can confirm this by clicking on the appropriate CPU Setup and Optimization icons and checking the values that appear in the corresponding dialog boxes.

# Enabling Time Optimization

1. Click the Optimize time icon to activate Seamless time optimizations. The Time Optimizations icon button (shown below) is now “pressed” and highlighted yellow.




**Optimize time by allowing software to run ahead of hardware (using Time Optimization dialog box settings)**

2. Go to the hardware simulator’s main window and set up a waveform viewing window as you did earlier.

3. Click the run button in the hardware simulator.

   The Run button on the Seamless CVE session window turns green, indicating that cosimulation has begun.

4. Enter ***run*** at the (mdb) prompt in the software simulator’s terminal, as you did earlier in “Starting the Cosimulation.”

   Notice that the same number of instructions are executed as before, but in much less time. The software has run at full speed, decoupled from the hardware simulation, and far fewer clock cycles have occurred in the hardware simulation. The only time hardware clock cycles are required is when the program accesses the screen to print out the message. Although the tutorial program is too simple to show the full effect, usually over 99 percent of hardware clock cycles can be eliminated without affecting simulation results.

5. Select the **Optimize > Name Optimization** menu item. The Optimization Set dialog box appears.

6. Enter a name (different than the one you used previously) for the current optimization set, then click Ok.

7. Select the **Optimize > Recall Optimization** menu item. The Optimization Sets dialog box appears.

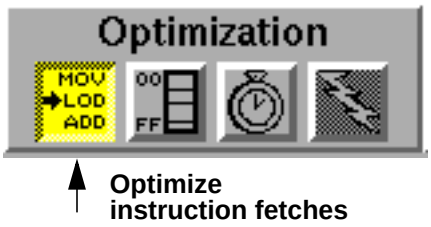
8. Select the first optimization set you saved by clicking on its name, then click the Apply button. Now select the optimization set you saved in this section and click Apply. Notice the effect on the Optimizaton icons.

9. Click the Close button to dismiss the Optimization Set dialog box.

10. Select the **Optimize > Unoptimize** menu item to clear the current optimization set.

# Enabling Instruction Fetch Optimization

1. Click in on the Instruction Fetch Optimizations icon. The icon becomes highlighted as shown below.




   Instruction fetch optimization is a convenient way to automatically enable optimizations for all instruction-fetch bus cycles. This eliminates hardware bus-cycle activity for instruction fetches, allowing the ISS to fetch the instructions directly from memory.

2. Run the hardware and software simulators as before.

3. Select the **Optimize > Unoptimize** menu item.

4. Run the hardware and software simulators again. Notice the difference in run time and bus activity with and without instruction fetch optimizations enabled.

This concludes the *Seamless CVE and ModelSim VHDL Tutorial.* You can experiment with different combinations of optimization settings to see how they

affect cosimulation. For example, try turning on optimizations for single addresses or ranges of addresses to see how they affect simulation speed and bus cycle activity.