SYNOPSYS®

DesignWare IBM PowerPC 405-S CPU Core

Design View coreKit Release Note

Database Release 1.1a

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Contents

DesignWare IBM PowerPC 405-S CPU Design View coreKit Release Note

This release note provides the latest information on Release 1.1a of the DesignWare IBM PowerPC 405-S CPU Design View coreKit. The Design View coreKit includes:

- A simulation model and simulation environment for the DesignWare IBM PowerPC 405-S CPU Core
- A simulation model and simulation environment for a PLB4XAHB bridge, which you can use to connect the PowerPC 405-S CPU processor local bus (PLB) to an AMBA high-performance bus (AHB)
- A timing model for an example implementation of the DesignWare IBM PowerPC 405-S CPU Core

For information regarding the Implementation View coreKit, which includes synthesizable RTL for the DesignWare IBM PowerPC 405-S CPU Core and the PLB4XAHB bridge, send email to designware@synopsys.com.

System Requirements

Before you install the DesignWare IBM PowerPC 405-S CPU Design View coreKit, verify that your system meets the following hardware and software configuration requirements.

Hardware Requirements

The PowerPC 405-S CPU Design View coreKit requires a SPARC or Linux-compatible workstation.

The SPARC workstation must be configured as follows:

- The Solaris 2.9 operating system, with all requisite patches installed.

The Linux workstation must be in one of the following configurations:

- The Red Hat Enterprise Linux v. 3 operating system, with all requisite patches installed.
- The AMD64 Red Hat Enterprise Linux v. 3 operating system, with all requisite patches installed.

Current information about supported system configurations and required patches is available at:

http://www.synopsys.com/products/sw_platform.html

Follow the links to Supported Operating Systems. The operating system and patch requirements for coreConsultant match the operating system and patch requirements for Y-Foundation.

Any of the above platforms also requires:

- 500 MB available disk space for installation
- 1 GB available swap space
- 1 GB RAM (physical memory) recommended
- Anonymous FTP access to ftp.synopsys.com

Software Requirements

The PowerPC 405-S CPU Design View coreKit requires the following software:

- Synopsys software and licenses:
  - coreConsultant, Version Y-2006.03-SP3 – Synopsys supplies coreConsultant for free to all DesignWare users. You must install coreConsultant before you install the PowerPC 405-S CPU Design View coreKit. For details on downloading and installing coreConsultant software, refer to the download instructions that Synopsys sent to you in response to your PowerPC 405-S CPU coreKit request. coreConsultant does not require a license.
  - Vera System Verifier, Version 2005.06-SP1 – For details about downloading and installing Vera software, refer to the download instructions that Synopsys sent to you in response to your PowerPC 405-S CPU coreKit request.

  License keys for each of the Synopsys tools above must be in a file location defined in your SNPSLMD_LICENSE_FILE variable.

  The absolute paths of the executables above must be in your path variable.

- Simulation tool. The currently supported simulators for the PowerPC 405-S CPU Design View coreKit are:

  Verilog:

  - Synopsys VCS, Version 2006.06
  - Mentor ModelSim, Version 6.1a
  - Cadence NC-Verilog, Version 5.7

  License keys for third-party tools above must be in a file location defined in your LM_LICENSE_FILE variable. The absolute path to the simulator executable must be in your path variable.

- C Compiler – You can use either cc or gcc.
  - 32-bit Linux: gcc version 3.4.3 or greater
  - 64-bit Linux: gcc version 3.4.4 or greater
  - 32-bit SunOS: gcc version 2.95.2 or greater
  - 64-bit Sparc64: Sun cc compiler is recommended.
- Perl, Version 5.0 or above
- make – The coreKit requires GNU make, Version 3.80.

  The absolute paths of these executables must be in your path variable.
- Optional software – Assembler utility for PowerPC, required if you want to compile and execute custom test programs in the supplied simulation environment. Synopsys uses the binutils/2.13 GNU assembler utility, configured to target powerpc-elf. You can download the 2.13 GNU assembler from http://ftp.gnu.org/gnu/binutils. The example scripts for compiling test programs are based on the binutils/2.13 GNU assembler. Additional setup and usage instructions are included in the *DesignWare IBM PowerPC 405-S CPU Core Design View coreKit User Guide*.

Note

The version of the IBM PowerPC Toolkit used in the PowerPC 405-S CPU Design View coreKit verification environment is PLB_TOOLKIT4X_012203.

Requirements for AHB Bridge Simulation

To work with the simulation environment provided for the PLB4XAHB bridge, you need the following additional resources:

- DesignWare AMBA, 2.0 AHB/APB Verification IP. – For instructions to download DesignWare AMBA 2.0 AHB/APB Verification IP, go to http://www.synopsys.com/designware/amba_solutions.html and follow the links to AMBA 2.0 AHB/APB Verification IP. Version 3.72 of the AMBA 2.0 AHB/APB Verification IP was tested for this release.

To set up and simulate the PLB4XAHB bridge verification environment, follow the instructions in the *PLB4XAHB Bridge Application Note*, which is available in your <*workspace*>/PLB4XAHB/docs directory (filename PLB4XAHB_application_note_<version>.pdf).

Supported Languages

This release of the PowerPC 405-S CPU Design View coreKit supports Verilog.

Environment Variables

Make sure the following environment variables are set before you begin the PowerPC 405-S CPU coreKit installation:

- VERA_HOME – The absolute path to where you installed Vera.
- SNPSLMD_LICENSE_FILE – Contains all Synopsys features including the coreConsultant and DesignWare keys:

```
% setenv SNPSLMD_LICENSE_FILE <path_to_Synopsys_key_file>
```

- LM_LICENSE_FILE – Contains third-party features:

```
% setenv LM_LICENSE_FILE <path_to_third_party_key_file>
```

- VCS_HOME – The absolute path to your VCS installation (if you are using VCS)
- VCS_CC – The absolute path to the SunPro C or gcc compiler (if you are using VCS)
- CDS_INST_DIR – The absolute path to your Cadence tools installation (if you are using NC-Verilog). For example, <*Cadence_install_path*>/tools.

- path – Include the absolute paths to:
  - coreConsultant (<*coreConsultant_install_dir*>/sparcOS5(or linux)/dware/bin)
  - GNU make
  - perl
  - $VERA_HOME/bin
  - $VCS_HOME/bin (if you are using VCS)
  - $CDS_INST_DIR/tools/bin (if you are using NC-Verilog)
- LD_LIBRARY_PATH:
  - Include $VERA_HOME/lib
  - Include $CDS_INST_DIR/tools/lib (if you are using NC-Verilog)

Example Setup File

```
#vera setup
setenv VERA_HOME <vera_path>
set path = ( $VERA_HOME/bin $path )
setenv LD_LIBRARY_PATH $VERA_HOME/lib:$LD_LIBRARY_PATH

#NC setup
setenv CDS_INST_DIR <Cadence_install_path>
set path = ($CDS_INST_DIR/tools/bin $path)
setenv LD_LIBRARY_PATH $CDS_INST_DIR/tools/lib:$LD_LIBRARY_PATH

#ModelSim setup
set path = ( <modelsim_path> $path )

#VCS setup
setenv VCS_HOME <vcs_path>
setenv VCS_CC /opt/SUNWspro/bin/cc
set path = ( ${VCS_HOME}/bin $path )

#license setup
setenv SNPSLMD_LICENSE_FILE <snpslmd_path>
setenv LM_LICENSE_FILE <cds_license_path>: \
  <snpslmd_path>:<sim_license_path>
```

Note

If you have problems in simulation with the LM_LICENSE file settings as shown above, then use the <*port*>:<*server*> type settings. For example:

```
setenv LM_LICENSE_FILE 1928@ricotta:1928@fettuccine:1928@adminac
```

Licensing Information

Table 1 shows the licence requirements for installation and simulation.

Install the Synopsys tool licenses in $SNPSLMD_LICENSE_FILE. Install your simulation tool license in $LM_LICENSE_FILE.

Table 1: License Features Required for Design View coreKit

Activity	Licenses Required
Installing the coreKit	DesignWare
Simulation	DesignWare or DesignWare-Regression Simulator License

Changes From Last Release

- The HP platform is no longer supported
- 64-bit mode simulations now supported.
- PLB-to-AHB replaced with the new PLB4XAHB bidirectional bridge

Known Problems and Limitations

There are no known problems or limitations in Release 1.1a of the DesignWare IBM PowerPC 405-S CPU Design View coreKit.

Refer to the *coreConsultant Release Note*, available from the coreConsultant Help menu, for a list of known problems and limitations in coreConsultant.

Questions

For customer support:

- Log on to http://solvnet.synopsys.com using your SolvNet ID and password
  - Under My Support, click “Enter a Call to the support center” at the top right corner
  - Select DesignWare Star IP from the Product menu
  - Select Processors from the Sub-Product menu
  - Specify PowerPC 405-S CPU on the subject line
  - Fill in all relevant details, then click Submit
- Send an e-mail message to support@synopsys.com
- Call our Customer Support Hotline: 1-800-245-8005

Other DesignWare Products

For additional information about DesignWare products, or to subscribe to the DesignWare Technical Bulletin, send e-mail to designware@synopsys.com.

You can also visit the DesignWare Web site at http://www.synopsys.com/designware.