eASIC® Announces Tape-out of First Structured ASIC Array

The Structured eASIC test application was released to a European IDM partner for fabrication in 0.13 micron process technology

San Jose, California, May 28, 2004 -- eASIC® Corporation, a provider of breakthrough Structured ASIC technology and products, today announced taping out of its first Structured ASIC array to be fabricated by a European IDM partner at 0.13 micron process technology. The taped-out array called FA1, is the smallest member of the company's ***Structured eASIC*** product family. The initial parts will be used to characterize timing and power for the Structured ASIC fabric and cell libraries. The complete product family is scheduled to be released for production in early Q1 2005. This product is being co-developed with Flextronics Semiconductor who will also be offering Structured ASIC products and services.

"The Structured ASIC evolved out of the need for a more flexible, less costly approach for completing medium-complexity ASIC designs in a more-timely manner to meet changing market conditions" said Rich Wawrzyniak, Senior Analyst, ASIC – SoC at Semico Research Corp. "The rising costs and increasing design cycle times for Standard Cell and System-on-a-Chip products has pushed many would-be users out of the market and forced them to explore other alternatives. The Structured ASIC approach provides these would-be users with a welcome alternative. The Direct-write eBeam approach employed by eASIC allows for an even lower manufacturing cost which enables even more would-be users to consider an ASIC solution once again and increases the potential market even more."

"Taping out our first Structured ASIC device is an important milestone in our business strategy," said Zvi Or-Bach, eASIC President and CEO. "This move, which was achieved through joint efforts with Flextronics Semiconductor, is a step forward along the path to offering innovative, NRE-free Structured ASIC devices. There is a clear market need for alternative solutions to Standard Cell and a strong momentum is being built for Structured ASICs. The combination of our patented technology with Flextronics' expertise and resources creates a very powerful solution that allows customers to significantly cut cost and shorten time-to-market of ASIC designs."

Structured eASIC

eASIC® has developed a unique Structured ASIC technology called ***Structured eASIC***. The patented ***Structured eASIC*** architecture consists of an array of logic cells (eCells) with SRAM based LUTs (Look Up Table) and flip-flops. eCells are inter-connected by a segmented wiring grid utilizing upper metal layers, which are customized per customer design with a single Via-mask. Logic programming of the eCell is done similarly to an FPGA, by loading a bit-stream to program the LUTs and flip-flops after powering up the device. Thus, a customer design is implemented on the ***Structured eASIC*** fabric by using a combination of bit-stream to program the LUTs and single custom Via-mask for customizing the routing. Moreover, single Via-customization is a perfect fit for an alternative lithography approach, namely the Direct-write eBeam. Using Direct-write eBeam completely eliminates the customization tooling cost, shortens time-to-market and adds manufacturing flexibility.

FA1 – First Structured eASIC Family Member

FA1 is the smallest out of four members of the ***Structured eASIC*** product family.

FA1 Specifications:

- Usable ASIC gates: 600K
- bRAM (high density diffused single-port memory blocks): 384 Kb

- bRAM blocks: 12
- eRAM (configurable distributed dual-port memory, flexibly traded-off with logic gates, approximately one bit per gate): 640 Kb
- eRAM blocks: 160
- I/Os: 372
- PLL: 4

Target Characteristics:

- Gate Speed:
  - Fast input to output: 60ps
  - Average Gate Delay: 80ps
  - Flip-Flop CLK to Q: 100ps
- Operating frequencies: 400 MHz
- Gate Power: 20nW/MHz/gate
- bRAM Power (fully used): 6mW/block @ 100 MHz
- System Power: 350 mW (typical)

Structured eASIC Family Characteristics:

- ASIC gates: 0.6M - 3M
- Memory bits: 0.4M-1.6M
- User I/Os: 372 - 820
- PLL's: 4-8

About eASIC

eASIC® has developed a breakthrough Structured ASIC technology aimed at dramatically reducing the overall fabrication cost and time of customized high-performance semiconductor chips. eASIC's technology enables rapid and low-cost ASIC and System-on-Chip designs by its innovative use of proven programmable logic fabric in conjunction with single-via customizable segmented routing. As single-via generates ten times higher throughput of Direct-write e-Beam customization, it enables eASIC to offer NRE-free Structured ASIC. The ***Structured eASIC*** technology was successfully proven in silicon and validated by world-class semiconductor vendors. Partnering with industry leaders to jointly develop, manufacture and market Structured ASIC products, the company is positioned to become the preferred Structured ASIC solution.

Headquartered in San-Jose California, eASIC Corporation is a privately held company, founded in 1999 by Zvi Or-Bach, the founder of Chip Express. Or-Bach is viewed by many as the "father of Structured ASIC technology".

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