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Encounter® Menu Reference

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Contents

About This Manual . . . 61

Audience . . . 61
How This Manual Is Organized . . . 61
Conventions Used in This Manual . . . 62
Related Documents . . . 63

1
The Main Window . . . 65

Main Window Components . . . 67
Toolbar Widgets . . . 68
Design Views . . . 70
- Floorplan View . . . 71
- Amoeba View . . . 71
- Physical View . . . 71

Tool Widgets . . . 72
- Floorplan Widgets . . . 73
- Partition Widgets . . . 74
- Flip Chip Widget . . . 74
- Wire Editing Widgets . . . 75

Color Preferences . . . 77
Objects Page . . . 77
Wire/Via Page . . . 79
View Only Page . . . 80
Custom Page . . . 80
Cell Layout Page . . . 81
Customizing Layer Color Patterns . . . 82
Customize Tab . . . 83
Applying Preferences in the All Colors Form . . . 87
Save Color Preference . . . 87
Multicolor Layers . . . 88
Metal Layers and Other Layered Components . . . 88

Creating and Editing Color Groups . . . 89
Color Bar . . . 91
Color . . . 93
Viewing OA Cell Layout . . . 94
Set Ruler Mode . . . 96
Set Ruler Mode – Fields and Options . . . 96
Satellite Window . . . 98
Context Pop-up Attribute Viewer . . . 99
Auto Query . . . 101
Docking Sub-windows . . . 102
Tear-off Menus and Sub-menus . . . 103
Mouse Operation . . . 104
Keyboard Shortcuts . . . 104
Viewing the Documentation Library through the Help Menu . . . 105
Displaying the Encounter Version Number, and Patent- and Copyright-Information . . . 105

2
Design Menu . . . 107

Import Design . . . 108
Design Import – Basic . . . 109
Design Import – Basic Fields and Options . . . 110
Related Text Commands . . . 112
Related Topics . . . 112
Design Import – Advanced . . . 113
Delay Calculation . . . 114
Delay Calculation Fields and Options . . . 114
Related Text Commands . . . 115
Related Topics . . . 115
GDS . . . 116
GDS Fields and Options . . . 116
Related Text Commands . . . 117
ILM . . . 118
ILM Fields and Options . . . 118
IPO/CTS . . . 120
IPO/CTS Fields and Options . . . 120

Related Text Commands 120
OpenAccess 121
OpenAccess Fields and Options 121
Related Text Commands 122
Power 123
Power Fields and Options 123
Related Text Commands 124
Related Topics 124
RC Extraction 125
RC Extraction Fields and Options 126
Related Text Commands 128
Related Topics 128
RTL 129
RTL Fields and Options 129
SI Analysis 130
SI Analysis Fields and Options 130
Related Text Commands 131
Timing 132
Timing Fields and Options 133
Related Text Commands 134
Related Topics 134
Yield 135
Yield Fields and Options 136
Related Text Commands 136
MMMC 137
Fields and Options 137
MMMC Browser 139
Add Library Set 142
Fields and Options 142
Related Text Commands 143
Related Topics 143
Add OP Cond 144
Fields and Options 144
Related Text Commands 144
Related Topics 145
Add RC Corner 146

Fields and Options . . . 146
Related Text Commands . . . 148
Related Topics . . . 148
Add Constraint Mode . . . 149
Fields and Options . . . 149
Related Text Commands . . . 149
Related Topics . . . 150
Add Delay Corner . . . 151
Fields and Options . . . 153
Related Text Commands . . . 155
Related Topics . . . 155
Add Power Domain . . . 156
Fields and Options . . . 157
Related Text Commands . . . 159
Related Topics . . . 159
Add Analysis View . . . 160
Fields and Options . . . 160
Related Text Commands . . . 160
Related Topics . . . 161
Add Hold Analysis View . . . 162
Fields and Options . . . 162
Related Text Commands . . . 163
Related Topics . . . 163
Add Setup Analysis View . . . 164
Fields and Options . . . 164
Related Text Commands . . . 165
Related Topics . . . 165
MMMC Preferences . . . 166
Fields and Options . . . 166
Related Text Commands . . . 167
Add Object . . . 168
Fields and Options . . . 168
Related Text Commands . . . 168
Edit Library Set . . . 169
Fields and Options . . . 169
Related Text Commands . . . 170

Edit OP Cond . . . 171
Fields and Options . . . 171
Related Text Commands . . . 172
Edit RC Corner . . . 173
Fields and Options . . . 173
Related Text Commands . . . 175
Edit Constraint Mode . . . 176
Fields and Options . . . 176
Related Text Commands . . . 177
Edit Delay Corner . . . 178
Fields and Options . . . 179
Related Text Commands . . . 180
Edit Power Domain . . . 181
Fields and Options . . . 182
Related Text Commands . . . 183
Import RTL . . . 184
RTL Import – Logical . . . 185
RTL Import – Logical Fields and Options . . . 186
Related Text Commands . . . 187
RTL Import – Physical . . . 188
RTL Import – Physical Fields and Options . . . 188
Related Text Commands . . . 189
RTL Files . . . 190
RTL Files Fields and Options . . . 190
VHDL Import . . . 191
VHDL Import Fields and Options . . . 191
VHDL Files . . . 192
VHDL Files Fields and Options . . . 192
DEF File . . . 193
DEF File Fields and Options . . . 193
Restore Design . . . 194
Restore Design . . . 195
Restore Design Fields and Options . . . 195
Related Text Commands . . . 195
Related Topics . . . 195
Restore OA Design . . . 196

Restore OA Design Fields and Options . . . 196
Related Text Commands . . . 196
Related Topics . . . 196
ECO Design . . . 197
ecoDesign Fields and Options . . . 197
Related Text Commands . . . 198
Save Design As . . . 199
Save Design . . . 200
Save Design Fields and Options . . . 200
Related Text Commands . . . 200
Related Topics . . . 201
Save OA Design . . . 202
Save OA Design Fields and Options . . . 202
Related Text Commands . . . 202
Related Topics . . . 202
Load . . . 203
Load – Partition . . . 204
Load Partition Fields and Options . . . 204
Related Text Commands . . . 205
Related Topics . . . 205
Load – Floorplan . . . 206
Load FPlan File Fields and Options . . . 206
Related Text Commands . . . 206
Related Topics . . . 206
Load – Place . . . 207
Load Placement Fields and Options . . . 207
Related Text Commands . . . 207
Related Topics . . . 208
Load – Route . . . 209
Load Route Fields and Options . . . 209
Related Text Commands . . . 209
Related Topics . . . 210
Load – DEF . . . 211
Load DEF File Fields and Options . . . 211
Related Text Commands . . . 211
Related Topics . . . 212

Load – TDF . . . 213
Load TDF File Fields and Options . . . 213
Related Text Commands . . . 213
Related Topics . . . 214
Load – PDEF . . . 215
Load PDEF File Fields and Options . . . 215
Related Text Commands . . . 215
Related Topics . . . 216
Load – I/O File . . . 217
Load I/O File Fields and Options . . . 217
Related Text Commands . . . 217
Related Topics . . . 217
Load – SPEF . . . 218
Load SPEF File Fields and Options . . . 218
Related Text Commands . . . 218
Related Topics . . . 219
Load – SDF . . . 220
Load SDF File Fields and Options . . . 220
Related Text Commands . . . 220
Related Topics . . . 221
Load – Power Waveform . . . 222
Load – OA Database . . . 223
Load OA Database Fields and Options . . . 223
Related Text Commands . . . 223
Related Topics . . . 223
Save . . . 224
Save – Partition . . . 225
Save Partition Fields and Options . . . 225
Related Text Commands . . . 226
Related Topics . . . 226
Save – Floorplan . . . 227
Save FPlan File Fields and Options . . . 227
Related Text Commands . . . 227
Related Topics . . . 228
Save – Place . . . 229
Save Placement File Fields and Options . . . 229

Related Text Commands . . . 229
Related Topics . . . 230
Save – Route . . . 231
Save Route File Fields and Options . . . 231
Related Text Commands . . . 231
Related Topics . . . 232
Save – Netlist . . . 233
Save Netlist Fields and Options . . . 233
Related Text Commands . . . 233
Related Topics . . . 234
Save – DEF . . . 235
Save DEF Fields and Options . . . 235
Related Text Commands . . . 236
Related Topics . . . 236
Save – TDF . . . 237
Save TDF Fields and Options . . . 237
Related Text Commands . . . 237
Related Topics . . . 238
Save – PDEF . . . 239
Save PDEF Fields and Options . . . 239
Related Text Commands . . . 239
Related Topics . . . 239
Save – I/O File . . . 240
Save I/O File Fields and Options . . . 240
Related Text Commands . . . 241
Related Topics . . . 241
Save – Rail Analysis Results . . . 242
Save Rail Analysis Results Fields and Options . . . 242
Related Text Commands . . . 242
Related Topics . . . 243
Save – Save Timing Budget . . . 244
Save – Save Timing Budget Fields and Options . . . 244
Related Text Commands . . . 245
Related Topics . . . 245
Save – GDS . . . 246
Save – GDS Fields and Options . . . 246

Related Text Commands 250
Related Topics 250
Check Design 251
Check Design Fields and Options 252
HTML Check Design Report 255
Related Text Commands 256
Report 257
Summary Report 258
Summary Report Fields and Options 259
HTML Summary Report 260
Related Text Commands 262
Gate Count Report 263
Gate Count Report Fields and Options 263
Related Text Commands 263
Netlist Statistics 264
Preferences 265
Preferences – Design 266
Preferences – Design Fields and Options 266
Cell Layout Preference 268
Cell Layout Preference Form – Fields and Options 268
Related Text Commands 269
Preferences – Display 270
Preferences – Display Fields and Options 270
Related Text Commands 276
Preferences – Floorplan 277
Preferences – Floorplan Fields and Options 277
Related Text Commands 279
Preferences – Selection 280
Preferences – Selection Fields and Options 280
Related Text Commands 281
Preferences – Windows 282
Preferences – Windows Fields and Options 282
Related Text Commands 283
Preferences – Flightline 284
Binding Key 288
Binding Key Fields and Options 288

Related Text Commands . . . 289
Default Binding Key Settings . . . 289
Mode Setup . . . 294
Mode Setup – Clock Mesh . . . 295
Clock Mesh – Analysis . . . 296
Fields and Options . . . 296
Related Text Commands . . . 298
Clock Mesh – Synthesis . . . 299
Fields and Options . . . 299
Related Text Commands . . . 300
Clock Mesh – Optimization . . . 301
Fields and Options . . . 301
Related Text Commands . . . 302
Mode Setup – CTS . . . 303
CTS – Trace . . . 304
Fields and Options . . . 305
Related Text Commands . . . 305
CTS – Route/EM . . . 306
Fields and Options . . . 307
Related Text Commands . . . 308
CTS – Optimization . . . 309
Fields and Options . . . 309
Related Text Commands . . . 310
CTS – Miscellaneous . . . 311
Fields and Options . . . 311
Related Text Commands . . . 313
Mode Setup – Filler . . . 314
Fields and Options . . . 314
Related Text Commands . . . 315
Mode Setup – NanoRoute . . . 316
NanoRoute – Route . . . 317
Fields and Options . . . 318
Related Text Commands . . . 321
NanoRoute – Timing/SI . . . 322
Fields and Options . . . 323
Related Text Commands . . . 324

NanoRoute – DFM . . . 325
Fields and Options . . . 325
Related Text Commands . . . 329
NanoRoute – Antenna . . . 330
Fields and Options . . . 330
Related Text Commands . . . 332
NanoRoute – AdvDRC . . . 333
Fields and Options . . . 333
Related Text Commands . . . 334
NanoRoute – Misc . . . 335
Fields and Options . . . 335
Related Text Commands . . . 337
Mode Setup – Optimization . . . 338
Optimization Fields andOptions . . . 338
Related Text Commands . . . 342
Mode Setup – Placement . . . 343
Placement . . . 344
Fields and Options . . . 344
Related Text Commands . . . 349
RefinePlace . . . 350
Fields and Options . . . 350
Related Text Commands . . . 351
Mode Setup – ScanReorder . . . 352
Fields and Options . . . 352
Related Text Commands . . . 353
Mode Setup – StreamOut . . . 354
Fields and Options . . . 355
Related Text Commands . . . 356
Mode Setup – TieHiLo . . . 357
Fields and Options . . . 357
Related Text Commands . . . 358
Mode Setup – Trial Route Mode . . . 359
Trial Route Mode – Basic . . . 360
Fields and Options . . . 360
Related Text Commands . . . 365
Trial Route Mode – Advanced . . . 366

Fields and Options 366
Related Text Commands 370
Global Variables 371
Global Variable Editor – Fields and Options 371
Related Text Commands 372
Multiple CPU Processing 373
Multiple CPU Processing – Basic 374
Multiple CPU Processing – Basic Fields and Options 374
Related Text Command 375
Related Topics 375
Multiple CPU Processing – Host Setup 377
Multiple CPU Processing – Host Setup Fields and Options 377
Related Text Command 379
Related Topics 379
Show/Hide 380
Exit 381

3
Edit Menu 383

Find/Select Object 385
Find/Select Object Fields and Options 386
Mode Settings 389
Related Text Commands 392
Deselect All 394
Highlight Selected 395
Related Text Commands 395
Clear Highlight 396
Related Text Commands 396
Edit Highlight Color 397
Edit Highlight Color Fields and Options 397
Related Text Commands 397
Clear Ruler 398
Pin Editor 399
Pin Editor Fields and Options 400
Related Command 404

Related Topics 404
Reorder Pin List 405
Reorder Pin List Fields and Options 405
Pin Alignment 407
Pin Alignment Fields and Options 407
Related Text Command 408
Wire Editor 409
Edit Route– Route 410
Edit Route – Route Fields and Options 410
Related Text Commands 411
Edit Route – Nets 412
Edit Route – Nets Fields and Options 413
Related Text Commands 414
Select A File (for Net Names) 415
Select A File (for Net Names) Fields and Options 415
Edit Route – Override 417
Edit Route – Override Fields and Options 417
Related Text Commands 418
Select A File (for Override Values) 419
Select A File (for Override Values) Fields and Options 420
Edit Route – Shielding 421
Edit Route – Shielding Fields and Options 421
Related Text Commands 422
Edit Route – Snap 423
Edit Route – Snap Fields and Options 423
Related Text Commands 424
Edit Route – Via 425
Edit Route – Snap Fields and Options 425
Related Text Commands 426
Edit Route – Wire Group 427
Edit Route – Wire Group Fields and Options 428
Edit Route – Miscellaneous 433
Edit Route – Miscellaneous Fields and Options 433
Related Text Commands 435
Special Route Options 437
Special Route Options Fields and Options 437

Related Text Commands 438
Select/Delete/Deselect Routes 439
Select/Delete/Deselect Routes Fields and Options 440
Related Text Commands 441
Edit Via 442
Edit Via – Geometry 442
Edit Via – Geometry Fields and Options 443
Related Topics 445
Related Text Commands 445
Edit Via – Viacell 446
Edit Via – Viacell Fields and Options 446
Related Topics 446
Edit Route Widgets 447
Object 449
Edit Pin Group 450
Edit Pin Group Fields and Options 450
Add Group Pins 451
Add Group Pin Fields and Options 452
Related Text Commands 453
Edit Net Group 454
Edit Net Group Fields and Options 454
Add Group Nets 455
Add Group Net Fields and Options 456
Related Text Commands 457
Create Non Default Rules 458
Fields and Options 458
Related Text Commands 459
Add Via Cell 460
Add Via Cell Fields and Options 460
Custom Object Editor 461
Custom Object Editor Fields and Options 461

4
Synthesis Menu 463
RTL Synthesis 464

RTL Synthesis Fields and Options . . . 464
Related Text Commands . . . 465
Supported Subforms . . . 465
RTL Synthesis Basic Options . . . 466
RTL Synthesis Options – Basic Fields and Options . . . 466
Related Text Commands . . . 468
RTL Synthesis Advanced Options . . . 469
RTL Synthesis Options – Advanced Fields and Options . . . 469
Related Text Commands . . . 470
RTL Synthesis Variables Setting . . . 471
RTLC Variables Setting Fields and Options . . . 471
Related Text Commands . . . 472
RTL Synthesis Attributes Setting . . . 473
RTL Attributes Setting Fields and Options . . . 473
Related Text Commands . . . 474
Gates Synthesis . . . 475
N2N Synthesis Fields and Options . . . 475
Related Text Commands . . . 476
Supported Subforms . . . 476
Gates Synthesis Basic Options . . . 477
N2N Options – Basic Fields and Options . . . 477
Related Text Commands . . . 479
Gates Synthesis Advanced Options . . . 480
N2N Options – Advanced Fields and Options . . . 480
Related Text Commands . . . 481

5
Partition Menu . . . 483

Specify Partition . . . 484
Specify Partition Fields and Options . . . 485
Related Text Commands . . . 489
Related Topics . . . 489
Power Domain . . . 490
Power Domain Fields and Options . . . 490
Related Text Commands . . . 491

Related Topics 492
Specify Black Box 493
Specify Black Box Fields and Options 493
Specify Macros 496
Specify Macros Fields and Options 497
Related Text Commands 497
Related Topics 497
Create Physical Feedthrough 498
Create Physical Feedthrough Fields and Options 498
Related Text Commands 499
Related Topics 499
Show Wire Crossing 500
Show Wire Crossing – Basic 501
Show Wire Crossing - Basic Fields and Options 501
Related Text Commands 502
Related Topics 503
Add Net Names 504
Add Net Names - Fields and Options 504
Related Text Commands 505
Related Topics 505
Show Wire Crossing – Advanced 506
Show Wire Crossing - Advanced Fields and Options 506
Related Text Commands 507
Related Topics 507
Insert Feedthrough Buffer 508
Insert Feedthrough Buffer Fields and Options 508
Related Text Commands 510
Related Topics 510
Channel Estimation/FPlan Adjustment 511
Channel Estimation/FPlan Adjustment Fields and Options 511
Related Text Commands 511
Related Topics 512
Assign Partition Pins 513
Assign Partition Pins – Basic 514
Partition Fields and Options 514
Related Text Commands 515

Related Topics . . . 515
Assign Partition Pins – Advanced . . . 516
Assign Partition Pins – Advanced Fields and Options . . . 516
Related Text Commands . . . 518
Related Topics . . . 518
DeriveTimingBudget . . . 519
Derive Timing Budget – Basic . . . 520
Derive Timing Budget – Basic Fields and Options . . . 521
Related Text Commands . . . 522
Related Topics . . . 522
Derive Timing Budget – Advanced . . . 523
Derive Timing Budget – Advanced Fields and Options . . . 524
Related Text Commands . . . 525
Related Topics . . . 525
Commit Partition . . . 526
Partition Design – Fields and Options . . . 526
Related Text Commands . . . 527
Related Topics . . . 528
Run Parallel . . . 529
Run Parallel – Partition Fields and Options . . . 529
Related Text Commands . . . 530
Related Topics . . . 530
Unpartition . . . 531
Unpartition Fields and Options . . . 531
Related Text Commands . . . 531
Related Topics . . . 531
Check Pin Assignment . . . 532
Related Text Commands . . . 532
Related Topics . . . 532
Change Partition View . . . 533
Related Text Commands . . . 533

6
Floorplan Menu . . . 535

Specify Floorplan . . . 536

Specify Floorplan – Basic 537
Specify Floorplan – Fields and Options 537
Specify Floorplan – Advanced 540
Specify Floorplan – Advanced Fields and Options 540
Related Text Commands 542
Related Topics 542
Specify BlackBlob 543
Specify BlackBlob – . . . . . Fields and Options 543
Select Empty Module 544
Related Text Commands 545
Related Topics 546
Specify BlackBlob Size 547
Specify BlackBlob Size – . . . . . Fields and Options 547
Related Text Commands 549
Related Topics 549
Specify Blob Macros 550
Specify Blob Macro – . . . . . Fields and Options 550
Related Text Commands 551
Related Topics 551
Specify BlackBlob Routing Porosity 552
Specify BlackBlob Routing Porosity . . . . . Fields and Options 552
Related Text Commands 553
Related Topics 553
Automatic Floorplan 554
Plan Design 555
Plan Design – planDesign 556
Fields and Options 556
Related Text Commands 557
Plan Design – setPlanDesignMode 558
Fields and Options 559
Related Text Commands 563
Refine Macro Placement 564
Fields and Options 564
Related Text Commands 565
Related Topics 565
Finish Floorplan 566

Report Plan Design . . . 568
Related Text Commands . . . 568
Multi Plan Design . . . 569
Multi Plan Design – Auto Trials . . . 570
Fields and Options . . . 571
Related Text Commands . . . 572
Multi Plan Design – User Options . . . 574
Fields and Options . . . 575
Related Text Commands . . . 578
Floor Plan Ranking Result . . . 579
Module Colors . . . 580
Fields and Options . . . 580
FlipChip . . . 581
Resize Floorplan . . . 582
Resize Floorplan – Fields and Options . . . 583
Related Text Commands . . . 587
Relative Floorplan . . . 588
Edit Constraints . . . 589
Relative Floorplan – Place . . . 590
Relative Floorplan – Place Fields and Options . . . 590
Related Text Commands . . . 592
Related Topics . . . 592
Relative Floorplan – Reshape . . . 593
Relative Floorplan – Reshape Fields and Options . . . 593
Related Text Commands . . . 595
Related Topics . . . 595
Relative Floorplan – Resize . . . 596
Relative Floorplan – Resize Fields and Options . . . 596
Related Text Commands . . . 598
Related Topics . . . 598
Relative Floorplan – Pre-Route . . . 599
Relative Floorplan – Pre-Route Fields and Options . . . 599
Related Text Commands . . . 600
Related Topics . . . 600
Generate Constraints . . . 601
Generate Constraints Fields and Options . . . 601

Related Text Commands 604
Define Array Constraints 605
Define Array Constraints Fields and Options 605
Related Text Commands 610
Save Constraints 612
Clear Constraints 613
Create Physical Hierarchy 614
Group Instances Fields and Options 614
Related Text Commands 615
Related Topics 615
Connect Global Nets 616
Global Net Connections Fields and Options 616
Related Text Commands 619
Related Topics 619
Edit Floorplan 620
Align Instances 621
Align Instances/Modules Fields and Options 621
Related Text Commands 622
Shift Instances 623
Shift Instances/Modules Fields and Options 623
Related Text Commands 624
Space Instances 625
Space Instances/Modules Fields and Options 625
Related Text Commands 625
Flip/Rotate Instances 626
Flip/Rotate Selected Instances Fields and Options 626
Related Text Commands 627
Snap Floorplan 628
Snap Loaded Floorplan Fields and Options 628
Related Text Commands 629
Legalize Floorplan 630
Legalize Floorplan Fields and Options 630
Related Text Commands 631
Set Block Placement Status 632
Set Placement Status Fields and Options 632
Related Text Commands 632

Edit Halos . . . 633
Edit Halos Fields and Options . . . 633
Related Text Commands . . . 634
Edit IO Row . . . 636
Edit IO Row Fields and Options . . . 636
Related Text Commands . . . 636
Core Row . . . 637
Create Core Rows . . . 638
Create Core Rows Fields and Options . . . 638
Related Text Commands . . . 639
Cut Core Rows . . . 640
Cut Core Rows Fields and Options . . . 640
Related Text Commands . . . 641
Stretch Selected Rows . . . 642
Stretch Selected Rows Fields and Options . . . 642
Related Text Commands . . . 642
Clear Floorplan . . . 643
Clear Floorplan Fields and Options . . . 643
Related Text Commands . . . 645
Check Floorplan . . . 646
Check Floorplan Fields and Options . . . 646
Related Text Commands . . . 647
Generate FP Guide . . . 648
Generate FP Guide Fields and Options . . . 648
Related Text Commands . . . 649
Generate Regrouped Netlist . . . 650
Generate Regrouped Netlist Fields and Options . . . 650
Related Text Commands . . . 651
Group Pin(s) Move . . . 652
Group Pin(s) Move Fields and Options . . . 652
Related Text Commands . . . 653
Related Topics . . . 653
Swap Two Selected I/O Cells . . . 654
View Relative Floorplan Through Context Menu . . . 655
Flip Hierarchical Instances on X-axis or Y-axis . . . 656

7
FlipChip Menu 657

Create Bump Array 658
- Create Bump Array Fields and Options 659
- Related Text Commands 660
- Related Topics 661

Edit Bump Array 662
- Edit Bump Array Fields and Options 663
- Related Text Commands 664
- Related Topics 665

Add Bump To Array 666
- Add Bump To Bump Array Fields and Options 666
- Related Text Commands 667
- Related Topics 667

Create Area IO Rows 668
- Setup Chip IO – IO Driver Row Fields and Options 669
- Related Text Commands 671
- Related Topics 671

Assign Signals 672
- Assign/Unassign Signals Fields and Options 672
- Related Text Commands 673
- Related Topics 673

Assign Power/Ground Bumps 674
- Assign Power/Ground Bumps Fields and Options 674
- Related Text Commands 675
- Related Topics 675

Unassign Bump 676
- Related Text Commands 676
- Related Topics 676

Swap Signals 677
- Related Text Commands 677
- Related Topics 677

Show Pin Status 678
- Tile Pin/Bump Status Fields and Options 678

Display Options 680

Display Options Fields and Options 680
Related Text Commands 681

8
Power Menu 683
Multiple Supply Voltage 684
Load/Commit CPF 685
Load/Commit CPF Fields and Options 685
Related Text Commands 686
Create/Modify Power Domain 687
Create Power Domain Fields and Options 689
Related Text Commands 691
Related Topics 692
Specify Timing Libraries – min 693
Specify Timing Libraries Fields and Options 693
Related Text Commands 694
Related Topics 694
Specify Timing Libraries – max 695
Specify Timing Libraries Fields and Options 696
Related Text Commands 696
Related Topics 696
Cut Power Domain by Overlaps 697
Cut Power Domain by Overlaps Fields and Options 697
Related Text Commands 697
Create Shifter Rows 698
Create Shifter Rows Fields and Options 698
Related Text Commands 698
Adjust Power Domain to Align Rows 699
Adjust Power Domain to Align Rows Fields and Options 699
Related Text Commands 700
Shifter/Isolation Cells 701
Load Shifter/Isolation Cells File 702
Shifter/Isolation Cells File Fields and Options 702
Related Text Commands 702
Generate Shifter/Isolation Cells Template 703

Generate Shifter/Isolation Cells Template Fields and Options 703
Related Text Commands 704
Add Shifter/Isolation Cells 705
Add Shifter/Isolation Cells Fields and Options 705
Related Text Commands 706
Related Topics 706
Report Shifter/Isolation Cells 707
Report Shifter/Isolation Cells Fields and Options 707
Related Text Commands 707
Remove Redundant Shifter/Isolation Cells 708
Remove Shifter/Isolation Cells Fields and Options 708
Related Text Commands 708
Power Switch Insertion 709
Power Switch Insertion – Ring 710
Power Switch Insertion – Ring – Sides 711
Power Switch Insertion – Ring – Sides Fields and Options 712
Related Text Commands 713
Power Switch Insertion – Ring – Switch 714
Power Switch Insertion – Ring – Switch Fields and Options 715
Related Text Commands 716
Power Switch Insertion – Ring – Filler 717
Power Switch Insertion – Ring – Filler Fields and Options 718
Related Text Commands 719
Power Switch Insertion – Ring – Buffer 720
Power Switch Insertion – Ring – Buffer Fields and Options 721
Related Text Commands 722
Power Switch Insertion – Ring – Breaker 723
Power Switch Insertion – Ring – Breaker Fields and Options 724
Related Text Commands 725
Power Switch Insertion – Ring – Corner Cells 726
Power Switch Insertion – Ring – Corner Cells Fields and Options 727
Related Text Commands 727
Power Switch Insertion – Ring – Enable Connection 728
Power Switch Insertion – Ring – Enable Connection Fields and Options 729
Related Text Commands 730
Power Switch Insertion – Ring – Switch Cell Count 731

Power Switch Insertion – Ring – Switch Cell Count Fields and Options 732
Related Text Commands 734
Power Switch Insertion – Ring – Cell Offset 735
Power Switch Insertion – Ring – Cell Offset Fields and Options 736
Related Text Commands 738
Power Switch Insertion – Ring – Cell Orientation 739
Power Switch Insertion – Ring – Cell Orientation Fields and Options 740
Related Text Commands 741
Power Switch Insertion – Column 742
Power Switch Insertion – Column – Switch Cell and Enable Connection 743
Power Switch Insertion – Column – Switch Cell and Enable Connections Fields and Options 744
Related Text Commands 746
Power Switch Insertion – Column – Switch Arrangement 747
Power Switch Insertion – Column – Switch Arrangement Fields and Options 748
Related Text Commands 749
Delete Power Switches 750
Delete Power Switches Fields and Options 750
Related Text Commands 750
Highlight Power Domains 752
Highlight MSV Objects – Power Domain 753
Highlight MSV Objects – Power Domain Fields and Options 753
Highlight MSV Objects – Signal Net/HLS Cell 755
Highlight MSV Objects – Highlight Set Fields and Options 755
Related Text Commands 757
Highlight MSV Objects – Highlight Set 758
Highlight MSV Objects – Highlight Set Fields and Options 758
Related Text Commands 759
Color 760
Color Fields and Options 760
Related Text Commands 761
Report Power Domain 762
Report Power Domain Fields and Options 762
Related Text Commands 763
Verify Power Domain 764
Verify Power Domain Fields and Options 764

Related Text Commands 765
Power Planning 766
Specify Electromigration Limits 767
Specify Electromigration Limits Fields and Options 767
Edit Power Planning Option 769
Edit Power Planning Option – RING – Ring Style 772
Edit Power Planning Option – RING – Ring Offset 773
Edit Power Planning Option – RING – Merge 774
Edit Power Planning Option – RING – Jog 775
Edit Power Planning Option – RING – Wire Group 776
Edit Power Planning Option – RING – Wire Snap 777
Edit Power Planning Option – RING – Connection Layer Range 778
Edit Power Planning Option – RING – Partial Intersection Connection 779
Edit Power Planning Option – RING – Orthogonal Connection 780
Edit Power Planning Option – RING – Split Long Via 781
Edit Power Planning Option – RING – Make Via Connect to 782
Edit Power Planning Option – STRIPE – Stripe Boundary 783
Edit Power Planning Option – STRIPE – First / Last Stripe 784
Edit Power Planning Option – STRIPE – Stripe Breaking 785
Edit Power Planning Option – STRIPE – Pad / Core Ring Connection – Jog 786
Edit Power Planning Option – STRIPE – Block Ring Connection – Jog 787
Edit Power Planning Option – STRIPE – Block Ring Connection – Merge 788
Edit Power Planning Option – STRIPE – Jog Length 789
Edit Power Planning Option – STRIPE – Pad / Core Ring Connection 790
Edit Power Planning Option – STRIPE – Block Ring Connection 791
Edit Power Planning Option – STRIPE – Wire Group 792
Edit Power Planning Option – STRIPE – Wire Snap 793
Edit Power Planning Option – STRIPE – Connection Layer Range 794
Edit Power Planning Option – STRIPE – Partial Intersection Connection 795
Edit Power Planning Option – STRIPE – Orthogonal Connection 796
Edit Power Planning Option – STRIPE – Split Long Via 797
Edit Power Planning Option – STRIPE – Make Via Connect to 798
Edit Power Planning Option – STRIPE – Split Vias 799
Edit Power Planning Option – STRIPE – Same Size Stack Vias 800
Edit Power Planning Option – STRIPE – Same Layer Target Connection 801
Edit Power Planning Option – STRIPE – Stripe Over Row 802

Edit Power Planning Option – STRIPE – Closest Target 803
Edit Power Planning Option – STRIPE – Switch Cell Pin Target 804
Edit Power Planning Option – STRIPE – Split Wire 805
Edit Power Planning Option – STRIPE – Spacing From Block 806
Edit Power Planning Option – STRIPE – Minimum Length 807
Synthesize Power Plan 808
Synthesize Power Plan Fields and Options 808
Related Text Command 809
Related Topics 809
Edit Power Plan Template 810
Edit Power Plan Template – Design 811
Changing the Routing Direction of Stripes 811
Changing the Stripe Pattern 811
Edit Power Plan Template – Design Fields and Options 812
Related Command 816
Related Topics 816
Edit Power Plan Template – IP Block 817
Edit Power Plan Template – IP Block Fields and Options 819
Related Text Commands 824
Related Topics 824
Specify Template Parameter 825
General Description of Specify Template Parameter Form Features 826
Associating a Region Template with a Top-level Design or Power Domain 826
General Observations on the Template Instantiation Form 827
Specify Template Parameter Fields and Options 828
Related Text Commands 831
Related Topics 831
Add Rings 832
Add Rings – Basic 833
Add Rings – Basic Fields and Options 833
Related Text Commands 839
Add Rings – Advanced 840
Add Rings – Advanced Fields and Options 841
Related Text Commands 843
Add Rings – Via Generation 844
Add Rings – Via Generation Fields and Options 844

Related Text Commands 847
Add Ring Environment Variables 848
Add Rings Environment Variables Fields and Options 848
Related Text Commands 850
Add Stripes 851
Add Stripes – Basic 852
Add Stripes – Basic Fields and Options 853
Related Text Commands 858
Related Topics 859
Add Stripes – Advanced 860
Add Stripes – Advanced Fields and Options 861
Related Text Commands 863
Add Stripes – Via Generation 864
Add Stripes – Via Generation Fields and Options 865
Related Text Commands 867
Add Stripe Environment Variables 868
Add Stripe Environment Variables Fields and Options 869
Related Text Commands 872
Add XStripes 873
Add XStripes – Basic 874
Add XStripes – Basic Fields and Options 875
Related Text Commands 877
Add XStripes – Via Generation 878
Add XStripes – Via Generation Fields and Options 879
Related Text Commands 879
Create P/G Pin 880
Create P/G Pin Fields and Options 880
Related Text Commands 881
Edit Power Vias 882
Edit Power Vias – Basic 883
Edit Power Vias – Basic Fields and Options 885
Related Text Commands 886
Related Topics 886
Edit Power Vias – Advanced 887
Edit Power Vias – Advanced Fields and Options 888
Related Text Commands 889

Repair Power Stripes 890
Repair Power Stripes – Basic 891
Repair Power Stripes – Basic Fields and Options 891
Related Text Commands 892
Repair Power Stripes – Advanced 893
Repair Power Stripes – Advanced Fields and Options 893
Related Text Commands 894
Repair Power Stripes – Via Generation 895
Repair Power Stripes – Via Generation Fields and Options 897
Related Text Commands 899
Optimize Power Plan 900
Optimize Power Plan – Basic 901
Optimize Power Plan – Basic Fields and Options 901
Related Text Command 903
Optimize Power Plan – Advanced 904
Optimize Power Plan – Advance Fields and Options 905
Related Text Command 906
Power Analysis 907
Read Activity File 908
Read Activity File – VCD 909
Read Activity File – VCD Fields and Options 909
Related Text Commands 910
Related Topics 910
Read Activity File – TCF 911
Read Activity File – TCF Fields and Options 911
Related Text Commands 911
Related Topics 911
Read Activity File – SAF 912
Read Activity File – SAF Fields and Options 912
Related Text Commands 912
Related Topics 912
Set Cell/Instance Power 913
Set Cell/Instance Power Fields and Options 913
Related Text Commands 914
Related Topics 914
Set Default Switching Activity 915

Set Default Switching Activity – Global 916
Set Default Switching Activity – Global Fields and Options 916
Related Text Commands 917
Related Topics 917
Set Default Switching Activity – Specific 918
Set Default Switching Activity – Specific Fields and Options 918
Related Text Commands 919
Related Topics 919
Set Switching Activity 920
Set Switching Activity Fields and Options 920
Related Text Commands 922
Related Topics 922
Set Power Analysis Mode 923
Set Power Analysis Mode Fields and Options 923
Related Text Commands 924
Related Topics 924
Report Power 925
Report Power – Report Power 926
Report Power Fields and Options 927
Related Text Commands 928
Related Topics 929
Report Power – Format 930
Report Power – Format Fields and Options 931
Related Text Commands 931
Related Topics 932
Write TCF 933
Write TCF Fields and Options 933
Related Text Commands 933
Related Topics 933
Debug Power 934
Debug Power Fields and Options 935
Related Text Commands 935
Related Topics 935
Rail Analysis 936
Edit Pad Location 937
Edit Pad Location Fields and Options 938

Related Text Commands . . . 939
Related Topics . . . 939
Edit Net Toggle Probability . . . 940
Edit Net Toggle Probability Fields and Options . . . 940
Related Text Commands . . . 942
Power Analysis . . . 943
Power Analysis Static Mode . . . 944
Power Analysis Static Mode Fields and Options . . . 945
Power Analysis Statistical Mode . . . 948
Power Analysis Statistical Mode Fields and Options . . . 949
Related Text Commands . . . 953
Related Topics . . . 953
Power Analysis Simulation-Based . . . 954
Power Analysis Simulation-Based Fields and Options . . . 956
Related Text Command . . . 960
Related Topics . . . 960
Rail Analysis . . . 961
Rail Analysis: Average Mode . . . 962
Rail Analysis: Average Mode Field and Options . . . 963
Related Text Commands . . . 965
Related Topics . . . 966
Sign-off Analysis . . . 967
VoltageStorm Analysis . . . 968
VoltageStorm Analysis – Basic . . . 969
VoltageStorm Analysis - Basic Fields and Options . . . 971
Related Text Commands . . . 977
Related Topics . . . 977
VoltageStorm Analysis – Advanced . . . 978
VoltageStorm Analysis – Advanced Fields and Options . . . 979
Related Text Commands . . . 984
Cell View Specification . . . 985
Cell View Specification Fields and Options . . . 985
Related Text Commands . . . 987
Layer Bias Specification . . . 988
Layer Bias Specification Fields and Options . . . 988
Related Text Commands . . . 989

Layer Names Maps Specification 990
Layer Names Maps Specification Fields and Options 990
Related Text Commands 991
Display 992
Display Pad Location 993
Display Pad Location Fields and Options 993
Related Text Commands 993
Clear Pad Location Display 994
Related Text Commands 994
Display Rail Analysis Results 995
Display Rail Analysis Results Display Fields and Options 996
Related Text Commands 1001
Clear Rail Analysis Display 1002
Related Text Commands 1002
Display Macro I Source Location 1003
Display Macro I Source Location Fields and Options 1003
Related Text Commands 1003
Related Topics 1003
Clear Macro I Source Location Display 1004
Related Text Commands 1004

9
Place Menu 1005

Specify 1006
Spare Cells 1007
Specify Spare Cells Fields and Options 1007
Related Text Commands 1008
Related Topics 1008
Cell Padding 1009
Specify Cell Padding Fields and Options 1009
Related Text Commands 1010
Related Topics 1010
Jtag Cells 1011
Specify Jtag Cells Fields and Options 1011
Related Text Commands 1012

Related Topics 1012
Placement Blockage 1013
Specify Placement Blockage for Strip and Routing Blockage Fields and Options . 1014
Related Text Commands 1014
Related Topics 1014
Place Jtag 1015
Place Jtag Logic Fields and Options 1015
Related Text Commands 1016
Related Topics 1016
Standard Cells 1017
Place Fields and Options 1017
Related Text Command 1018
Related Topics 1018
Place Flip Chip I/O 1019
Place Area I/O 1019
Place Area I/O Fields and Options 1019
Related Text Commands 1020
Related Topics 1020
Place Peripheral I/O 1021
Place Area I/O Fields and Options 1021
Related Text Commands 1022
Related Topics 1022
Refine Placement 1023
Refine Placement Fields and Options 1024
ECO Placement 1026
ECO Place Fields and Options 1026
Related Text Commands 1027
Related Topics 1027
Place Spare Cell 1028
Spare Cell - Create 1029
Spare Cell – Create Fields and Options 1029
Related Text Commands 1030
Spare Cell - Place 1031
Spare Cell – Place Fields and Options 1031
Related Text Commands 1032
Spare Cell - Delete 1033

Spare Cell - Delete Fields and Options 1033
Related Text Commands 1034
Filler 1035
Add Well Tap 1036
Add Well Tap Instances Fields and Options 1036
Related Text Commands 1038
Related Topics 1038
Add End Cap 1039
Add End Cap Instances Fields and Options 1039
Related Text Commands 1040
Related Topics 1040
Add Filler 1041
Add Filler Fields and Options 1042
Related Text Commands 1043
Related Topics 1043
Delete Filler 1044
Delete Instances Fields and Options 1044
Related Text Commands 1045
Related Topics 1045
Add IO Filler 1046
Add IO Filler Fields and Options 1046
Related Text Commands 1047
Delete IO Filler 1048
Delete IO Filler Fields and Options 1048
Related Text Commands 1049
Tie HI/LO 1050
Add 1051
Add Tie Hi/Lo Instances Fields and Options 1051
Related Text Commands 1052
Related Topics 1052
Delete 1053
Delete Tie Hi/Lo Instances Fields and Options 1053
Related Text Commands 1053
Related Topics 1053
Scan 1055
Delete 1056

Delete Scan Groups Fields and Options 1056
Related Text Commands 1056
Related Topics 1056
Reorder 1057
Reorder Scan Chain Fields and Options 1057
Related Text Commands 1058
Related Topics 1058
Check Placement 1059
Check Placement Fields and Options 1060
Related Text Commands 1061
Display 1062
Display Spare Cells 1063
Related Text Commands 1063
Clear Spare Cells Display 1064
Related Text Commands 1064
Display Scan 1065
Display Scan Connections Fields and Options 1065
Related Text Commands 1065
Clear Scan Display 1066
Clear Scan Display Fields and Options 1066
Related Text Commands 1066
Display Density Map 1067
Display Density Map Fields and Options 1068
Related Text Commands 1069

10
Clock Menu 1071

Design Clock 1072
Related Controls 1072
Synthesize Clock Tree – Basic 1073
Fields and Options 1073
Related Text Commands 1074
Clock Specification Files 1075
Fields and Options 1075
Related Text Command 1076

Generate Clock Spec 1077
Fields and Options 1077
Related Text Commands 1078
Related Topics 1078
Synthesize Clock Tree – Advanced 1079
Fields and Options 1079
Related Text Commands 1081
Trace Pre-CTS Clock Tree 1082
Related Text Commands 1085
Load Clock Tree Trace File 1086
Fields and Options 1086
Pre-CTS Clock Tree Tracer Search 1087
Fields and Options 1088
Search & Hilite 1089
Fields and Options 1089
Clock Info 1091
Fields and Options 1091
Clock Tree Browser 1093
Fields and Options 1094
Clock Tree Browser – Clock Tree Diagram 1095
Fields and Options 1095
Related Text Commands 1098
Clock Tree Browser – Clock Tree Histogram 1099
Save Clock Tree Browser 1100
Fields and Options 1100
Clock Tree Analyst 1101
Clock Tree Analyst Main Window 1102
Main Window Features 1103
Clock Tree Analyst – Clock Setup 1105
Clock Tree Analyst – Clock Setup Fields and Options 1105
Clock Tree Analyst – Clock – Preference – Display 1107
Fields and Options 1107
Clock Tree Analyst – Clock – Preference – Color 1109
Fields and Options 1109
Clock Tree Analyst – Clock – Preference – Color – Set Mixed Color 1110
Clock – Preference – Color – Set Mixed Color Fields and Options 1110

Clock Tree Analyst – Tool – Find – Instance 1111
Fields and Options 1111
Clock Tree Analyst – Tool – List Flip-Flops Not In Any Clock 1113
Fields and Options 1114
Clock Tree Analyst – Find – Reconvergence 1115
Fields and Options 1115
Clock Tree Analyst – Find – Path 1116
Fields and Options 1116
Clock Tree Analyst – Tool – Dump View 1118
Fields and Options 1118
Clock Tree Analyst – List Sink 1119
Fields and Options 1120
Display 1121
Display Clock Tree 1122
Fields and Options 1123
Related Text Command 1124
Clear Clock Tree Display 1125
Related Text Command 1125
Save Clock Nets 1126
Fields and Options 1126
Related Text Command 1126
Generate Clock Tree Spice 1127
Fields and Options 1127
Related Text Command 1128
Clock Mesh 1129
Edit Clock Mesh Specification 1130
Common Controls 1130
Related Text Commands 1132
Related Topics 1132
Edit Clock Mesh Specification – Route Types 1133
Fields and Options 1133
Edit Clock Mesh Specification – Constraints 1135
Fields and Options 1135
Edit Clock Mesh Specification – Scope 1137
Fields and Options 1137
Edit Clock Mesh Specification – Chain 1139

Fields and Options 1139
Edit Clock Mesh Specification – Mesh Structure 1141
Fields and Options 1141
Edit Clock Mesh Specification – Mesh Stage 1144
Fields and Options 1144
Edit Clock Mesh Specification – Local Tree 1147
Fields and Options 1147
Load Clock Mesh 1149
Related Text Commands 1149
Unspecify Clock Mesh 1150
Fields and Options 1150
Related Text Commands 1150
Save Clock Mesh 1151
Fields and Options 1151
Related Text Commands 1151
Synthesize Clock Mesh 1152
Fields and Options 1153
Related Text Commands 1154
Delete Clock Mesh 1155
Fields and Options 1155
Related Text Commands 1155
Route Clock Mesh 1156
Fields and Options 1156
Related Text Commands 1156
Trim Clock Mesh 1157
Fields and Options 1157
Related Text Commands 1158
Analyze 1159
Related Text Commands 1159
Report Clock Mesh 1160
Fields and Options 1160
Related Text Commands 1161
Display Clock Mesh 1162
Fields and Options 1162
Related Text Commands 1164
Mode 1165

11
Route Menu

Route Menu . . . 1167
Trial Route . . . 1168
Trial Route Fields and Options . . . 1168
Related Text Commands . . . 1170
Related Topics . . . 1170
Special Route . . . 1171
SRoute – Basic . . . 1172
SRoute – Basic Fields and Options . . . 1172
Related Text Commands . . . 1178
SRoute – Advanced . . . 1179
SRoute – Advanced – Block Pins . . . 1180
SRoute – Advanced – Block Pins Fields and Options . . . 1181
Related Text Commands . . . 1183
SRoute – Advanced – Pad Pins . . . 1184
SRoute – Advanced – Pad Pins Fields and Options . . . 1185
Related Text Commands . . . 1186
SRoute – Advanced – Pad Rings . . . 1187
SRoute – Advanced – Pad Rings Fields and Options . . . 1188
Related Text Commands . . . 1188
SRoute – Advanced – Standard Cell Pins . . . 1189
SRoute – Advanced – Standard Cell Pins Fields and Options . . . 1190
Related Text Commands . . . 1190
SRoute – Advanced – Power Domains . . . 1191
SRoute – Advanced – Power Domains Fields and Options . . . 1192
Related Text Commands . . . 1192
SRoute – Advanced – Extension Control . . . 1193
SRoute – Advanced – Extension Control Fields and Options . . . 1194
Related Text Commands . . . 1196
SRoute – Advanced – Target List Editing . . . 1197
SRoute – Advanced – Target List Editing Fields and Options . . . 1198
Related Text Commands . . . 1200
SRoute – Advanced – Extra Config Editing . . . 1201
SRoute – Advanced – Extra Config Editing Fields and Options . . . 1201
SRoute – Via Generation . . . 1203

SRoute – Via Generation Fields and Options 1204
Related Text Commands 1208
NanoRoute 1209
NanoRoute/Attributes 1210
NanoRoute/Attributes Fields and Options 1210
Related Topics 1214
Related Text Commands 1214
NanoRoute 1215
NanoRoute Fields and Options 1216
Related Topics 1221
Related Text Commands 1222
Set Congestion Map Style 1223
Set Congestion Map Style – Trial Route 1224
Set Congestion Map Style Fields and Options 1224
Set Congestion Map Style – NanoRoute 1227
Mixed Signal 1229
Mixed Signal Router 1230
Mixed Signal Router Fields and Options 1230
Related Text Commands 1233
Metal Fill 1234
Setup Metal Fill Options 1235
Setup Metal Fill Options – Size & Spacing 1236
Setup Metal Fill Options – Size & Spacing Fields and Options 1236
Related Topics 1238
Related Text Commands 1239
Setup Metal Fill Options – Window & Density 1240
Setup Metal Fill Options– Window & Density Fields and Options 1240
Related Topics 1242
Related Text Commands 1242
Add Metal Fill 1243
Add Metal Fill Fields and Options 1244
Related Topics 1247
Related Text Commands 1247
Trim 1248
Related Topics 1248
Related Text Commands 1248

Via Fill 1249
Setup Via Fill Options 1250
Setup Via Fill Fields and Options 1250
Related Text Commands 1251
Add Via Fill 1252
Add Via Fill Fields and Options 1252
Related Text Commands 1252
Flip Chip 1253
Flip Chip Route – Basic 1254
Flip Chip Route – Basic Fields and Options 1255
Related Text Commands 1257
Flip Chip Route – Advanced 1258
Flip Chip Route – Advanced – Routing Style 1259
Flip Chip Route – Advanced – Routing Style Fields and Options 1260
Related Text Commands 1261
Flip Chip Route – Advanced – Prototype 1262
Flip Chip Route – Advanced – Prototype Fields and Options 1263
Related Topics 1263
Related Text Commands 1263
Flip Chip Route – Advanced – Splitting 1264
Flip Chip Route – Advanced – Splitting Fields and Options 1265
Flip Chip Route – Advanced – Routing Constraints 1266
Flip Chip Route – Advanced – Routing Constraints Fields and Options 1267
Virtuoso CAR Interface 1268
Virtuoso CAR Fields and Options 1269
Related Topics 1272
Related Text Commands 1272
WRoute 1273
WRoute – Basic 1274
WRoute – Basic Fields and Options 1274
Related Text Commands 1279
Related Topics 1279
WRoute – Advanced 1280
Job Control 1281
Job Control Fields and Options 1281
Related Text Commands 1282

Related Topics 1282
Net Options 1283
Net Options Fields and Options 1283
Related Text Commands 1285
Related Topics 1285
Pin Access 1286
Pin Access Fields and Options 1286
Related Text Commands 1287
Related Topics 1287
Process Antenna 1288
Process Antenna Fields and Options 1288
Related Text Commands 1290
Related Topics 1290
Routing Layer Limits 1291
Routing Layer Limits Fields and Options 1291
Related Text Commands 1292
Related Topics 1292
Search and Repair 1293
Search and Repair Fields and Options 1293
Related Text Commands 1294
Related Topics 1294
Tapering 1295
Tapering Fields and Options 1295
Related Text Commands 1296
Related Topics 1296
Crosstalk Options 1297
Crosstalk Options Fields and Options 1297
Related Text Commands 1300
Related Topics 1300
Route Optimization 1301
Route Optimization Fields and Options 1301
Related Text Commands 1302
Related Topics 1302
Expert Options 1303
Expert Options Fields and Options 1303
Related Text Commands 1305

Related Topics 1305
Generate Routing Guide 1306
Routing Guide File 1306
Routing Guide File Fields and Options 1307
Related Text Commands 1307

12
Timing Menu 1309
Analysis Condition 1311
Specify Operating Condition 1312
Specify Operating Condition Fields and Options 1312
Related Text Commands 1313
Specify RC Extraction Mode 1314
RC Extraction Mode Fields and Options 1315
Related Text Commands 1316
Related Topics 1317
Specify Analysis Mode 1318
Specify Analysis Mode – Basic 1319
Specify Analysis Mode – Basic Fields and Options 1319
Related Text Commands 1320
Related Topics 1320
Specify Analysis Mode – Advanced 1321
Specify Analysis Mode – Advanced Fields and Options 1321
Related Text Commands 1323
Related Topics 1323
Set Timing Derate 1324
Set Timing Derate Fields and Options 1324
Related Text Commands 1325
Related Topics 1325
Specify Delay Calculation Mode 1326
Delay Calculation Mode Fields and Options 1326
Related Text Commands 1326
Related Topics 1326
Configure MMMC 1327
Load Timing Constraints 1330

Load Timing Constraint Fields and Options 1330
Related Text Commands 1330
Related Topics 1330
Cell Footprint 1331
Load 1332
Load Timing Constraint Fields and Options 1332
Related Text Commands 1332
Check 1333
Related Text Commands 1333
Extract RC 1334
Extract RC Fields and Options 1334
Related Text Commands 1335
Related Topics 1335
QRC Standalone Extraction 1336
Extraction Setup Fields and Options 1337
Related Text Commands 1340
Related Topics 1341
Fire & Ice Extract RC 1342
Extraction Advanced Setup Options 1343
Extraction Advanced Setup Fields and Options 1344
Related Text Commands 1345
Related Topics 1346
Library Generation 1347
Library Generation – Basic 1348
Library Generation – Basic Fields and Options 1349
Related Text Commands 1351
Related Topics 1352
Library Generation – Advanced 1353
Library Generation – Advanced Fields and Options 1354
Related Text Commands 1356
Related Topics 1356
Analyze Timing 1357
Timing Analysis – Basic 1358
Timing Analysis – Basic Fields and Options 1359
Related Text Commands 1360
Timing Analysis – Advanced 1361

Timing Analysis – Advanced Fields and Options 1362
Related Text Commands 1362
Specify Path Groups 1363
Specify Path Groups Fields and Options 1364
Debug Timing 1365
Display/Generate Timing Report 1366
Display/Generate Timing Report Fields and Options 1366
Related Text Commands 1367
Timing Debug – Browser 1368
Timing Debug 1371
Timing Debug Fields and Options 1372
Related Text Commands 1376
Timing Debug – Edit Table Column 1377
Edit Table Column Fields and Options 1377
Timing Debug – Edit Table Columns – Load GTD Preferences File 1380
Timing Debug – Edit Table Columns – Load GTD Preferences File Fields and Options 1380
Timing Debug – File 1381
Timing Debug – File – Write Text Report 1382
Timing Debug – Write Textual Report File Fields and Options 1382
Timing Debug – File – Column Width Table 1384
Write Text Report – Column Width Table Fields and Options 1384
Timing Debug – File – Write Category Report File 1386
Timing Debug – Write Category Report Fields and Options 1386
Timing Debug – Timing Debug Preferences 1387
Timing Debug Preferences - General 1388
Timing Debug Preferences Fields and Options 1388
Timing Debug Preferences - Color 1390
Timing Debug Preferences - Color Fields and Options 1390
Timing Debug Preferences - Color – Set Color 1391
Timing Debug Preferences - Color - Set Color Violation Fields and Options 1391
Timing Debug Preferences - Bottleneck Analysis 1392
Timing Debug Preferences - Bottleneck Analysis Fields and Options 1392
Timing Debug Preferences - Set Color 1394
Timing Preferences – Set Color Fields and Options 1394
Timing Debug Preferences - Cell Coloring 1395

Timing Debug Preferences - Cell Coloring Fields and Options 1395
Timing Debug – Analysis 1397
Path Analysis (Path Groups) 1398
Path Analysis (Path Groups) Fields and Options 1399
Related Text Commands 1399
Path Analysis (Clock Analysis) 1400
Path Analysis (Clock Analysis) Fields and Options 1401
Related Text Commands 1401
Path Analysis (Hierarchical Analysis) 1402
Path Analysis (Hierarchical Analysis) Fields and Options 1403
Related Text Commands 1403
Path Analysis (View Analysis) 1404
Path Analysis (View Analysis) Fields and Options 1405
Related Text Commands 1405
Path Analysis (Bottleneck Analysis) 1406
Path Analysis (Bottleneck Analysis) Fields and Options 1407
Path Analysis (DRV Analysis) 1408
Path Analysis (drv) Fields and Options 1408
Path Analysis (False Path Analysis) 1410
Path Analysis (False Path Analysis) Fields and Options 1411
Hierarchical Analysis Viewer 1412
Hierarchical Analysis Viewer Fields and Options 1413
Create Path Category 1414
Create Path Category Fields and Options 1414
Related Text Commands 1419
Timing Path Analyzer 1420
Timing Path Analyzer - Data Path 1421
Timing Path Analyzer - Data Path Fields and Options 1421
Timing Path Analyzer - Launch Clock 1423
Timing Path Analyzer - Launch Clock Fields and Options 1424
Timing Path Analyzer - Capture Clock 1425
Timing Path Analyzer - Capture Clock Fields and Options 1426
Timing Path Analyzer - Path SDC 1427
Timing Path Analyzer - Path SDC Fields and Options 1428
Timing Path Analyzer – Timing Interpretation 1429
Timing Path Analyzer - Timing Interpretation Fields and Options 1430

Edit Timing Interpretation 1432
Timing Path Analyzer – Edit Timing Interpretation Fields and Options 1432
Timing Path Analyzer - Schematics 1435
Timing Path Analyzer - Schematics Fields and Options 1435
Analyze What-If Timing 1436
Black Box/Blob What-If Timing Analysis – Browser 1437
Black Box/Blob What-If Timing Analysis Fields and Options 1438
Related Text Commands 1439
Related Topics 1439
Create Timing Arcs 1440
Create Timing Arc Fields and Options 1440
Related Text Commands 1441
Related Topics 1441
Set Timing Arc 1442
Set Timing Arc Fields and Options 1442
Related Text Commands 1442
Related Topics 1443
Set Output Driver 1444
Set Output Driver Fields and Options 1444
Related Text Commands 1445
Related Topics 1445
Set Clock Latency 1446
Set Clock Latency Fields and Options 1446
Related Text Commands 1447
Related Topics 1447
Set Black Box Clock Port 1448
Set Black Box Clock Port Fields and Options 1448
Related Text Commands 1448
Related Topics 1448
Create Internal Generated Clock 1449
Create Internal Generated Clock Fields and Options 1449
Related Text Commands 1450
Related Topics 1450
Black Box What-If Timing Analysis – Options 1451
Black Box What-If Timing Analysis – Options – timing mode 1452
Black Box What-If Timing Analysis Fields and Options 1453

Related Text Commands 1453
Related Topics 1454
Black Box What-If Timing Analysis – Options – new timing arc authorization 1455
Black Box What-If Timing Analysis – Options – new timing arc authorization Fields and Options 1456
Related Text Commands 1456
Related Topics 1456
Black Box What-If Timing Analysis – Options – timing arcs of the library 1457
Black Box What-If Timing Analysis – Options – timing arcs of the library Fields and Options 1458
Related Text Commands 1458
Related Topics 1458
Optimize 1459
Timing – Optimization Fields and Options 1460
Related Text Commands 1462
Related Topics 1462
Interactive ECO 1463
Interactive ECO – Add Repeater 1464
Interactive ECO - Add Repeater Fields and Options 1464
Related Text Commands 1467
Related Topics 1467
Interactive ECO – Change Cell 1468
Interactive ECO - Change Cell Fields and Options 1468
Related Text Commands 1469
Related Topics 1470
Interactive ECO – Delete Repeater 1471
Interactive ECO - Del Repeater Fields and Options 1471
Related Text Commands 1472
Related Topics 1472
Interactive ECO – Display Buffer Trees 1473
Interactive ECO - Display Buffer Tree Fields and Options 1473
Related Text Commands 1474
Related Topics 1474
Timing Library 1475
Timing Library – Check 1476
Related Text Commands 1476

Related Topics 1476
Timing Library – Report 1477
Report Timing Library Fields and Options 1477
Related Text Commands 1477
Related Topics 1478
Report 1479
Clock Waveform 1480
Related Text Commands 1480
Related Topics 1481
Cell Footprint 1482
Report Cell Footprint Fields and Options 1482
Related Text Commands 1482
Related Topics 1483
Calculate Delay 1484
Calculate Delay Fields and Options 1484
Related Text Commands 1484
Related Topics 1484
Generate 1485
Capacitance Table 1486
Generate Capacitance Table Fields and Options 1487
Related Text Commands 1488
Related Topics 1488
Wire-Load Model 1489
Generate Wireload Model Fields and Options 1489
Related Text Commands 1490

13
SI Menu 1493

Run CeltIC Crosstalk Analysis 1494
Run CeltIC Crosstalk Analysis Fields and Options 1494
Related Text Commands 1496
Related Topics 1496
Display Noise Net 1497
Display Noise Net Fields and Options 1497
Related Text Commands 1498

Related Topics 1498
CeltIC Result Browser 1499
Fix Crosstalk 1502
Fix Crosstalk Fields and Options 1503
Related Text Commands 1505
Related Topics 1505

14
Verify Menu 1507

Verify Connectivity 1508
Verify Connectivity Fields and Options 1509
Related Text Commands 1513
Verify Metal Density 1514
Verify Metal Density – Basic 1515
Verify Metal Density – Basic Fields and Options 1515
Related Text Commands 1516
Verify Metal Density – Window & Density 1517
Verify Metal Density – Window & Density Fields and Options 1517
Related Text Commands 1518
Verify Cut Density 1519
Verify Cut Density – Basic 1520
Verify Cut Density – Basic Fields and Options 1520
Related Text Commands 1521
Verify Cut Density – Window & Density 1522
Verify Cut Density – Window & Density Fields and Options 1522
Related Text Commands 1523
Verify Geometry 1524
Verify Geometry – Basic 1525
Verify Geometry – Basic Fields and Options 1526
Related Text Commands 1529
Verify Geometry – Advanced 1530
Verify Geometry – Advanced Fields and Options 1531
Related Text Commands 1532
Verify Process Antenna 1533
Verify Process Antenna Fields and Options 1533

Related Text Commands 1534
Verify AC Limit 1535
Verify AC Limit Fields and Options 1536
Related Text Commands 1538
Verify Mixed Signal Constraints 1539
Verify Mixed Signal Constraints – Routing 1540
Verify Mixed Signal Constraints – Routing Fields and Options 1542
Related Text Commands 1544
Verify Mixed Signal Constraints – Electrical 1545
Verify Mixed Signal Constraints – Electrical Fields and Options 1546
Related Text Commands 1546
Verify Mixed Signal Routing Constraints Filter Output 1547
Verify Mixed Signal Routing Constraints Filter Output Fields and Options 1547

15
Tools Menu 1549

Design Browser 1550
Design Browser Tool Widgets 1552
Attribute Editor 1554
Attribute Editor Fields and Options 1554
Connectivity Browser 1556
Connectivity Browser Fields and Options 1556
Schematics 1557
Menu Bar 1558
Toolbar 1559
Object Field 1560
Global View Window 1560
Module Schematics Display 1561
Print Schematic 1562
Color Selection 1563
Color Settings 1564
Font Settings 1565
Find Schematic Object 1566
Floorplan Toolbox 1567
Flip Chip Toolbox 1568

Violation Browser 1570
Violation Browser Fields and Options 1571
Related Text Commands 1572
Related Topics 1573
Violation Browser Settings 1574
Violation Browser – Settings Fields and Options 1575
Related Text Commands 1577
Related Topics 1577
Load Violation Report 1578
Load Violation Report Fields and Options 1578
Related Text Commands 1579
Related Topics 1579
Clear Violation 1580
Related Text Commands 1580
Conformal 1581
Conformal Equivalence Checker 1582
Conformal Equivalence Checker Form Fields and Options 1582
Conformal Check Constraints 1583
Conformal Check Constraints - Basic 1584
Conformal Check Constraints – Basic Fields and Options 1584
Related Text Command 1585
Conformal Check Constraints - Advanced 1586
Conformal Check Constraints – Advanced Fields and Options 1586
Related Text Command 1587
Conformal Check Budget Constraints 1588
Conformal Check Budget Constraints - Basic 1589
Conformal Check Budget Constraints – Basic Fields and Options 1589
Related Text Command 1590
Conformal Check Budget Constraints - Files 1591
Conformal Check Budget Constraints – Files Fields and Options 1591
Related Text Command 1592
Conformal Check Budget Constraints - Misc 1593
Conformal Check Budget Constraints – Misc Fields and Options 1594
Related Text Command 1596
Conformal Check Assembled Constraints 1597
Conformal Check Assembled Constraints - Basic 1598

Conformal Check Assembled Constraints – Basic Fields and Options 1598
Related Text Command 1600
Conformal Check Assembled Constraints - Advanced 1601
Conformal Check Assembled Constraints – Advanced Fields and Options 1602
Related Text Command 1603
Conformal Derive Critical False Path 1604
Conformal Derive Critical False Path - Basic 1605
Conformal Derive Critical False Path – Basic Fields and Options 1605
Related Text Command 1607
Conformal Derive Critical False Path - Advanced 1608
Conformal Derive Critical False Path – Advanced Fields and Options 1609
Related Text Command 1610
Conformal Promote Constraints 1611
Conformal Promote Constraints - Basic 1612
Conformal Promote Constraints – Basic Fields and Options 1612
Related Text Command 1613
Conformal Promote Constraints - Advanced 1614
Conformal Promote Constraints – Advanced Fields and Options 1615
Related Text Command 1616
Report Yield 1617
Report Yield Fields and Options 1617
Related Text Commands 1618
Related Topics 1618
Mixed Signal 1619
Mixed Signal Constraint Editor 1620
Routing Constraints 1621
Diff Pairs 1622
Diff Pairs Fields and Options 1623
Related Topics 1626
Matched Pairs 1627
Matched Pairs Fields and Options 1628
Related Topics 1631
Route Nets 1632
Route Nets Fields and Options 1632
Related Topics 1635
Shield Nets 1637

Shield Nets Fields and Options 1638
Related Topics 1640
Bus 1642
Bus Fields and Options 1643
Related Topics 1646
Dont Cross 1647
Dont Cross Fields and Options 1647
Display All 1649
All Fields and Options 1649
Electrical Constraints 1651
Max IR Drop 1652
Max IR Drop Fields and Options 1652
Analog Pin 1654
Analog Pin Fields and Options 1654
Analog Net 1655
Analog Net Fields and Options 1655
Analog Inst 1656
Analog Inst Fields and Options 1656
Display All 1657
All Fields and Options 1657
Select Constraint Member 1658
Select Constraint Member Fields and Options 1658
UltraSim 1660
UltraSim Fields and Options 1661
Related Text Commands 1662
Input Instances 1663
Input Instances Fields and Options 1663
Tie-Off Nets 1664
Tie-Off Nets Fields and Options 1665
Log Viewer 1666
Menu Bar 1666
Related Text Commands 1667
Find in this log file 1668
Fields and Options 1668
Screen Capture 1669
Dump To GIF File 1670

Screen Dump 1671
Display Screen Dump 1672
Express Flow Tool 1673
Main EFT Form 1675
Express Flow Tool Fields and Options 1676
Toolbar Commands 1680
Import Tcl 1683
Import Tcl Flow Fields and Options 1683
Related Text Commands 1684
Select Flow 1685
Select Subflows Fields and Options 1685
Related Text Commands 1685
Load Preferences File 1686
Load Preferences Fields and Options 1686
Related Text Commands 1686
Load Tcl File 1687
Load Tcl Fields and Options 1687
Related Text Commands 1688
Save Preferences 1689
Save Preferences Fields and Options 1689
Related Text Commands 1689
Preferences 1690
Preferences Fields and Options 1691
Related Text Commands 1693
New Run 1694
New Run Fields and Options 1694
Related Text Commands 1694
View Script 1695
View Script Fields and Options 1695
Related Text Commands 1696
Load Run State File 1697
Load Run State File Fields and Options 1697
Related Text Commands 1697
Save Run State 1698
Save Run State Fields and Options 1698
Related Text Commands 1698

Configure Flow 1699
Configure Flow Definition Fields and Options 1699
Related Text Commands 1700
Options 1701
Run Options Fields and Options 1701
Related Text Commands 1702
Specify Run 1703
New Run Fields and Options 1704
Related Text Commands 1704
View/Edit Status Condition 1705
View/Edit Status Condition Fields and Options 1705
Related Text Commands 1706
Configure Run 1707
Configure Flow Fields and Options 1707
Related Text Commands 1708
Generate Script 1709
Related Text Commands 1709
Run Script 1710
Related Text Commands 1710
Generate & Run Script 1711
Related Text Commands 1711
View Results 1712
View Results Fields and Options 1713
Related Text Commands 1713
Stop Script 1714
Related Text Commands 1714
Refresh 1715
Related Text Commands 1715
Save Flow Definition State 1716
Load Flow Definition State Fields and Options 1716
Related Text Commands 1717
View Run Graph 1718
View Run Graph Fields and Options 1719
Related Text Commands 1719
Report – Write PDF 1720
Report (Write PDF) Fields and Options 1720

Related Text Commands 1721
Report – Write HTML 1722
Report (Write HTML) Fields and Options 1722
Related Text Commands 1723
Report Preferences – PDF and HTML 1724
Report Preferences Fields and Options 1724
Related Text Commands 1725

Index. 1727

About This Manual

The Cadence® Encounter™ family of products provides an integrated solution for an RTL-to-GDSII design flow. This manual describes provides information specific to the forms and commands available from the Encounter graphical user interface.

Audience

This manual is written for experienced designers of digital integrated circuits. Such designers must be familiar with design planning, placement and routing, block implementation, chip assembly, and design verification. Designers must also have a solid understanding of UNIX and Tcl/Tk programming.

How This Manual Is Organized

The chapters in this manual are organized to correspond to the menus in the Encounter graphical user interface (GUI). Each chapter contains one of more of the following sections. A particular section is omitted from a chapter if there is no significant information related to the topic.

Form Overview	Introduces the features available through the various menu selections and provides an illustration of the forms and screens used to set options and run the features.
Forms and Options	Lists and describes the fields and options on each screen.
Related Topics	Provides links to related tasks and concepts in the Encounter User Guide.
Related Commands	Lists the text commands that correspond to the GUI forms for this feature.

Conventions Used in This Manual

This section describes the typographic and syntax conventions used in this manual.

`text`	Indicates text that you must type exactly as shown. For example: `analyze_connectivity -analyze all`
`text`	Indicates information for which you must substitute a name or value. In the following example, you must substitute the name of a specific file for *`configfile`*: `wroute -filename` *`configfile`*
text	Indicates the following: ■ Text found in the graphical user interface (GUI), including form names, button labels, and field names ■ Terms that are new to the manual, are the subject of discussion, or need special emphasis ■ Titles of manuals
`[ ]`	Indicates optional arguments. In the following example, you can specify none, one, or both of the bracketed arguments: `command [-arg1] [arg2` *`value`*`]`
`[ | ]`	Indicates an optional choice from a mutually exclusive list. In the following example, you can specify any of the arguments or none of the arguments, but you cannot specify more than one: `command [arg1 | arg2 | arg3 | arg4]`
`{ | }`	Indicates a required choice from a mutually exclusive list. In the following example, you must specify one, and only one, of the arguments: `command {arg1 | arg2 | arg3}`

`{[ ] [ ]}`	Indicates a required choice of one or more items in a list. In the following example, you must choose one argument from the list, but you can choose more than one: `command {[arg1] [arg2] [arg3]}`
`{ }`	Indicates curly braces that must be entered with the command syntax. In the following example, you must type the curly braces: `command arg1` **`{`**`x y`**`}`**
`. . .`	Indicates that you can repeat the previous argument.
. : .	Indicates an omission in an example of computer output or input.
Command – Subcommand	Indicates a command sequence, which shows the order in which you choose commands and subcommands from the GUI menu. In the following example, you choose *Floorplan* from the menu, then *Power Planning* from the submenu, and then *Add Rings* from the displayed list: *Floorplan – Power Planning – Add Rings* This sequence opens the Add Rings form.

Related Documents

For more information about the Encounter family of products, see the following documents. You can access these and other Cadence documents with the Cadence Help online documentation system.

- *Encounter User Guide*

  Describes how to install, configure, and use Encounter to implement digital integrated circuits.

- *Encounter Database Access Command Reference*

  Lists all of the Encounter database access commands and provides a brief description of syntax and usage.

- *Encounter Timing Closure Guide*

Addresses issues related to timing closure for challenging designs. It presents a recommended task flow and provides tips on how to resolve or avoid common timing closure problems typically found in a design.

- *Encounter Known Problems and Solutions*

  Describes important Cadence Change Requests (CCRs) for the Encounter family of products, including solutions for working around known problems.

- *Encounter Library Development Guide*

  Describes library development guidelines for the independent tools that make up the Encounter family of products.

- *Encounter Text Command Reference*

  Describes the Encounter text commands, including syntax and examples.

- *What's New in Encounter*

  Provides information about new and changed features in this release of the Encounter family of products.

- `README` file

  Contains installation, compatibility, and other prerequisite information, including a list of CCRs that were resolved in this release. You can read this file online at downloads.cadence.com.

For a complete list of documents provided with this release, see the Cadene Help online documentation system..

8/28/08

1

The Main Window

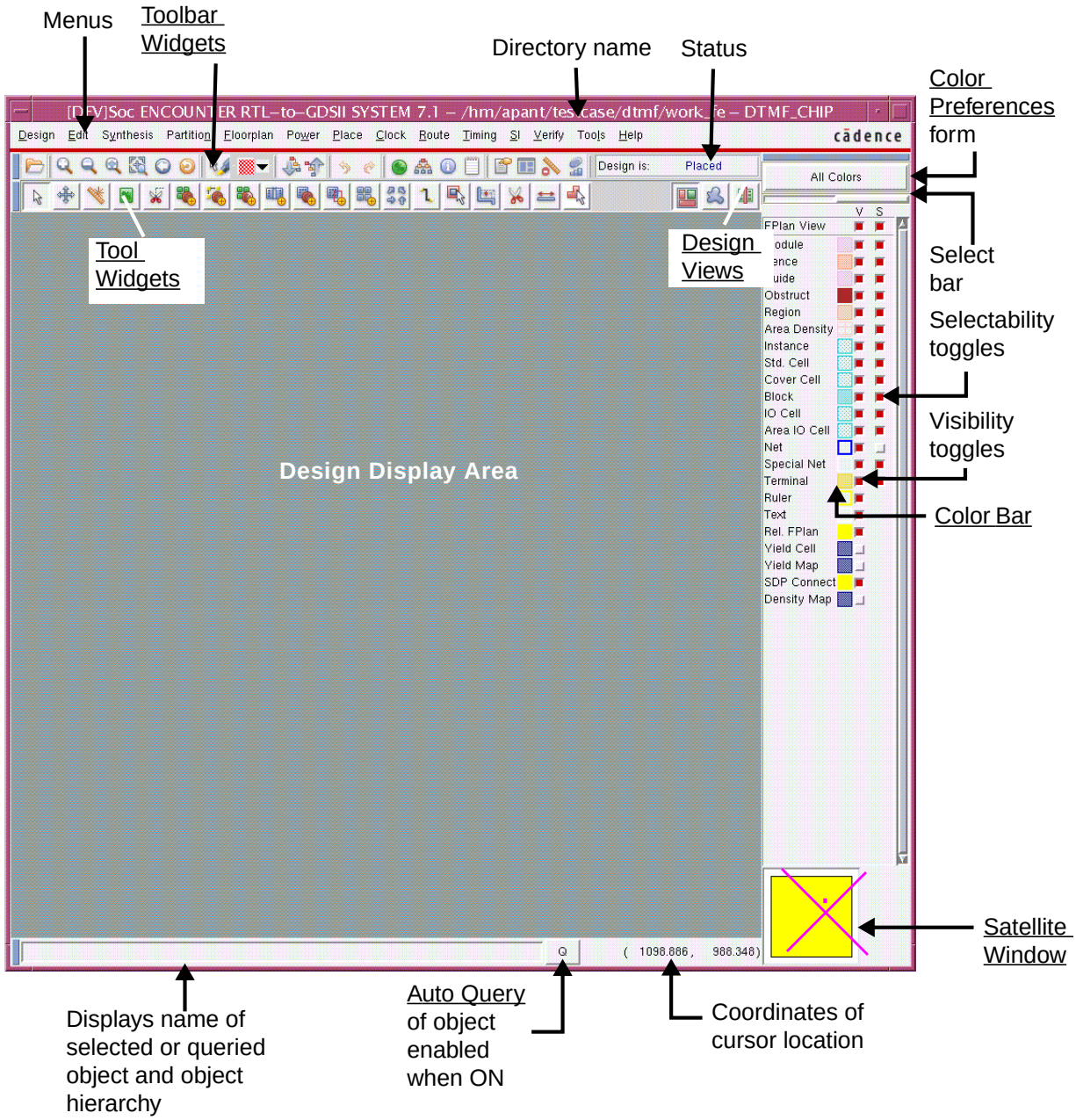
- Main Window Components on page 67
- Toolbar Widgets on page 68
- Design Views on page 70
  - Floorplan View on page 71
  - Amoeba View on page 71
  - Physical View on page 71
- Tool Widgets on page 72
  - Floorplan Widgets on page 73
  - Partition Widgets on page 74
  - Flip Chip Widget on page 74
  - Wire Editing Widgets on page 75
- Color Preferences on page 77
  - Objects Page on page 77
  - Wire/Via Page on page 79
  - View Only Page on page 80
  - Custom Page on page 80
  - Cell Layout Page on page 81
  - Customizing Layer Color Patterns on page 82
  - Customize Tab on page 83
  - Applying Preferences in the All Colors Form on page 87
  - Save Color Preference on page 87

- Multicolor Layers on page 88
- Metal Layers and Other Layered Components on page 88

- Creating and Editing Color Groups on page 89
- Color Bar on page 91
- Color on page 93
- Viewing OA Cell Layout on page 94
- Set Ruler Mode on page 96
- Satellite Window on page 98
- Context Pop-up Attribute Viewer on page 99
- Auto Query on page 101
- Docking Sub-windows on page 102
- Tear-off Menus and Sub-menus on page 103
- Mouse Operation on page 104
- Keyboard Shortcuts on page 104
- Viewing the Documentation Library through the Help Menu on page 105
- Displaying the Encounter Version Number, and Patent- and Copyright-Information on page 105

Main Window Components

The components in the Encounter main window are identified in the following figure, and described in the sections that follow.



Toolbar Widgets

The following row of widgets, located below the menus and above the design display area, includes shortcuts for some commonly used Encounter commands.

The following table describes the widgets that are located in the Toolbar Widget area:

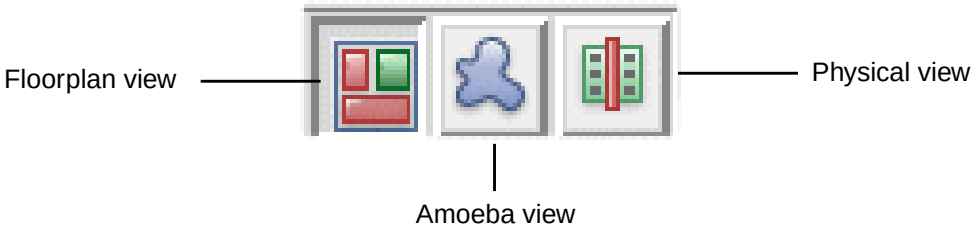
Widget	Description
	Design Import—Opens the Design Import form. For more information, see Design Import in the Design chapter.
	Zoom In—Click this widget to display a smaller area of the design in greater detail. Each click zooms in one level. The equivalent bindkey is `z`. The equivalent text command is `zoomIn`.
	Zoom Out—Click this widget to display a larger area of the design in less detail. Each click zooms out one level. The equivalent bindkey is `Z`. The equivalent text command is `zoomOut`.
	Fit—Click this widget to display the entire placed design within the design display area. The equivalent bindkey is `f`.
	Zoom Selected—Select one or more design objects, then click this widget to zoom into the area that contains the selected objects. The equivalent text command is `zoomSelected`.
	Zoom Previous—Click this widget to toggle the display between the previous location/zoom level and the current location/zoom level. The equivalent bindkey is `l` (the letter L).
	Redraw—Click this widget to update the display with new colors or stipple patterns that you selected from the More Colors form.
	Highlight Selected—Click this widget to highlight the objects selected in the GUI. You can also select the highlight color from the available choices through the Select Highlight Color drop-down menu that appears next to the Highlight Selected toolbar widget.

Widget	Description
	Hierarchy Down—Click this widget to display the submodules for a selected module guide. Each time you click this widget, you move further down the hierarchy. The equivalent bindkey is u.
	Hierarchy Up—Click this widget to display the next module up for a selected module guide. Each time you click this widget, you move further up the hierarchy. The equivalent bindkey is g.
	Undo—Click this widget to undo the previous action. You can only undo a single action. You can undo any wire editor action, any power planning action, and the following floorplanning actions: ■ Align Instances ■ Shift Instance ■ Space Instance ■ Flip/Rotate Instance ■ Snap Floorplan The equivalent bindkey is U. The equivalent text command is undo.
	Redo—Click this widget to restore the design to the same state as before you clicked the undo button. You can only redo a single undo action. You can redo any wire editor action, any power planning action, and the following floorplanning actions: ■ Align Instances ■ Shift Instance ■ Space Instance ■ Flip/Rotate Instance ■ Snap Floorplan ■ Resize Floorplan The equivalent bindkey is R. The equivalent text command is redo
	Display/Calculate Effective Utilization—Click this widget to output the module density. For more information, see the Effective Utilization Display section in the “Floorplanning the Design” chapter of the Encounter User Guide.

Widget	Description
	Design Browser—Opens the Design Browser form. For more information, see Design Browser in the Tools chapter.
	Attribute Editor—Opens the Attribute Editor form. For more information, see Attribute Editor in the Tools chapter.
	Report Select Obj(s)—Runs the reportSelect command.
	Summary Report—Opens the Summary Report form. For more information, see Summary Report in the Tools chapter.
	Floorplan Toolbox—Provides access to the features commonly used during floorplanning. For more information, see Floorplan Toolbox in the Tools menu chapter.
	Clear All Ruler—Clears all rulers from the display area.
	Report Yield—Runs the `reportYield` Command.

Design Views

The Encounter main window includes three different design views that you can toggle during a session: the Floorplan view, the Amoeba view, and the Physical view.



Selecting a design view also changes the display of the available tool widgets. For a descriptions of all the widgets, see Tool Widgets on page 72.

Floorplan View

The Floorplan view displays the hierarchical module and block guides, connection flight lines, and floorplan objects, including block placement, and power and ground nets.

Use the `G` key (ungroup), or click the *Hierarchy Down* icon, to display the submodules for a selected module guide. Each time you use the `G` key, you move further down the hierarchy. Use the `g` key (group), or click the *Hierarchy Up* icon, to move up the hierarchy.

Amoeba View

The Amoeba view displays the outline of the modules and submodules after placement, showing physical locality of the module.

Use the `G` key (ungroup), or click the *Hierarchy Down* icon, to display the submodules for a selected module guide. Each time you use the `G` key, you move further down the hierarchy. Use the `g` key (group), or click the *Hierarchy Up* icon, to move up the hierarchy.

Physical View

The Physical view displays the detailed placements of the module's blocks, standard cells, nets, and interconnects. You can move standard cells, blocks, and power and ground objects in the Physical and Floorplan views.

Viewing Floorplan Objects in Physical View

You can view the floorplan objects even in the physical view. To enable this feature:

1. Select Design – Preferences.
2. Select the Display page.
3. Select the option *Show Floorplan Objects in Physical View*.

You can use this feature together with color groups to create a custom view. For example, you can create a color group that has a custom setting for block colors and use this color group while viewing floorplan objects in the physical view.

Tool Widgets

The Encounter main window includes several types of tool widgets, which are located on the left side of the design view icons. Selecting a design view displays the tool widgets that are available for that operation.

The main window also contains *toolbar* widgets across the top of the window. For more information about these widgets, see "Toolbar Widgets" on page 68.

The following table describes the tool widgets for all aspects of design editing:

Widget	Description
	Select—Click this widget, then click a floorplan object to select it. To select multiple objects, use the *Shift* key or click and drag the mouse.
	Move/Resize/Reshape—Click this widget, then click a floorplan object or I/O pad and click on a new location. Use the *Shift* key to select multiple objects to move. Move the mouse to the side or corner of a floorplan object and click and hold to resize and reshape. To create a rectilinear power domain cut, see Step 3 in the Creating a Rectilinear Power Domain section of the "Multiple Supply Voltages" of the *Encounter User Guide*.
	Ruler—Click this widget, then left-click in the design display area and drag the mouse to add a ruler (in micrometers), and left-click again to end the ruler. To move the ruler, left-click and drag it to a new location. Left-click the ruler again to keep it in the new location. To remove a ruler, left-click on it and press *Esc*. To remove all rulers, press `K` (`Shift-k`). You can set the direction in which rulers can be drawn by clicking the widget, then pressing the `F3` key to display the Set Ruler Mode form. You can choose to draw orthogonal, vertical, horizontal, or diagonal rulers. You can also snap rulers to floorplan objects. For more information, see the next section Set Ruler Mode.

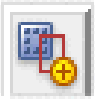
Floorplan Widgets

The following table describes tool widgets for editing the floorplan. For more information on floorplanning, see the "Floorplanning the Design" chapter in the *Encounter User's Guide*.

Widget	Description
	Query Placement Utilization—Click this widget, then drag the mouse across an area in the design. The placement density utilization for that area is written to the Encounter console. The equivalent text command is `queryDensityInBox`.
	Add Placement Blockage—Click this widget, then drag the mouse over an area in the design to draw a placement blockage. This can be done in the *Floorplan* view.
	Add Routing Blockage—Click this widget, then drag the mouse to create a routing blockage on a specified metal layer. To change or specify more than one layer, double-click the routing blockage to open the Attribute Editor.
	Add Partial Placement Blockage—Click this widget to digitize a screen over an area to assign a percentage of placement blockage. Open the Attribute Editor (by double-clicking an object) to set a placement blockage value. **Note:** If you set placement blockage on an area to 100%, during initial placement, this area is not used for standard cell placement, but during IPO operations.
	Create LPDR—Click this Widget to create a Local Preferred Direction Routing (LPDR) area. *Important* Creating Local Preferred Direction Regions (LPDR) and X routing features are obsolete and will be removed in the next major release of the software. For designs that support X routing, you can use LPDR areas to guide the routes in a direction different from the default direction. For more information, see Creating a Local Preferred Direction Routing Area in the "Floorplanning the Design" chapter of the *Encounter User Guide*.

Partition Widgets

The following table describes tool widgets for editing the partition. For more information on floorplanning, see the "Partitioning the Design" chapter in the *Encounter User's Guide*.

Widget	Description
	Add Partition Feedthrough—Click this widget, then drag the mouse over both sides of a partition to insert physical feedthroughs.
	Add Partition Pin Blockage—Click this widget, then drag the mouse over a partition to block the area from creating pins on specific metal layers. To change or specify more than one layer, double-click the partition pin blockage to open the Attribute Editor.
	*Add Partition Pin Guides*—Click this widget, then drag the mouse over an area that overlaps a partition fence or top cell to create a port for a net or bus.
	Cut Rectilinear—Click this widget, then left-click and drag the mouse over a module or partition to create a rectilinear area.

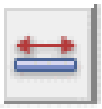
Flip Chip Widget

The following table describes tool widgets for flip chip editing. For more information on floorplanning, see the "Flip Chip and Area I/O" chapter in the *Encounter User's Guide*.

Widget	Description
	Add Tile—Click this widget to create a tile base, then left-click and drag the mouse over the tile base to create tiles.

Wire Editing Widgets

The following table describes tool widgets for wire editing. For more information on editing wires, see the "Editing Wires" chapter in the *Encounter User Guide*.

Widget	Description
	Add Wire—When you click this widget, the cursor changes to a pencil when moved into the design area. You can add power or signal wires. Click at a start point and move the cursor. A second click makes a turn. To end the route, double-click the left mouse button. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `A`
	Add Via—When you click this widget, the cursor changes to a set of concentric squares when moved into the design area. Press the `F3` key to open the Edit Via form. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `o`
	Move Wire—When you click this widget, the cursor changes to a cross when moved into the design area. Use the mouse or the arrow keys to move the wires. You can move horizontal wires vertically and vertical wires horizontally. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `m`
	Cut Wire—When you click this widget, the cursor changes to scissors when moved into the design display area. Move the cursor to draw a draw a line indicating where to cut a wire. The cut must go all the way through the wire. You can cut special wires horizontally and vertically. The results retain the same direction as the original wire. You can also cut rectangles. Signal wires maintain a one-half wire width extension after being cut. Power wires do not maintain an extension. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `X`
	*Stretch or Shrink Wire*—Click this widget to snap selected wires to the next manufacturing grid in the direction that you move the cursor. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *Equivalent keyboard shortcut:* `s`

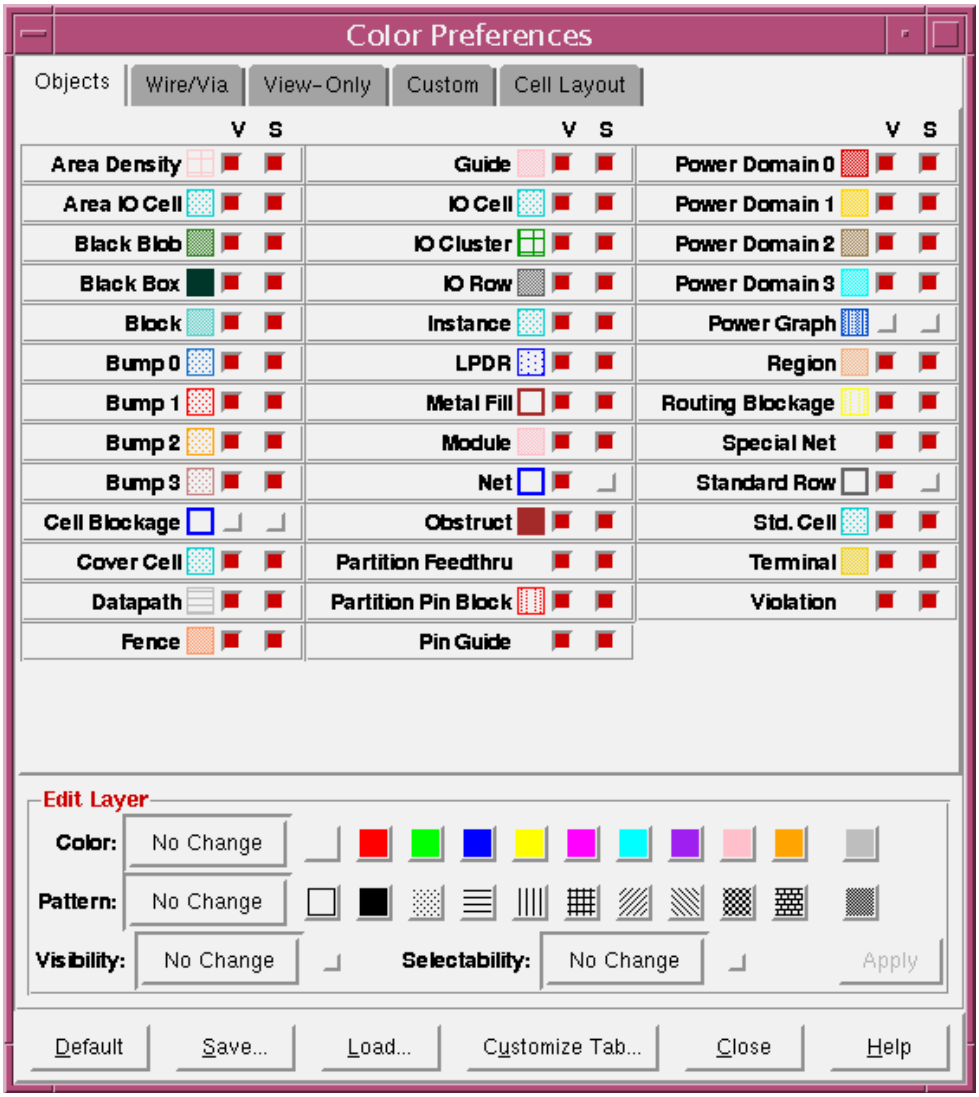
Widget	Description
	Add Polygon—When you click this widget, the cursor changes to a pencil when moved into the design area. Click in the main window at the start point of the polygon and move the cursor. Click once for each turn. Backspace to cancel the last point in the wire. Double-click to commit the wire. Click the *Select* widget or press the a keyboard shortcut to return to *select* mode. *No equivalent keyboard shortcut.*

Color Preferences

To set advanced color options, click the *All Colors* button in the Colors panel on the main window. This opens the Color Preferences form, which has five pages: *Objects*, *Wire/Via*, *View-Only*, *Custom*, and *Cell Layout*

The visibility settings between the pages and the main window are synchronized. That is, as soon you change any setting on any page, the corresponding changes are applied in the main window. For example, if you change the visibility setting of blackblobs, the changes are immediately applied to any blackblobs in the main window.

Objects Page



The Objects page includes the visibility and selectability controls for objects that can be viewed and selected. Each object type has the following features:

- A color button that displays the current color and stipple pattern used to identify the object in the design display area.
  - Click a color button to select it, then click a new color and pattern from the *Edit Layer* section of the form. Click *Apply* to update the Color Preferences form.
  - Double-click the color button for an object to open the Color form.
- A check box for indicating whether the object type is visible in the design display area.
- A check box for making the object type selectable.

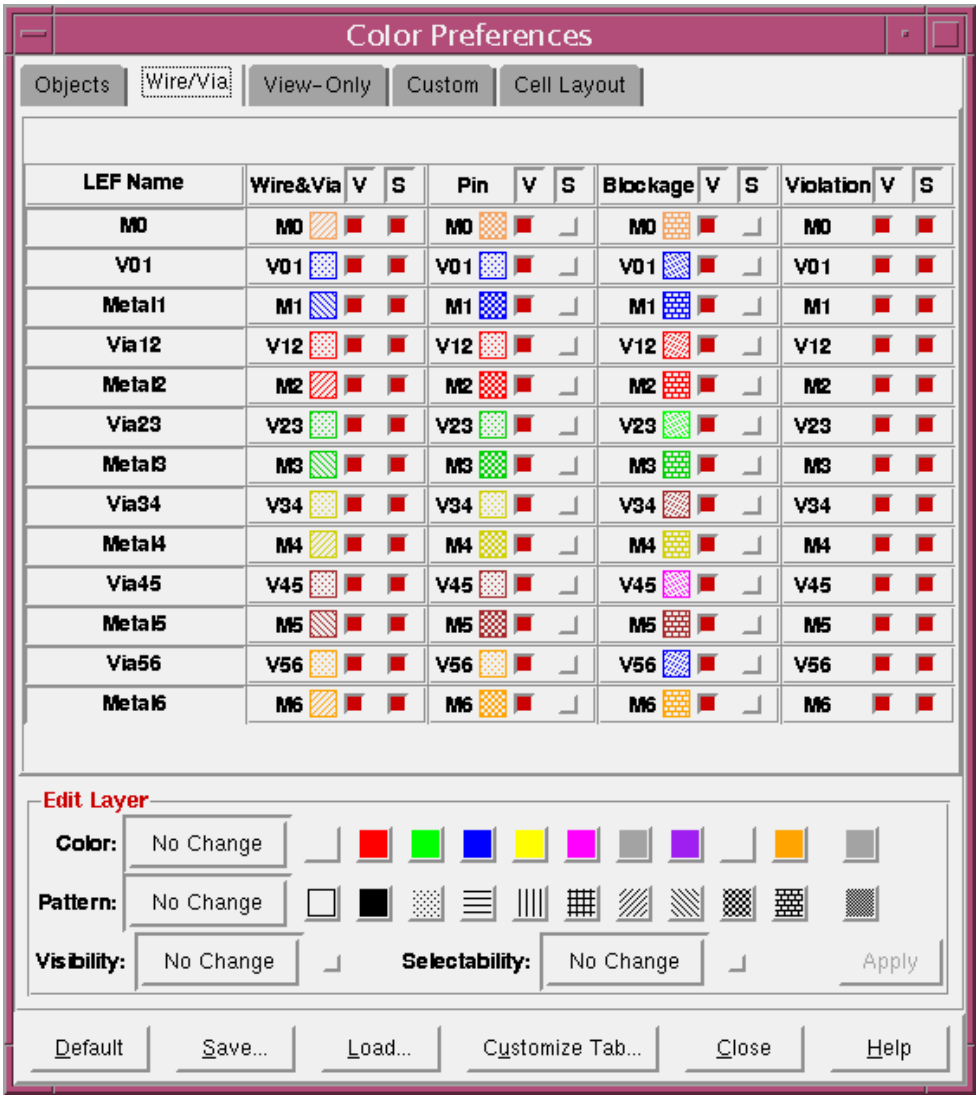
  Note: If an object type does not have a Selectability check box, it cannot be selected.

Tip

When you move the cursor over an object layer name, the equivalent database object name is displayed.

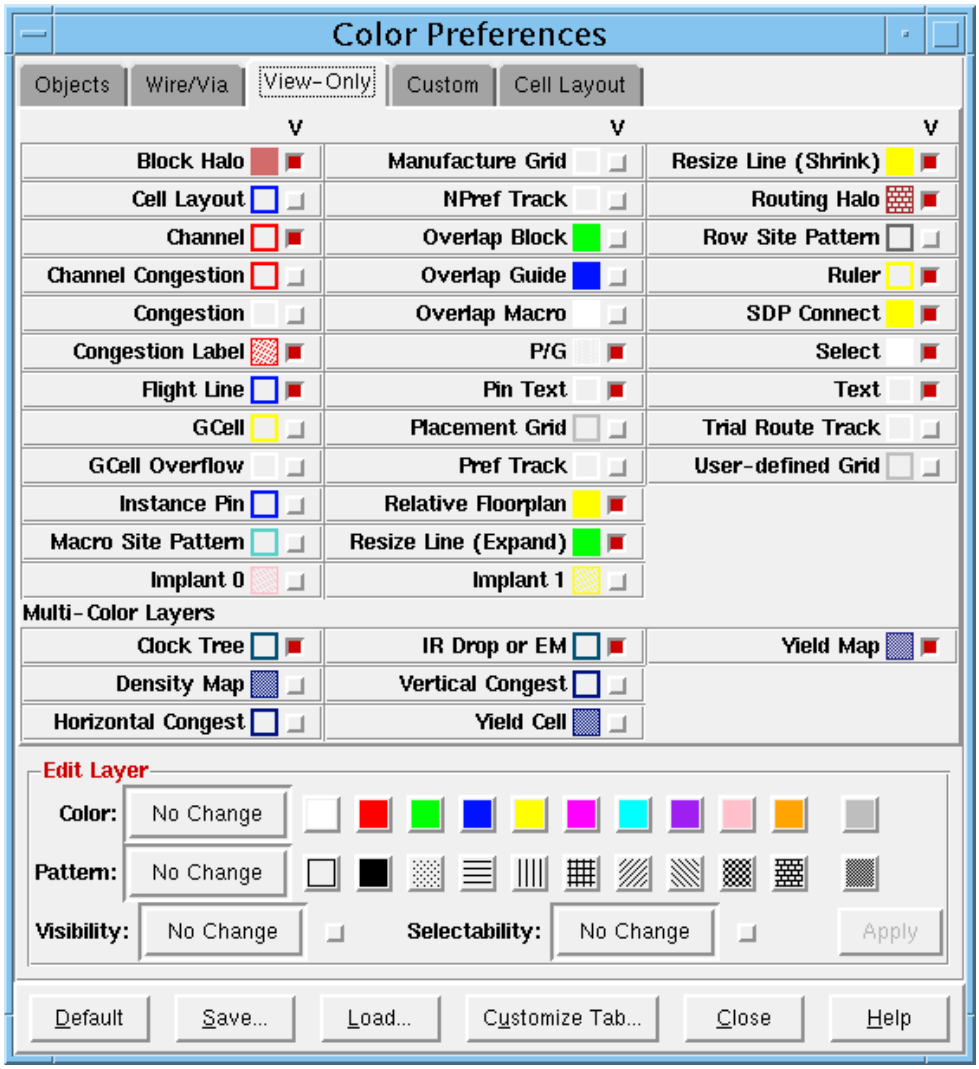
Wire/Via Page

The Wire/Via page includes the visibility and selectability controls for layer-based objects: Wires and Vias, Pins, Blockages, and Violations. You can set global display controls for all objects on the same layer. You can also set controls for individual objects on specific layers.



View Only Page

The View-Only page includes the visibility controls for objects that can be viewed but not selected in the main Encounter window.



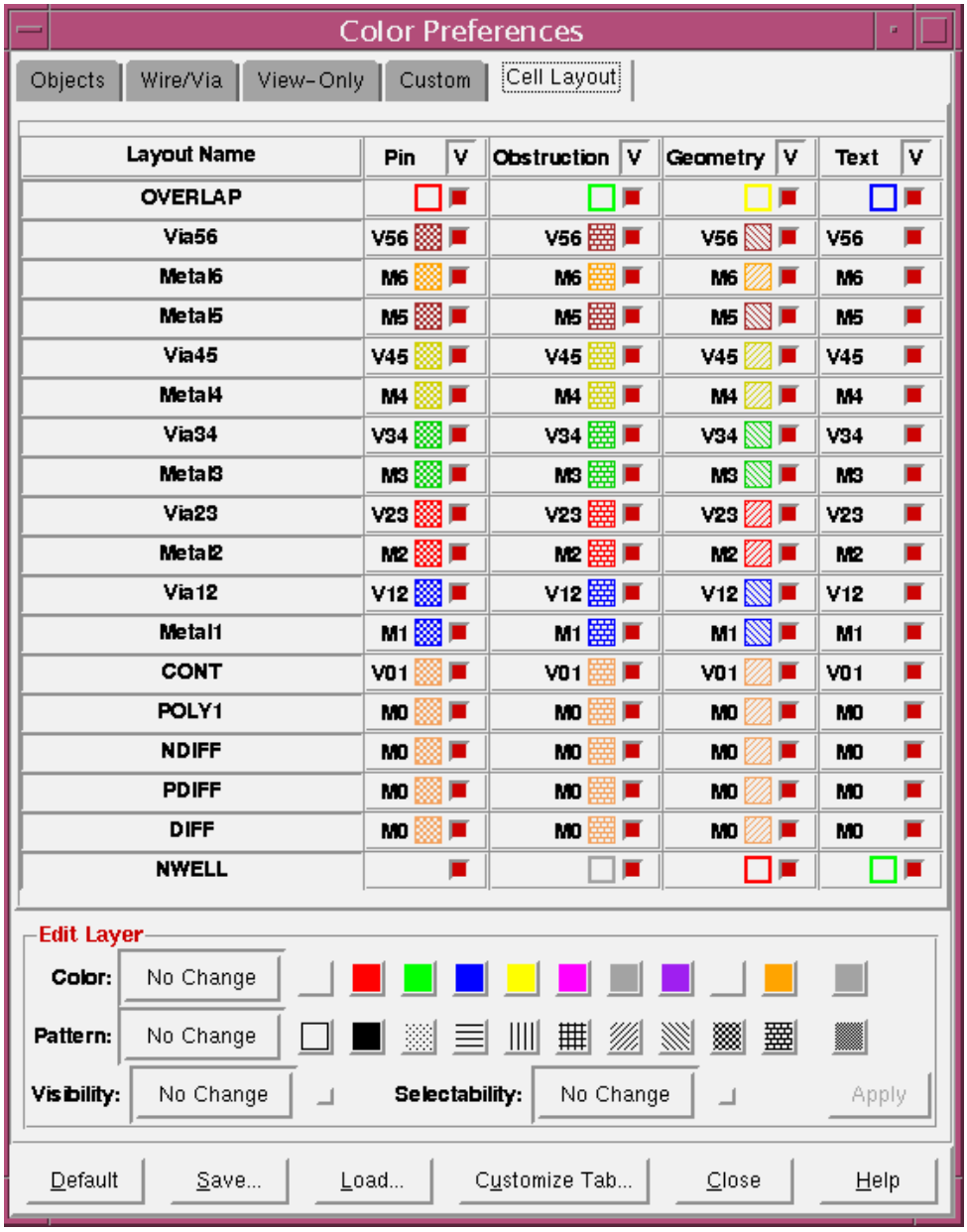
Custom Page

The Custom page contains custom objects. These objects are either imported through the GDS file or created using the Custom Object Editor, accessible through *Edit - Custom Object Editor* menu.

To select a group of objects that are to have the same color and fill pattern, `Shift`-click the first and last objects in the group, click the new color and the new fill pattern, then click *Close.*

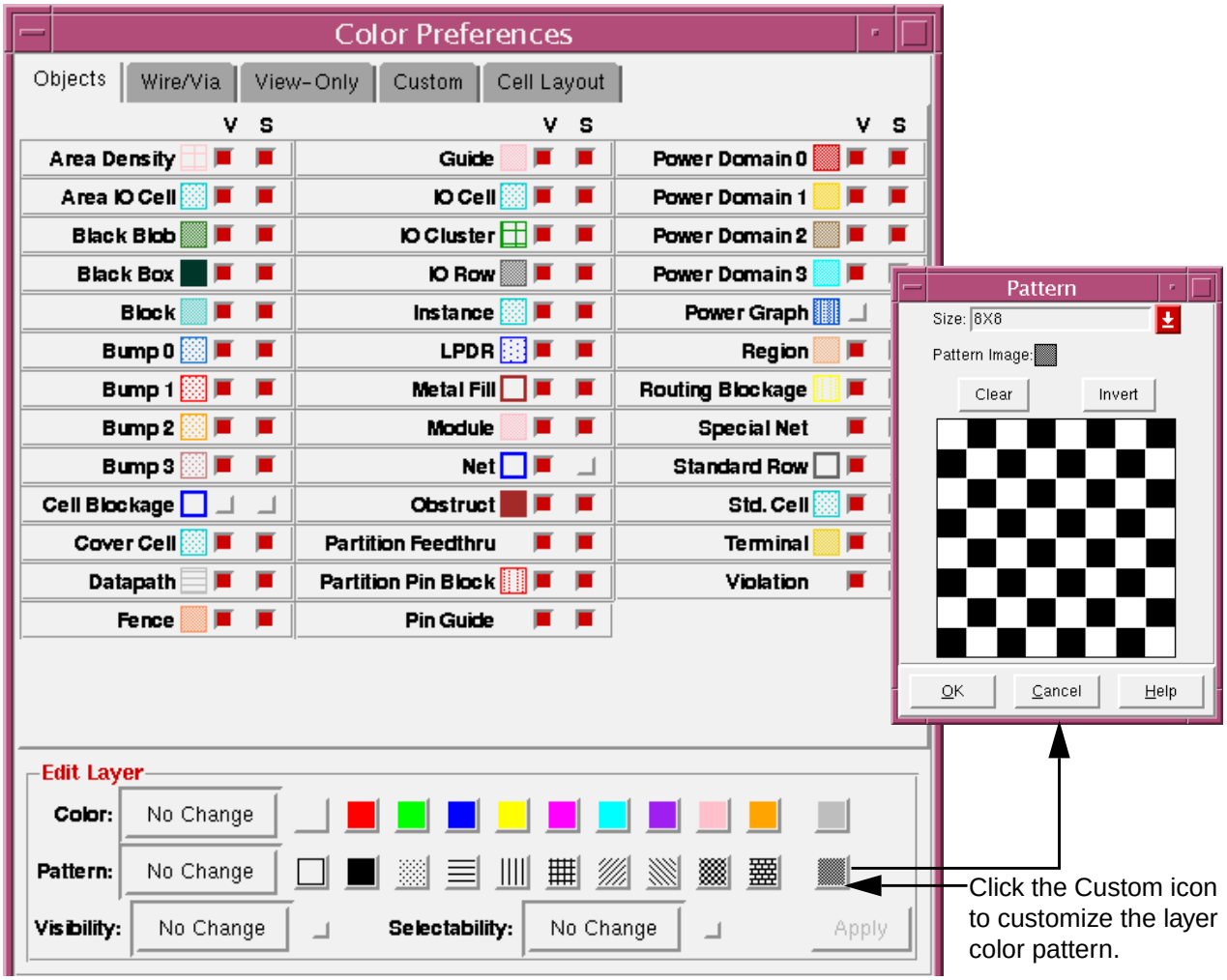
Cell Layout Page

Use the Cell Layout page to set the color preferences for the OA cell layout.

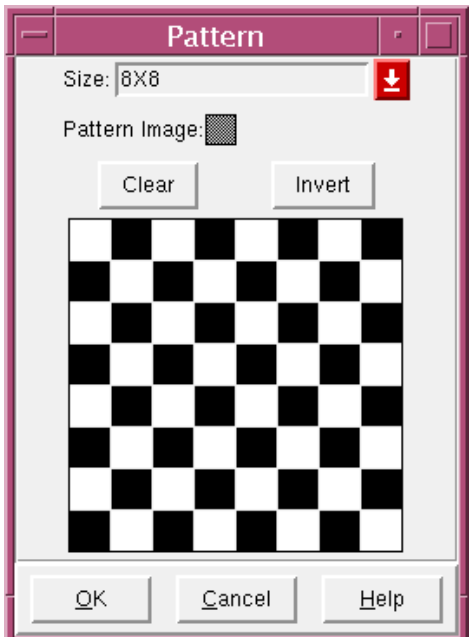


Customizing Layer Color Patterns

You can customize the color patterns for the layers by clicking the Custom pattern icon in the Edit Layer group. The Custom pattern icon is the rightmost icon in the Pattern field.



➤ Click the Custom icon to display the Pattern form.

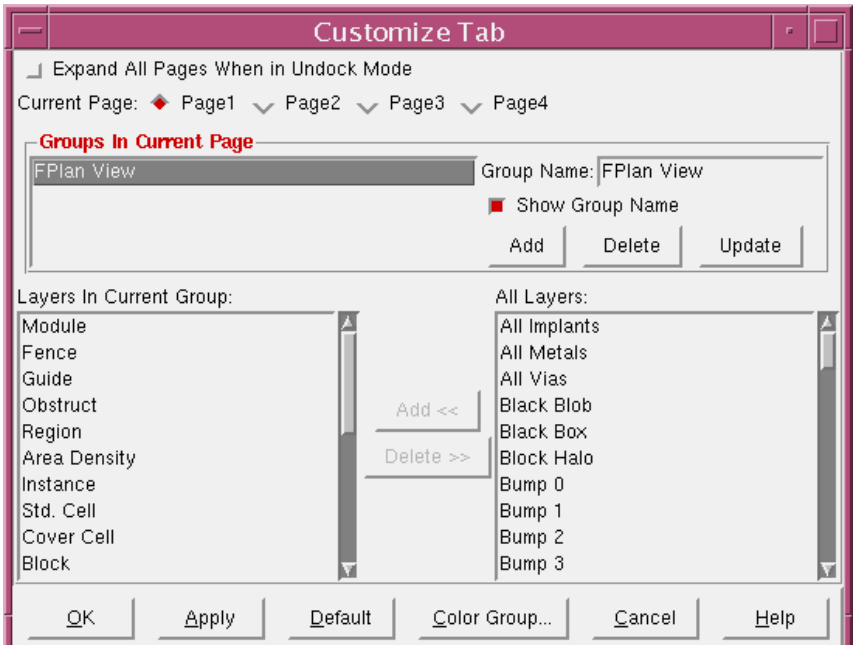


- To clear the pattern, click the *Clear* button.
- To invert the pattern, click the *Invert* button.
- To customize the pattern, do the following:
  - To change a square to black color, click on the square with the left mouse button.
  - To change a square to white color, click on the square with the right mouse button.

Customize Tab

You can use the *Customize Tabs* form, accessible by clicking the *Customize Tabs* button in any page on the Color Preferences form, to customize--or add additional pages to--the Color Bar in the main window.

➤ In any of the pages of the Color Preferences Form, click *Customize Tab*.



Customize Tab Form – Fields and Options

Expand All Pages When in Undock Mode

Displays all pages of the Object Color window when you undock the window.

Current Page

Selects the Page in the Color Bar Window that should be customized. By default, the color bar has two pages, but you can create up to four pages.

Groups in Current Page

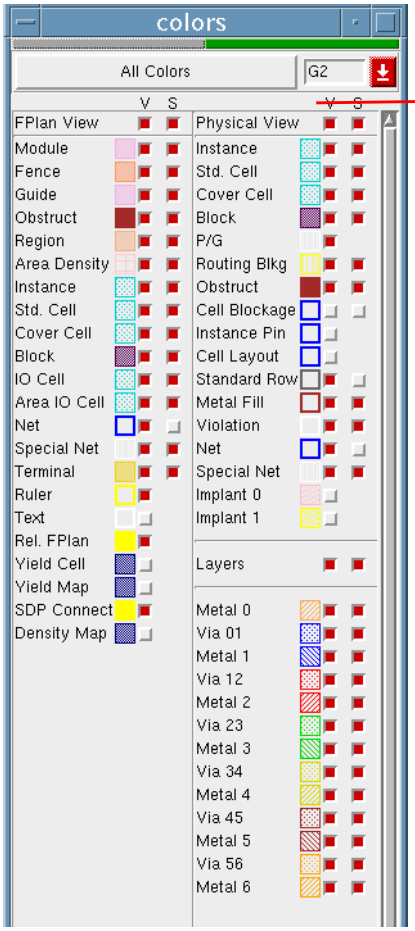
Displays a selectable list of the names of the groups in the current color bar. A group is a collection of objects that are grouped together in the Color Bar. This way you can view the color and visibility controls for related objects together. A page in the color bar can have more than one group.

The default first page in the Color Bar displayed in the main window contains the group FPlan View. The default second page contains two groups: Physical View and Layers.

You can add, delete, or rename the groups in a Color Bar page.

Group Name	This is an editable field that displays the name of the group currently selected in the *Groups in Current Page* field.
Show Group Name	Displays the name of the group in the Color Bar page. If this option is not selected, the objects in the group are displayed in the Color Bar page, but the name of the group is not displayed. *Default*: The default is *Selected*.
Add	Adds a new group to the page. To add a new group, specify the name of the group in the Group Name field, and then click the Add button. You can then add objects to this group by selecting the objects in the *Add Layer* field and then clicking the *Add* button.
Delete	Deletes the group currently selected in the *Groups in Current Page* field.
Updates	Edits the name of the group currently selected in the *Groups in Current Page* field. To edit the name of the group, first edit the name in the Group Name field, and then click Update.
All Layers	Displays a list of all objects that you can add to a group.
Layers in Current Group	
	Displays the objects currently part of the group.
Add	Adds the object currently selected in the All Layers field to the Layers in Current Group field.
Delete	Removes the object currently selected in the *Layers in Current Group* field.

The following figure illustrates how you can use the *Expand All Pages When in Undock Mode* option:



All pages of the Object Color window are displayed

Applying Preferences in the All Colors Form

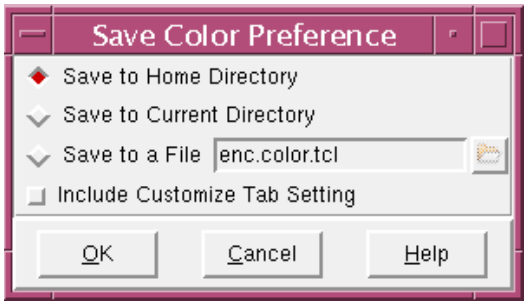
After making changes to the All Colors form, you can perform the following actions:

- To apply the changes in visibility, selectability, color, and stipple pattern to objects in the design display area, click *Close*.
- To save a color preference file, click *Save*. For more information, see Save Color Preference on page 87.
- To load a preference file, click *Load*.

Save Color Preference

Use the Save Color Preference form to save a color preference file. A preference file is a Tcl file that contains color preference information and preference information from the Preferences form (*Design – Preferences*). The recommended filename and extension name is `enc.color.tcl`.

In the Color Preference form, click *Save*.



Save Color Preferences Form—Fields and Options

Save to Home Directory	Saves the color preferences file in your home directory.
Save to Current Directory	Saves the color preferences file in the current working directory.
Save to a File	Saves the color preferences file in the specified location.
Include Customize Tab Setting	

Along with the color preference information, also saves the settings specified through the *Customize Tab* form.

Related Text Command

For information on the following related text command, see the Encounter Text Command Reference:

- `setLayerPreference`.

Multicolor Layers

During a design session, the following object types do not have a single color, but each object has a color that shows a level of severity and magnitude:

- *Horizontal Congest*
- *Vertical Congest*
- *IR Drop or EM*
- *Clock Tree*

To see the level indicator colors, double-click the color button for the object type. This opens a color preferences form for that object type.

Metal Layers and Other Layered Components

Click the *Wire/Via* tab to see the metal layers available in the design. *M0 Wire* represents the masterslice layer, *M1 Wire* represents the bottom metal layer, and so on. The vias are also shown, with *V01* representing the via between the masterslice layer and the first metal layer, *V12* representing the via between the first and second metal layers, and so on.

You can set preferences for other layered components in addition to wires and vias. For each metal layer, you can set the color, stipple pattern, visibility, and selectability for pins, tracks, blockages, and violations.

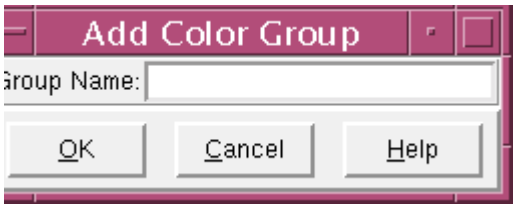
Note: Violations are not selectable.

Creating and Editing Color Groups

You can create color groups to customize the color settings in Encounter. A color group can contain custom color settings for various objects—for example, you can set the blockage color to red in one color group and to blue in another color group. You can switch between color views during an Encounter session. The settings specified in a color group are applied in all views.

To create a Color Group, do the following

1. In the main window, click the *All Colors* button. The *Color Preferences* form appears.
2. Create the custom color settings that you want for the group. For example, you might want to set the block color, or the visibility of blockages.
3. Click the *Customize Tab* button. The *Customize Tab* form appears.
4. Click the *Color Group* button. The *Edit Color Group* dialog box appears.
5. Click the *Add* button. The Add Color Group form appears.



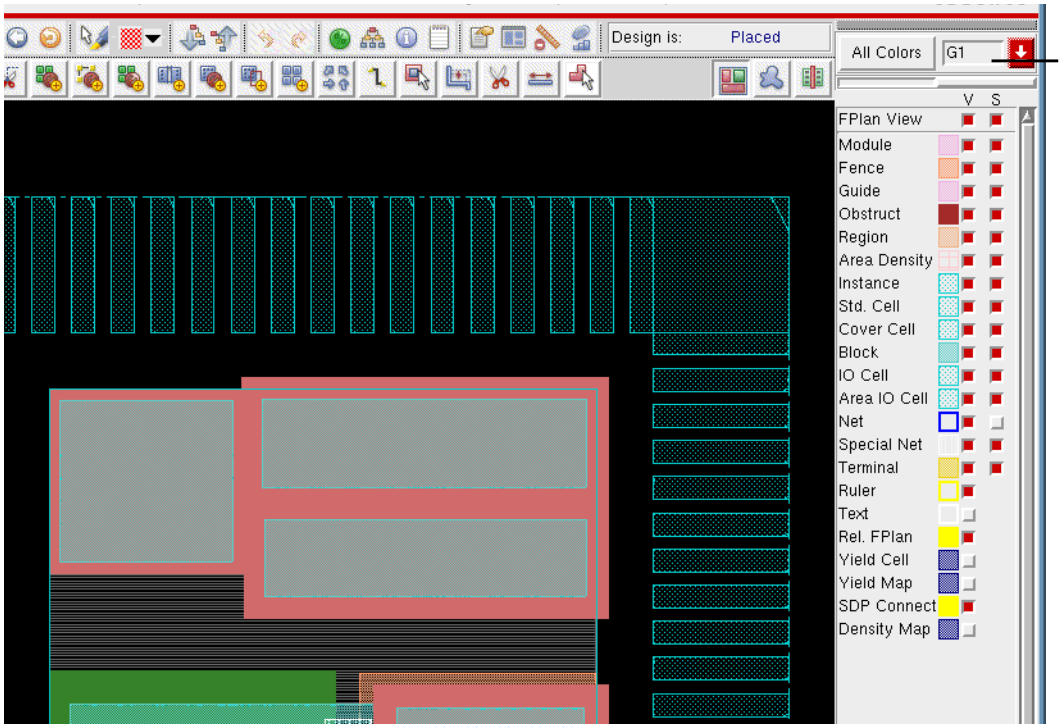
6. In the Group Name field, enter the name of the new color group, and click OK.

The new color group is created.

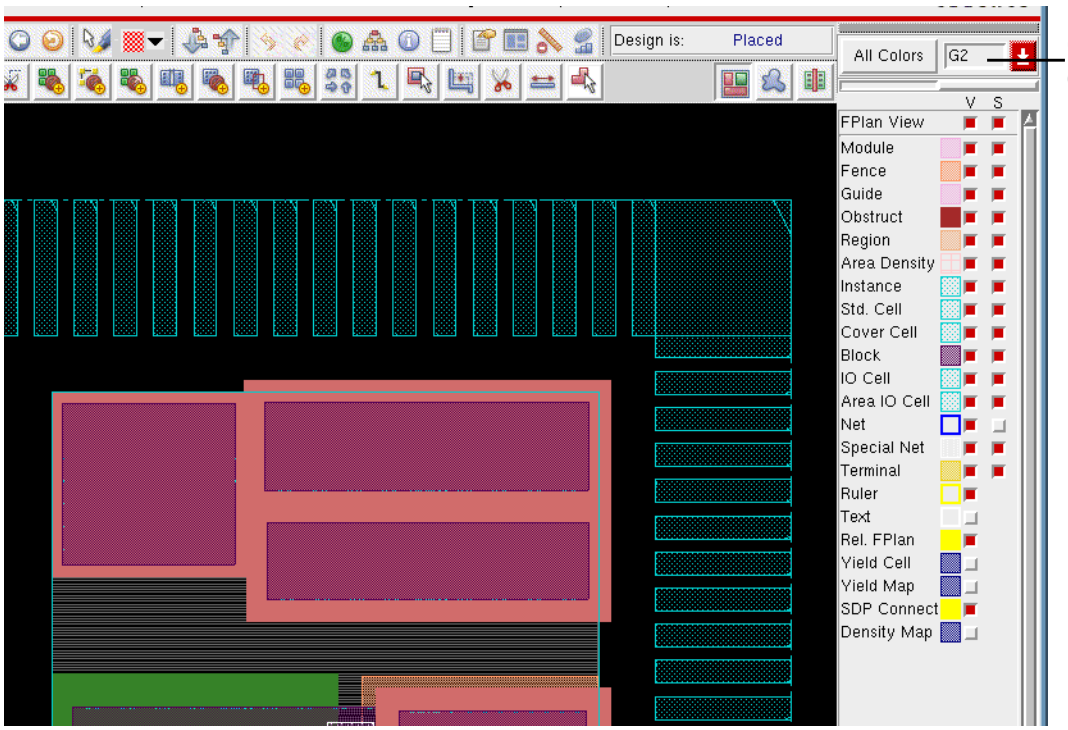
To specify or change the color settings for the Color Group, do the following:

1. In the main window, click the *All Colors* button. The *Color Preferences* form appears.
2. Create the custom color settings that you want for the group. For example, you might want to change the instance color, or the visibility of blackboxes.
3. Click the *Customize Tab* button. The Customize Tab form appears.
4. Click the *Color Group* button. The Edit Color Group dialog box appears.
5. Select the name of the *Color Group* to which the changed color settings should be applied.
6. Click the *Set* button. The settings are applied to the selected Color Group.

Once you create one or more color groups, the color setting for a particular group can be applied be selecting the group name from a drop-down menu next to the *All Colors* button in the main form. You can thus select the color group from the main window.



Color settings with group G1 selected



Color settings with group G2 selected

Color Bar

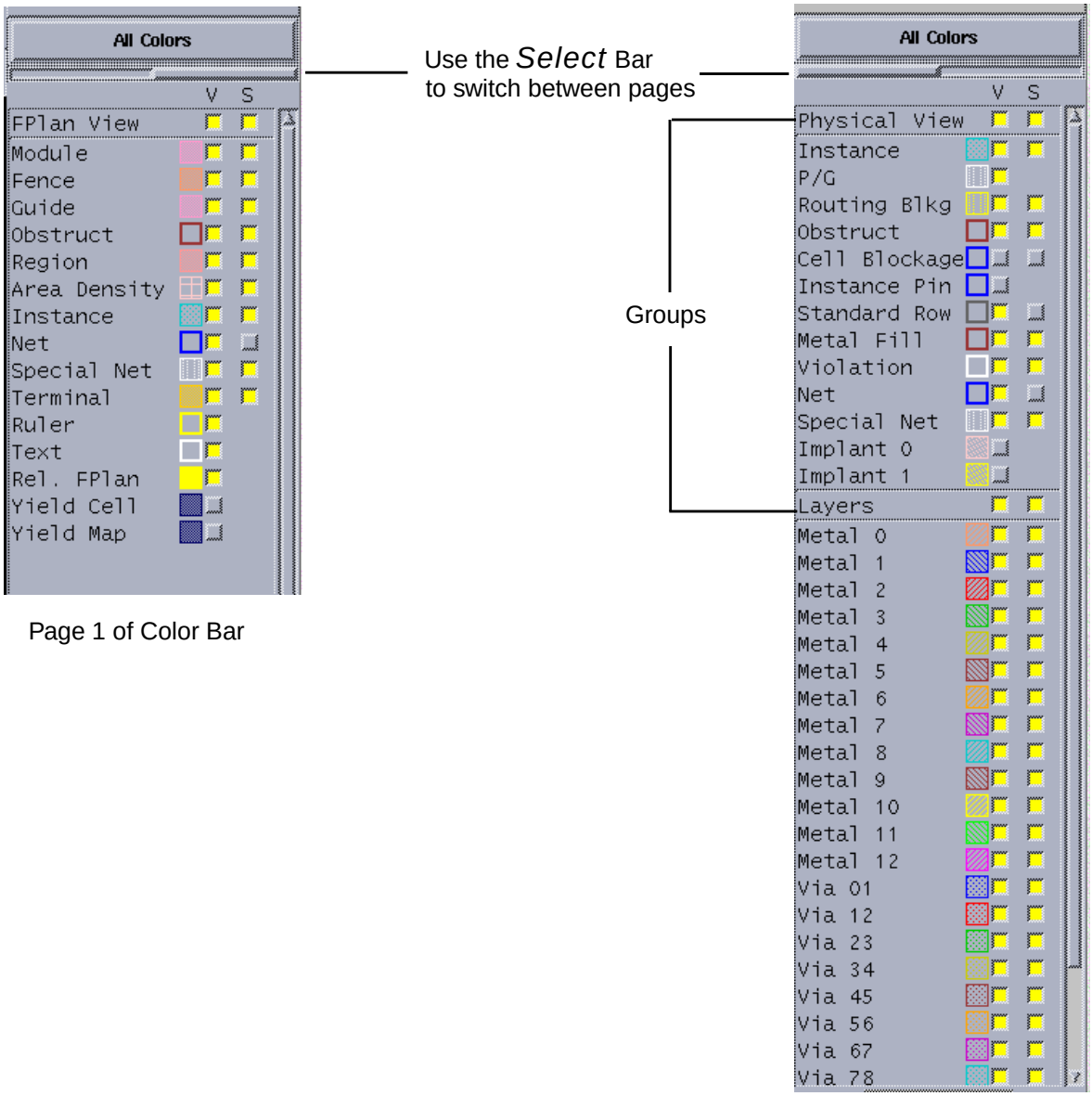
The Encounter main window includes an Object Color Bar that has color display buttons for objects in the design display area. Each object type has a check box for displaying the object in the design display area and a color button that displays the current color used to identify the object in the design display area.

By default, the Object Color Bar has two pages, but you can create up to four pages. Each page in the color bar can have one or more group. A group is a collection of objects that are grouped together in the Object Color Bar. This way you can view the color and visibility controls for related objects together. The default first page in the Object Color Bar displayed in the main window contains the group FPlan View. The default second page contains two groups: Physical View and Layers.

You can use the Customize Tab form to add pages to the Object Color Bar, add or delete the groups, and to add objects in each group. The Customize Tab form is available on all pages of the Color Preferences form. For more information, see Customize Tab on page 83.

Note: You can right-click on an individual layer to toggle the visibility/selectability of all objects on the layer.

To switch between the pages, click the *Select* bar.



Page 1 of Color Bar

Page 2 of Color Bar

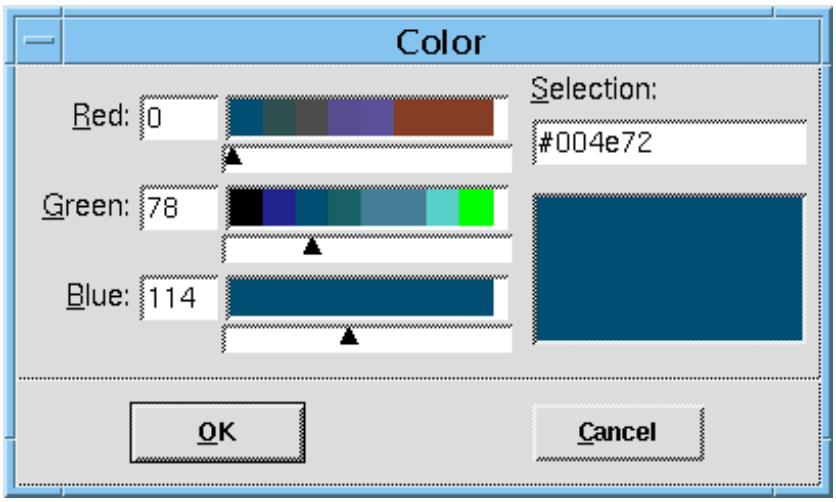
- If you select the *V* (Visibility) check box for an object type, the object type displays in the design display area in the specified color. If you clear the check box, the object type does not display in the design display area.
- If you select the *S* (Selectability) check box for an object type, the object type can be selected in the design display area when you use the *Selection* icon. If you clear the check box, the object type cannot be selected.

Note: Objects that are not visible are not selectable.

Color

Use the color form to customize the display color of an object

➤ Click on the color indicator of the object type to open the Color form.



Important

If you use the text fields, you must press the `Return` key after your text entry.

Viewing OA Cell Layout

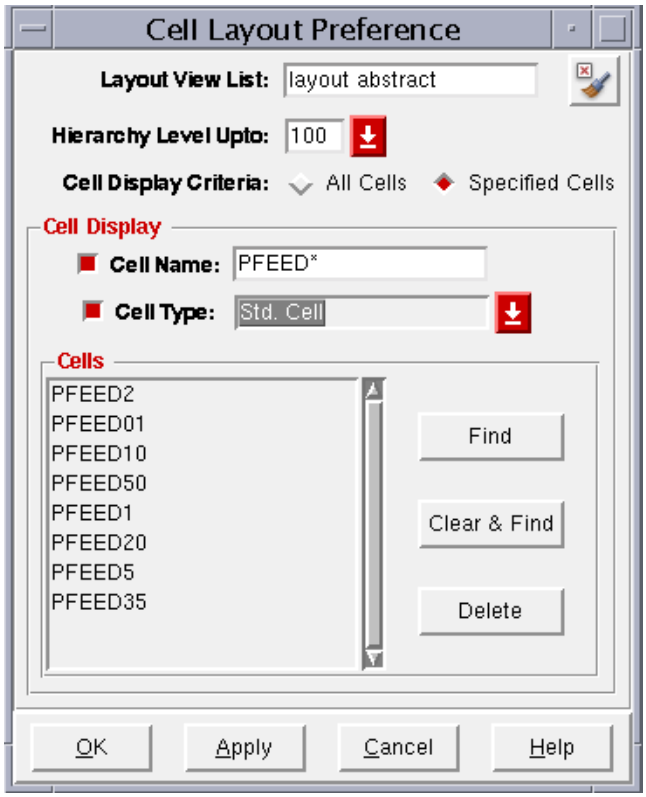
For designs that support Open Access (OA) database, you can view the OA cell layout view in Encounter.

To enable the OA layout view, enable the visibility of the Cell Layout option in the Object Color bar in the main window or in the View-Only page in the Color preferences form (accessed by clicking the All Colors button in the main window).

To change the color settings for OA cell layout, use the Cell Layout Page in the Color Preferences form.

To select the cells whose layout should be displayed, do the following:

1. Select Design – Preferences.
2. Select the Design page if it is not already selected.
3. Click the Cell Layout Preference button. The Cell Layout Preference form appears.



In the Cell Layout Preference form, select the cells to be displayed. For more information on the fields and options in the Cell Layout Preference form, see Cell Layout Preference in the “Design Menu” chapter of this document.

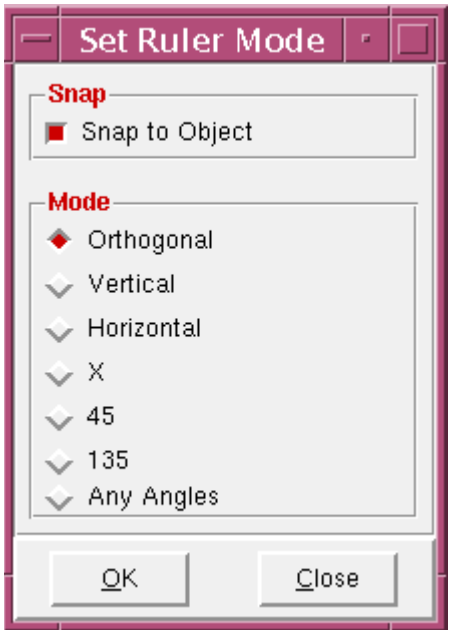
Set Ruler Mode

Use the Set Ruler Mode form to set the direction in which ruler lines are drawn.

To open the Set Ruler Mode form:

1. Click the Ruler widget

2. Press the F3 key.



Set Ruler Mode – Fields and Options

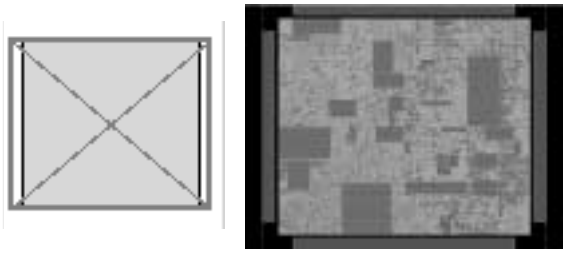
Snap to Object	
	Specifies that the ruler should snap to the nearest floorplan object.
Orthogonal	Specifies that ruler lines can be drawn in horizontal as well as vertical directions.
Vertical	Specifies that ruler lines will be drawn in the vertical direction.
Horizontal	Specifies that ruler lines will be drawn in the horizontal direction.

X	Specifies that ruler lines can be drawn at a 45 degree angle as well as at a 135 degree angle.
45	Specifies that ruler lines will be drawn at a 45 degree angle.
135	Specifies that ruler lines will be drawn at a 135 degree angle.
Any Angle	Specifies that ruler lines can be drawn in any direction.

Satellite Window

The main window includes a satellite window, which identifies the location of the current view in the design display area, relative to the entire design. The chip area is identified by a yellow box, the satellite view is identified by the pink crossbox. When you display an entire chip in the design display area, the satellite crossbox encompasses the chip area yellow box.

Satellite crossbox
(entire chip)

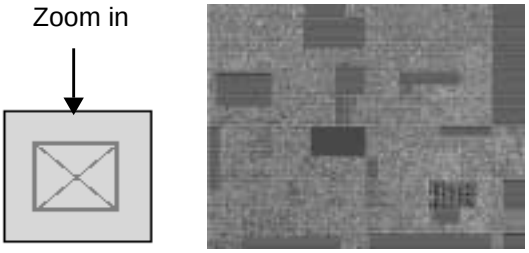


Design display area
(entire chip)

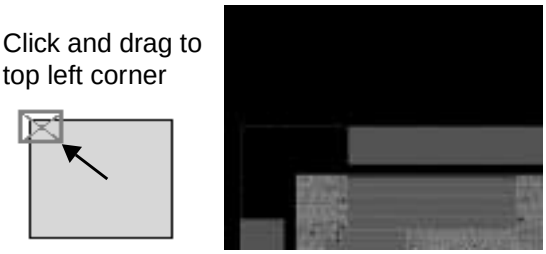
When you zoom and pan through the chip in the design display area, the satellite crossbox identifies where you are relative to the entire chip.

- To move to an area in the design display area, click and drag on the satellite crossbox.
- To select a new area in the design display area, click and drag on the satellite crossbox.
- To resize an area in the satellite window, click with the `Shift` key and drag a corner of the crossbox.

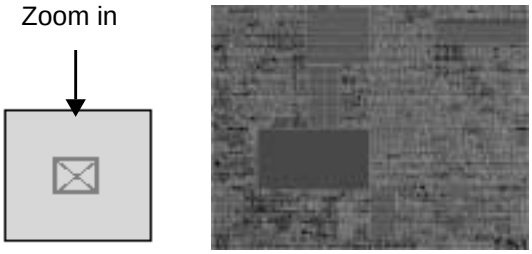
Zoom in



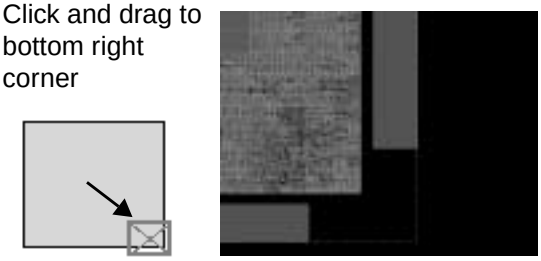
Click and drag to
top left corner



Zoom in



Click and drag to
bottom right
corner

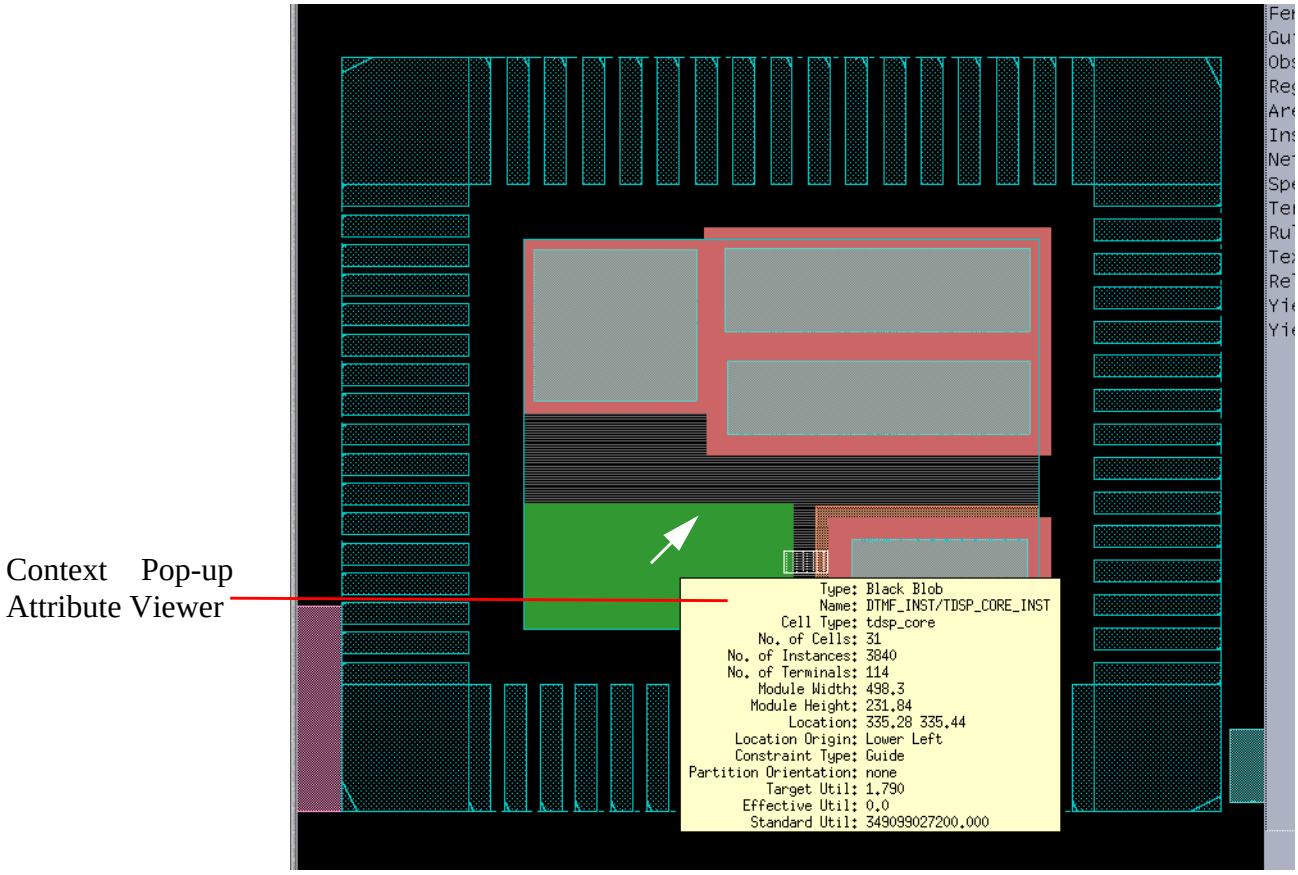


- To define a chip area in the satellite window, right-click and drag on an area.

Context Pop-up Attribute Viewer

The basic properties of an object are displayed in the Context Pop-up Attribute Viewer that appears when you hold the cursor over the object. The previous Attribute Viewer has, therefore, been removed.

You can view properties of overlapping objects--use the n key to view the next object and the p key to view the previous object.



You can turn off the Context Pop-up Attribute Viewer by deselecting the *Show Attributes Popup* checkbox in the Display page of the Preferences GUI, accessible by selecting *Design - Preferences* from the menu. By default, the *Show Attributes Popup* checkbox is selected.

Note: For this feature to work, the Auto Query mode (bindkey Q) should be enabled.

Note: The Context Pop-up Attribute Viewer, which appears on mouse-over, displays the basic properties of objects. To view all the properties of an object, open the Attribute Editor by double-clicking the object or by clicking the middle mouse button and selecting *Attribute Editor*.

To turn this feature on or off, use *Design – Show/Hide – Properties*.

Auto Query

The main window includes a *Q* icon located at the bottom of the design display area that enables and disables the auto query. When you enable auto query, text information displays for any object that is under the cursor. You can use auto query for blockages, hand-drawn or inside cell instances, instance pins, special route wires and vias, and cell instances. When you use the `loadViolationReport` command to load a file with violation markers generated by external tools, auto query displays the rule names for the markers.

If there are overlapping objects under the cursor, text information displays for the object that is on top. Use the n key to get information on the next object, and the p key to get information on the previous object. You can also use the `F8` binding key to copy auto query text from the message bar in the Encounter main window to the Encounter console. The text is displayed in the Encounter console with the prefix `Message`.

Docking Sub-windows

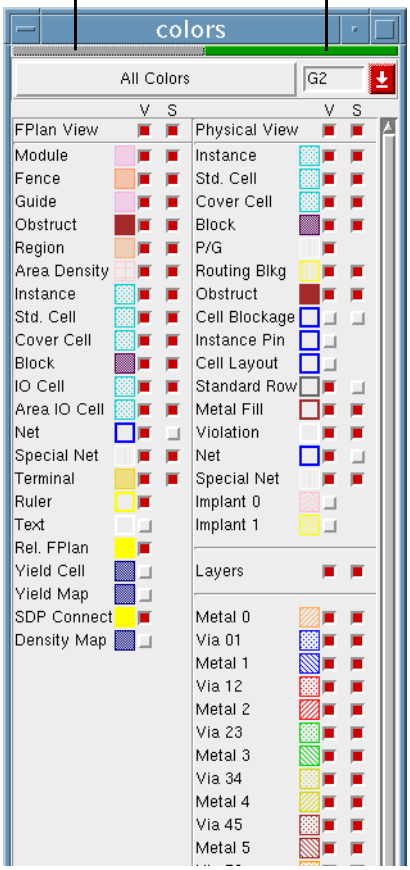
You can dock any sub-window except the artwork window, to the side, top, or bottom of the display area. The docking feature applies to tool widgets and toolbar widgets as well

- Click on the sub-window handle (blank raised area in the left of the sub-window).
- Drag to the desired location.

You can place the sub-window anywhere in the design area. You can dock tool widgets and toolbar widgets as well. Once you place a window somewhere in the design area, you can dock it back with a single click by clicking on the green area of the dock/undock handle. For ease-of-recognition, the mouse cursor changes to a ‘hand’ icon when you place it over the green area. You can use the grey area of the handle to drag the undocked window to any portion of the Encounter main window. The following example shows an undocked Object Color window.

Click on the grey part of the handle and drag the mouse to move the window to another location

Click on the green part of the handle to undock the window immediately



Tear-off Menus and Sub-menus

You can tear off any menu or sub-menu and place it anywhere in the design area. To tear off a menu or sub-menu, click on the dotted line that appears at the top of the menu or sub-menu, and drag the menu to where you want it displayed in the design area. The menu remains on the screen as a window when you release the mouse button.

Mouse Operation

You can use the mouse buttons to perform various command shortcuts.

- Left-click the mouse to perform the action of the active icon.

  The *Select Object* icon is active by default. Each of the three design views allows certain objects to be selectable. The following table shows which objects can be selected for each view:

View	Selectable Objects
Floorplan	Modules, blocks, and floorplan objects.
Amoeba	Modules and blocks
Physical	Blocks, instances, and nets

  - Use the `Shift` key for multiple object selections, and to move multiple objects. You can also left-click and drag the mouse to select objects, such as partition pins and block pins.
  - Use the space bar to change the highlighting focus on an object.
  - Double-click the left mouse button on an object to view or change object attributes.

- Hold the `Shift` key and right-click and drag the mouse to pan the display. The design shifts as you move the mouse.
- Right-click and drag the mouse to specify an area that you want to see in greater detail. When you release the mouse button, the display zooms in to the selected area.

Keyboard Shortcuts

Encounter provides keyboard shortcuts, called binding keys, to access commands in the design display area. For information on creating or modifying bindkeys, see Binding Key in the “Design Menu” chapter.

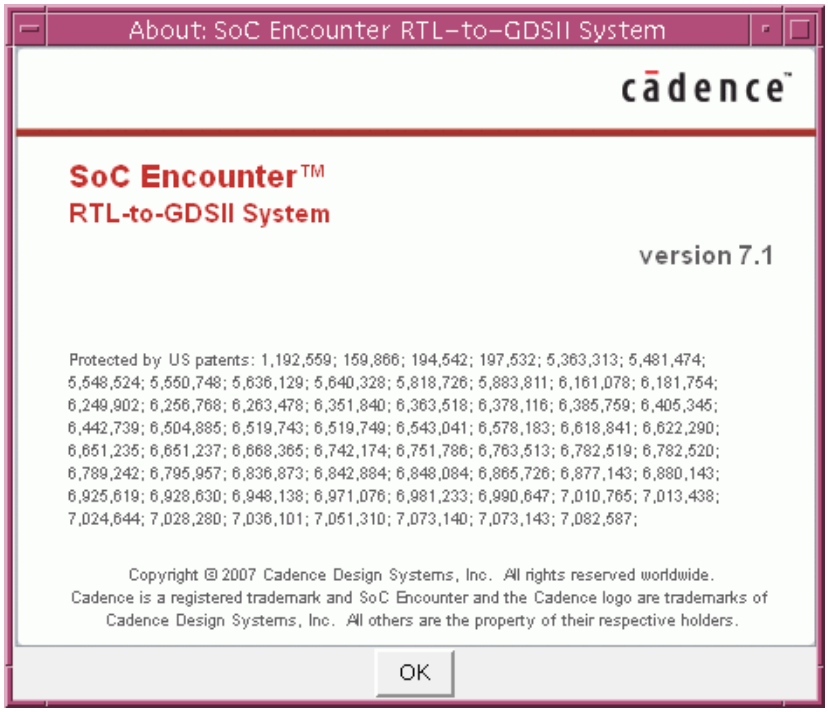
Viewing the Documentation Library through the Help Menu

You can access the complete library of Encounter documentation through the Help menu. The *Help – Help Library* link opens the Cadence Help viewer with all the books in the Encounter documentation suite.

You can also view the individual books through their respective links from the Help menu—for example, to view the Encounter Text Command reference, select *Help – Encounter Text Command Reference.*

Displaying the Encounter Version Number, and Patent- and Copyright-Information

The Help – About menu brings up the About Encounter dialog box. This dialog box displays the version number as well as patent- and copyright-related information.



2

Design Menu

- Import Design on page 108
- Import RTL on page 184
- Restore Design on page 194
- Save Design As on page 199
- Load on page 203
- Save on page 224
- Check Design on page 251
- Report on page 257
- Preferences on page 265
  - Binding Key on page 288
- Mode Setup on page 294
- Global Variables on page 371
- Multiple CPU Processing on page 373
- Show/Hide on page 380
- Exit on page 381

Import Design

The Design Import form enables you to set up the design for import into the Encounter software. Use this form to import a full chip design; a partial design, such as a module; or a partitioned design.

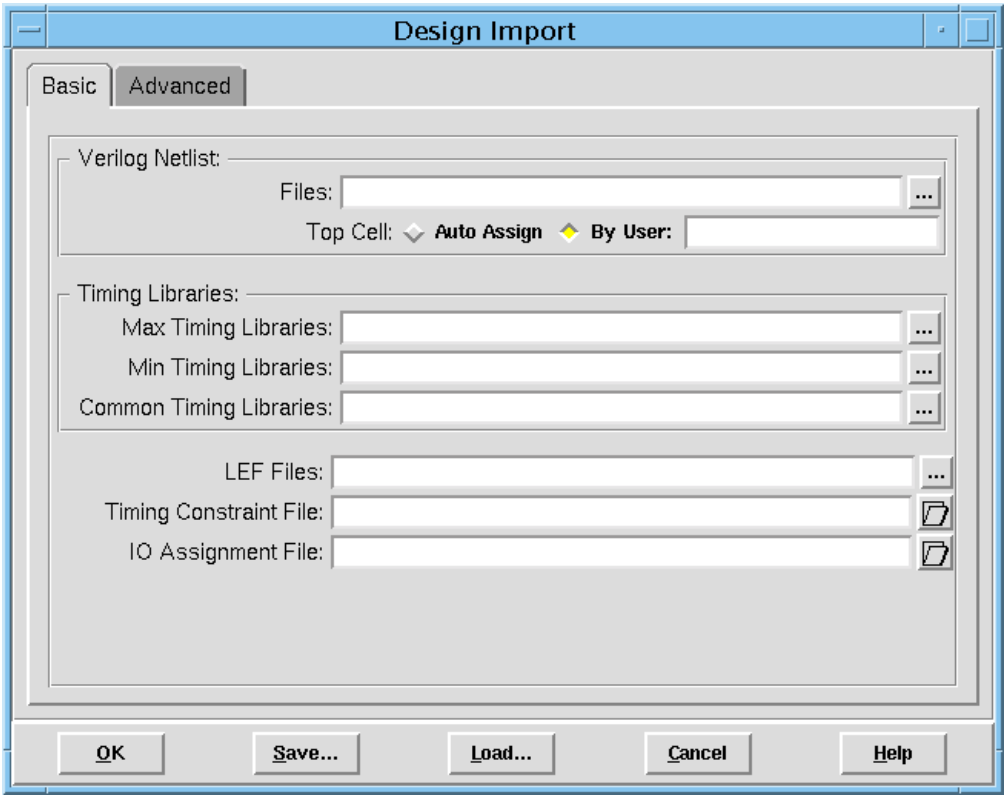
The Design Import form contains the following two pages:

- Design Import – Basic on page 109
- Design Import – Advanced on page 113

Design Import – Basic

Use the *Basic* page of the Design Import form to specify the gate-level Verilog® (structural) netlist, timing libraries and constraint file, LEF files, and I/O assignment file to be imported into the software.

➤ Choose *Design – Import Design* and click the *Basic* tab.



Design Import – Basic Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

Files

Specifies the gate-level Verilog netlist files to import. Encounter automatically checks whether the netlist is unique, and displays a message accordingly.

If specifying multiple names in the text field, use spaces to separate the names. You can use wildcards (`*.extension`) or directory names to specify multiple files. You can specify compressed files (`.gz` extension).

Auto Assign

Extracts the design's top cell name from the netlist, provided the netlist contains only one design.

Default: Off

By User

Specifies the name of the design's top cell when a netlist contains more than one design (more than one top design name). The top cell name specified is the design the software imports and processes.

Default: On

Max Timing Libraries

Specifies the name of the timing libraries containing worst-case conditions for setup-time analysis.

Min Timing Libraries

Specifies the name of the timing libraries containing best-case conditions for hold-time analysis.

Common Timing Libraries

Specifies the name of the libraries common to both the *Min Timing Libraries* and the *Max Timing Libraries*, which are used in both setup and hold analysis.

For information about running single value analysis, see the "Timing Analysis" chapter of the Encounter User Guide.

LEF Files

Specifies the LEF files to import.

You must specify the technology LEF file first, then specify the standard cell LEF and block LEF in any order.

The LEF file provides technology information, such as metal layer and via layer information and via generation rules, which is used in the Add Rings and Add Stripes forms. The router also uses the technology information contained in the LEF file.

If a cell is defined multiple times, Encounter reads the geometry information only from the first definition. For subsequent definitions, Encounter reads the antenna information only.

Note: If the LEF file contains all the physical information for the design, no other files are required for the *Technology Information/Physical Libraries* panel.

Note: Use either an all-LEF flow or an all-OpenAccess flow. Do not mix these two.

Timing Constraint File

Specifies the Synopsys Design Constraint (SDC) constraint file to import. You can import one or more constraint files.

You do not need to translate the files before reading them in. However, you cannot mix formats when reading in files. The Design Compiler timing constraints file is a single file. For the PrimeTime timing constraints file, enter only the top-level file.

The timing constraints reader automatically switches to the proper file format during import; and for PrimeTime constraints files, the reader supports the `include` statements to read the entire design constraints.

For more information on creating timing constraints files, see “Data Preparation” in the Encounter User Guide.

IO Assignment File

Specifies the I/O files to import.

The I/O assignment file assigns an I/O pad for a chip design, or a pin for a block design. The I/O assignment file can be in line order sequence for the I/O pad instance names, or can be rule based. If I/O pads are placed from loading a floorplan file, you do not need to specify an assignment file.

For information on creating an I/O assignment file, see “Generating the I/O Assignment File,” in the “Data Preparation” chapter of the *Encounter User Guide*.

Related Text Commands

- `commitConfig`
- `loadConfig`
- `loadLefFile`
- `loadIoFile`
- `setTimingLibrary`

Related Topics

For information on preparing the design for import, see “Data Preparation” in the *Encounter User Guide*.

For information on the following topics, see “Design Import” in the *Encounter User Guide*:

- Importing Designs
- Selecting Files
- Removing Assign Nets From a Verilog Netlist

Design Import – Advanced

Use the *Advanced* page of the Design Import form to specify additional information to import into the design.

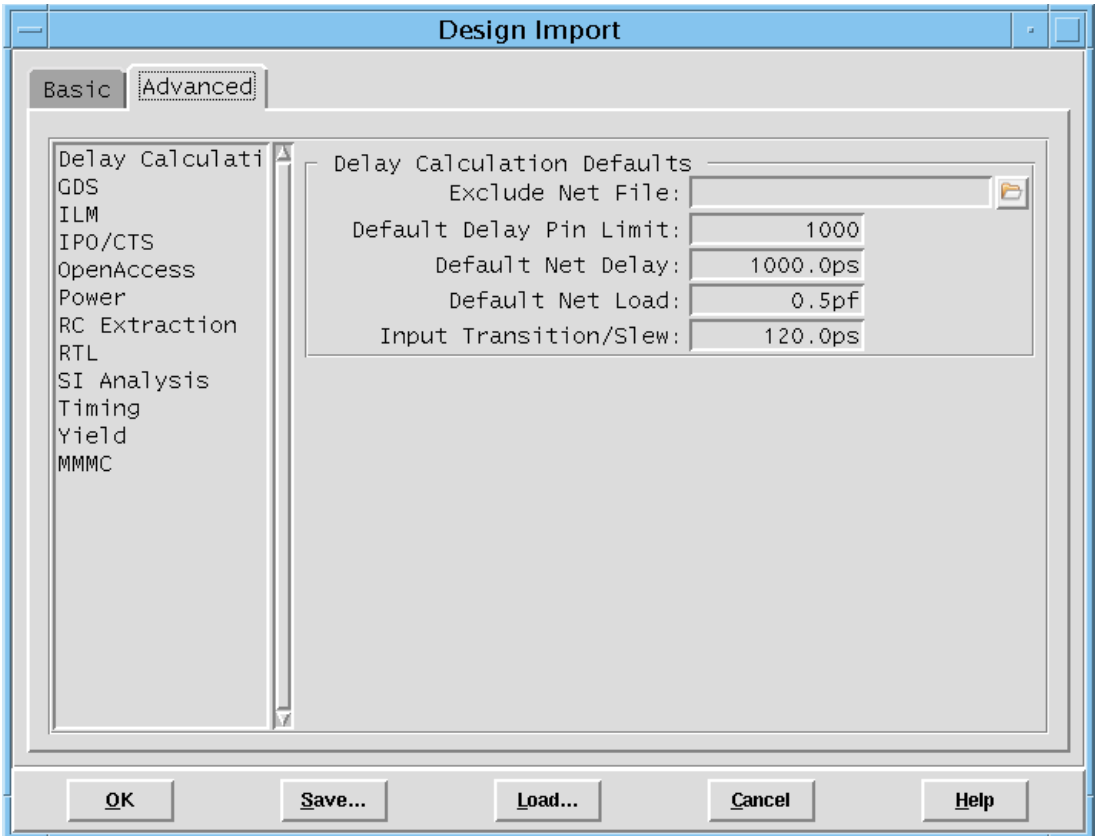
The *Advanced* page contains the following subpages:

- Delay Calculation on page 114
- GDS on page 116
- ILM on page 118
- IPO/CTS on page 120
- OpenAccess on page 121
- Power on page 123
- RC Extraction on page 125
- RTL on page 129
- SI Analysis on page 130
- Timing on page 132
- Yield on page 135
- MMMC on page 137

Delay Calculation

Use the *Delay Calculation* page of the Design Import form to specify the default values used by the delay calculation program and by the timing analyzer to build the timing graph.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *Delay Calculation*.



Delay Calculation Fields and Options

Exclude Net File

Specifies hierarchical nets to be excluded from delay calculation, and assigned the default delay values from this form. These are usually high fanout nets (greater than 1,000 terminals, by default) that increase the run time of the program.

This file can have one of two formats:

- `netName netDelay netOutputTran netLoad`
- `netName netDelay`

Default Delay Pin Limit	Sets the minimum pin count number for a net that is excluded from delay calculation. Nets with terminal counts equal to or greater than the specified value are assigned the default net delay and net load entries. *Default:* `1000`
Default Net Delay	Sets the delay value for a net that meets the pin limit default. *Default:* `1000.0ps`
Default Net Load	Sets the load for a net that meets the pin limit default. *Default:* `0.5pf`
Input Transition/Slew	Sets the default input transition delays and the ideal clock transition time for delay calculation. The Encounter software uses this default for nets that exceed 1,000 terminals. *Default:* `0.0ps`

Related Text Commands

- `setExcludeNet`
- `setUseDefaultDelayLimit`
- `setDefaultNetDelay`
- `setDefaultNetLoad`
- `setInputTransitionDelay`

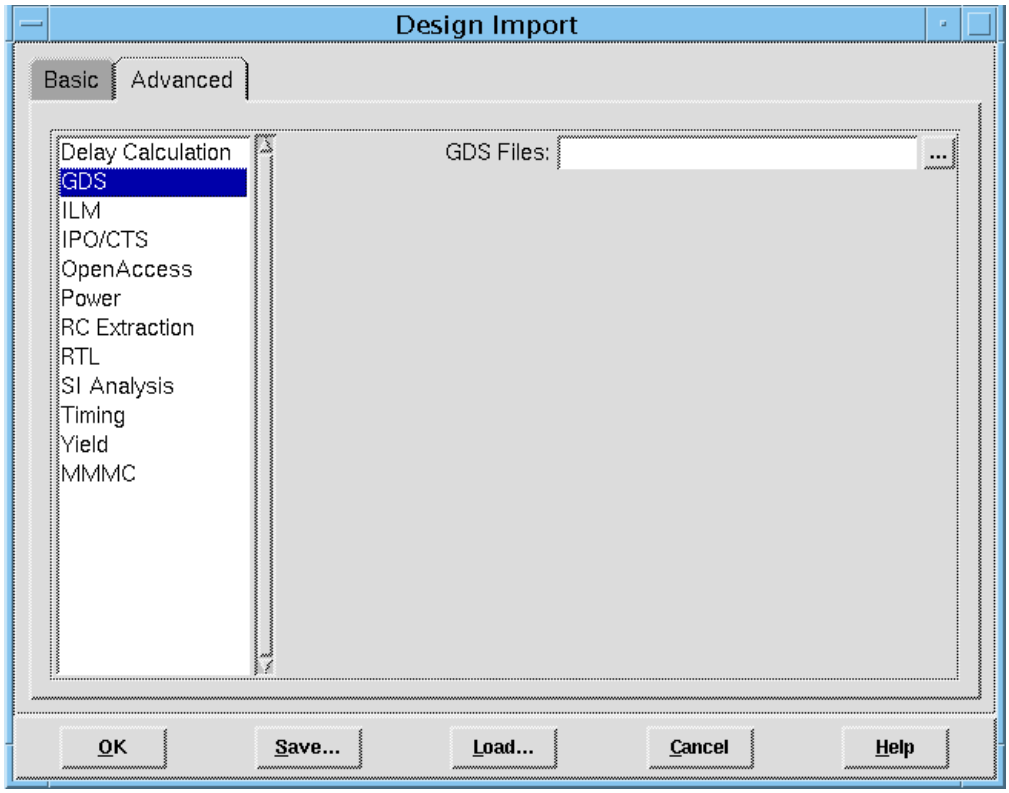
Related Topics

- Delay Calculation Modes and Related Controls

GDS

Use the *GDS* page of the Design Import form to specify information about GDS libraries.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *GDS*.



GDS Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

GDS Files

Specifies a list of GDS files (separated by spaces) to import. After you specify the file names in this form, the names appear in the *Merge Stream Files* field on the GDS Export form. Specifying these files also creates custom layers for display. Custom layer names are of the form `GDS`*x*, where *x* is the GDS layer number.

Related Text Commands

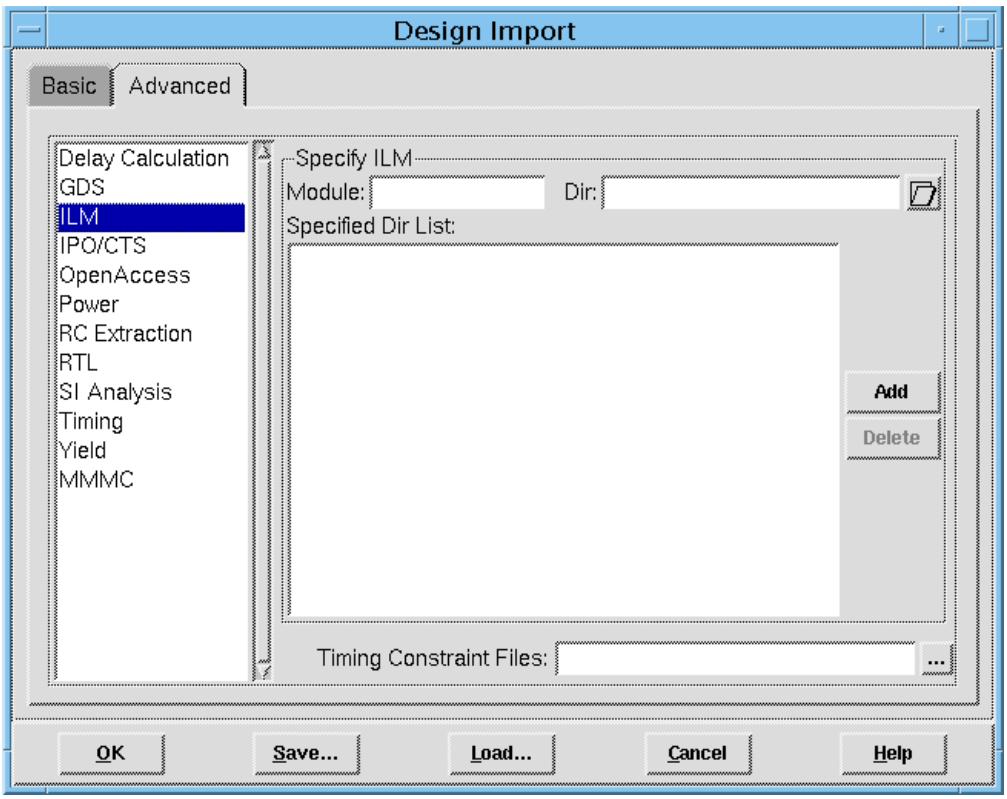
There are no related text commands.

ILM

Use the *ILM* page of the Design Import form to specify the ILM directory for the specified block.

Note: You can use this form only if the ILMs are unflattened (`unflattenIlm`) or the design is in black box view. You cannot change ILM settings in flattened or ILM view.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *ILM*.



ILM Fields and Options

Module	Specifies the module name for the ILM.
Dir	Specifies the directory from where you want to read the ILM files for the specified module. **Note:** The browse (...) button next to this fields opens a form from which you can load selected files.
Add	Adds the specified directory to the directory list.

Delete Removes the selected directory from the directory list.

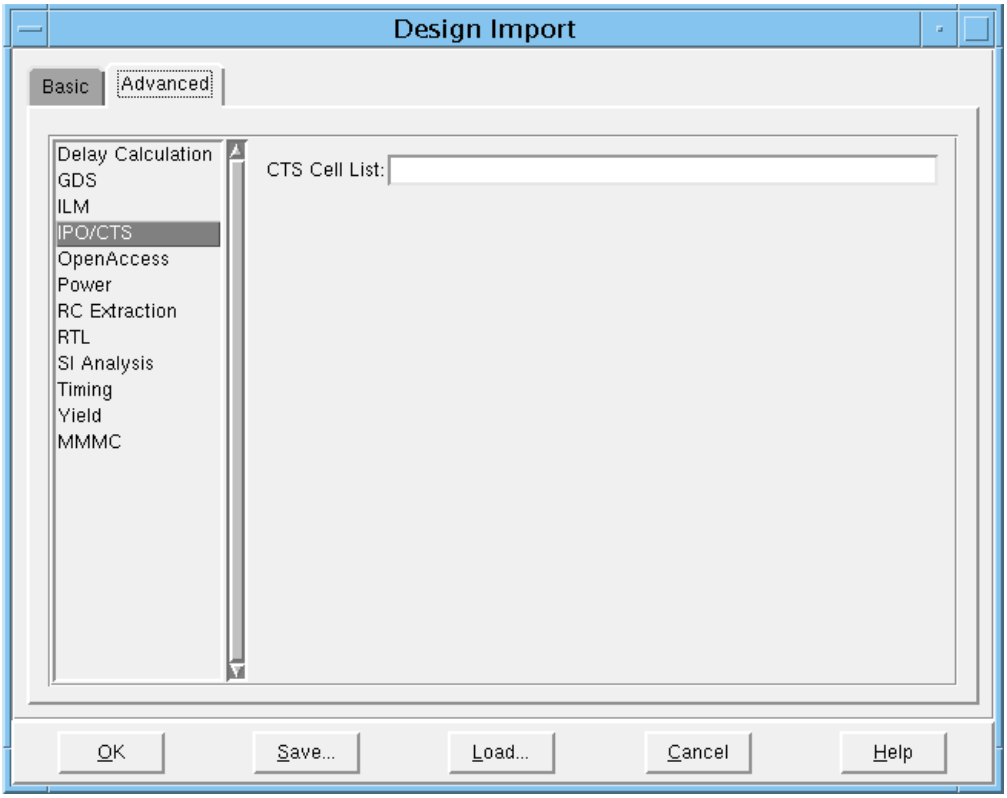
Timing Constraints Files

Specifies the interface logic model (ILM) constraint file. The software reads the specified ILM constraint file, and uses it in the ILM view. This file is not used in the blackbox view.

IPO/CTS

Use the *IPO/CTS* page of the Design Import form to specify a list of buffer or inverter names for timing optimization and clock tree synthesis.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *IPO/CTS*.



IPO/CTS Fields and Options

CTS Cell List	Specifies a list of buffer and inverter names for CTS.

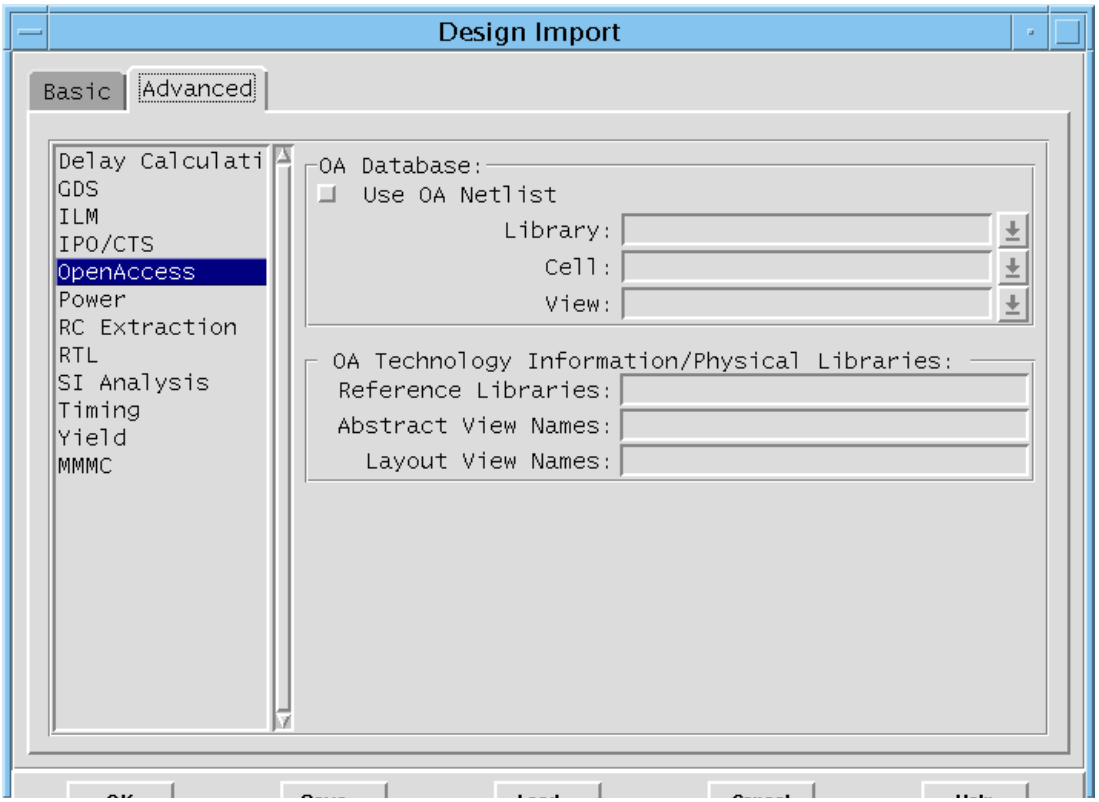
Related Text Commands

- `loadFootPrint`

OpenAccess

Use the *OpenAccess* page of the Design Import form to specify the OpenAccess database, technology information, and physical libraries to import into the software.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *OpenAccess*.



OpenAccess Fields and Options

Use OA Netlist — Selects the OA Database type.

(Use either an all-LEF flow or an all-OpenAccess flow. Do not mix these two.)

Library — Specifies the OpenAccess database library.

Cell — Specifies the OpenAccess database cell.

View — Specifies the OpenAccess database view.

Reference Libraries	Specifies the OpenAccess reference libraries to import. The first OpenAccess reference library listed in this field must contain the technology information for the leaf cells. Specifying these libraries is a prerequisite to using the Save OA Design form (*Design – Save OA Design*). The library names appear in the *Library* field on this form.
Abstract View Names	Specifies the OpenAccess view names in that the software should examine to find the equivalent of the LEF `MACRO` information (for example, `PINS`, `OBS`, `FOREIGN`)
Layout View Names	Specifies the layout view names (separated by spaces) to import. The software uses these layout view names to create custom layers for displaying the GDSII equivalent cell contents. The custom layer names are derived from the Open Access technology library.

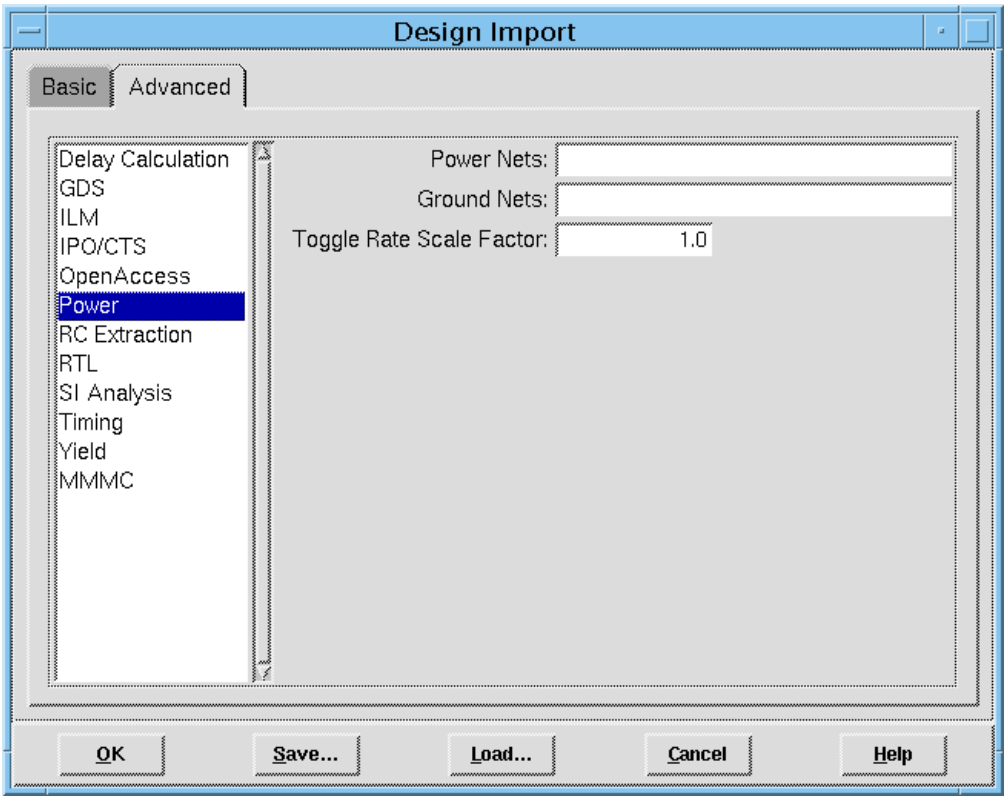
Related Text Commands

- `oaIn`

Power

Use the *Power* page of the Design Import form to specify the power and ground net names, and the scale factors used for power analysis.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *Power*.



Power Fields and Options

Power Nets/ Ground Nets

Specifies the names of the *Power Nets* and *Ground Nets*. You can enter multiple names by separating the net names with a space, for example:

```
VDD VDD1 GND GND1
```

Use the same power and ground net names specified here when creating the power and ground strips in the floorplan.

Toggle Rate Scale Factor

Sets the scaling value that is used to multiply the toggle rate in the Power Analysis form to a new scaled value.

Default: `1.0` (No toggle scaling is done)

Related Text Commands

- `connectToGlobalNet`

Related Topics

- Power Planning and Routing
- Power Analysis

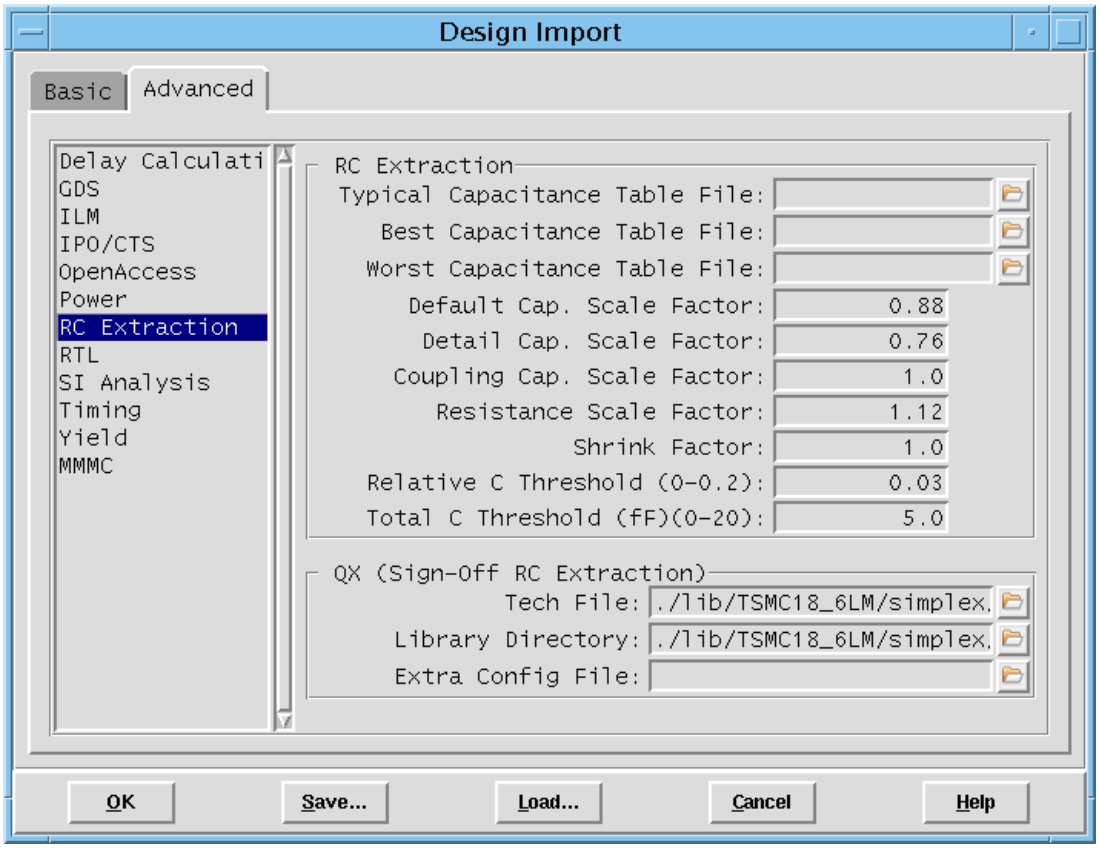
RC Extraction

Use the *RC Extraction* page of the Design Import form to specify scale factors for extracted interconnect resistance and capacitance values. Scaled values you specify here are used by all of the extraction and delay calculation programs.

Note: The Encounter technology file can specify capacitance and resistance scale values. In these cases, the scale values read from the Encounter technology file are used, provided the capacitance and resistance scale default values of 1.0 are not changed.

You can also use the *RC Extraction* page to specify information about the Fire & Ice® QX gate-level extraction files and directories.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *RC Extraction*.



RC Extraction Fields and Options

Typical Capacitance Table File

Specifies the typical case capacitance table to import.

You can generate a capacitance table using the 2-D field solver provided in the Encounter software. For more information, see "Timing – Generate Capacitance Table" on page 484.

Best Capacitance Table File

Specifies the best case capacitance table to import.

You can generate a capacitance table using the 2-D field solver provided in the Encounter software. For more information, see "Timing – Generate Capacitance Table" on page 484.

Worst Capacitance Table File

Specifies the worst case capacitance table to import.

You can generate a capacitance table using the 2-D field solver provided in the Encounter software. For more information, see "Timing – Generate Capacitance Table" on page 484.

Default Cap. Scale Factor

Sets the default scaling values to multiply the extracted interconnect capacitance value to a new scaled value. This scale factor is used for process shrinks.

For information on generating scale factors, see "Correlating Native Extraction With Sign-Off Extraction" in the *Encounter User Guide*.

Default: `1.0`. (The software does not perform scaling)

Detail Cap. Scale Factor

Sets the detail scaling values to multiply the extracted interconnect capacitance value to a new scaled value. This scale factor is used for process shrinks.

For information on generating scale factors, see "Correlating Native Extraction With Sign-Off Extraction" in the *Encounter User Guide*.

Default: `1.0` (The software does not perform scaling)

Coupling Cap. Scale Factor

Sets the scaling values to multiply the extracted interconnect coupling capacitance value to a new scaled value.

Default: `1.0`

Resistance Scale Factor

Sets the scaling value to multiply the extracted interconnect resistance value to a new scaled value. This scale factor is used for process shrinks.

Default: `1.0`. (The software does not perform scaling)

Shrink Factor

Specifies the value by which the software shrinks a design.

Default: `1.0`. (The software does not perform scaling)

Relative C Threshold (0-0.2)

Specifies the relative capacitance threshold value that the software uses to populate the RC Extraction Mode form (*Timing – Analysis Condition – Specify RC Extraction Mode*) and the Extraction Setup form (*Timing – Fire & Ice Extract RC*). If you change this value on the Design Import, RC Extraction Mode, or Extraction Setup forms, the changed value propagates to the other two forms.

This value indicates that the coupling between net A and B is recorded when it is higher than the specified fraction of the total capacitance of net A and B.

Default: `0.03` (3%).

Total C Threshold (fF)(0-20)

Specifies the total capacitance threshold value that Encounter uses to populate the RC Extraction Mode form (*Timing – Analysis Condition – Specify RC Extraction Mode*) and the Extraction Setup form (*Timing – Fire & Ice Extract RC*). If you change this value on the Design Import, RC Extraction Mode, or Extraction Setup forms, the changed value propagates to the other two forms.

This value indicates that if the total capacitance of a net is smaller than this value, the software will ground any coupling capacitance for this net.

Default: `5.0` (fF)

QX (Sign-Off RC Extraction	
Tech File	Specifies the name of an icecaps technology file used by Fire & Ice for RC extraction. The file extension is `.tch`.
Library Directory	Specifies the path to the cell library created within Fire & Ice.
Extra Config File	Specifies the name of a user-created Fire & Ice configuration file that contains additional commands to use during Fire & Ice extraction.

Related Text Commands

For information on the following commands, see “RC Extraction Commands” in the *Encounter Text Command Reference.*

- `readCapTable`
- `setRCFactor`
- `setExtractRCMode`
- `setShrinkFactor`

Related Topics

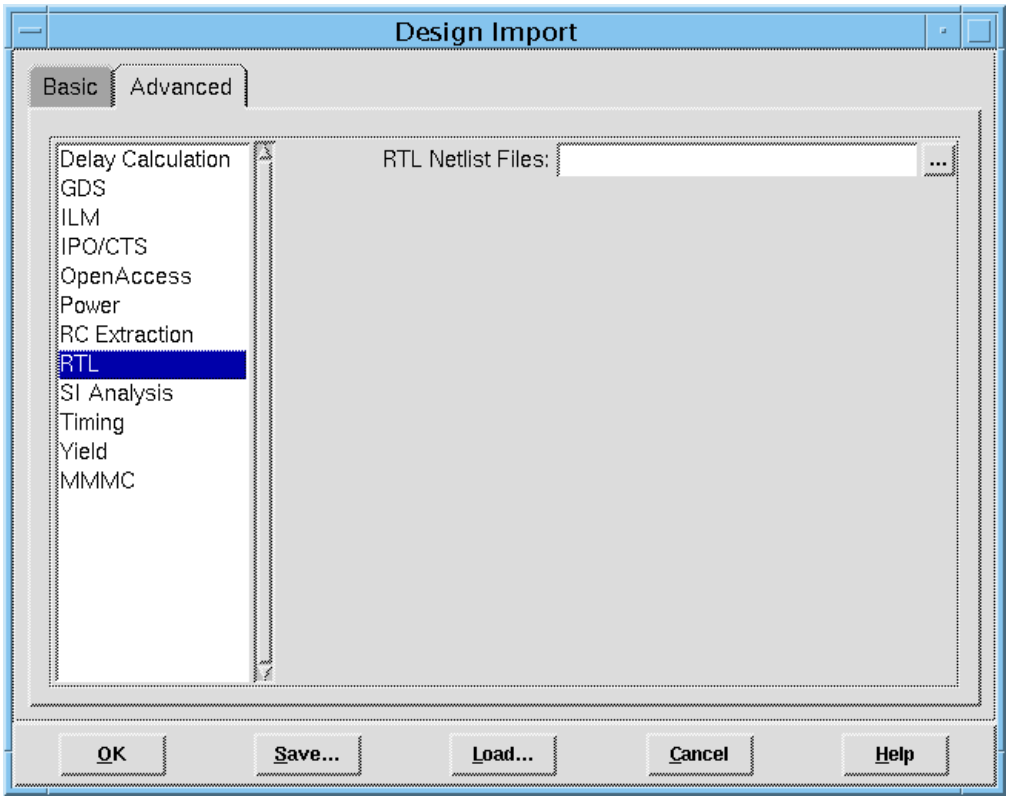
For more information on the following topics, see “RC Extraction” in the *Encounter User Guide*:

- Generating a Capacitance Table
- Capacitance Table Generation Flow
- Reading a Capacitance Table

RTL

Use the *RTL* page of the Design Import form to specify the RTL netlist files.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *RTL*.



RTL Fields and Options

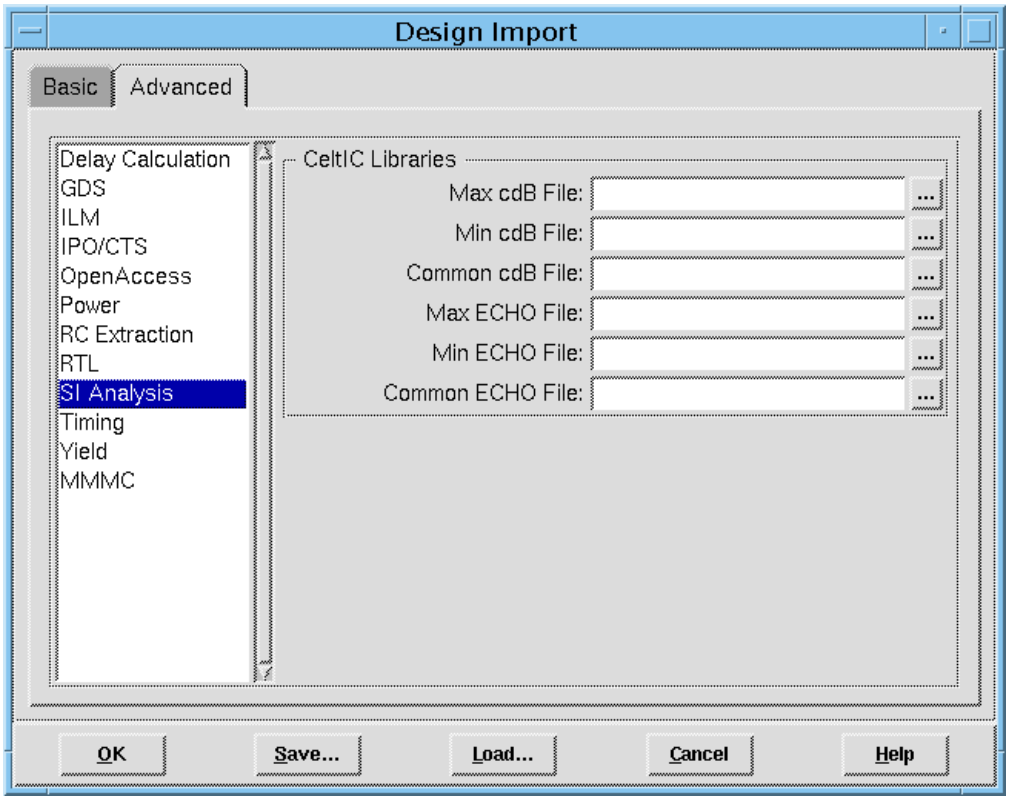
Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

RTL Netlist Files	Specifies the RTL netlist files to import. If specifying multiple names in the text field, use spaces to separate the names. You can also use wildcards (*`*.extension`*) or directory names to specify multiple files.

SI Analysis

Use the *SI Analysis* page of the Design Import form to specify information about CeltIC NDC libraries.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *SI Analysis*.



SI Analysis Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

Max cdB File	Specifies the noise library (cdB) files used in setup analysis mode. In setup analysis mode, the common cdB files and the max cdB files are passed to CeltIC NDC.
Min cdB File	Specifies the noise library (cdB) files used in hold analysis mode. In hold analysis mode, the common cdB files and the min cdB files are passed to CeltIC NDC.

Common cdB File	Specifies the name of the common noise library (cdB) files used in CeltIC NDC analysis.
Max ECHO File	Specifies the ECHO model files used in hold analysis mode. In hold analysis mode, the common ECHO model files and the max ECHO files are passed to CeltIC NDC.
Min ECHO File	Specifies the ECHO model files used in hold analysis mode. In hold analysis mode, the common ECHO model files and the min ECHO files are passed to CeltIC NDC.
Common ECHO File	Specifies the name of the common ECHO noise model files used in CeltIC NDC analysis.

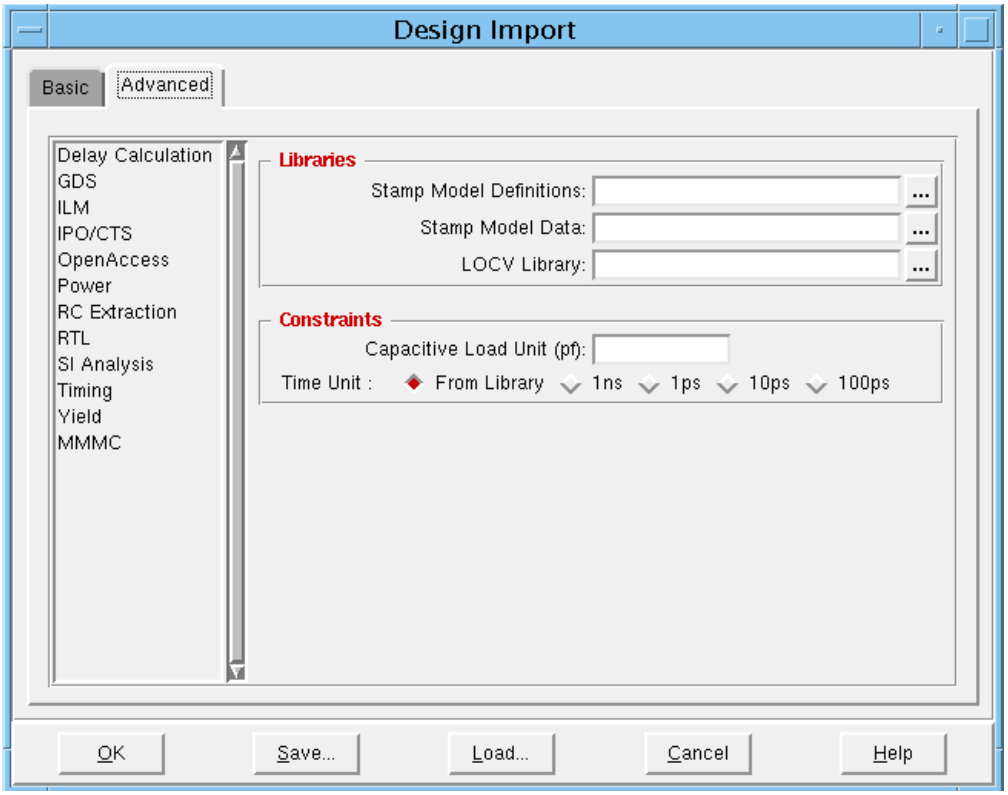
Related Text Commands

- `setSIMode`

Timing

Use the *Timing* page of the Design Import form to specify stamp model and timing constraint information to import into the software.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *Timing*.



Timing Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

Stamp Model Definitions

Specifies the Stamp model definition files.

Stamp model files contain timing information for a module, such as an instantiated module, block, or partitioned module. You do not need to translate these files before reading them into the software. However, currently you can only read in constant value models.

Stamp timing specifications supersede timing information read from the timing library.

Stamp Model Data

Specifies the Stamp model data files.

LOCV Library

Specifies the LOCV library file.

An LOCV library file contains one or more LOCV tables, which are used for determining derating factors for LOCV timing analysis.

You can specify encrypted (binary) LOCV library files.

Capacitive Load Unit (pf)

Specifies the capacitive load unit for objects specific to capacitive load.

If the library files have the same load units, you do not need to specify a value.

Default: The capacitive load unit is assumed to be the one specified in the timing library. If the library files have different load units, specify a value and choose a *Time Unit* option. If you do not specify a value, the default is set to `1.0` pf.

Time Unit

Specifies the time unit to be used for timing constraints.

If the libraries have the same time units, select the *From Library* (default) option. If the libraries have different time units, or require a change, select a new time unit.

Note: These values apply only to timing constraints, and have no effect on the timing library.

Default: The design units in the timing constraints files are based on the units specified in the timing libraries. At times, multiple timing libraries are read in during design import, and the capacitive load units and timing units in these libraries might not be consistent. The *Timing Library Units* panel enables you to explicitly specify the time units for the constraints file.

Related Text Commands

- `loadStampModel`
- `loadTimingCon`
- `read_locvlib`
- `writeTimingCon`

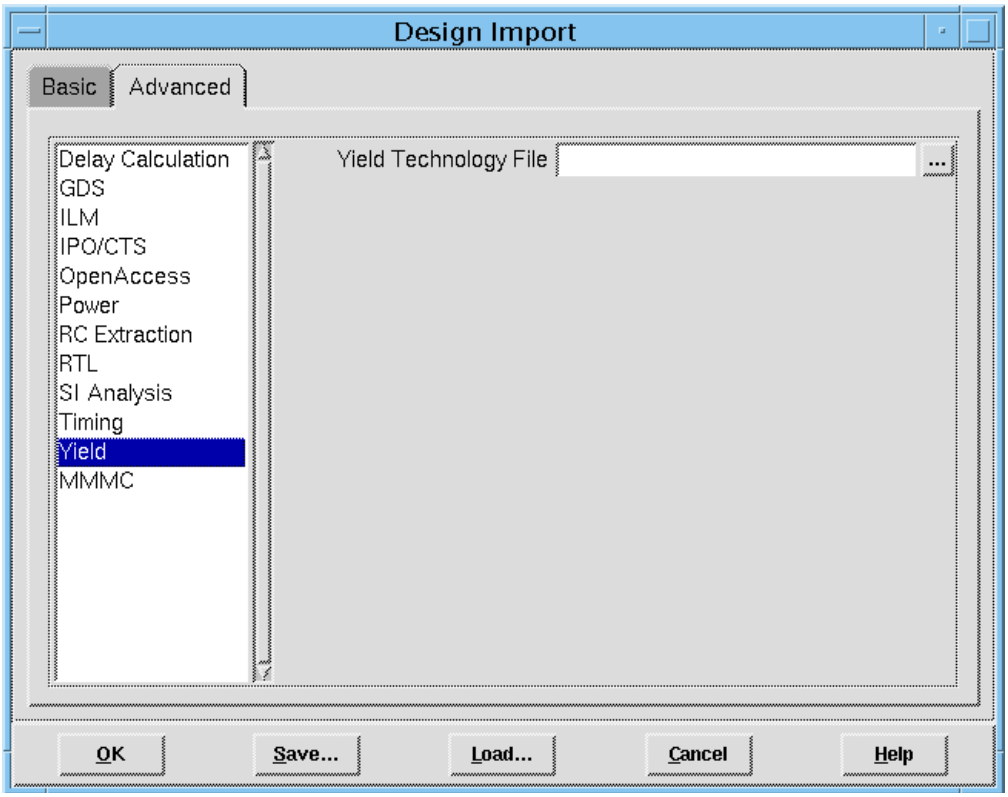
Related Topics

- Preparing Timing Constraints
- Constraints Supported by the writeTimingCon Command

Yield

Use the *Yield* page of the Design Import form to specify a yield file to import into the design. A yield file contains models for calculating the probability of failure of cells, vias, and routing. The Encounter software uses the yield file when it calculates the yield of a particular design.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *Yield*.



Yield Fields and Options

Note: The browse (...) button next to the text field opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

Yield Technology File

Specifies a yield file to import. The file contains yield coefficients for short defects, open defects, via failure rates, and cell failure rates, as supplied by the fab or library vendor. All of the yield data can be supplied by one file, or it can be split among several files. Often the cell yield data is in a separate file from the via and routing yield data.

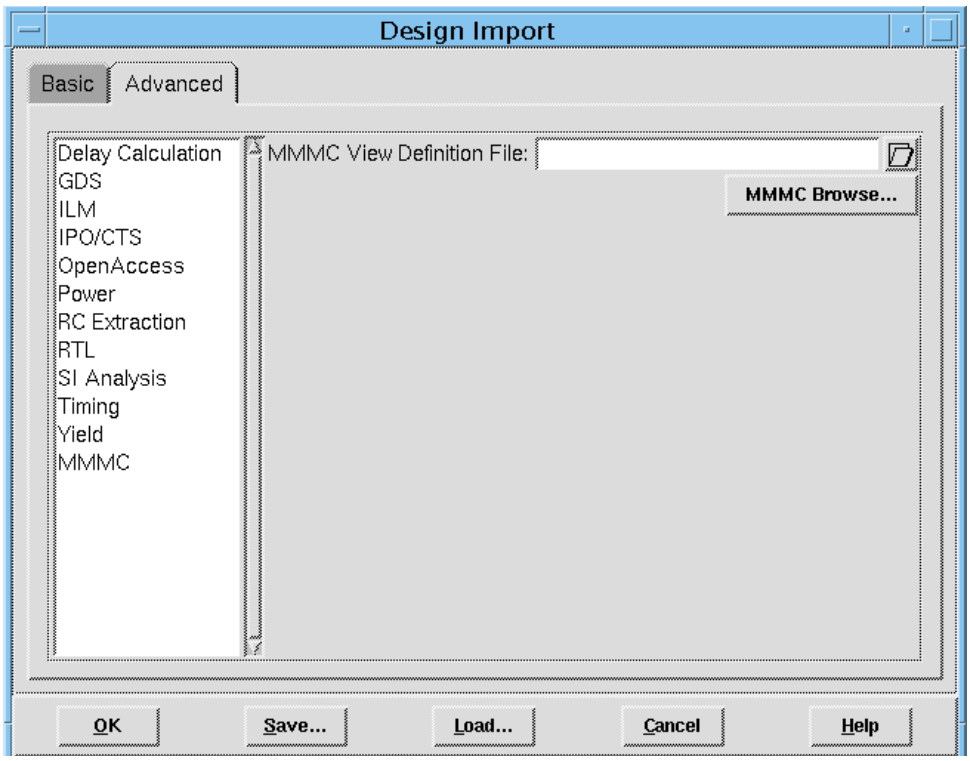
Related Text Commands

- `loadYieldTechFile`

MMMC

Use the *MMMC* page of the Design Import form to load a Tcl command script that contains the analysis view configurations for multi-mode multi-corner timing analysis and optimization.

➤ Choose *Design – Import Design*, click the *Advanced* tab, and select *MMMC*.



Fields and Options

MMMC View Definition File

Specifies a Tcl command script that contains the analysis view configurations for multi-mode multi-corner timing analysis and optimization. The file contains a list of Tcl commands that create library sets, constraint modes, RC corners, delay corners, and analysis views.

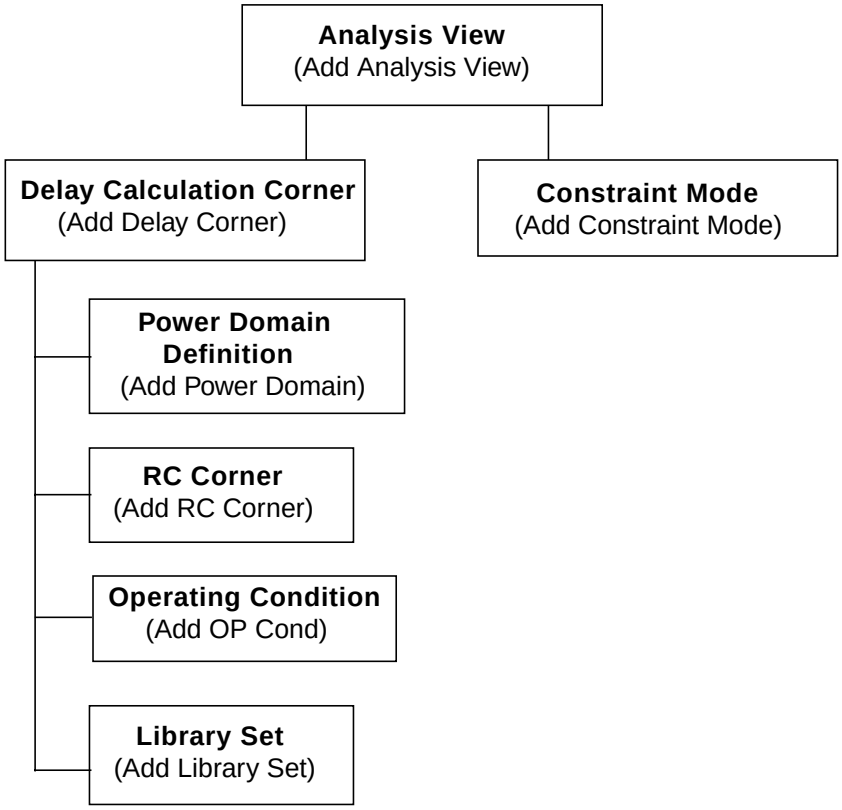
Processing the file does not automatically place the software in multi-mode multi-corner analysis mode. If the file also contains a `set_analysis_view` command, then the software is placed in multi-mode multi-corner analysis mode after the file is processed.

MMMC Browse ... Opens the Multi-Mode Multi-Corner Browser (MMMC Browser). The browser displays the multi-mode multi-corner configuration, and allows you to create and edit the various objects and analysis views necessary for multi-mode multi-corner analysis.

MMMC Browser

Use the MMMC Browser to hierarchically create the view configurations necessary for multi-mode multi-corner analysis. Each top-level set of information is called an analysis view, and is composed of a delay calculation corner and a constraint mode. The active analysis views defined in the software represent the different design variations that will be analyzed.

Figure 2-1 Hierarchical Analysis View Configuration



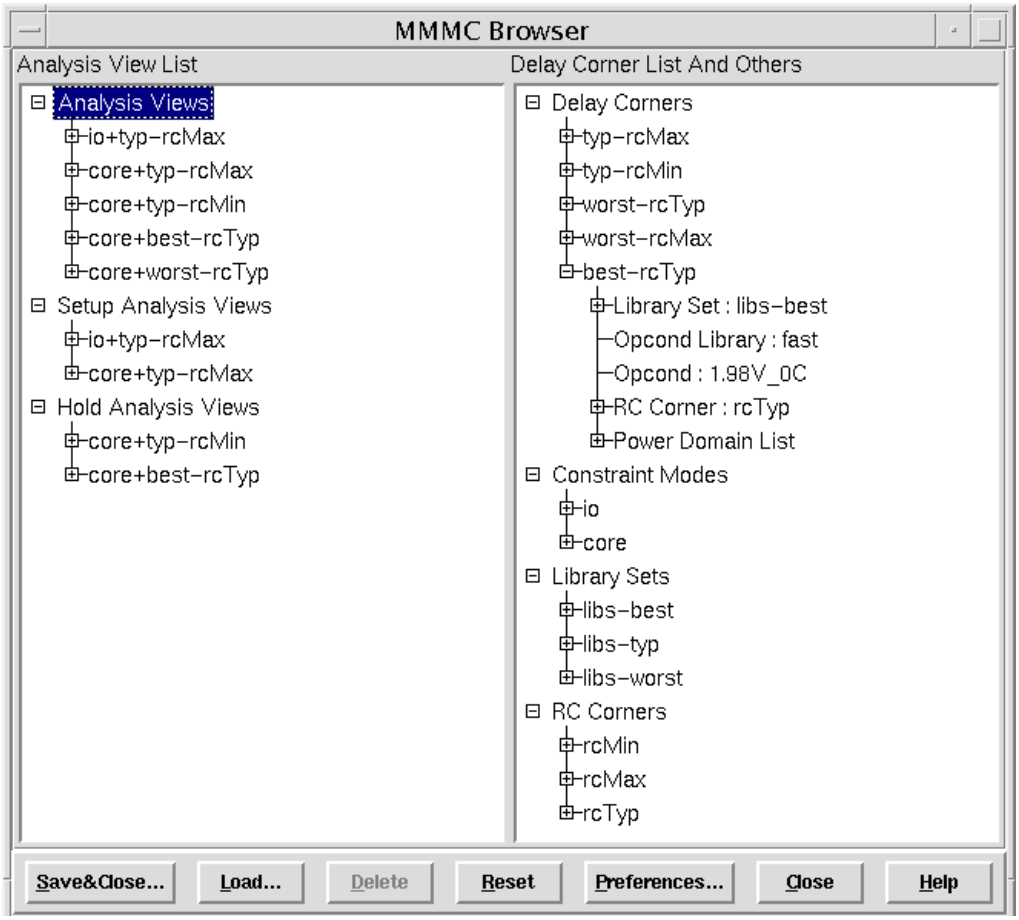
You can access the MMMC Browser from the *Design Import* form, and from the *Timing* menu. Use the MMMC Browser accessed from the *Design Import* form to create a new multi-mode multi-corner configuration for the design. Use the MMMC Browser accessed from the *Timing* menu to add new objects and control analysis views to the existing multi-mode multi-corner configuration that is in memory for the design.

The view configurations that you create are stored as Tcl commands in a view definition file that can then be loaded into the design.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, and click the *MMMC Browse* button.

or

➤ Choose *Timing – Configure MMMC*.



You can access the following forms from the MMMC Browser by double clicking on the generic object or view name:

- Add Library Set on page 142
- Add OP Cond on page 144
- Add RC Corner on page 146
- Add Constraint Mode on page 149
- Add Delay Corner on page 151
- Add Power Domain on page 156
- Add Analysis View on page 160

- Add Hold Analysis View on page 162
- Add Setup Analysis View on page 164

You also can access the following editing forms from the MMMC Browser by double clicking on a specific object name.

- Edit Library Set on page 169
- Edit OP Cond on page 171
- Edit RC Corner on page 173
- Edit Constraint Mode on page 176
- Edit Delay Corner on page 178
- Edit Power Domain on page 181

Note: The editing forms are available only before the multi-mode multi-corner view definition file is loaded into the database. After the software processes the file, the objects can no longer be edited; however, you can still control the selection of active analysis views.

Additionally, you can access the following form to change how the configuration is displayed in the MMMC Browser.

- MMMC Preferences on page 166

Add Library Set

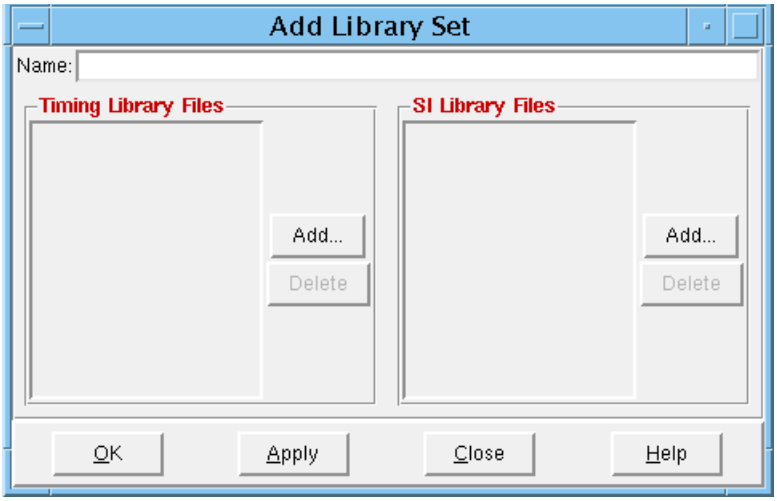
Use the Add Library Set form to associate a list of timing and signal integrity (cdB) libraries with a library set name. Library sets allow a group of library files to be treated as a single entity so that higher-level descriptions (delay calculation corners) can simply refer to the library configuration by name. The same library set can be referenced multiple times by different delay calculation corners.

Note: The order in which you define timing libraries is important. The software considers the first library you specify in the list as the master library, with each successive library having a lower priority.

➤ Choose *Design – Design Import*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Library Sets*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Library Sets*.



Fields and Options

Name	Specifies the name for the library set being created. This name is used to associate the library list with a specific delay calculation corner.
Timing Library Files	Specifies the timing libraries to include in the library set.
SI Library Files	Specifies the cdB libraries to include in the library set. The cdB libraries are required for CeltIC-based signal integrity.

Related Text Commands

- `create library set`
- `get library set`
- `all library sets`

Related Topics

- Creating Library Sets
- Flow Library Requirements

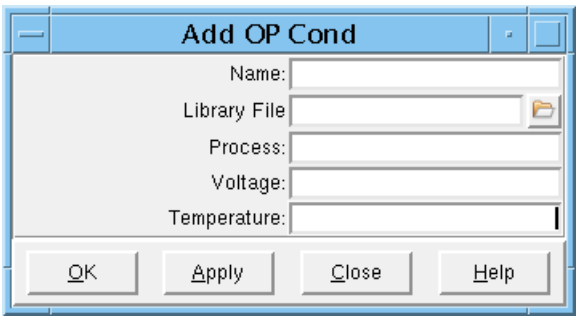
Add OP Cond

Use the Add OP Cond form to create a set of virtual operating conditions in the specified library without actually modifying the library. These virtual operating conditions can then be referenced by a delay calculation corner as if they actually exist in the library.

➤ Choose *Design – Design Import*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *OP Conds*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *OP Conds*.



Fields and Options

Name	Specifies the name for the operating condition being created.
Library File	Specifies the library for which to create the virtual operating conditions.
Process	Specifies the process value for the operating condition.
Voltage	Specifies the voltage value for the operating condition.
Temperature	Specifies the temperature value for the operating condition.

Related Text Commands

- `create_op_cond`
- `get_op_cond`
- `all_op_conds`

Related Topics

Creating Virtual Operating Conditions

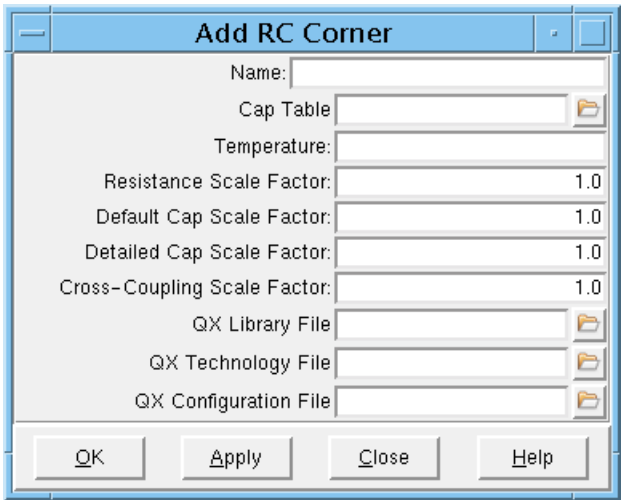
Add RC Corner

Use the Add RC Corner form to create a named RC corner object that can be referenced later when creating a delay calculation corner object. An RC corner object provides the software with all of the information necessary to properly extract, annotate, and use the RCs for delay calculation.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *RC Corners*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *RC Corners*.



Fields and Options

Name	Specifies the name for the RC corner object being created. You can choose any name for an RC corner object, but it is recommended that you use a name that can be easily recognized as referring to a specific RC corner (for example, rc-min, rc-max, c-min, c-max, and so on).
Cap Table	Specifies the capacitance table to use for extraction when using this RC corner. If you do not specify a capacitance table, the software extraction system uses internal rules for extracting resistances and capacitances.

Temperature

Specifies the temperature, in units of Celsius, to use to derate resistance values.

Use this option when you want to override the default temperature specified in the capacitance table.

Note: The software does not require that the temperature specified by the PVT operating condition at the delay calculation corner level be the same as the RC nominal or user-specified temperature value.

If you do not specify a temperature, the Encounter extraction system uses the default temperature of 25 degrees Celsius, unless it is overridden by the capacitance table itself.

Resistance Scale Factor

Specifies the resistance scale factor for correlation.

Default: `1.0`

Default Cap Scale Factor

Specifies the capacitance scale factor for RC extraction in default mode.

Default: `1.0`

Detailed Cap Scale Factor

Specifies the capacitance scale factor for RC extraction in detailed mode.

Default: `1.0`

Cross-Coupling Scale Factor

Specifies the cross-coupling capacitance scale factor.

Default: `1.0`

QX Library File

Specifies the name of the cell library file used by Fire & Ice extraction to perform sign-off RC extraction. You can either specify an existing library filename, or use the `runLibGen` command to generate a library file.

QX Technology File

Specifies the name of an IceCaps technology (`.tch`) file used by Fire & Ice extraction to perform sign-off RC extraction.

The technology file is generated by IceCaps, a built-in functionality of Fire & Ice. For most technologies you can get this file from the technology vendors such as TSMC and UMC. For technologies that are not available through the technology vendors, you enter the fabrication process information into an ASCII-format interconnect technology (ICT) input file. The ICT file is then used as input to IceCaps, which in turn generates the technology file.

For more information on creating the ICT files, see Appendix A "Creating the ICT File", in the *Encounter User Guide*.

QX Configuration File

Specifies the name of a user-created configuration file to use with Fire & Ice® QX gate-level extraction. Use Fire & Ice when you want to perform sign-off RC extraction.

The configuration file contains commands and variables that define the extraction environment (technology filename, library name, and so on), specifies the net(s) to extract and how to extract them, controls the resistance and capacitance extraction, and specifies the extraction outputs.

Related Text Commands

- `create_rc_corner`
- `get_rc_corner`
- `all_rc_corners`

Related Topics

- Creating RC Corner Objects
- Creating Pre-Scaled Capacitance Tables

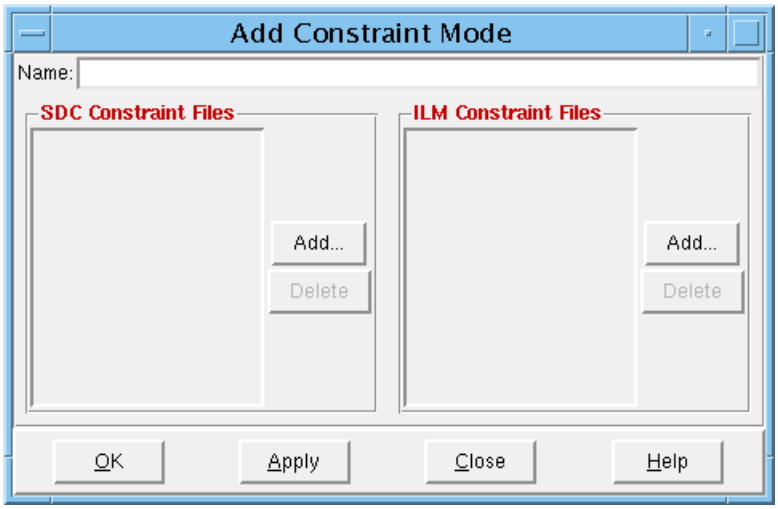
Add Constraint Mode

Use the Add Constraint Mode form to associate a list of SDC constraint files with a specified constraint mode name. This constraint mode name can be referred to later when creating analysis views. A constraint mode defines one of possibly many different functional, test behaviors, or Dynamic Voltage and Frequency Scaling (DVFS) modes of a design. SDC files can be shared by many different constraint modes, and the same constraint mode can be associated with multiple analysis views.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Constraint Modes*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Constraint Modes*.



Fields and Options

Name	Specifies the name of the mode to be created.
SDC Constraint Files	Specifies a list of SDC files to be included in the mode.
ILM Constraint Files	Specifies a list of ILM constraint files to be included in the mode.

Related Text Commands

■ `create_constraint_mode`

- `get_constraint_mode`
- `all_constraint_modes`

Related Topics

- Creating Constraint Mode Objects
- Constraint Support in Multi-Mode and Multi-Mode Multi-Corner Analysis

Add Delay Corner

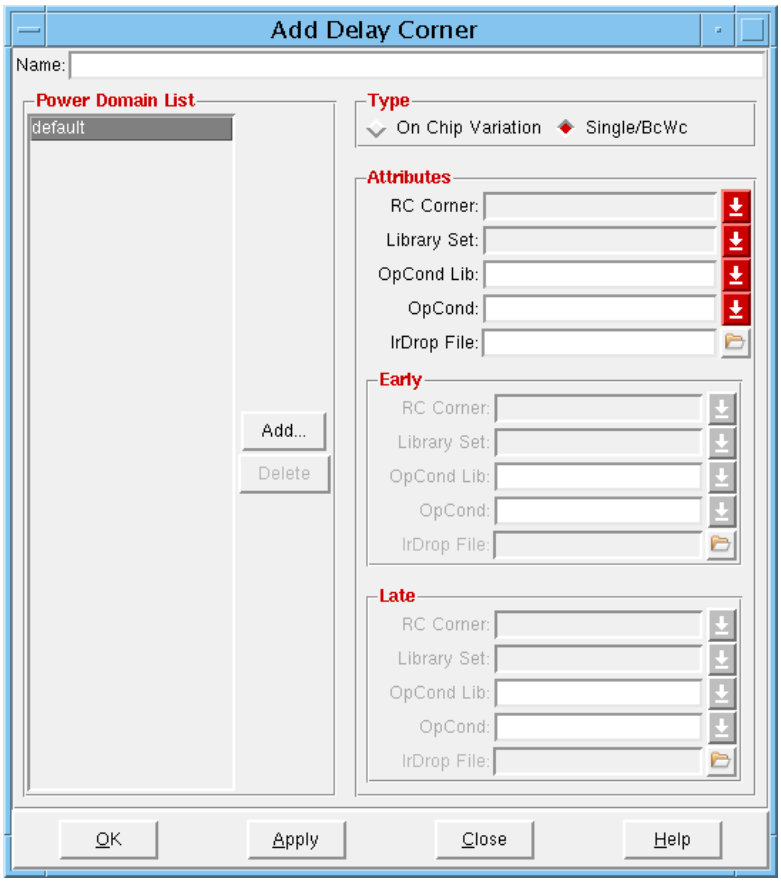
Use the Add Delay Corner form to create a named delay calculation corner object that can be referenced later when creating an analysis view. A delay calculation corner provides all of the information necessary to control delay calculation for a specific view. Each corner contains information on the libraries to use, the operating conditions with which the libraries should be accessed, and the RC extraction parameters to use for calculating parasitic data. Delay corner objects can be shared by multiple top-level analysis views.

Note: A single delay calculation corner object specifies the delay calculation rules for the entire design. If a design includes power domains, the delay calculation corner can contain domain-specific subsections that specify the required operating condition information, and any necessary timing library rebinding for the power domain. Use the Add Power Domain form to add a power domain definition to a delay calculation corner.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Delay Corners*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Delay Corners*.



Fields and Options

Name	Specifies the name for the delay calculation corner object being created.
Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a delay calculation corner generally contains one library set and one RC corner object. When running on-chip-variation timing analysis, a delay calculation corner can contain early and late library sets and RC corners. **Note:** If you use a delay calculation corner containing early and late attributes when the software is in BC-WC mode, the software uses the early information for analysis of hold views, and the late information for the analysis of setup views.
RC Corner	Specifies the RC corner object to associate with this delay calculation corner object.
Library Set	Specifies the library set to associate with this delay calculation corner object.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the library set for the specified operating condition (`-opcond`), starting with the master library.
OpCond	Specifies the operating condition to use for setup and hold analysis. If you do not specify an operating condition, each library in the library set uses its own default operating condition.
Ir Drop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.
Early RC Corner	**Note:** The 6.2 version of the Encounter software does not support the use of early and late RC corners; therefore, this field is disabled. Specifies the RC corner object to associate with this delay calculation corner object for calculating early arrival times at a single delay corner.

Early Library Set	Specifies the library set to associate with this delay calculation corner object for calculating early arrival times at a single delay corner.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the early library set for the specified operating condition (*Early OpCond*), starting with the master library.
Early OpCond	Specifies the operating condition to use for calculating early arrival times at a single delay corner. If you do not specify an operating condition, each library in the early library set uses its own default operating condition.
Early IR Drop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.
Late RC Corner	**Note:** The 6.2 version of the Encounter software does not support the use of early and late RC corners; therefore, this field is disabled. Specifies the RC corner object to associate with this delay calculation corner object for calculating late arrival times at a single delay corner.
Late Library Set	Specifies the library set to associate with this delay calculation corner object for calculating late arrival times at a single delay corner.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the late library set for the specified operating condition (*Late OpCond*), starting with the master library.
Late OpCond	Specifies the operating condition to use for calculating late arrival times at a single delay calculation corner. If you do not specify an operating condition, each library in the late library set uses its own default operating condition.
Late IR Drop File	Specifies the IR drop files to apply when calculating late arrival times at a single delay corner.

Power Domain List

Displays a list of the delay calculation corner's power domain definitions.

To add a power domain definition to the delay corner, click the *Add* button to open the Add Power Domain form. To delete a power domain definition from the delay corner, choose the power domain in the list and click the *Delete* button.

Related Text Commands

- `create_delay_corner`
- `get_delay_corner`
- `all_delay_corners`
- `update_delay_corner`

Related Topics

- Creating Delay Calculation Corner Objects
- Adding A Power Domain Definition To A Delay Calculation Corner

Add Power Domain

Use the Add Power Domain form to add a power domain definition to the specified delay calculation corner. Instances contained within an MSMV power domain often require a different library or operating condition that used for the default power domain. Power domain definitions within a delay calculation corner object can be used to assign specific libraries and PVT settings per power domain.

Note: Use separate delay calculation corners to define Best-Case Worst-Case differences. Use the *Early* and *Late* options within a single delay calculation corner to control on-chip-variation.

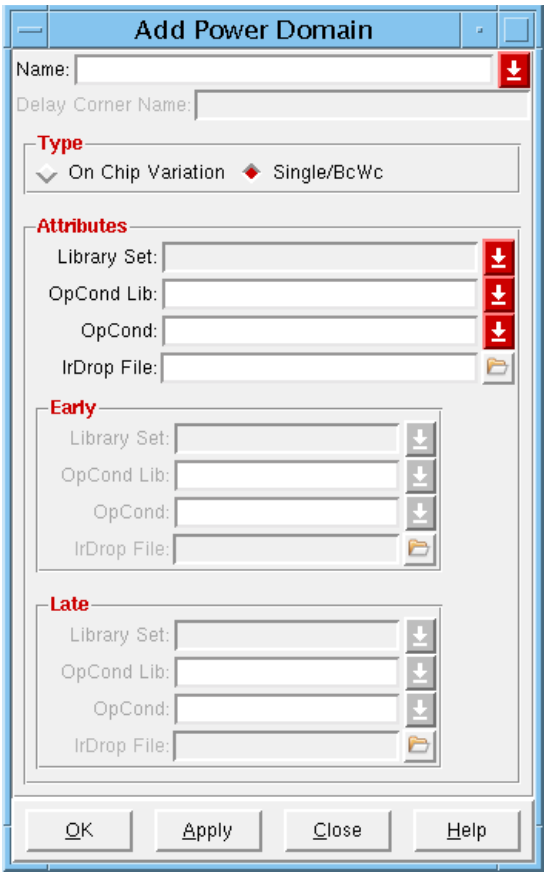
Important

You must use the same power domain names that you intend to specify when using the `createPowerDomain` command to define the physical aspects of the domain.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Power Domains*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Power Domains*.



Fields and Options

Name	Specifies the name of the power domain to add to the delay calculation corner. This name must match the name of a power domain specified with the `createPowerDomain` command.
Delay Corner Name	Displays the name of the delay calculation corner to which the power domain definition is being added.

Type

Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment.

When running Single or Best-Case Worst-Case (BcWc) timing analysis, a power domain generally contains one library set and operating condition. When running on-chip-variation timing analysis, a power domain can contain early and late library sets and operating conditions.

Note: When the software is not in multi-mode multi-corner mode, the binding of timing libraries and operating conditions to power domains are specified using `createPowerDomain -minTimingLibs` and `-maxTimingLibs`, and `setOpCond -powerDomain` parameters. When the software is in multi-mode multi-corner mode, this use model is disabled.

Library Set

Specifies the library set to associate with the power domain. All of the cells and macros in the power domain get their timing and power information from these libraries.

OpCond Lib

Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name.

If you do not specify a library name, the software searches the library set for the specified operating condition (*OpCond*), starting with the master library.

OpCond

Specifies the operating condition to use for the power domain.

If you do not specify an operating condition, each library in the library set uses its own default operating condition.

IR Drop File

Specifies the IR drop files to apply to both early and late delay calculation for this power domain object.

Early Library Set

Specifies the library set to associate with the power domain for calculating early arrival times for this power domain.

Early OpCond Lib

Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name.

If you do not specify a library name, the software searches the early library set for the specified operating condition (*Early OpCond*), starting with the master library.

Early OpCond	Specifies the operating condition to use for calculating early arrival times for this power domain. *Default:* If you do not specify an operating condition, each library in the early library set uses its own default operating condition.
Early IR Drop File	Specifies the IR drop files to apply when calculating early arrival times at a single power domain.
Late Library Set	Specifies the library set to associate with this delay corner object for calculating late arrival times for this power domain.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name. If you do not specify a library name, the software searches the late library set for the specified operating condition (*Late OpCond*), starting with the master library.
Late OpCond	Specifies the operating condition to use for calculating late arrival times for this power domain. *Default:* If you do not specify an operating condition, each library in the late library set uses its own default operating condition.
Late IR Drop File	Specifies the IR drop files to apply when calculating late arrival times at a single power domain.

Related Text Commands

- `update delay corner`

Related Topics

- Adding A Power Domain Definition To A Delay Calculation Corner

Add Analysis View

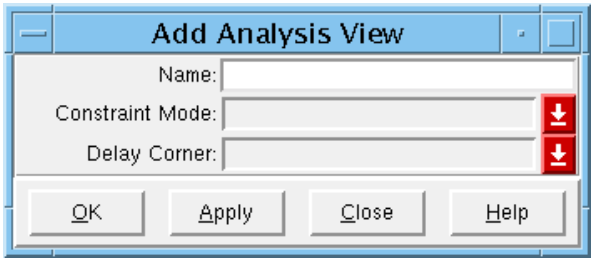
Use Creates an analysis view object that associates a delay calculation corner with a constraint mode An analysis view object provides all of the information necessary to control a given multi-mode multi-corner analysis.

After creating analysis view objects, use Add Hold Analysis View and Add Setup Analysis View forms to specify which views to use for setup and hold optimization or timing analysis.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Analysis Views*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Analysis Views*.



Fields and Options

Name	Specifies the name of the analysis view being defined.
Constraint Mode	Specifies the name of the constraint mode to associate with this analysis view. A constraint mode groups a set of constraints to be used with any given analysis. To create a constraint mode, use the Add Constraint Mode form.
Delay Corner	Specifies the name of the delay calculation corner object to associate with this analysis view. A delay calculation corner object contains all of the information needed to control delay calculation for a specific analysis view. To create a delay calculation corner, use the Add Delay Corner form.

Related Text Commands

■ `create_analysis_view`

- `get_analysis_view`
- `all_analysis_views`

Related Topics

- Creating Analysis Views

Add Hold Analysis View

Use the Add Hold Analysis View form to define the analysis views to use for hold analysis and optimization. These “active” views represent the different design variations that will be analyzed. Active views can be changed throughout the flow to utilize different subsets of views. Encounter applications can handle the views concurrently, sequentially, or in a distributed manner, depending on their individual capabilities. Libraries and data are loaded into the system, as required to support the selected set of active views. You must define at least one setup and one hold analysis view in a multi-mode multi-corner configuration.

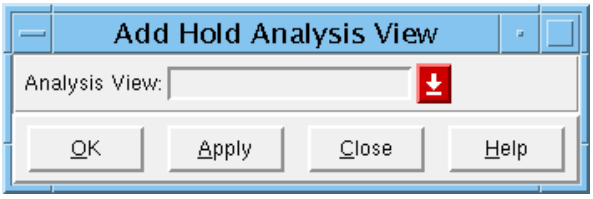
The order in which you specify hold views is important. By default, the first view defined is the default hold view. Certain Encounter applications that do not support multi-mode multi-corner can only process the data defined for a single view. These applications use the information defined for the default view.

Note: Use the `set_default_view` command, if you want to change the default analysis view. Using the `set_default_view` command does not affect software performance because it only uses views that are already active in the design. If you use the Add Hold Analysis View form to change the default views, the existing timing, delay calculation, and RC data is reset.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Hold Analysis Views*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Hold Analysis Views*.



Fields and Options

Analysis View	Specifies the active view for hold analysis. Use the Add Hold Analysis View form multiple times to specify more than one active hold analysis view.

Related Text Commands

- `set analysis view`
- `all hold analysis views`

Related Topics

- Setting Active Analysis Views
- Guidelines For Setting Active Analysis Views
- Changing the Default Active Analysis View

Add Setup Analysis View

Use the Add Setup Analysis View form to define which views to use for setup analysis and optimization. These “active” views represent the different design variations that will be analyzed. Active views can be changed throughout the flow to utilize different subsets of views. Encounter applications can handle the views concurrently, sequentially, or in a distributed manner, depending on their individual capabilities. Libraries and data are loaded into the system, as required to support the selected set of active views. You must define at least one setup and one hold analysis view in a multi-mode multi-corner configuration.

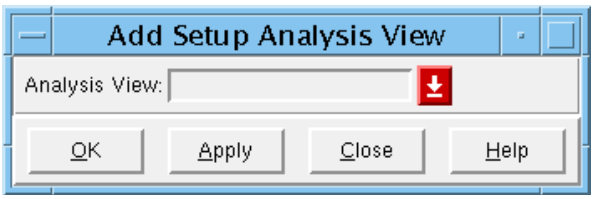
The order in which you specify setup views is important. By default, the first view defined is the default setup view. Certain Encounter applications that do not support multi-mode multi-corner can only process the data defined for a single view. These applications use the information defined for the default view.

Note: Use the `set_default_view` command, if you want to change the default analysis view. Using the `set_default_view` command does not affect software performance because it only uses views that are already active in the design. If you use the Add Setup Analysis View form to change the default views, the existing timing, delay calculation, and RC data is reset.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on *Setup Analysis Views*.

or

➤ Choose *Timing – Configure MMMC*, and double click on *Setup Analysis Views*.



Fields and Options

Analysis View — Specifies the active view for setup analysis. Use the Add Setup Analysis View form multiple times to specify more than one setup analysis view.

Related Text Commands

- `set analysis view`
- `all setup analysis views`

Related Topics

- Setting Active Analysis Views
- Guidelines For Setting Active Analysis Views
- Changing the Default Active Analysis View

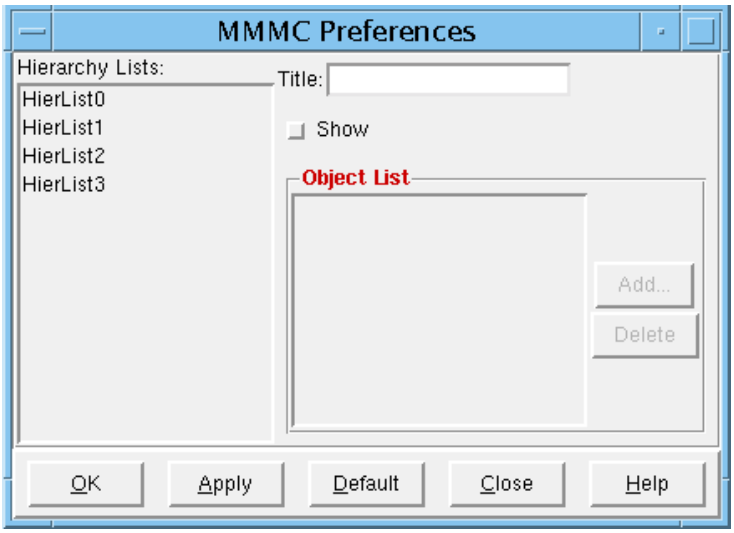
MMMC Preferences

Use the Preferences form to change how the MMMC Browser displays configuration information. By default, the MMMC Browser displays configuration information in two columns. You can change the number of columns displayed, rename the titles of the columns, change which objects are displayed in the columns, and rearrange the order in which the objects are listed.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and click the *Preferences* button.

or

➤ Choose *Timing – Configure MMMC*, and click the *Preferences* button.



Fields and Options

Hierarchy Lists	Lists the four columns that can be displayed, from left to right, in the MMC Browser. When you select a column name in the *Hierarchy Lists* window, the form fields reflect the current settings for that column.
Title	Specifies the name of the selected column.
Show	Enables the display of the selected column in the Browser.

Object List

Lists the objects that are displayed in the selected column.

To add an object to the column, click the *Add* button and choose an object from the drop down list on the Add Object form.

To delete an object from the column, select the object and click the *Delete* button.

Note: You can rearrange the order of the objects in the list. Click and hold the left mouse button on the name of an object, and drag it to a different position in the list.

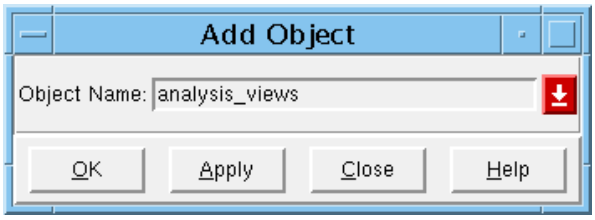
Related Text Commands

There is no equivalent text command for this function. You only can change how the Browser displays the configuration using the MMMC Preferences form.

Add Object

Use the Add Object form to add an object to the list of objects you want displayed for a specific column on the MMMC Browser.

➤ Clock the *Add* button on the Preferences form.



Fields and Options

Object Name	Specifies the object to add to the list.

Related Text Commands

There is no equivalent text command for this function. You only can add an object using the Add Object form.

Edit Library Set

Use the Edit Library Set form to add or delete library files from an existing library set.

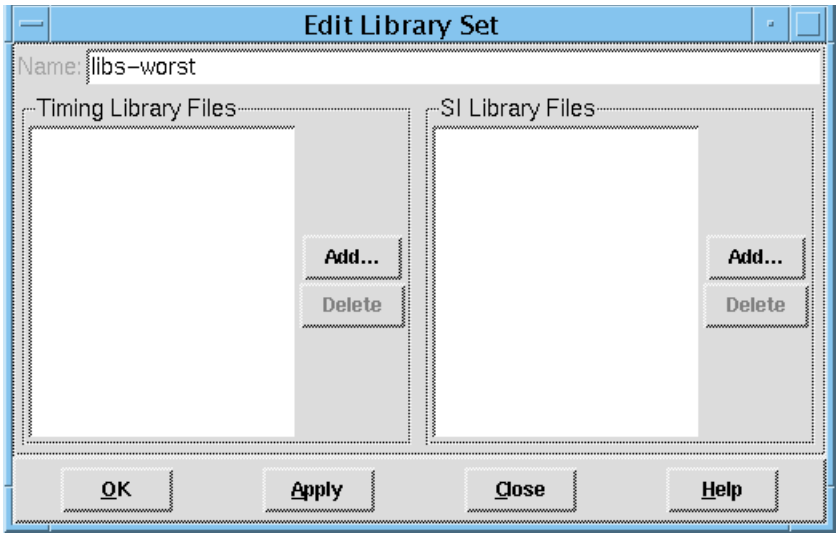
Important

You can edit a library set using the Edit Library Set Form only before the multi-mode multi-corner view definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the library set you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the library set you want to edit.



Fields and Options

Name	Specifies the name of the library set being edited.
Timing Library Files	Displays the timing libraries that are included in the library set. Use the *Add* button to add libraries to the list. Use the *Delete* button to delete libraries from the list.

SI Library Files	Displays the cdB libraries that are included in the library set. Use the *Add* button to add libraries to the list. Use the *Delete* button to delete libraries from the list.

Related Text Commands

- `update library set`

Edit OP Cond

Use the Edit OP Cond form to add, delete, or change attributes for an existing operating condition.

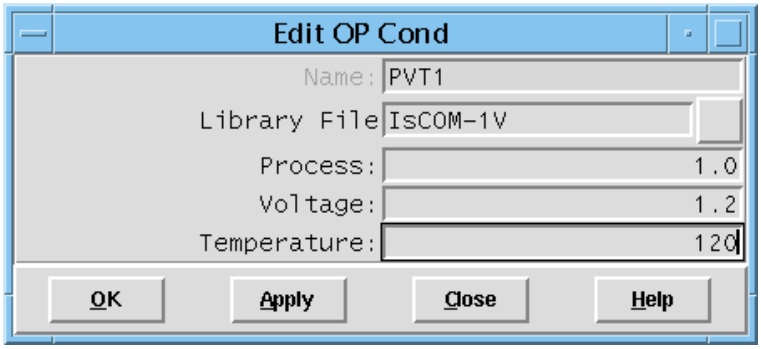
Important

You can edit an operating condition using the Edit Op Cond form only before the multi-mode multi-corner view definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the operating condition you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the operating condition you want to edit.



Fields and Options

Name	Specifies the name of the operating condition being edited.
Library File	Specifies the library with which to associate the virtual operating conditions.
Process	Specifies the process value for the operating condition.
Voltage	Specifies the voltage value for the operating condition.
Temperature	Specifies the temperature value for the operating condition.

Related Text Commands

There is no equivalent text command for this function. You only can edit an operating condition using the Edit OP Cond form.

Edit RC Corner

Use the Edit RC Corner form to add, delete, or change attributes for an existing RC corner object.

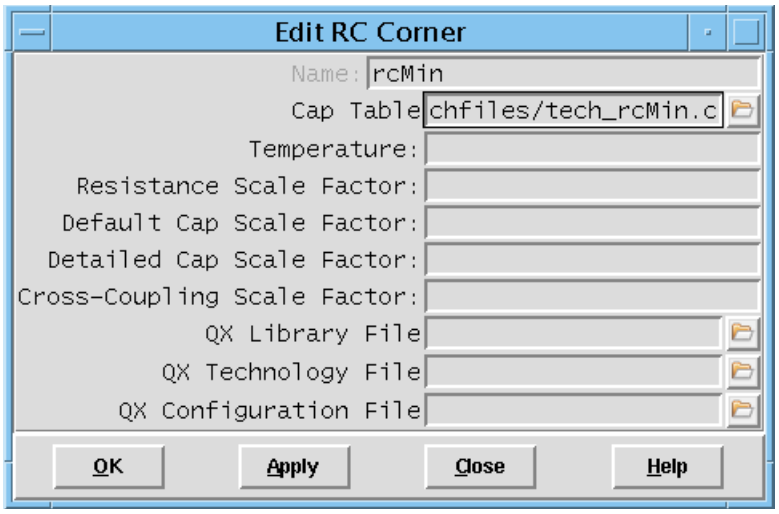
Important

You can edit an RC corner object using the Edit RC Corner form only before the multi-mode multi-corner definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the RC corner object you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the RC corner object you want to edit.



Fields and Options

Name	Specifies the name for the RC corner object being edited.
Cap Table	Specifies the capacitance table to use for extraction when using this RC corner.

Temperature

Specifies the temperature, in units of Celsius, to use to derate resistance values. The software scales resistances based on a nominal temperature of 25 degrees Celsius.

Use this option when you want to specify a temperature that is different than the device temperature defined in the delay calculation corner operating condition.

Note: The software does not require that the temperature specified by the PVT operating condition at the delay calculation corner level be the same as the RC nominal or user-specified temperature value.

Resistance Scale Factor

Specifies the resistance scale factor for correlation.

Default Cap Scale Factor

Specifies the capacitance scale factor for RC extraction in default mode.

Detailed Cap Scale Factor

Specifies the capacitance scale factor for RC extraction in detailed mode.

Cross-Coupling Scale Factor

Specifies the cross-coupling capacitance scale factor.

QX Library File

Specifies the name of the cell library file used by Fire & Ice extraction to perform sign-off RC extraction. You can either specify an existing library filename, or use the `runLibGen` command to generate a library file.

QX Technology File

Specifies the name of an IceCaps technology (`.tch`) file used by Fire & Ice extraction to perform sign-off RC extraction.

The technology file is generated by IceCaps, a built-in functionality of Fire & Ice. For most technologies you can get this file from the technology vendors such as TSMC and UMC. For technologies that are not available through the technology vendors, you enter the fabrication process information into an ASCII-format interconnect technology (ICT) input file. The ICT file is then used as input to IceCaps, which in turn generates the technology file.

For more information on creating the ICT files, see Appendix A "Creating the ICT File", in the *Encounter User Guide*.

QX Configuration File

Specifies the name of a user-created configuration file to use with Fire & Ice® QX gate-level extraction. Use Fire & Ice when you want to perform sign-off RC extraction.

The configuration file contains commands and variables that define the extraction environment (technology filename, library name, and so on), specifies the net(s) to extract and how to extract them, controls the resistance and capacitance extraction, and specifies the extraction outputs.

Related Text Commands

- `update_rc_corner`

Edit Constraint Mode

Use the Edit Constraint Mode form to add or delete SDC constraint files from an existing constraint mode object.

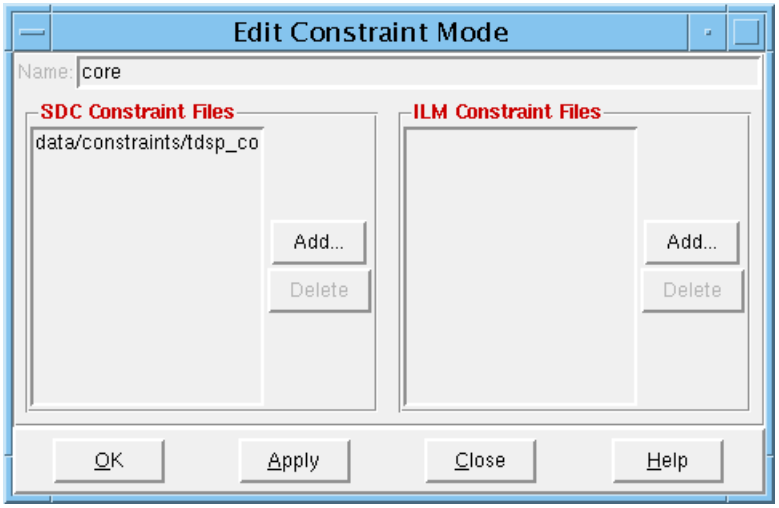
Important

You can edit a constraint mode object using the Edit Constraint Mode form only before the multi-mode multi-corner definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the constraint mode object you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the constraint mode object you want to edit.



Fields and Options

Name	Displays the name of the constraint mode object being edited.
SDC Constraint Files	Displays the SDC constraint files that are associated with the constraint mode object. Use the *Add* button to add SDC files to the list. Use the *Delete* button to delete SDC files from the list.

ILM Constraint Files Displays the SDC constraint files for the ILM flow that are associated with the constraint mose object. Use the *Add* button to add SDC files to the list. Use the *Delete* button to delete SDC files from the list.

Related Text Commands

- `update_constraint_mode`

Edit Delay Corner

Use the Edit Delay Corner form to add, delete, or change attributes for an existing delay calculation corner object.

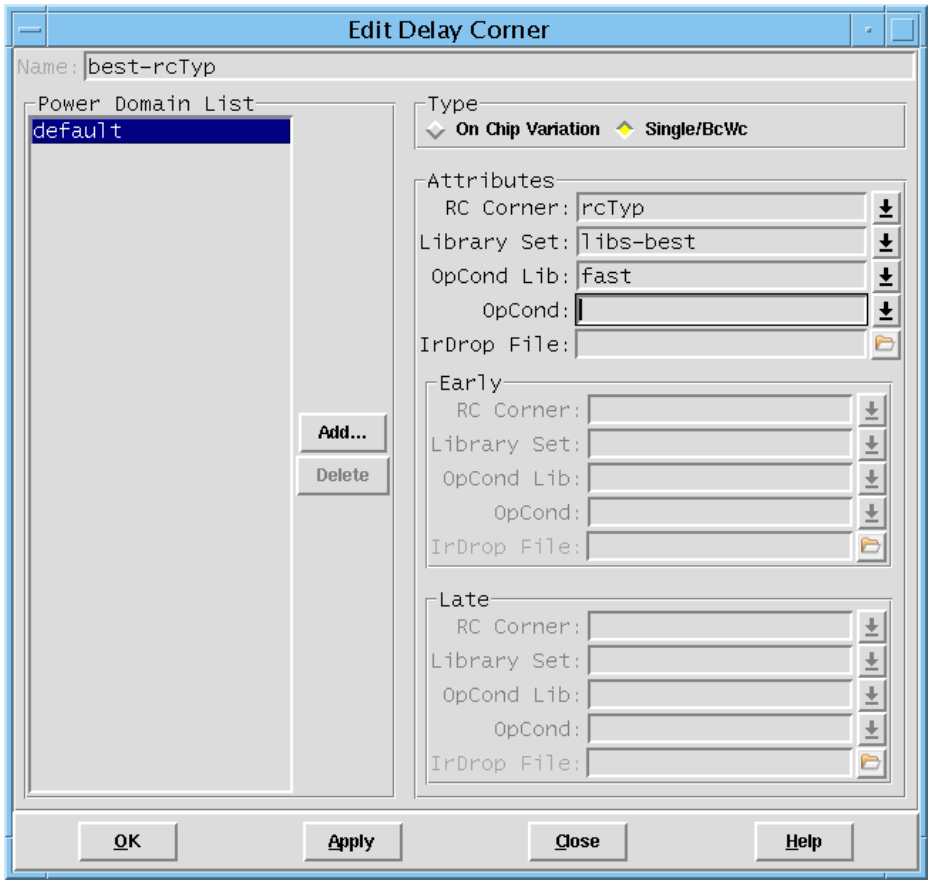
Important

You can edit a delay calculation corner object using the Edit Delay Corner form only before the multi-mode multi-corner definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the delay calculation corner you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the delay calculation corner you want to edit.



Fields and Options

Name	Displays the name for the delay calculation corner object being edited.
Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a delay calculation corner generally contains one library set and one RC corner object. When running on-chip-variation timing analysis, a delay calculation corner can contain early and late library sets and RC corners. **Note:** If you use a delay calculation corner containing early and late attributes when the software is in BC-WC mode, the software uses the early information for analysis of hold views, and the late information for the analysis of setup views.
RC Corner	Specifies an RC corner object to associate with this delay calculation corner object.
Library Set	Specifies a library set to associate with this delay calculation corner object.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name.
OpCond	Specifies an operating condition to use for setup and hold analysis.
IR Drop File	Specifies the IR drop files to apply to both early and late delay calculation for this delay corner object.
Early RC Corner	**Note:** The 7.1 version of the Encounter software does not support the use of early and late RC corners; therefore, this field is disabled. Specifies an RC corner object to associate with this delay calculation corner object for calculating early arrival times at a single delay calculation corner.
Early Library Set	Specifies a library set to associate with this delay calculation corner object for calculating early arrival times at a single delay calculation corner.

Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name.
Early OpCond	Specifies an operating condition to use for calculating early arrival times at a single delay calculation corner.
Early IR Drop File	Specifies the IR drop files to apply when calculating early arrival times at a single delay corner.
Late RC Corner	**Note:** The 7.1 version of the Encounter software does not support the use of early and late RC corners; therefore, this field is disabled. Specifies an RC corner object to associate with this delay calculation corner object for calculating late arrival times at a single delay corner.
Late Library Set	Specifies a library set to associate with this delay calculation corner object for calculating late arrival times at a single delay calculation corner.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name.
Late OpCond	Specifies an operating condition to use for calculating late arrival times at a single delay calculation corner.
Late IR Drop File	Specifies the IR drop files to apply when calculating late arrival times at a single delay corner.
Power Domain List	Displays a list the delay calculation corner's power domain definitions. To add a power domain definition to the delay calculation corner, click the *Add* button to open the Add Power Domain form. To delete a power domain definition from the delay calculation corner, choose the power domain in the list and click the *Delete* button.

Related Text Commands

- `update delay corner`

Edit Power Domain

Use the Edit Power Domain form to add, delete, or change attributes for an existing power domain definition.

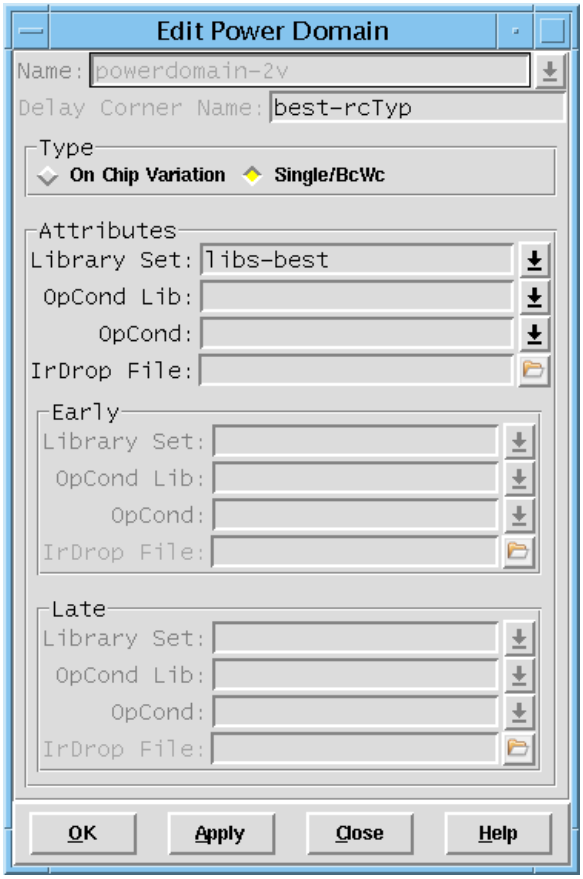
Important

You can edit a power domain using the Edit Power Domain form only before the multi-mode multi-corner definition file is loaded into the design. After the software processes the file, this form is no longer available.

➤ Choose *Design – Import Design*, click the *Advanced* tab, select *MMMC*, click the *MMMC Browse* button, and double click on the name of the power domain definition you want to edit.

or

➤ Choose *Timing – Configure MMMC*, and double click on the name of the power domain definition you want to edit.



Fields and Options

Name	Displays the name of the power domain being edited.
Type	Specifies the type of analysis for which you are configuring the multi-mode multi-corner environment. When running Single or Best-Case Worst-Case (BcWc) timing analysis, a power domain generally contains one library set and operating condition. When running on-chip-variation timing analysis, a power domain can contain early and late library sets and operating conditions. **Note:** When the software is not in multi-mode multi-corner mode, the binding of timing libraries and operating conditions to power domains are specified using `createPowerDomain -minTimingLibs` and `-maxTimingLibs`, and `setOpCond -powerDomain` parameters. When the software is in multi-mode multi-corner mode, this use model is disabled.
Delay Corner Name	Displays the delay calculation corner to which to the power domain definition belongs.
Library Set	Specifies a library set to associate with the power domain. All of the cells and macros in the power domain get their timing and power information from these libraries.
OpCond Lib	Specifies the internal library name for the library in which the operating condition is defined. This is *not* the library file name.
OpCond	Specifies an operating condition to use for the power domain.
IR Drop File	Specifies the IR drop files to apply to both early and late delay calculation for this power domain object.
Early Library Set	Specifies a library set to associate with the power domain for calculating early arrival times at a single delay corner.
Early OpCond Lib	Specifies the internal library name for the library in which the early operating condition is defined. This is *not* the library file name.
Early OpCond	Specifies an operating condition to use for calculating early arrival times at a single delay corner.
Early IR Drop File	Specifies the IR drop files to apply when calculating early arrival times at a single power domain.

Late Library Set	Specifies a library set to associate with this delay corner object for calculating late arrival times at a single delay corner.
Late OpCond Lib	Specifies the internal library name for the library in which the late operating condition is defined. This is *not* the library file name.
Late OpCond	Specifies an operating condition to use for calculating late arrival times at a single delay corner.
Late IR Drop File	Specifies the IR drop files to apply when calculating late arrival times at a single power domain.

Related Text Commands

- `update delay corner`

Import RTL

The RTL Import form lets you specify the files required for importing the files for a design at the register-transfer level.

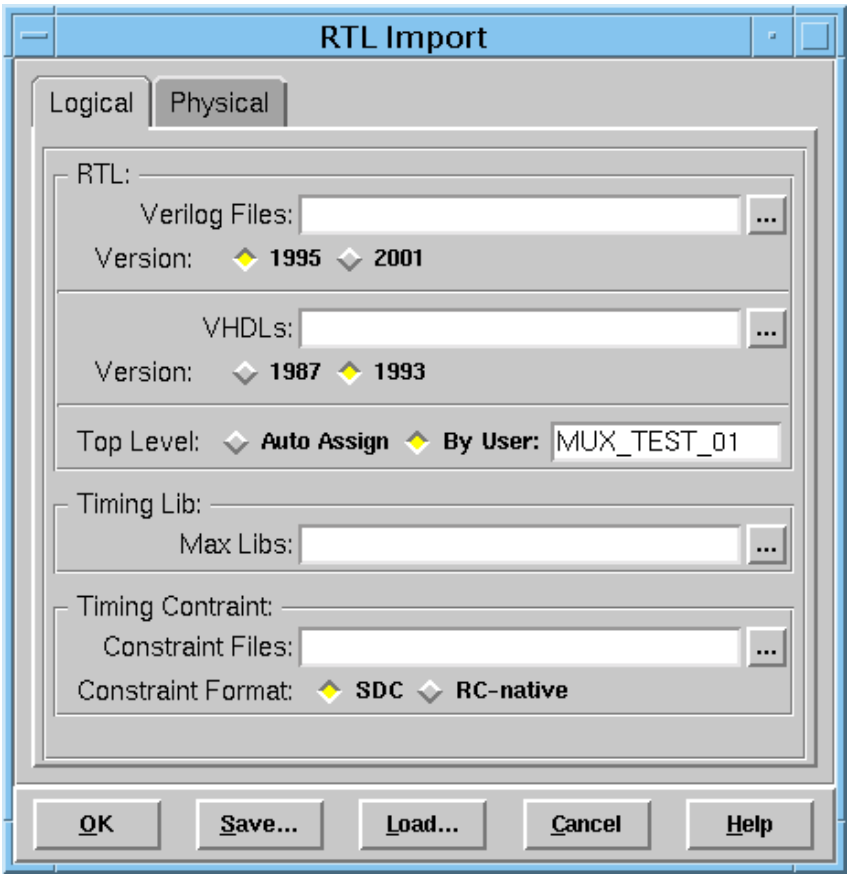
The RTL Import form contains the following pages:

- RTL Import – Logical on page 185
- RTL Import – Physical on page 188

RTL Import – Logical

Use the *Logical* page of the RTL Import form to specify the Verilog® RTL netlist, the timing library, the timing constraints file, and other library files to be imported into the software.

➤ Choose *Design – Import RTL* and click the *Logical* tab.



RTL Import – Logical Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading.

RTL

Specifies the gate-level netlist files to import. Encounter automatically checks whether the netlist is unique, and displays a message accordingly.

If specifying multiple names in the text field, use spaces to separate the names. You can use wildcards (*.*extension*) or directory names to specify multiple files. You can specify compressed files (`.gz` extension).

Verilog Files

Specifies the Verilog netlist files to import.

If specifying multiple names in the text field, use spaces to separate the names. You can also use wildcards (*.*extension*) or directory names to specify multiple files.

Using an ILM netlist normally provides better timing accuracy than using Stamp models.

Version

Specifies the version of Verilog RTL you are using.

Choose either *1995* or *2001*.

VHDLs

Specifies the nested list of VHDL library name, VHDL library directory, and list of VHDL files.

If specifying multiple names in the text field, use spaces to separate the names. You can also use wildcards (*.*extension*) or directory names to specify multiple files.

Version

Specifies version of VHDL RTL you are using.

Choose either *1987* or *1993*.

Top Level:

Specifies the top-level name for the design.

Choose one of the following:

Auto Assign — The top-level design name will be automatically assigned.

By User — Allows you to specify the top-level design name.

Timing Lib:

Max Libs: — Specifies the list of the timing libraries (.lib format) containing worst-case conditions.

Timing Constraints	*Constraint Files*	Specifies the name of the timing constraint files.
	Constraint Format	Specifies the type of constraint files to be used. Choose either *SDC* or *RC-native*.
OK	Caches the entries into corresponding globals.	
Save...	Saves the RTL values into an extended configuration file.	
Load ...	Loads in the extended configuration file and sets the necessary internal global variables. This command does not start any processes.	

Related Text Commands

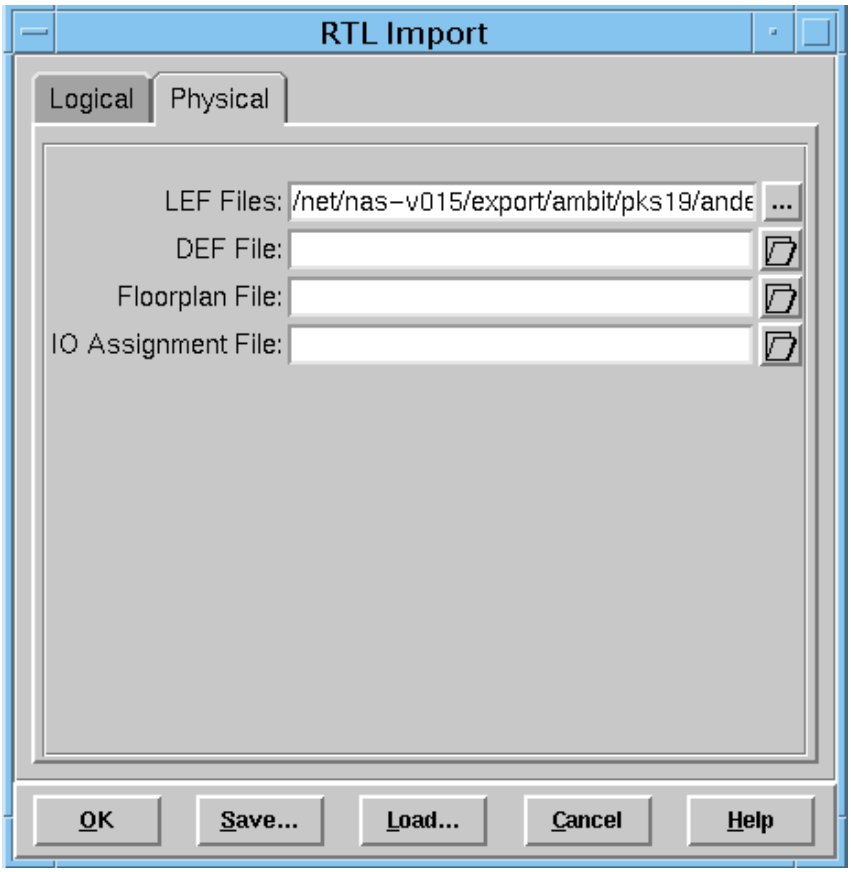
For information on the following commands, see “RTL Synthesis Commands” in the *Encounter Text Command Reference.*

- `loadRTLConfig`
- `saveRTLConfig`

RTL Import – Physical

Use the *Physical* page of the RTL Import form to specify the physical files for the design.

➤ Choose *Design – Import RTL* and click the *Physical* tab.



RTL Import – Physical Fields and Options

Note: The browse (...) button next to the text fields opens a form from which you can load selected files. The form that opens depends on the type of file you are loading. The button with the folder icon opens a form so you can browse to a directory and select the required file for each field.

LEF Files	Specifies the list of LEF files for the design.
DEF File	Specifies the DEF file for the design.
Floorplan File	Specifies the floorplan (.fp) file for the design.
IO Assignment File	Specifies the IO assignment file for the design.

Related Text Commands

For information on the following commands, see “Import Commands” in the *Encounter Text Command Reference.*

- `loadLefFile`
- `loadIoFile`
- `loadDefNetlist`

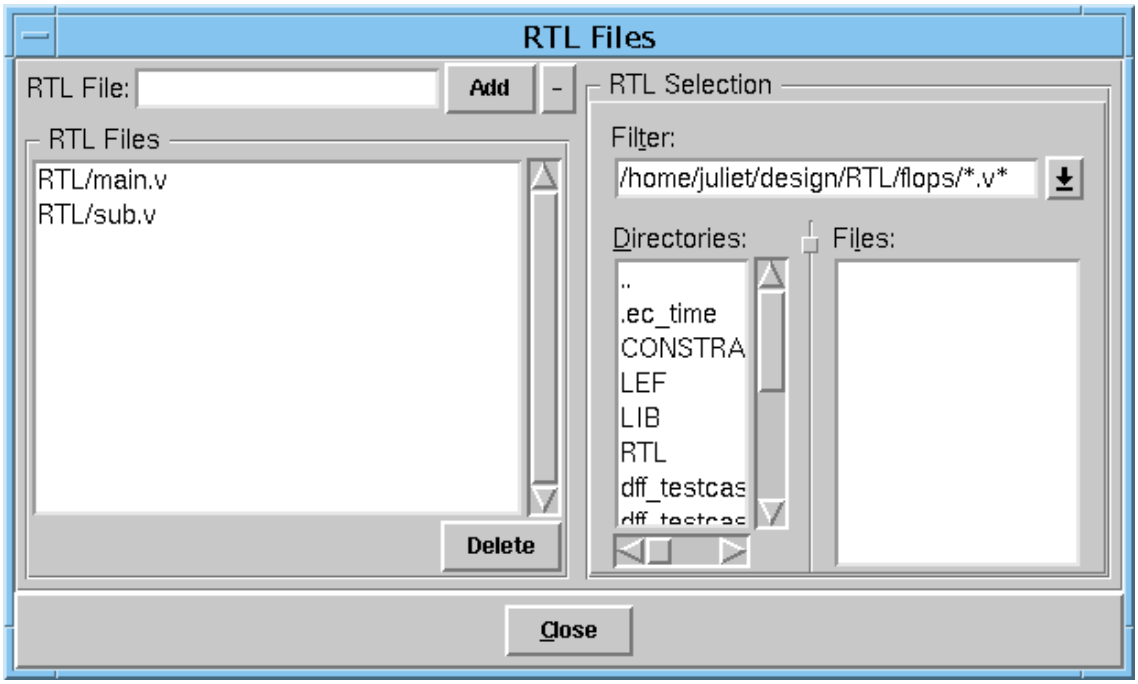
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference.*

- `loadFPlan`

RTL Files

Use the *RTL Files* form to specify the Verilog Files for the design.

1. Choose *Design – Import RTL* and click the *Logical* tab.
2. Click on the browser icon next to the *Verilog Files* field.
3. Click on the icon next to the *Add* button.



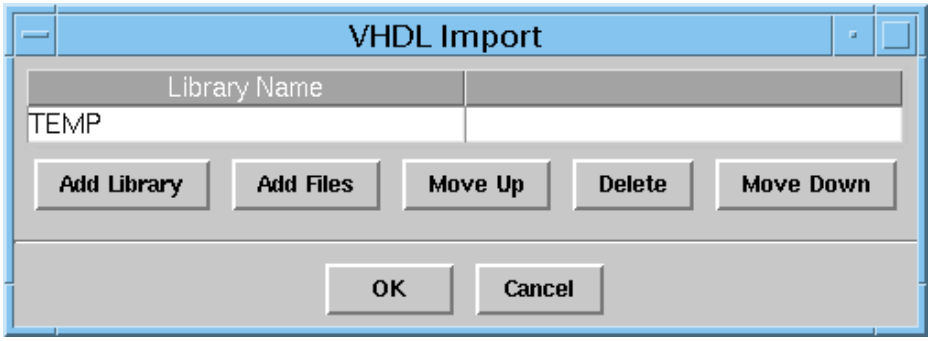
RTL Files Fields and Options

RTL File	Displays the name of the Verilog file to be added.
Filter	Displays the search filter.
Directories	Displays the list of directories to be searched.
Files	Displays the Verilog files in the directory.
Add	Adds the specified file to the list of files to be imported.
Delete	Removes the specified file from the list of files to be imported.

VHDL Import

Use the *VHDL Import* form to specify the VHDL libraries for the design.

1. Choose *Design – Import RTL* and click the *Logical* tab.
2. Click on the browser icon next to the VHDLs field.



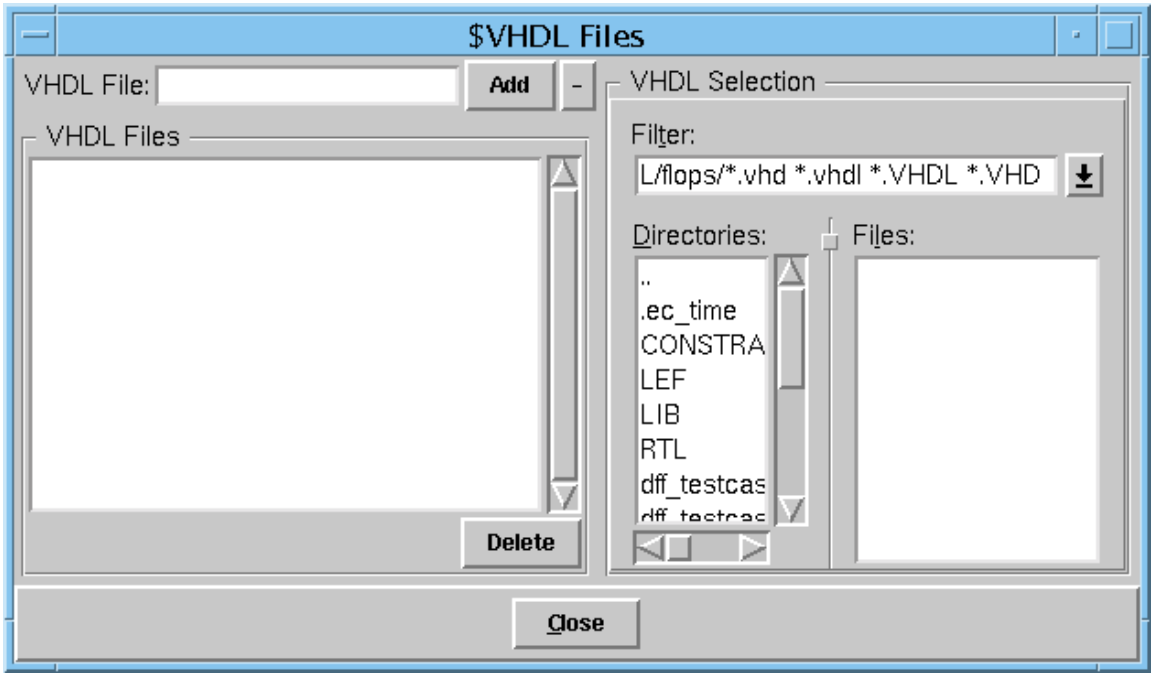
VHDL Import Fields and Options

Library Name	Displays the name of the VHDL library.
Add Library	Displays the Add Library form where you can enter the name of the VHDL library.
Add Files	Displays the VHDL Files form.
Move Up	Moves the selected library up in the list.
Delete	Deletes the selected library.
Move Down	Moves the selected library down in the list.

VHDL Files

Use the *VHDL Files* form to select the VHDL files to be imported.

1. Choose *Design – Import RTL* and click the *Physical* tab.
2. Click on the browser icon next to the VHDLs field.
3. Click on the *Add Files* button.
4. Click on the browser icon next to the *Add* button.



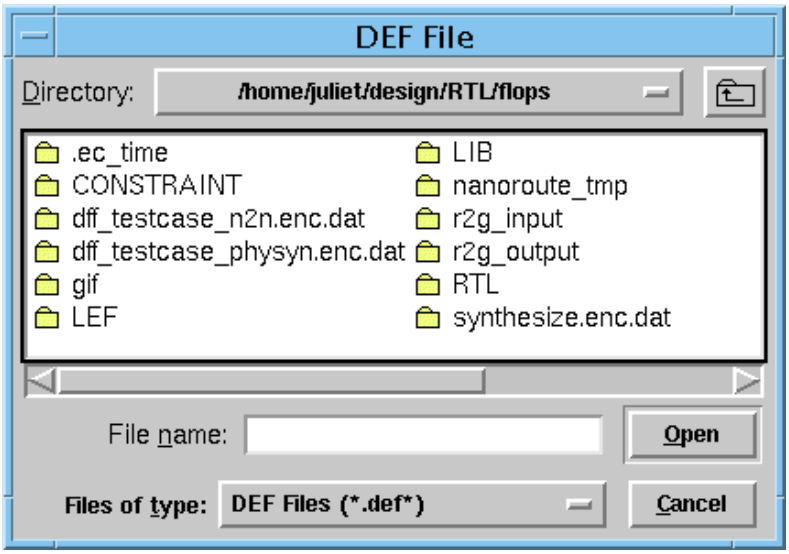
VHDL Files Fields and Options

VHDL File	Displays the name of the VHDL file to be added.
Filter	Displays the search filter.
Directories	Displays the list of directories to be searched.
Files	Displays the VHDL files in the directory.
Add	Adds the specified file to the list of files to be imported.
Delete	Removes the specified file from the list of files to be imported.

DEF File

Use the *DEF File* form to specify the DEF file for the design.

1. Choose *Design – Import RTL* and click the *Physical* tab.
2. Click on the browser icon next to the *DEF File* field.



DEF File Fields and Options

Directory	Displays the name of the directory and the contents.
File name	Displays the name of the selected DEF file.
Open	Opens the selected file.
Files of type	Displays the type of files to be displayed.

Restore Design

The Restore Design menu provides the following forms to restore design information from a previous Encounter session, restore design information using the OpenAccess database format, and to specify ECO design changes.

- Restore Design on page 195
- Restore OA Design on page 196
- ECO Design on page 197

Restore Design

Use the Restore Design form to load saved data from a previous design session.

➤ Choose *Design – Restore Design – SoCE*.

Restore Design Fields and Options

Restore Design File

Specifies the design file to restore.

Sync Relative Path

Synchronizes all relative paths in the configuration file to the current working directory.

Default: Off

With ERROR Line messages

Displays information messages while restoring the design.

Default: Off

With WARN messages

Displays any warning messages while restoring the design.

Default: Off

Related Text Commands

- `restoreDesign`

Related Topics

- Saving and Restoring Designs

Restore OA Design

Use the Restore OA Design form to restore all design information from the previous design session, using the OpenAccess database format.

➤ Choose *Design – Restore Design – OA.*

Restore OA Design Fields and Options

Library	Specifies name of the OpenAccess library where the data is saved.
Cell	Specifies the name of the *Cell* set by the Design – Save OA Design command when you saved the design in the previous session. You cannot change the *Cell* name because this name is specified as the top cell when the design was imported. See Design Import – Advanced – OpenAccess for more information.
View	Specifies the name of the cell view to restore. The values in this field are set by the Save OA Design form when you saved the design in the previous session. *Default:* The layout view.

Related Text Commands

- `restoreOaDesign`

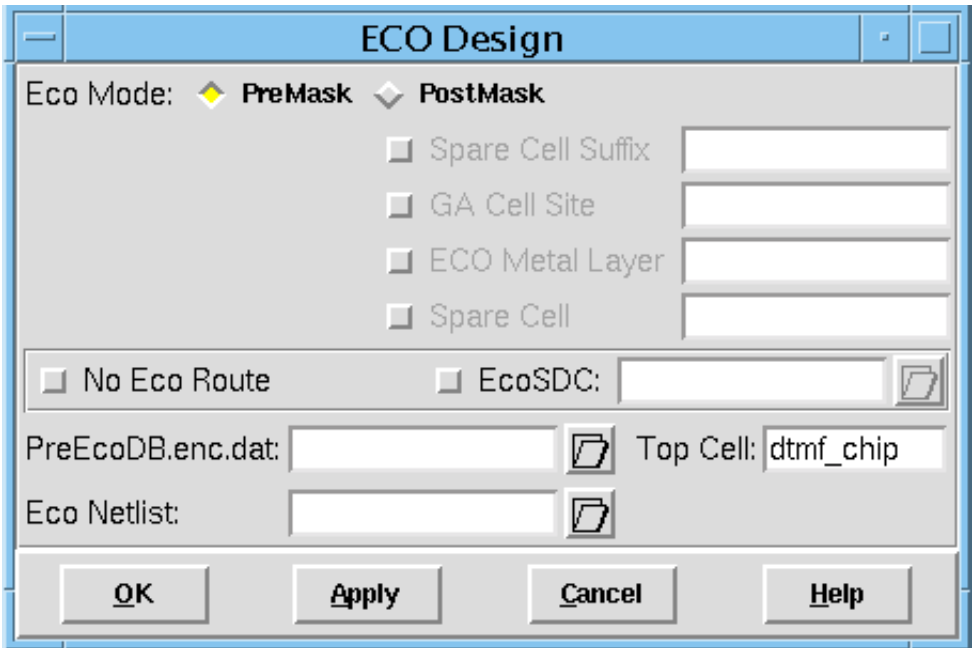
Related Topics

- Saving and Restoring Designs

ECO Design

Use the ECO Design form to select options related to making ECO changes to the design.

➤ Choose *Design – Restore Design – With ECO*.



ecoDesign Fields and Options

PreMask	Indicates that the ECO changes are being made to a pre-mask design. *Default:* On
PostMask	Specifies the options that are available during the post-mask ECO process. *Default:* Off
Spare Cell Suffix	Specifies the suffix to be appended to spare cell names. *Default:* Off
GA Cell Site	Specifies the location of the gate array cells. *Default:* Off

ECO Metal Layer	Specifies the layers to be modified during the ECO process. *Default:* Off
Spare Cell	Specifies the name of the spare cell to be modified during the ECO process *Default:* Off
No Eco Route	Prevents routing during the ECO process. *Default:* Off
EcoSDC	*Default:* Off
PreEcoDB.enc.dat	Specifies the name of the design to be modified.
Top Cell	Specifies the name of the top cell.
Eco Netlist	Specifies the name of the new netlist with the design changes to be implemented.

Related Text Commands

- `ecoDesign`

Save Design As

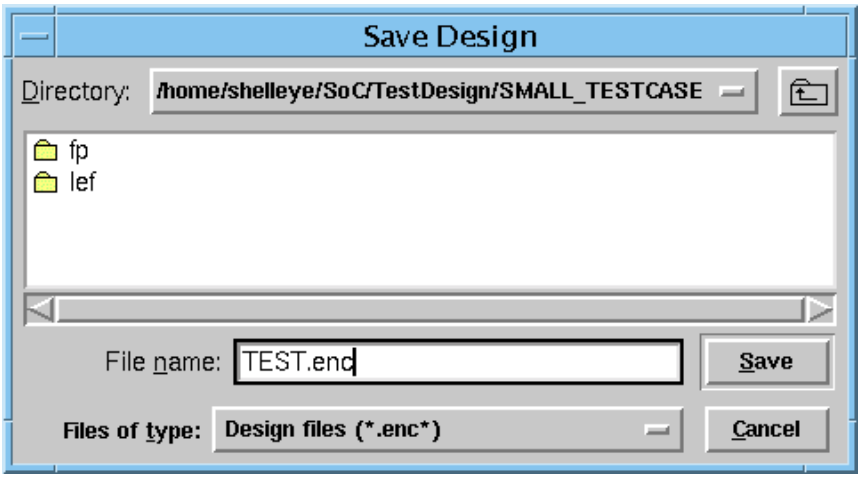
The Save Design As menu provides the following forms to save design files from the Encounter session, and to save all design information using the OpenAccess database format.

- Save Design on page 200
- Save OA Design on page 202

Save Design

Use the Save Design form to save design files in a user-specified directory at anytime in a design session. Only files that exist during the save are copied to the directory.

➤ Choose *Design – Save Design As – SoCE*.



Save Design Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the design. The recommended extension is `.enc`
Files of type	Specifies a file display filter. The default is `.enc`.

Related Text Commands

For information on the following command, see “General Commands” in the *Encounter Text Command Reference*.

■ `saveDesign`

Related Topics

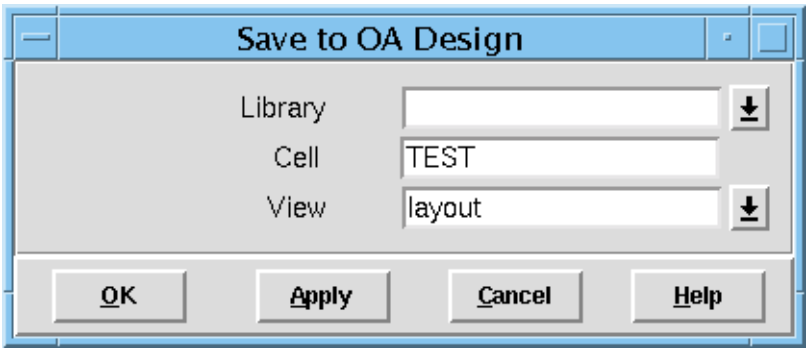
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Saving and Restoring Designs

Save OA Design

Use the Save to OA Design forms to save all information from the current design session, using the OA database format.

➤ Choose *Design – Save Design As – OA.*



Save OA Design Fields and Options

Library	Specifies the target OpenAccess library name.
Cell	Specifies the top cell filename to save.
View	Specifies the view to save.

Note: You must specify the reference library and view names on the Design Import – Advanced – OpenAccess form. You cannot specify them on this form.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

■ `saveOaDesign`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

■ Saving and Restoring Designs

Load

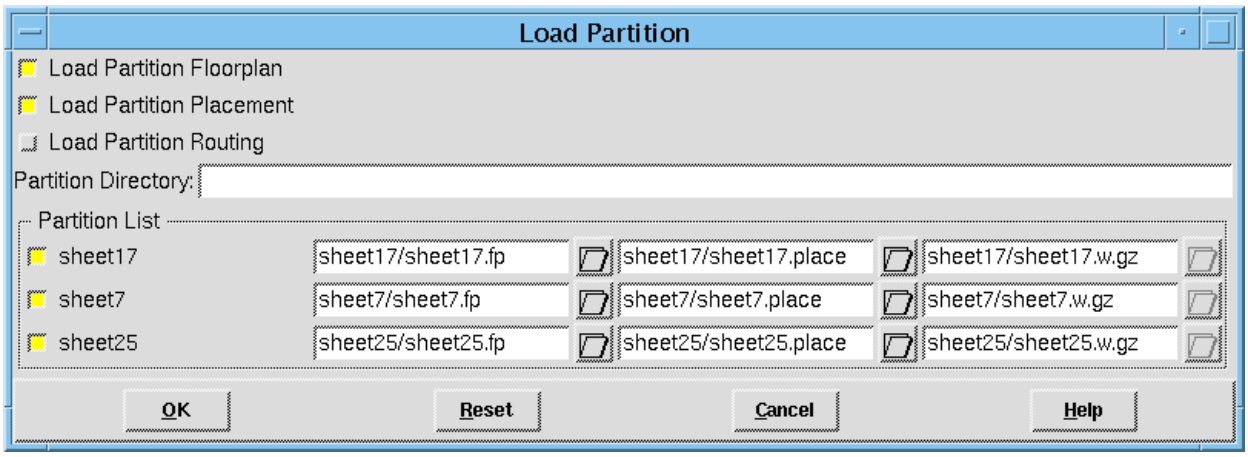
The *Design* menu's *Load* forms enable you to restore individual design files during a design session. The following forms are available:

- Load – Partition on page 204
- Load – Floorplan on page 206
- Load – Place on page 207
- Load – Route on page 209
- Load – DEF on page 211
- Load – TDF on page 213
- Load – PDEF on page 215
- Load – I/O File on page 217
- Load – SPEF on page 218
- Load – SDF on page 220
- Load – Power Waveform on page 222
- Load – OA Database on page 223

Load – Partition

Use the Load Partition form to load partition floorplan, placement, and routing files. Loading the partition data to the top level prepares the partition for timing budget refinement flow and top-level timing analysis.

➤ Choose *Design – Load – Partition.*



Load Partition Fields and Options

Load Partition Floorplan

Allows you to load a partition floorplan file.

Load Partition Placement

Allows you to load a partition placement file.

Load Partition Routing

Allows you to load a partition routing file.

Partition Directory Directory name where the partition data was saved.

Partition List Allows you to browse and select a floorplan, placement, or routing file for each module partition.

Note: All the partitioned modules are displayed as hard blocks.

Related Text Commands

For information on the following commands, see the *Encounter Text Command Reference*.

- `loadFPlan`
- `restorePlace`
- `restoreRoute`
- `setTopCell`

Related Topics

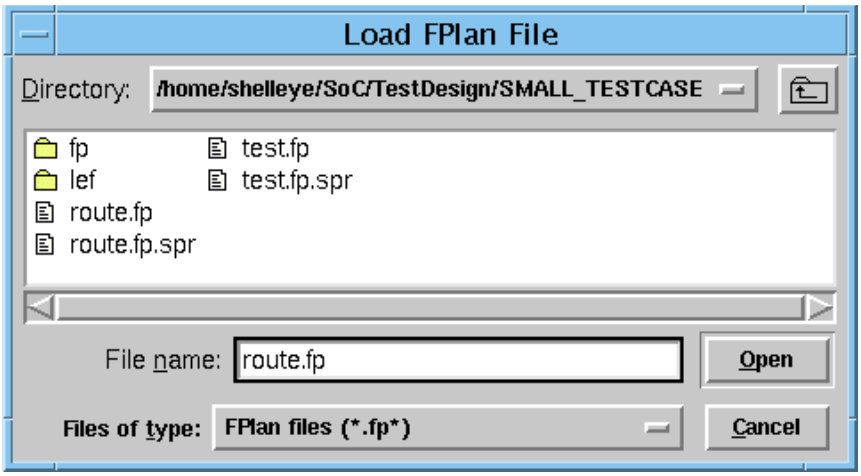
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – Floorplan

Use the Load FPlan File form to load floorplan data for a design session.

➤ Choose *Design – Load – Floorplan.*



Load FPlan File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the floor plan data you want to load.
Files of type	Specifies a file display filter. The default is `.fp`.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

■ `loadFPlan`

Related Topics

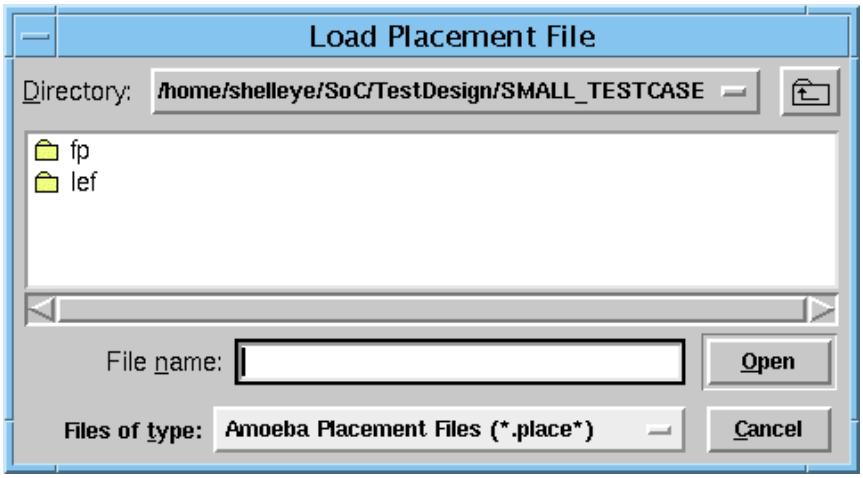
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

■ Importing and Exporting Design Data

Load – Place

Use the Load Placement File form to restore placement data from a previous design session. You can restore the data from a file that was previously saved in Encounter.

➤ Choose *Design – Load – Floorplan.*



Load Placement Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the placement data you want to load.
Files of type	Specifies a file display filter. The default is `.place`.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

■ `restorePlace`

Related Topics

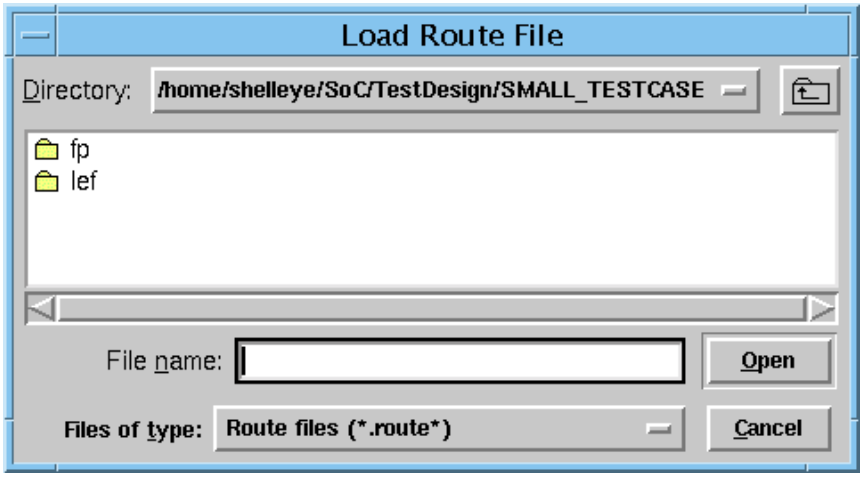
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – Route

Use the Load Route File form to load any routing data from either Trial Route, WRoute, or NanoRoute.

➤ Choose *Design – Load – Route*.



Load Route Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the routing data you want to load.
Files of type	Specifies a file display filter. The default is `.route`.

Related Text Commands

For information on the following command, see “Route Commands” in the *Encounter Text Command Reference*.

■ `restoreRoute`

Related Topics

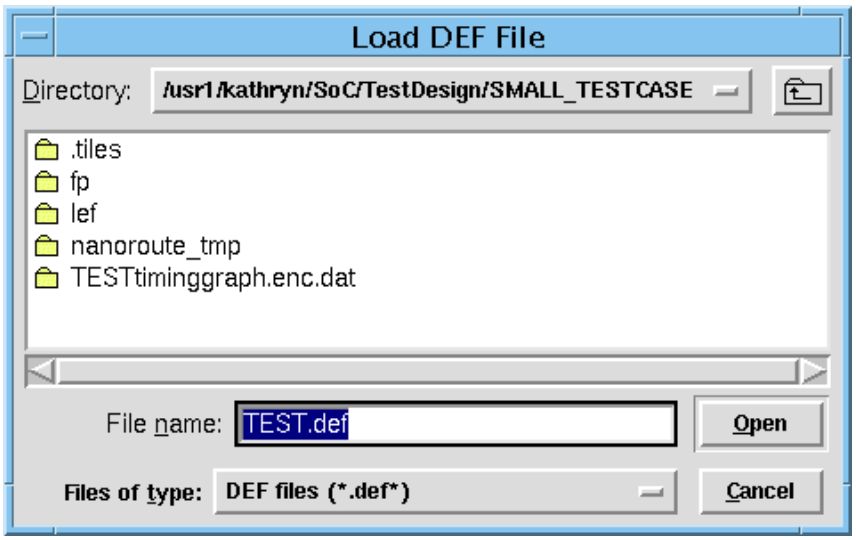
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – DEF

Use the Load DEF File form to load a Design Exchange Format (DEF) file.

➤ Choose *Design – Load – DEF*.



Load DEF File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the DEF file you want to load.
Files of type	Specifies a file display filter. The default is `.def`.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

■ `defIn`

Related Topics

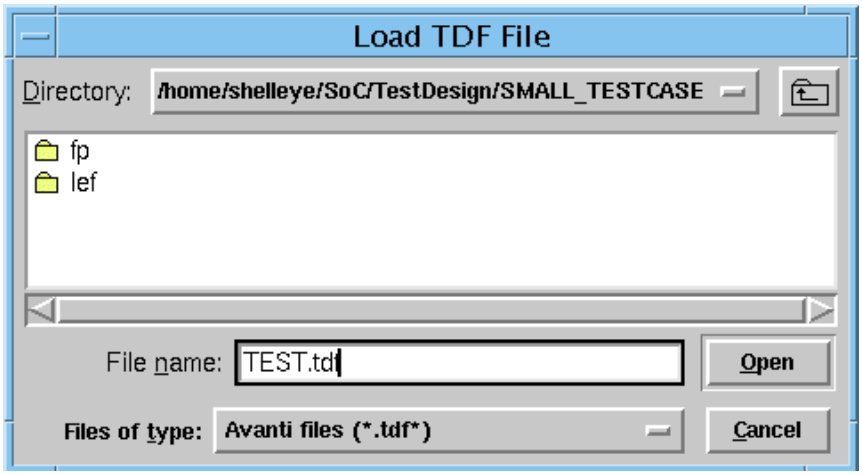
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – TDF

Use the Load TDF File form to load an individual Top Design Format (TDF) file. You can have floorplanning data, placement data, and routing data in a single TDF file, or you can put each type of data in a separate TDF file. If you have separate data files, then you will need to use the `tdfIn` command to individually load each file.

➤ Choose *Design – Load – TDF.*



Load TDF File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the TDF file you want to load.
Files of type	Specifies a file display filter. The default is `.tdf`.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

■ `tdfIn`

Related Topics

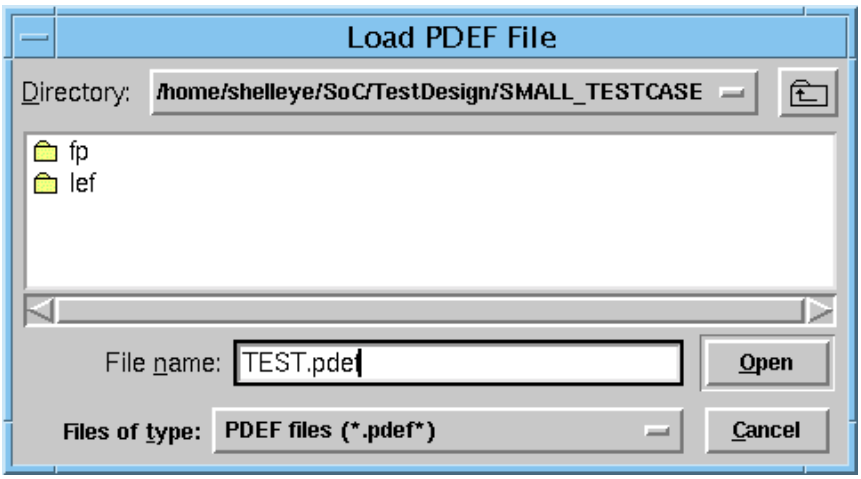
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – PDEF

Use the Load PDEF File form to load a Physical Design Exchange Format (PDEF) file.

➤ Choose *Design – Load – PDEF*.



Load PDEF File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the PDEF file you want to load.
Files of type	Specifies a file display filter. The default is `.pdef`.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

- `pdefIn`

Related Topics

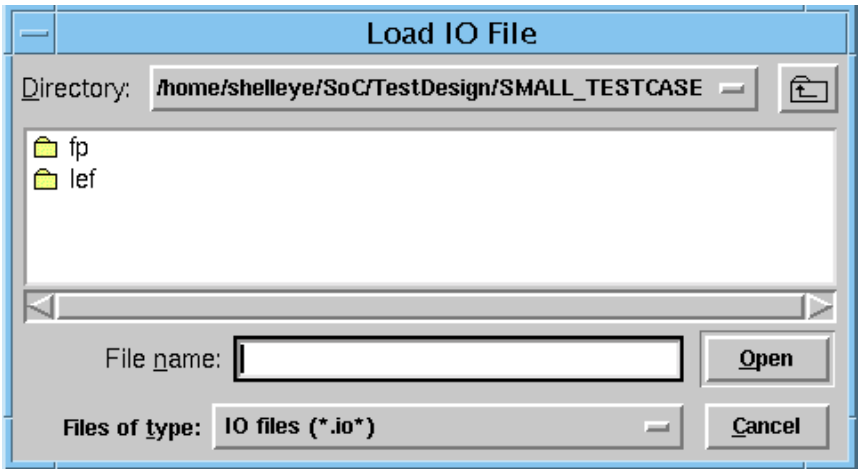
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – I/O File

Use the Load IO File form to load an I/O assignment file.

➤ Choose *Design – Load – I/O File*.



Load I/O File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the I/O file you want to load.
Files of type	Specifies a file display filter. The default is `.io`.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `loadIoFile`

Related Topics

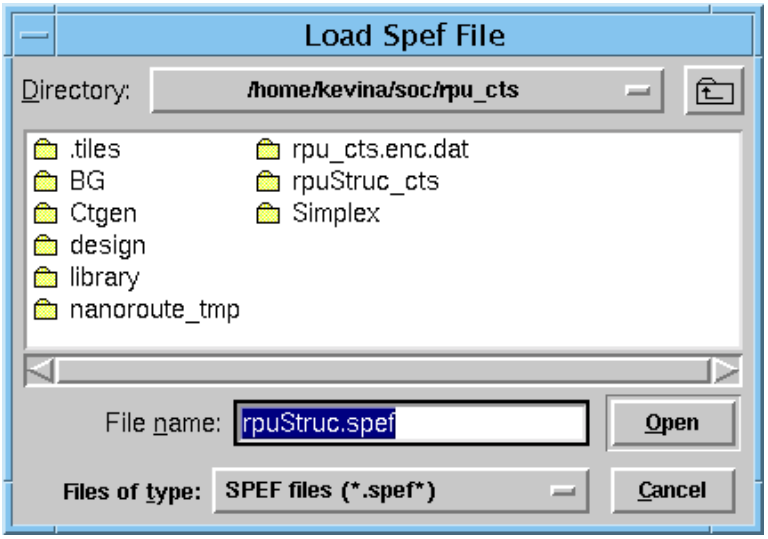
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – SPEF

Use the Load SPEF form to load a SPEF file.

➤ Choose *Design – Load – SPEF.*



Load SPEF File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the SPEF file you want to load.
Files of type	Specifies a file display filter. The default is `.spef`.

Related Text Commands

For information on the following command, see “Timing Commands” in the *Encounter Text Command Reference*.

■ `spefIn`

Related Topics

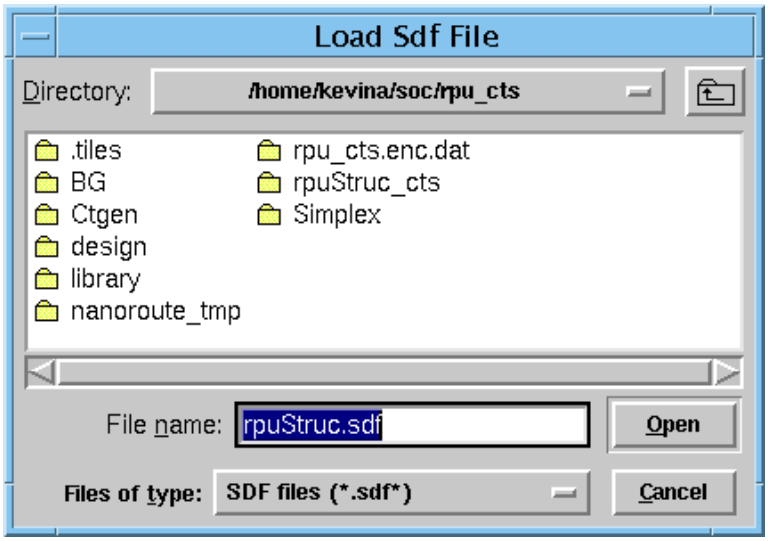
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – SDF

Use the Load SDF form to load an SDF file.

➤ Choose *Design – Load – SDF.*



Load SDF File Fields and Options

Directory	Displays the name and contents of a directory where you can load your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file containing the SDF file you want to load.
Files of type	Specifies a file display filter. The default is `.sdf`.

Related Text Commands

For information on the following command, see “Timing Commands” in the *Encounter Text Command Reference*.

■ `sdfin`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Load – Power Waveform

Use the Load Power Waveform File form to load the power waveform. This option is activated only when the *Design is: Power Analyzed*.

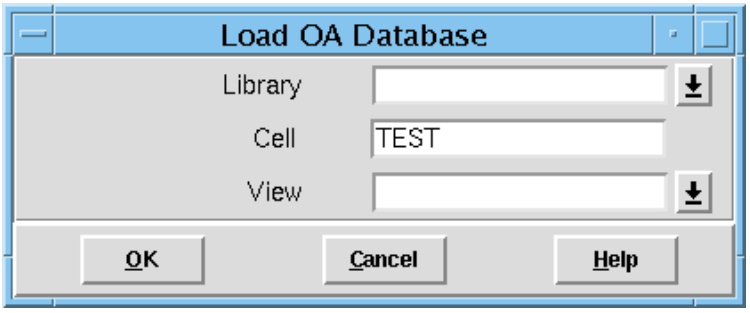
Important

The Novas Debussy waveform viewer is no longer licensed through Encounter. To view the power consumption profile, you can use the Cadence SimVision analysis environment with the SST2 file generated during simulation-based power analysis. Contact your Cadence representative for information on obtaining a license for the SimVision analysis environment.

Load – OA Database

Use the Load OA Database form to load floorplan, placement, and routing information in the OpenAccess format.

➤ Choose *Design – Load – OA Database*.



Load OA Database Fields and Options

Library	Specifies the name of the OpenAccess library where the design has been saved.
Cell	Specifies the name of the top cell.
View	Specifies the name of the cell view to load.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

■ `oaIn`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

■ Importing and Exporting Design Data

Save

The *Design* menu's *Save* forms enable you to save individual design files during a design session. You can also save a detailed RC extraction file, but you cannot save a normal extraction file. You can save the design information at any time while working in a design session. You can then use this saved data to restore a design session.

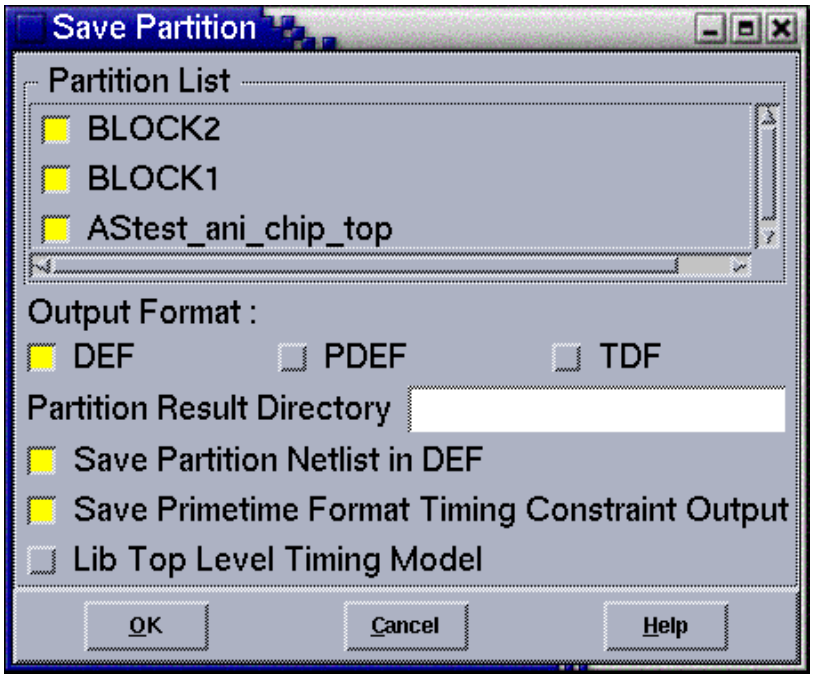
The following forms are available:

- Save – Partition on page 225
- Save – Floorplan on page 227
- Save – Place on page 229
- Save – Route on page 231
- Save – Netlist on page 233
- Save – DEF on page 235
- Save – TDF on page 237
- Save – PDEF on page 239
- Save – I/O File on page 240
- Save – Rail Analysis Results on page 242
- Save – Save Timing Budget on page 244
- Save – GDS on page 246

Save – Partition

Use the Save Partition form to save the partition design files to separate partition directories.

➤ Choose *Design – Save – Partition*.



Save Partition Fields and Options

Partition List	Displays an entry for each module partition and one entry for the top-level partition. All the partitioned modules are displayed as hard blocks.
Output Format	Select *DEF* (the default), *PDEF*, or *TDF* output format. The files saved are used for specific back-end third-party tools. Generated pins can also be viewed in a TDF file in the partition subdirectory. The TDF file has the name `Partition_name_pin.tdf`. **Note:** Regardless of these choices, the Verilog® netlist, configuration file, floorplan file, and cdump files are always saved.

Partition Result Directory
Specifies a directory name to save the resulting partition file. If a name is not entered, the top-level and partition directories are created in the work directory.

Save Partition Netlist in DEF
Saves the partitioned netlist file for each partition in DEF. A top-level netlist file is also saved. The netlist is always saved in Verilog format for the top level and for each of the partitions.

Save Primetime Format Timing Constraint Output
Writes out the timing budget for the partitions in Primetime format.

Important

You can use the option only if you selected *Derive Timing Budget* when you ran the Partition program.

Lib Top Level Timing Model
Generates timing model (.lib) for each partition block at top-level design.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `savePartition`

Related Topics

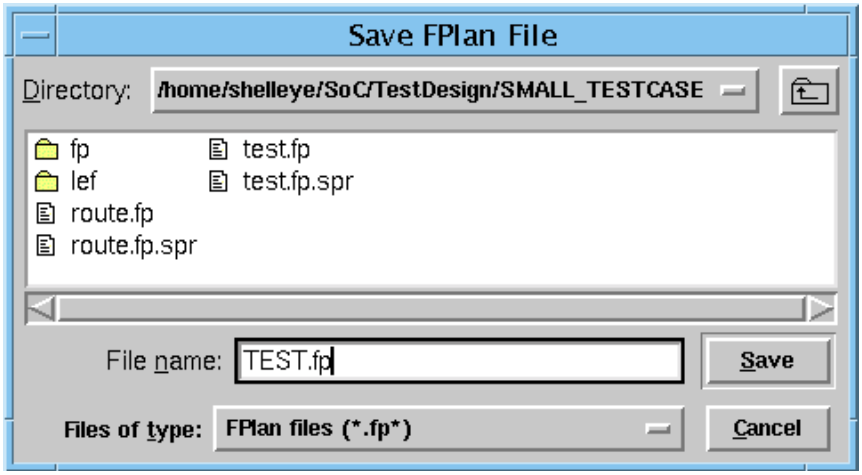
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – Floorplan

Use the Save FPlan File form to save floorplan data at any time during a design session.

➤ Choose *Design – Save – Floorplan*.



Save FPlan File Fields and Options

Directory	Displays the name and contents of a directory where you can save your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the floor plan data.
Files of type	Specifies a file display filter. The default is `.fp`.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

■ `saveFPlan`

Related Topics

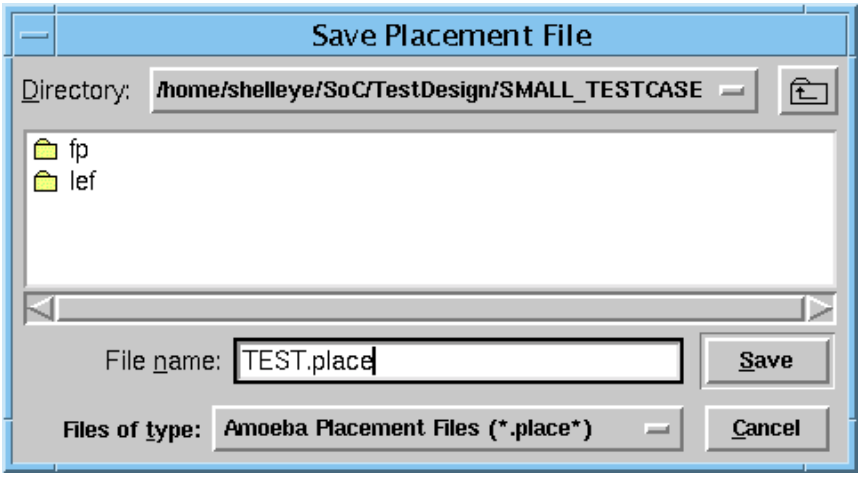
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – Place

Use the Save Placement File form to write placement information to a file in Encounter placement data format. To save the placement data in DEF, PDEF, or TDF format, see "Save" on page 224.

➤ Choose *Design – Save – Place*.



Save Placement File Fields and Options

Directory	Displays the name and contents of a directory where you can save your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the placement data.
Files of type	Specifies a file display filter. *Default:* `.place`

Related Text Commands

For information on the following command, see "Placement Commands" in the *Encounter Text Command Reference*.

■ `savePlace`

Related Topics

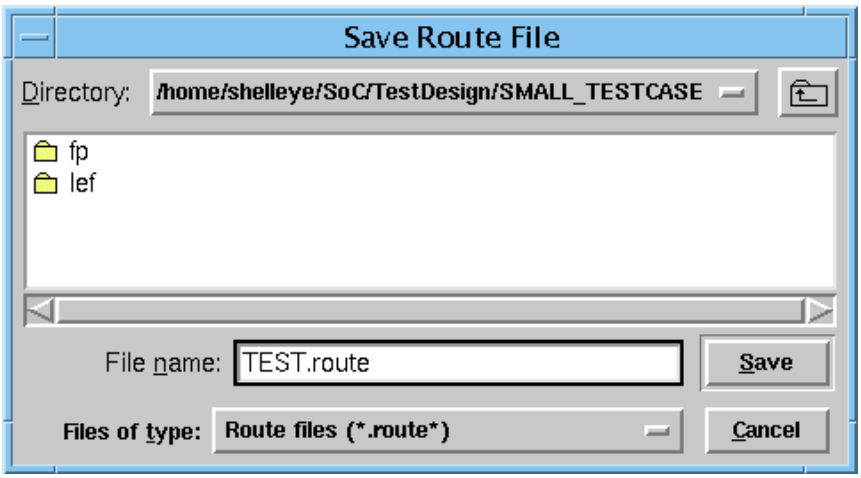
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – Route

Use the Save Route File form to save routing information to a file.

➤ Choose *Design – Save – Route*.



Save Route File Fields and Options

Directory	Displays the name and contents of a directory where you can save your file. Click on the directory pull-down to choose a different directory.
File name	Enter the name of the file to which you want to save the routing data.
Files of type	Specifies a file display filter. *Default:* `.route`

Related Text Commands

For information on the following command, see “Route Commands” in the *Encounter Text Command Reference*.

■ `saveRoute`

Related Topics

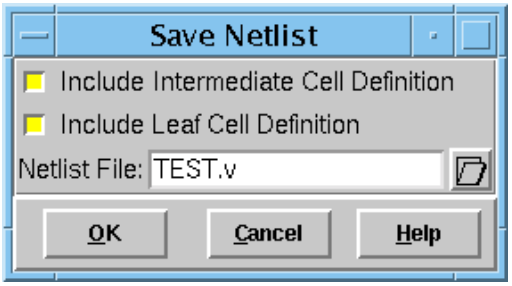
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – Netlist

Use the Save Netlist form to write a netlist file of the design in Encounter. The netlist is in hierarchical Verilog format only if the original netlist loaded was hierarchical. The netlist is saved after running placement with timing driven option, clock tree synthesis, scan group reorder, or IPO. You must save the netlist if you performed timing-driven placement, scan optimization, clock tree synthesis (CTS), or in-place optimization (IPO) during the design session.

➤ Choose *Design – Save – Netlist.*



Save Netlist Fields and Options

Intermediate Cell Definition	Includes all the intermediate cell definitions in the netlist file. You must choose this to generate the design's complete netlist. Do not choose this option if you want to generate only leaf cell definitions.
Include Leaf Cell Definition	Includes all leaf cell definitions to the netlist file. Leaf cell definitions are needed when pin orders are implied in the netlist.
Netlist File	Specify a name for the netlist file.

Related Text Commands

For information on the following command, see "General Commands" in the *Encounter Text Command Reference*.

■ `saveNetlist`

Related Topics

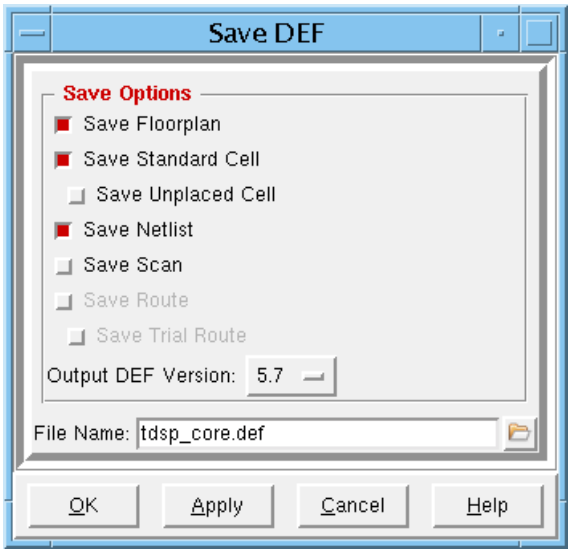
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – DEF

Use the Save DEF form to save DEF information to a file. The DEF file can contain floorplan, placement, scan, or route data. Each data type is saved into a single DEF file.

➤ Choose *Design – Save – DEF*.



Save DEF Fields and Options

Save Floorplan	Saves DEF rows, tracks, die area, gcell grids, corebox, block placement, special nets, and I/Os.
Save Standard Cell	Saves standard cell placements.
Save Unplaced Cell	Saves unplaced standard cell information. This option is available only if *Save Standard Cell* is selected.
Save Netlist	Saves netlist connectivity information.
Save Scan	Saves scan cell information.
Save Route	Saves `NET`s wiring. Trial routes are ignored unless Trial Route is selected.
Save Trial Route	Saves trial route data.
Output DEF Version	Specifies the DEF file version. The available options are 5.7, 5.6, 5.5, 5.4, and 5.3. The default value is `5.7`.

File Name	Specify a name for the DEF file.

Note: Fields are available based on the status of the design. For example, if the design is placed, the *Save Route* field is unavailable.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

- `defOut`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

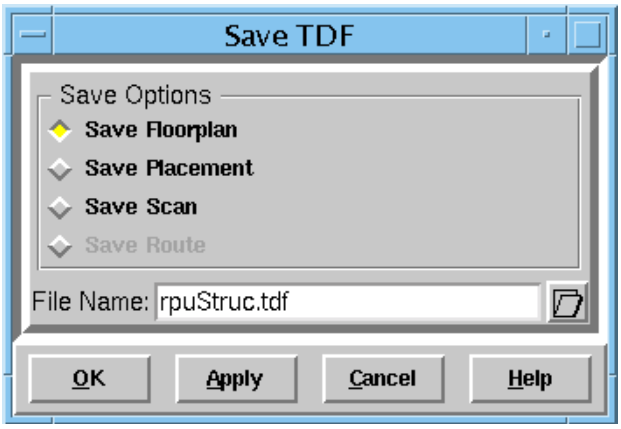
- Importing and Exporting Design Data

Save – TDF

Use the Save TDF form to save TDF information to a file. The TDF file can contain floorplan, placement, scan, or route data. Each data type is saved in a separate TDF file.

Note: This command does not apply to power strips.

➤ Choose *Design – Save – TDF*.



Save TDF Fields and Options

Save Floorplan	Writes out the floorplan command replay file for the Apollo tool. The filename is `*.tdf.fp.cmd`.
Save Placement	Writes out only the standard cell placement obstruction layer data.
Save Scan	Includes scan chain information in the output file.
Save Route	Writes out only the routing data to the output file.
File Name	Specify a name for the DEF file.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

■ `tdfOut`

Related Topics

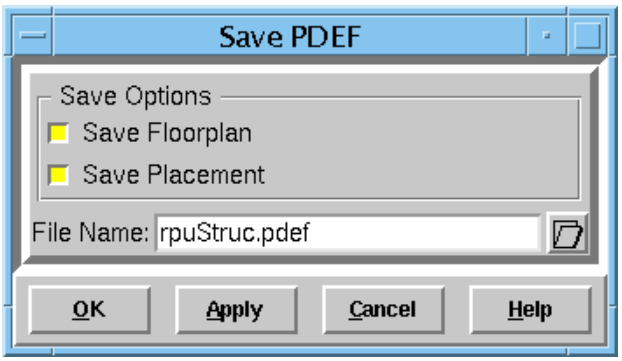
For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – PDEF

Use the Save PDEF form to save floorplan information to a file.

➤ Choose *Design – Save – PDEF*.



Save PDEF Fields and Options

Save Floorplan	Specifies that only floorplan information be written into the output PDEF file. If you do not specify this option, both floorplanning and placement information appear in the output PDEF file.
Save Placement	Saves placement information to the output PDEF file.
File Name	Specify a name for the PDEF file.

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

- `pdefOut`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

- Importing and Exporting Design Data

Save – I/O File

Use the Save IO File form to save the design's I/O pad and pin information to a file. This file can be edited to customize the placement of pads and pins.

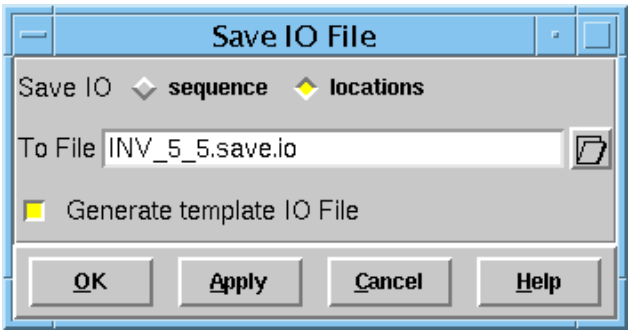
You can save the I/O information any time after floorplanning is complete. The results can be reloaded for future designs.

Important

By default, the I/O information is saved to a version: 3 file, for the current release version of Encounter. For the release versions 6.2 and below, you must save the I/O information to a version: 2 file, by specifying the *-v2* parameter in the `saveIoFile` command.

Note: This form can be used after loading I/O pad and pin placement data using DEF or TDF.

➤ Choose *Design – Save – I/O File*.



Save I/O File Fields and Options

Save IO	Choose an I/O file type.
Sequence	Creates a file that contains the pad and pin names in sequence for all sides of the die area. This file can be edited to customize I/O rule based commands and be read in during design import.
Location	Creates a file that contains the pad and pin names and their placement locations.
To File	Specify a name for the I/O file. The recommended filename extension is `.io`. The file format is ASCII.
Generate template IO File	Creates a template file with the extension `.io.tdf`

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `saveIoFile`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

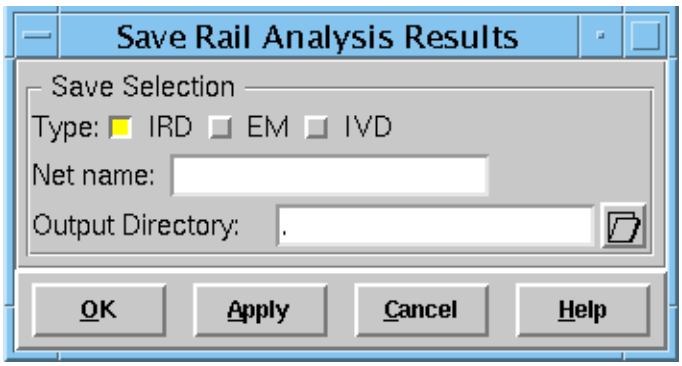
- Importing and Exporting Design Data

Save – Rail Analysis Results

Use the Save Rail Analysis Results form to save a snapshot of the display for any power nets that have been analyzed. It is not necessary to display the rail analysis results for the net prior to saving.

Note: This form is available only after you perform power analysis.

➤ Choose *Design – Save – Rail Analysis Results*.



Save Rail Analysis Results Fields and Options

Type	Select one or more of the following types of displays to save:	
	IRD	Saves a display of IR drop analysis.
	EM	Saves a display of EM violations.
	IVD	Saves a display of instance voltage drop.
Net Name	Specify a net name for which you want to save the electromigration values.	
Output Directory	Specify an output directory name.	

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `saveEM`
- `saveIRDrop`
- `saveIVD`

Related Topics

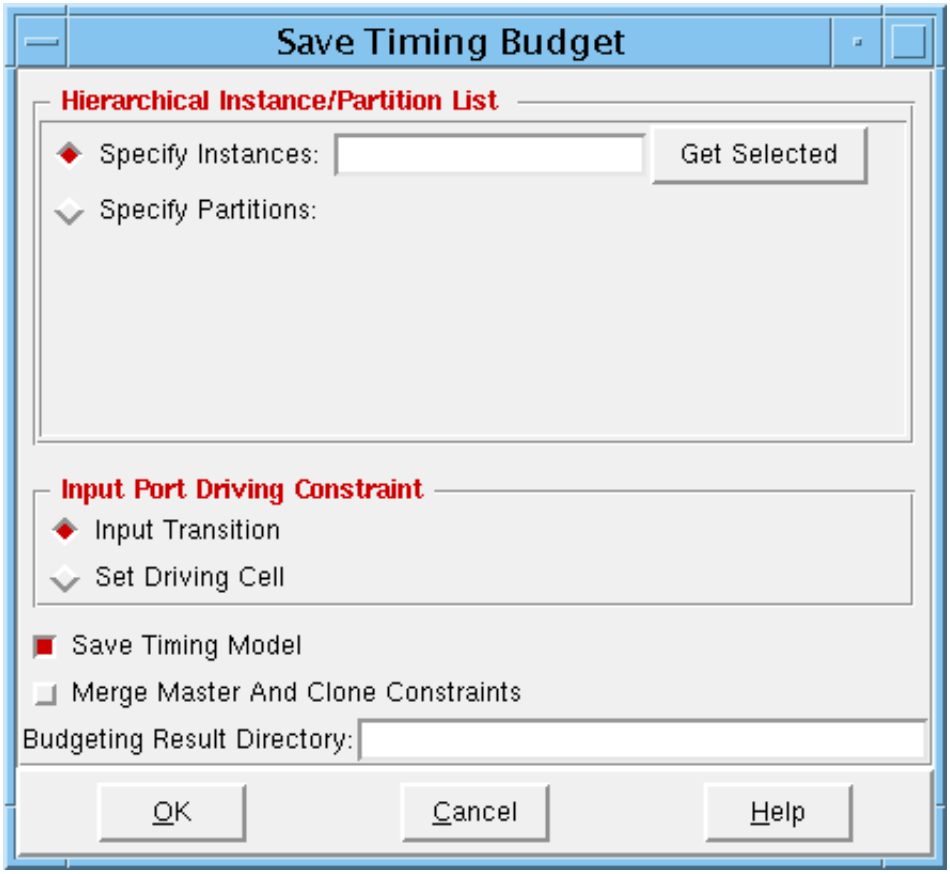
For information on the following topic, see “Power Analysis” in the *Encounter User Guide*.

- Saving Rail Analysis Values

Save – Save Timing Budget

Use the Save Timing Budget form to save time budget files of specified hierarchical instances to a specified directory.

➤ Choose *Design – Save – Save Timing Budget*.



Save – Save Timing Budget Fields and Options

Specify Instances	Saves the budget files for instances.
Specify Partitions	Saves the budget files for partitions.
Input Transition	Writes out input transition time in the budgeting output files using the `set_input_transition` constraint.
Set Driving Cell	Writes out the boundary drive information using the `set_driving_cell` constraint.

Save Timing Model	Saves the timing model.
Merge Master and Clone Constraints	Saves the timing budgets for the masters/clones based on the worst-case timing data per pin. When used with the *Specify Instances*, this option saves the budget based on the worst-case data for the specified instances in the master/clone set. When used with *Specify Partitions*, this option saves the budget based on the worst-case data for all the partitions in the master/clone set.
Budgeting Result Directory	Specifies the directory name that contains the derived timing budget files. The files are derived in a subdirectory `dirName/cellTypeName/cellTypeName.constr.pt`. If you do not specify this option, the timing budget files are derived in the current directory.

Related Text Commands

For information on the following command, see “Timing Budgeting Commands” in the *Encounter Text Command Reference*.

- `saveTimingBudget`

Related Topics

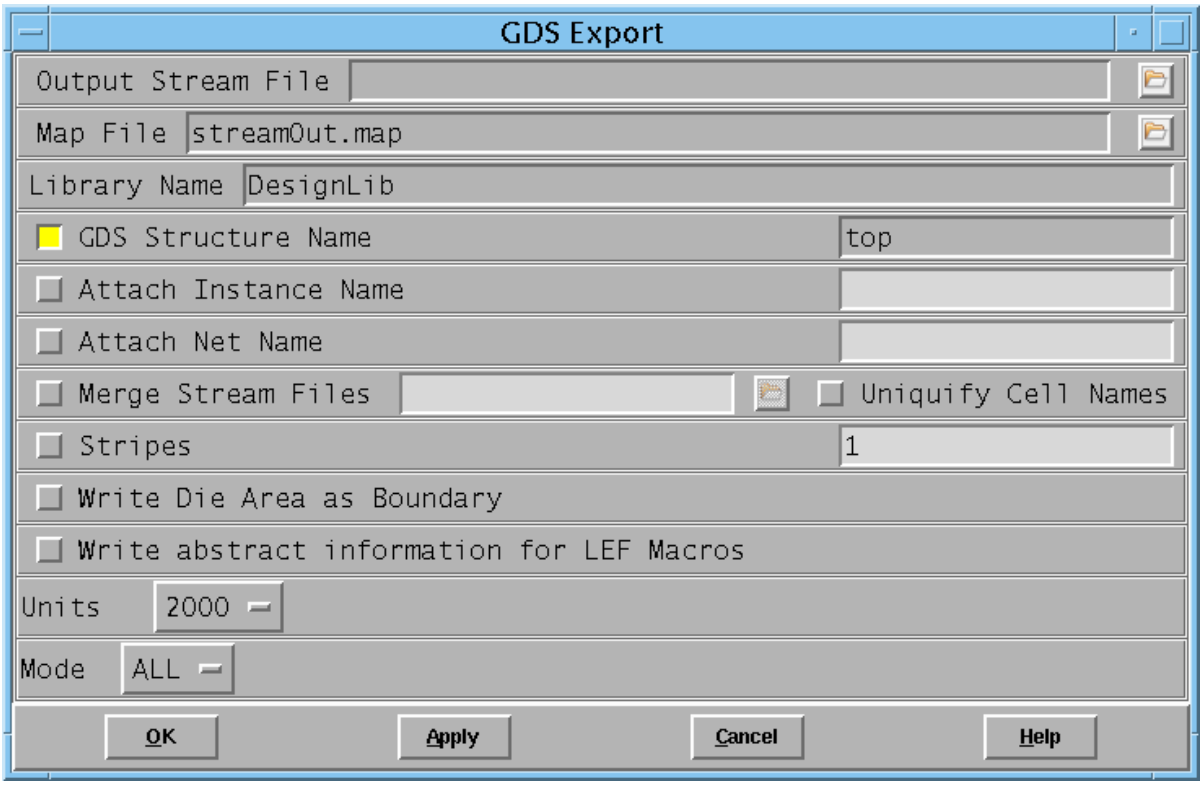
For information on the following topic, see “Timing Budgeting” in the *Encounter User Guide*.

- Deriving Timing Budgets

Save – GDS

Use the GDS Export form to create a GDSII Stream file version of the current database.

➤ Choose *Design – Save – GDS*.



Save – GDS Fields and Options

Output Stream File

Specifies the GDSII Stream output file. Use the file folder icon to find the directory and file you want.

Note: Add the `.gz` extension to the filename to enable compression (for example, `GDS_file.gds.gz`).

Map File	Specifies the file used for layer mapping between the Encounter software and GDSII Stream format. Use the file folder icon to find the file you want. If a file is not specified, the software creates a map file with the name `streamOut.map`. For more information, see the "About the GDSII Stream or OASIS Map File" section in the "Design" chapter of the *Encounter User Guide*.
Library Name	Specifies the library that you want to create in GDSII /Stream format. The default name is `DesignLib`.
GDS Structure Name	Specifies the structure name that consists of all geometries. The default is the current design's top cell name.
Attach Instance Name	Specifies the instance name value added to the attribute on SREF of the specified attribute number.
Attach Net Name	Specifies the attribute number for paths and via SREF. The Encounter software adds the net name values to this attribute.
Merge Stream Files	Specifies a single file or list of files to merge with the database. All files must be Stream GDSII files. Compressed files are acceptable. If a merge file contains extra cells that are not used in the design, the Encounter software merges only the cells used in the design. The software automatically creates blackboxes when merging and writing macro files.

Uniquify Cell Names

Creates unique cell names if there are name collisions when the Encounter software merges files.

When a cell name is repeated, the software renames the cell `cellName_filename`, where `filename` is the name of the merge file in which the cell name appears.

The Encounter software changes the name of references to that cell in the merge file. The software changes the reference name if the referenced cell is defined in the same file, regardless of whether the cell is defined before or after the reference. If a reference in a merge file refers to a cell definition in a different merge file, then the reference is not changed in the OASIS output file.

Note: You must select *Merge Stream Files* to enable this option.

Default: Off (The Encounter software ignores duplicate cell names.)

Stripes

Specifies the number of stripes that divide the design. For example, setting *Stripes* to 2 divides the design into two equal windows and creates three files. Setting *Stripes* to 3 divides the design into three equal windows and creates four files. The default is `1`.

Note: All polygons and shapes whose lower-left corner is in the current window are output with that stripe.

If the *Stripes* value is greater than `1`, the naming conventions are as follows:

- `GDS_file.gds`

  Contains top structure, SREFs for top structures of other stripes, and via definitions

- `GDS_file.gds.1`

  Contains stripe number 1, `structureName.1`

- `GDS_file.gds.2`

  Contains stripe number 2, `structureName.2`

Write Die Area as Boundary

Forces the Encounter software to output die areas as boundaries. If not specified, the software outputs die areas as bounding boxes.

Write abstract information for LEF Macros

Outputs LEF abstract information, such as LEF pin geometries and obstructions for macros.

Optionally, you can select *Write abstract information for LEF Macros* when you want to create a GDSII Stream output that contains the LEF macro structures as well as the design data.

This option can be used for debugging the LEF macro definitions against verification DRC rules. The output contains macro pins and obstructions.

Note: `LEFPIN` and `LEFOBS` apply only when *Write abstract information for LEF Macros* is enabled. Additionally, if you select *Write abstract information for LEF Macros* and `LEFPIN` and `LEFOBS` are not specified in the map file for the layers in the LEF `MACRO`s, the GDSII structures for those `MACRO`s will be empty.

Units

Selects the resolution for values in the GDSII Stream file. Choose one of the values provided in the cyclic field. The default unit value is the value that is specified in the LEF technology file.

Mode

Identifies the layers to write. Select one of the following:

ALL

Specifies all layer information in the map file:

- All instances
- All via instances
- All generated via cells

FILLONLY

Specifies only fill layers in the map file:

- No instances
- Only fill via instances
- Only generated fill via cells

NOFILL Specifies only non-fill layers in the map file:

- All instances
- Only non-fill via instances
- Only non-fill generated via cell

Related Text Commands

For information on the following command, see “Import Commands” in the *Encounter Text Command Reference*.

- `streamOut`

Related Topics

For information on the following topic, see “Importing and Exporting Designs” in the *Encounter User Guide*.

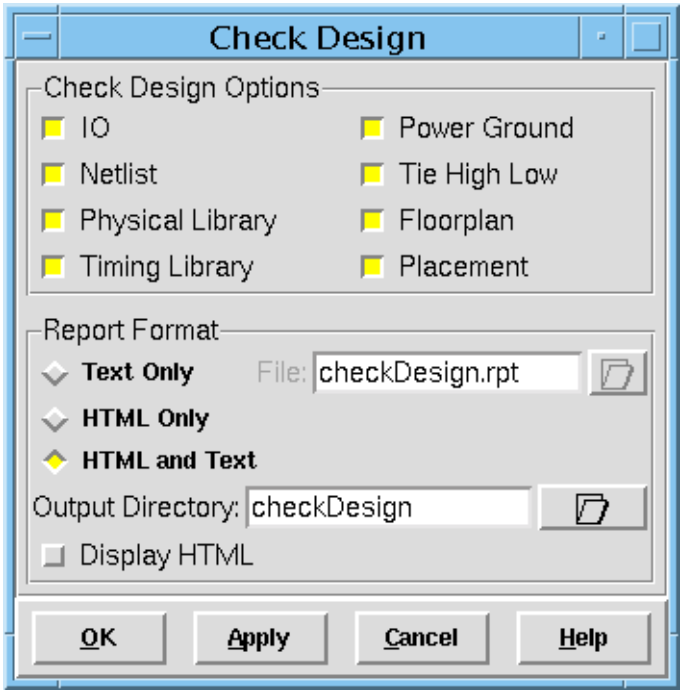
- Importing and Exporting Design Data
- Merging GDSII Files
- GDS Map File Format

Check Design

Use the Check Design form to check for missing or inconsistent library and design data at any stage of the design. Cadence recommends that you check libraries and data as follows:

- Perform I/O checking at any time. I/O problems might not impede any tool, but they might add to design problems.
- Perform netlist checking at any time after the design has been loaded.
- Perform physical library checking before floorplanning.
- Perform power/ground checking before routing and extraction, and verifying geometry and connectivity.
- Perform timing library checking before any timing-related operation (for example, timing driven placement or routing, timing optimization, clock-tree synthesis, and static timing analysis)
- Perform tie-high and tie-low checking before routing and extraction.

➤ Choose *Design – Check Design*.



Check Design Fields and Options

IO

Checks I/O pads, issues warning messages, and reports the following information:

- Unplaced I/O cells
- Floating pins that belongs to I/O pads (warning)
- I/O pins connected to non-I/O instances (directly connected to core cells)
- Unplaced I/O pins
- Floating I/O pins

Default: On

Netlist

Checks the netlist, issues error or warning messages, and reports the following information:

- Output pins tied to power/ground nets (for example, `BUFX1 U1 (.A(net1),.Y1(1'b0)))`
- Input pins floating (warning)
- Multiple driver nets (warning)

Default: On

Physical Library

Checks the physical libraries and reports whether all cells have LEF views. Issues error messages for the following conditions:

- Cells not defined in LEF
- Cells with missing dimensions
- Pins with missing direction
- Cells and pins with missing geometry
- Cell dimensions are not an integer multiple of the core site dimensions

Default: On

Timing Library

Checks whether the cells used in the design have been defined in the timing library. This option does not check for the presence of timing arcs. All physical cells are excluded from this check.

Default: On

Floorplan

Checks the floorplan, issues error or warning messages, and reports the following information:

- Off-grid horizontal and vertical tracks
- Instances not snapped to row site
- Unplaced I/O pins
- Off Grid Power/Ground Pre-routes
- Instances not on the manufacturing grid
- Preroutes not on the manufacturing grid (error)
- Regular preroutes not on tracks

Default: On

Power Ground

Checks power and ground connections, issues warning messages, and reports the following information:

- Power terminals connected to ground net
- Ground terminals connected to power net
- Floating power and ground terminals
- Power and ground terminals connected to non-power and ground nets.

Default: On

Tie High Low

Reports unconnected tie-high or tie-low terminals, and issues a warning message.

Default: On

Placement

Checks placement, issues error or warning messages, and reports the following information:

- Number of placed and unplaced instances
- Number of overlapping instances
- Number of placement blockage violations
- Placement density

Default: On

Text Only

Generates a text version of the report.

Default: Off

File

Writes the report information to the specified file.

Default: `checkDesign.rpt`

HTML Only

Generates an HTML version of the report. Some sections of the report include links to more detailed HTML reports. For an example of an HTML report, see "HTML Check Design Report" on page 255.

Default: Off

HTML and Text

Generates both an HTML version and a text version of the report.

Default: On

Output Directory

Saves the HTML version of the report to the specified directory. If you select the *HTML and Text* option, the software saves both the HTML and text versions of the report to the specified directory.

Default: `checkDesign`

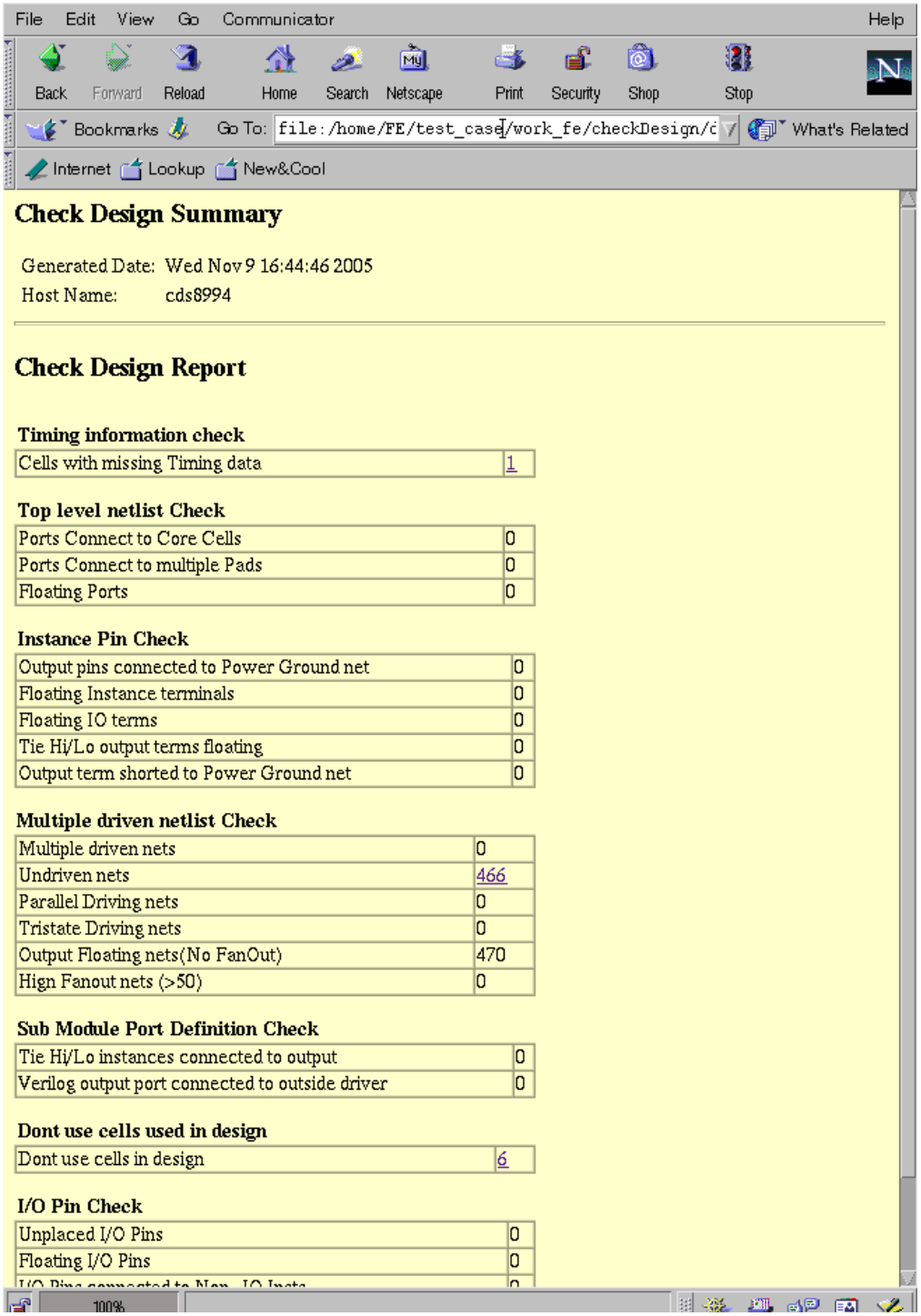
Display HTML

Opens a browser and displays the HTML version of the report.

Default: Off

HTML Check Design Report

The following is an example of an HTML report generated by the Check Design form.



Check Design Summary

Generated Date: Wed Nov 9 16:44:46 2005
Host Name: cds8994

Check Design Report

Timing information check

Cells with missing Timing data	1

Top level netlist Check

Ports Connect to Core Cells	0
Ports Connect to multiple Pads	0
Floating Ports	0

Instance Pin Check

Output pins connected to Power Ground net	0
Floating Instance terminals	0
Floating IO terms	0
Tie Hi/Lo output terms floating	0
Output term shorted to Power Ground net	0

Multiple driven netlist Check

Multiple driven nets	0
Undriven nets	466
Parallel Driving nets	0
Tristate Driving nets	0
Output Floating nets(No FanOut)	470
Hign Fanout nets (>50)	0

Sub Module Port Definition Check

Tie Hi/Lo instances connected to output	0
Verilog output port connected to outside driver	0

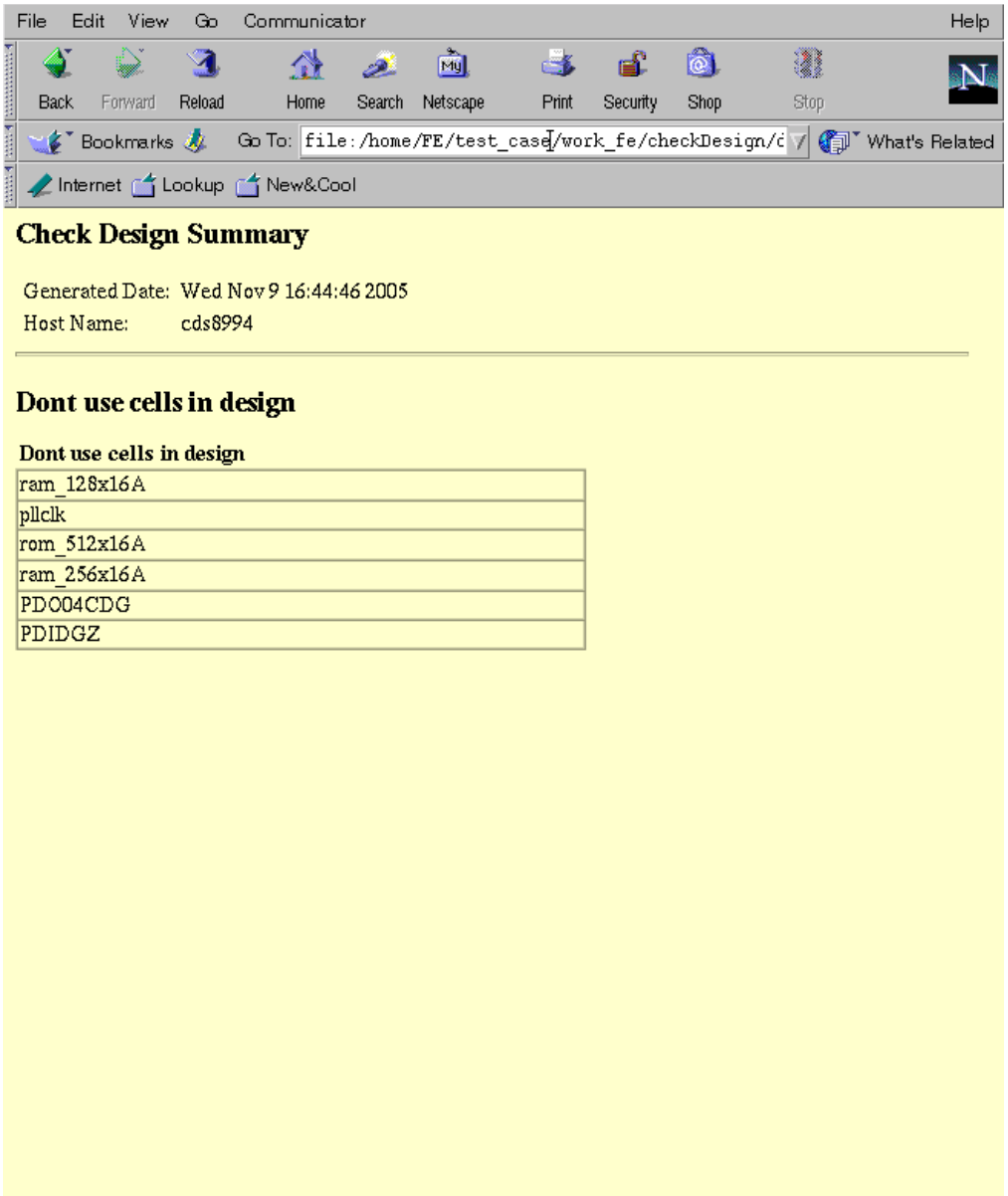
Dont use cells used in design

Dont use cells in design	6

I/O Pin Check

Unplaced I/O Pins	0
Floating I/O Pins	0

Some sections of the report include links to more detailed HTML reports. For example, if you click on the *Dont use cells in design* link on the main page of the HTML report, the software displays a list of the cells.



Related Text Commands

For information on the following command, see “Import and Export Commands” in the *Encounter Text Command Reference*.

- `checkDesign`

Report

The Report menu provides the following forms that allow you to generate reports that contain statistics for the entire design, calculate the gate count, and create a list of design statistics:

- Summary Report on page 258
- Gate Count Report on page 263
- Netlist Statistics on page 264

Summary Report

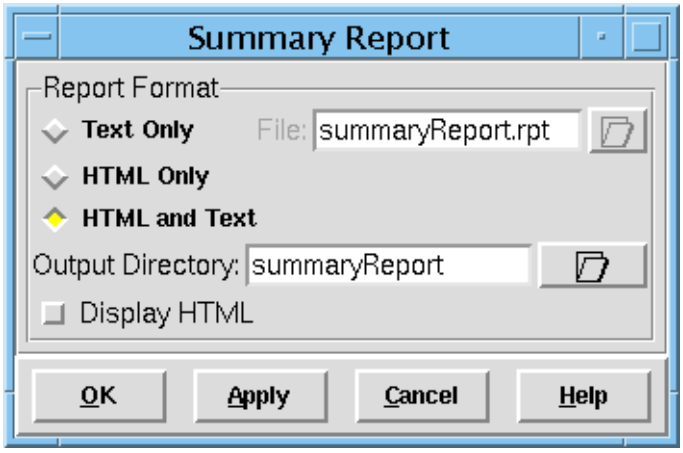
Use the Summary Report form to create a report that contains statistics for the entire design, or a selected object in the design.

A report on the entire design includes statistics for the following categories:

- General Design Information
- General Library Information
- Netlist Information
- Timing Information
- Floorplan/Placement Information

The information contained in a report on a selected object varies depending on the object you select. You can select a module, an instance, or a net.

1. Select an object in the design display area. (If you want to display information about the entire design, skip Step 1.)
2. Choose *Design – Report – Summary* or click the *Summary Report* widget on the toolbar.



Summary Report Fields and Options

Text Only

Generates a text version of the summary report.

Default: Off

File

Writes the report information to the specified file.

Default: `summaryReport.rpt`

HTML Only

Generates an HTML version of the summary report.

Some statistics in the sections include links to more detailed HTML reports. For example, if you click on the *# Layers* link under *General Library Information* section of the HTML report, the software displays a detailed HTML report on the layers in the design.

For an example of an HTML report, see "HTML Summary Report" on page 260

Default: Off

HTML and Text

Generates both a text version and an HTML version of the summary report.

Default: On

Output Directory

Saves the HTML version of the report to the specified directory. If you select the *HTML and Text* option, the software saves both the HTML and text versions of the report to the specified directory.

Default: `summaryReport`

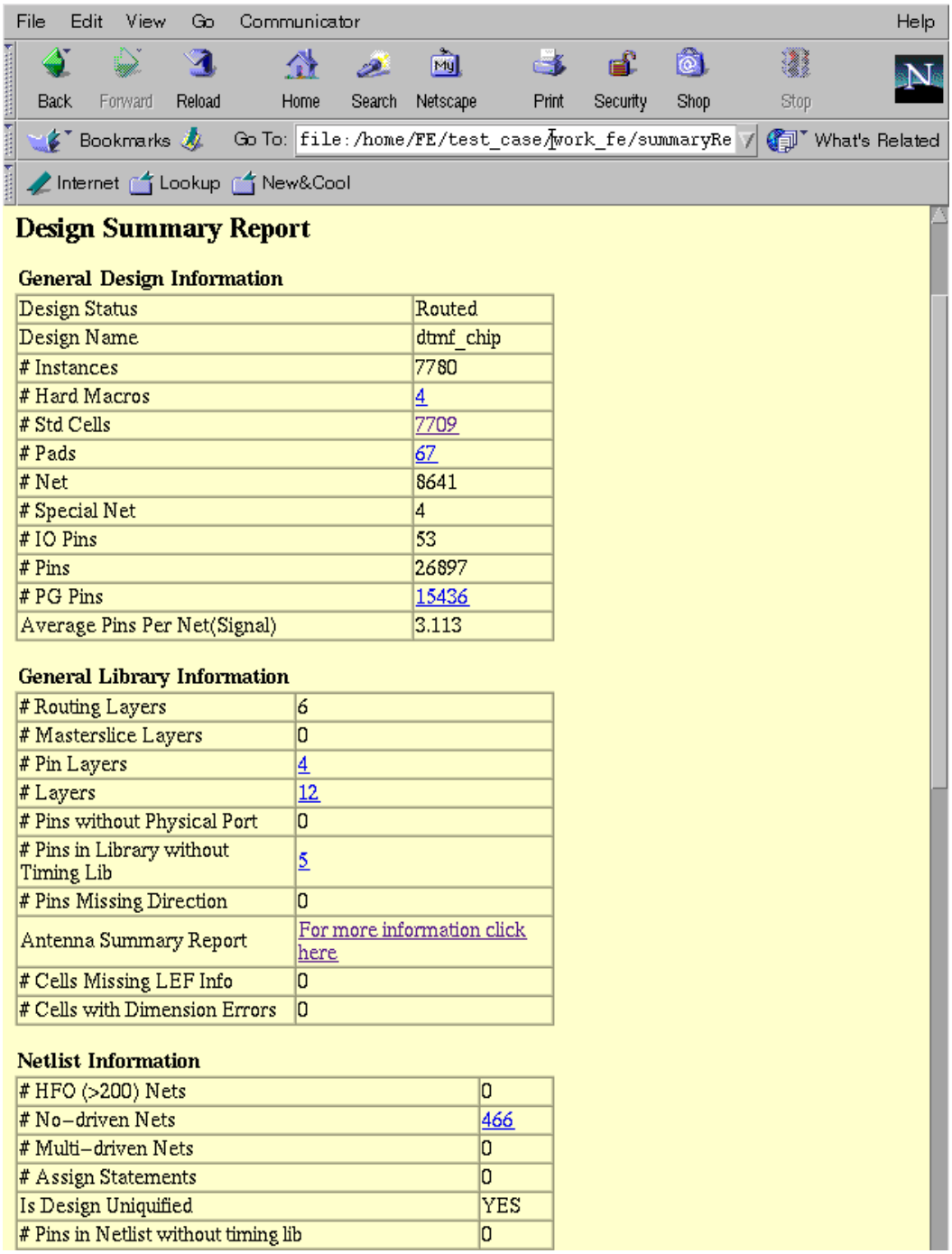
Display HTML

Opens a browser and displays the HTML version of the report.

Default: Off

HTML Summary Report

The following is an example of an HTML summary report for an entire design.



Design Summary Report

General Design Information

Design Status	Routed
Design Name	dtmf_chip
# Instances	7780
# Hard Macros	4
# Std Cells	7709
# Pads	67
# Net	8641
# Special Net	4
# IO Pins	53
# Pins	26897
# PG Pins	15436
Average Pins Per Net(Signal)	3.113

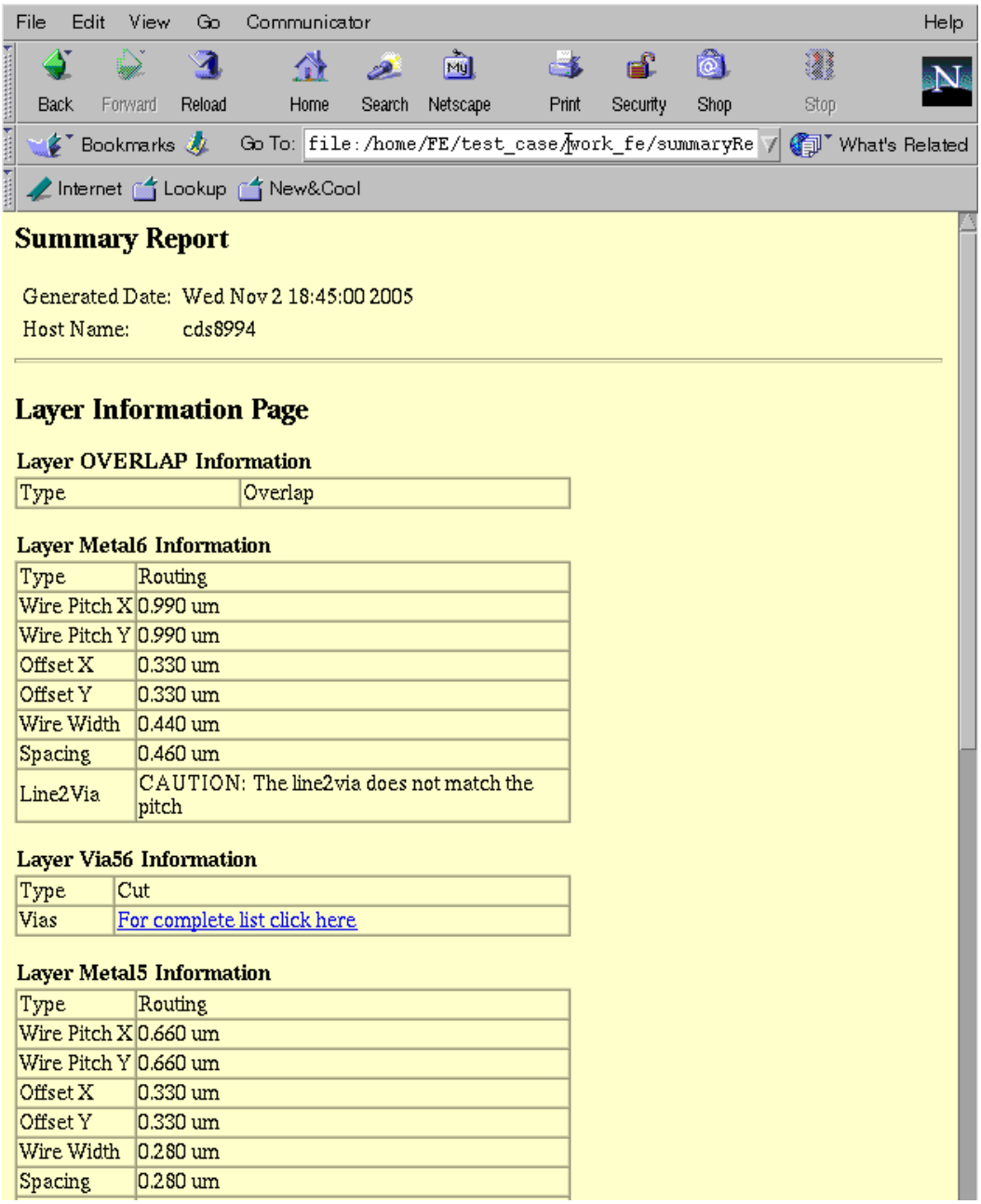
General Library Information

# Routing Layers	6
# Masterslice Layers	0
# Pin Layers	4
# Layers	12
# Pins without Physical Port	0
# Pins in Library without Timing Lib	5
# Pins Missing Direction	0
Antenna Summary Report	For more information click here
# Cells Missing LEF Info	0
# Cells with Dimension Errors	0

Netlist Information

# HFO (>200) Nets	0
# No-driven Nets	466
# Multi-driven Nets	0
# Assign Statements	0
Is Design Uniquified	YES
# Pins in Netlist without timing lib	0

Some statistics in the sections include links to more detailed HTML reports. For example, if you click on the # *Layers* link under the *General Library Information* section of the HTML report, the software displays a detailed HTML report on the layers in the design.



Summary Report

Generated Date: Wed Nov 2 18:45:00 2005
Host Name: cds8994

Layer Information Page

Layer OVERLAP Information

Type	Overlap

Layer Metal6 Information

Type	Routing
Wire Pitch X	0.990 um
Wire Pitch Y	0.990 um
Offset X	0.330 um
Offset Y	0.330 um
Wire Width	0.440 um
Spacing	0.460 um
Line2Via	CAUTION: The line2via does not match the pitch

Layer Via56 Information

Type	Cut
Vias	For complete list click here

Layer Metal5 Information

Type	Routing
Wire Pitch X	0.660 um
Wire Pitch Y	0.660 um
Offset X	0.330 um
Offset Y	0.330 um
Wire Width	0.280 um
Spacing	0.280 um

Related Text Commands

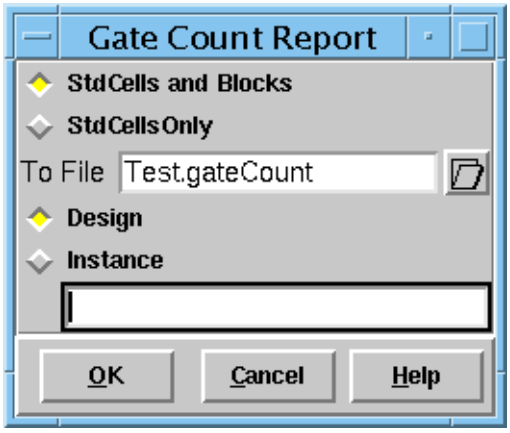
For information on the following command, see “General Commands” in the *Encounter Text Command Reference*.

- `summaryReport`

Gate Count Report

Use the Gate Count Report form to calculate the gate count based upon standard cells and blocks, or standard cells only. You can calculate gate counts for the entire design or for a specific instance.

➤ Choose *Design – Report – Gate Count*.



Gate Count Report Fields and Options

Std Cells and Blocks	Sets the gate count calculation for standard cells and blocks.
Std Cells Only	Sets the gate count calculation for standard cells only.
To File	Specifies the filename to which to output the report. The default file extension is `.gateCount`. Use this file extension so the report will display in the Encounter console.
Design	Calculates gate counts for the entire design.
Instance	Calculates gate counts for a specified instance. If you select this option, you must specify an instance name in the text field.

Related Text Commands

For information on the following command, see “General Commands” in the *Encounter Text Command Reference*.

■ `reportGateCount`

Netlist Statistics

Use the *Netlist Statistics* menu command to create a list of design statistics, such as number of cells, nets, pins, and instances. A summary of the netlist is printed to the Encounter console and a log file and saved in the run directory.

➤ To print a list of design statistics, choose *Design – Report – Netlist Statistics*.

Preferences

The Preferences form allows you to save custom preference settings to a file, load a previously saved file, or load default settings. The default settings are saved in the `enc.pref.tcl` file; custom settings can be saved with a different filename.

The Preference form also allows you to create, edit, apply, and save design keyboard shortcut commands (see Binding Key on page 288).

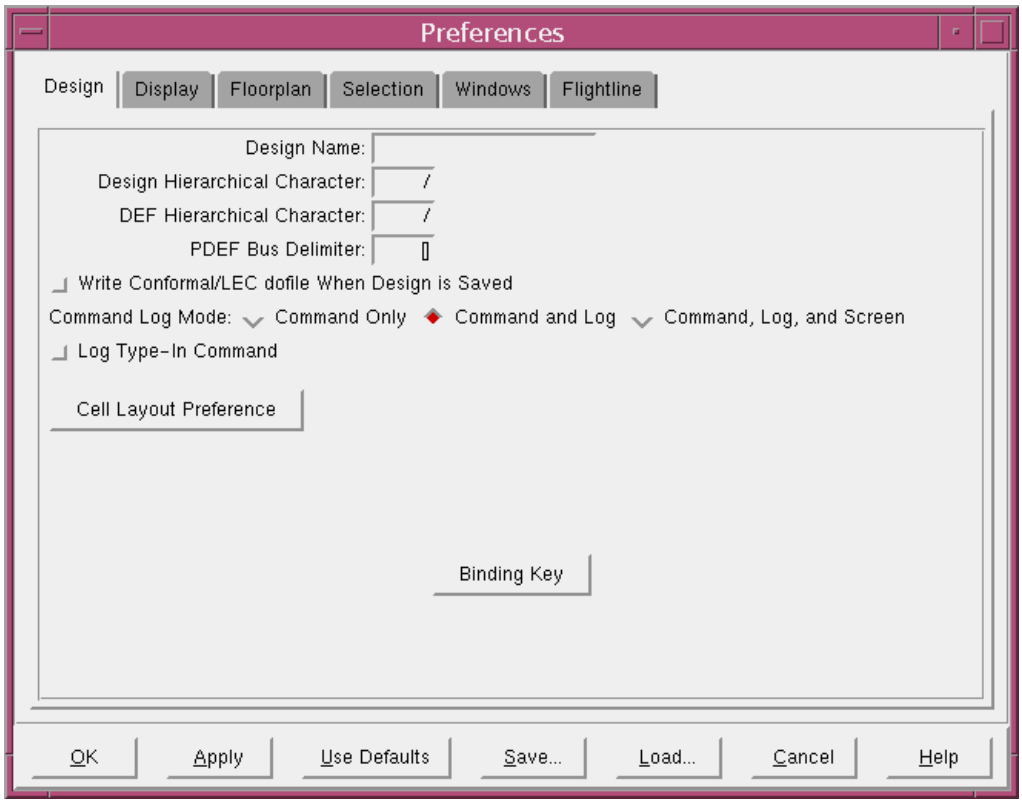
The Preferences form contains the following pages:

- Preferences – Design on page 266
- Preferences – Display on page 270
- Preferences – Floorplan on page 277
- Preferences – Selection on page 280
- Preferences – Windows on page 282
- Preferences – Flightline on page 284

Preferences – Design

Use the *Design* page of the Preferences form to set hierarchy levels in the netlist and DEF files, specify bus delimiters for PDEF files, denote output of command logs, and create binding key shortcuts. The default settings are saved in the `enc.pref.tcl` file; custom settings can be saved with a different filename.

➤ Choose *Design – Preferences* and click on the *Design* tab.



Preferences – Design Fields and Options

Design Name

Specifies the name of the design for which to set the preferences.

Design Hierarchical Char

Denotes the character being used as the hierarchy delimiter in a netlist. If the netlist uses another character, enter it in the text box and import the design.

Default: /

DEF Hierarchical Char

Denotes the character being used as the hierarchy delimiter in a DEF file. If the DEF file uses another character, enter it in the text box and load the DEF file. When writing a DEF file, the software uses the same character.

Default: /

PDEF Bus Delimiter

Denotes the character being used as the hierarchy delimiter in a PDEF file. If the PDEF file uses another character, enter it in the text box and load the PDEF file. When writing a PDEF file, the software uses the same character.

Default: `[]`

Write Conformal/LEC dofile when save design

When saving a netlist, this option saves a dofile (a set of commands contained in a specified file) for the Conformal® Equivalence Checking capabilities.

Default: Off

Command Log Mode

Specifies where the command log is written.

Default: cmd & log

cmd only Writes to the command file only.

cmd & log Writes to the command file and log files.

cmd & log & screen

Writes to the command file, log files, and screen.

Note: When writing to log file and screen, the commands are preceded with `<CMD>`.

Log Type-In Command

Logs whatever is manually entered (typed), to the command file.

In the case of `source` commands, only the `source` command is logged, and not the commands in the sourced file.

Default: Off

Cell Layout Preference

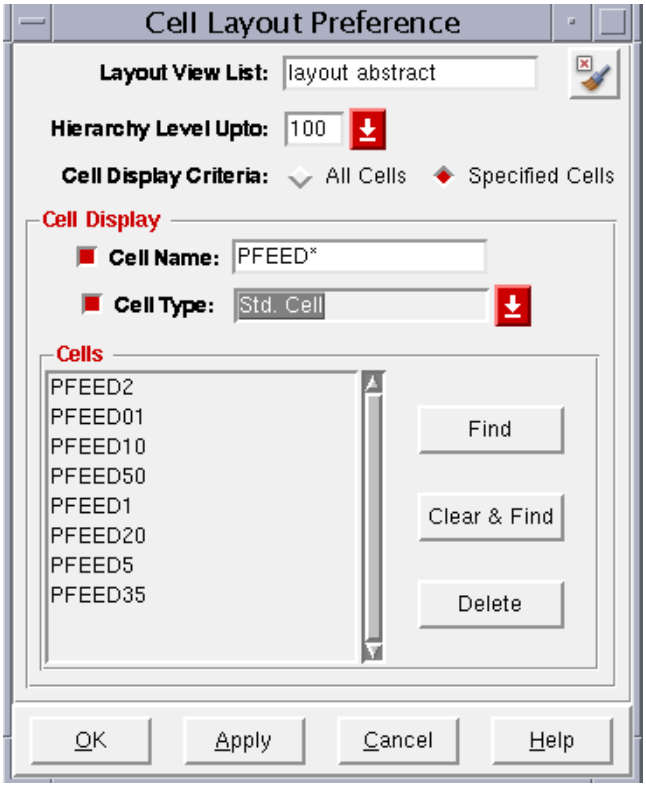
Opens the Cell Layout Preference form, which you can use to select the OA cells whose layout should be displayed. For more information, see Cell Layout Preference.

Binding Key — Opens the Binding Key form, which you use to edit or add binding keys. For more information, see Binding Key.

Cell Layout Preference

Use the Cell Layout Preference form to select the OA cells whose layout should be displayed. For information on displaying the OA cell layout, see Viewing OA Cell Layout in the “Getting Started” chapter of this document.

➤ In the Design Page of the Preferences form (Design – Preferences), click the Cell Layout Preference button.



Cell Layout Preference Form – Fields and Options

Layout View List — Displays the name of the layout view.

Removes cell layout data from memory.

Hierarchy Level Upto

	Specifies how many hierarchy levels should be displayed. The available options are: 0, 1,2, 3, 4, 5, and 100. *Default:* 100
Cell Display Criteria	
	All Cells: Displays the layout for all the cells. *Specified Cells*: Displays the layout for the specified cells. To specify the cells, us the *Cell Name* or the *Cell Type* field.
Cell Name	Specify the name of the cell(s) whose layout should be displayed. You can use wildcard (*) for the cell name.
Cell Type	Specify the type of cell(s) whose layout should be displayed. The available options are: Std. Cell, Block, Black Box, Partition, and IO. *Default:* Std. Cell.
Find	Displays the cells in the *Cells* display list.
Clear and Find	Clears the previous result and displays the cells in the *Cells* display list.
Delete	Removes the cells from the *Cells* display list. **Note:** The cells are not actually deleted; they are only removed from the *Cells* display list. When you click OK or Apply, the layout for only those cells that are in the Cells display list is shown.

Related Text Commands

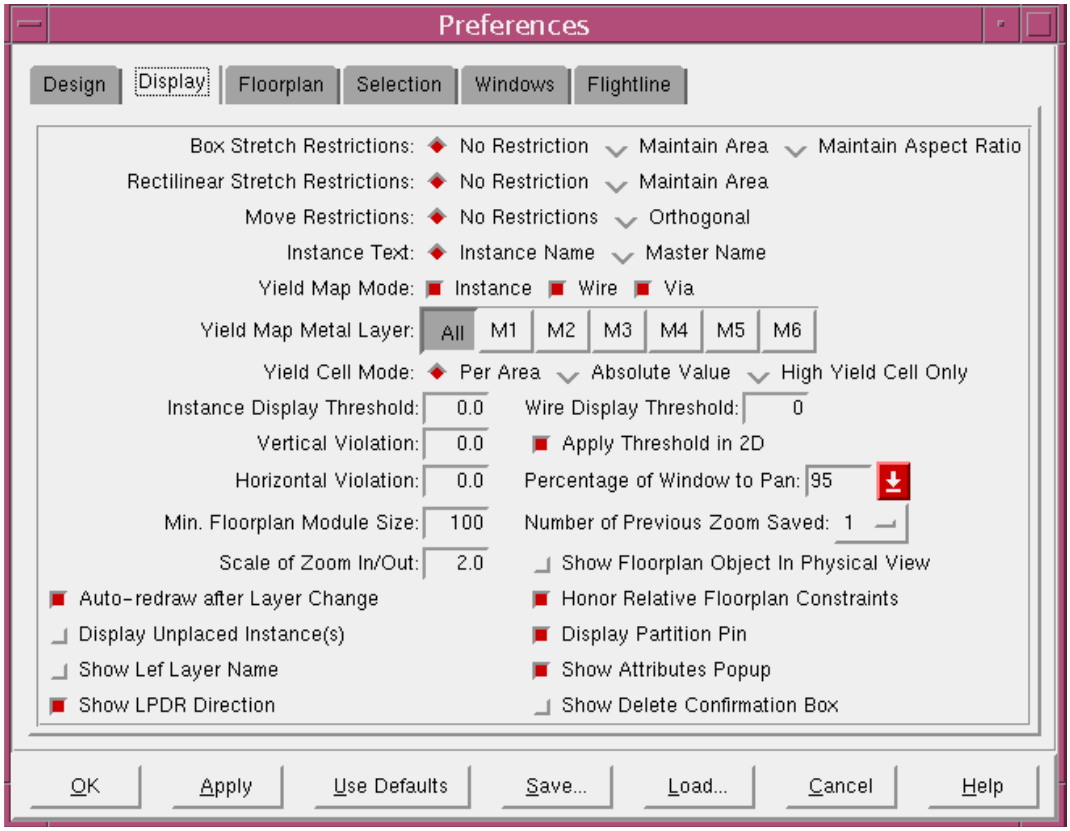
For information on the following commands, see “General Commands” in the *Encounter Text Command Reference*.

- `setLayerPreference`
- `setPreference`

Preferences – Display

Use the *Display* page of the *Preferences* form to set viewing preferences for standard cells, wires, route congestion ranges, modules, and objects. The default settings are saved in the `enc.pref.tcl` file; custom settings can be saved with a different file name.

➤ Choose *Design – Preferences* and click the *Display* tab.



Preferences – Display Fields and Options

Box Stretch Restrictions

No Restriction	No restrictions when resizing an object. *Default:* On
Maintain Area	Maintains the area of an object when resizing. This is applicable for edge stretching as well as for corner resizing. *Default:* Off

Maintain Aspect Ratio

Maintains the aspect ratio of an object when resizing.

Default: Off

Rectilinear Stretch Restrictions

No Restriction — No restrictions when resizing a rectilinear object.

Default: On

Maintain Area — Maintains the area of a rectilinear object when resizing.

Default: Off

Maintain Aspect Ratio

Maintains the aspect ratio of a rectilinear object when resizing.

Default: Off

Move Restrictions

No Restriction — No restrictions when moving an object.

Default: On

Orthogonal — Restricts the object moves to straight vertical and horizontal directions.

Default: Off

Instance Text

Instance Name — Displays the instance name for the block.

Default: On

Master Name — Displays the master name for the block.

Default: Off

Yield Map Mode — Controls the display of the defect-limited yield of one or more of the following: instances, wires, vias. Darker colors indicate higher yield.

Default: On (for all)

Yield Map Metal Layer

Specifies the metal layer for the yield map.

Default: All

Yield Cell Mode

Controls the display of yield cells. The Encounter software expresses yield as a cost, and uses different colors for different yield levels. Darker colors indicate higher yield.

Note: You must turn on the visibility of the yield cell layer to see the yield cells.

Default: Per Area

Per Area

Displays ten yield levels.

The software calculates the cell yield of each cell according to the cell yield probability value in the yield technology file. It divides the yield for each cell by the cell size to find the yield per area. Then ten levels are obtained by subtracting minimum yield per area from maximum yield per area and dividing the difference by ten. Each cell falling into one of these ten levels has a different color.

Absolute Value

Displays ten yield levels.

The software calculates the cell yield of each cell according to the cell yield probability value in the yield technology file. Then ten levels are obtained by subtracting minimum yield per area from maximum yield per area and dividing the difference by ten. Each cell falling into one of these ten levels has a different color.

High Yield Cell Only

Displays two yield levels for cells of the same function based on footprint.

The yield of high-yield cells is higher than the average yield of cells of the same function. The yield of low-yield cells is equal to or lower than cells of the same function.

Instance Display Threshold

Sets the draw size of the standard cell instance in the physical view. The default value of `0.0` draws all standard cells. A value of `2.0` draws fewer standard cells, thereby yielding faster draw speed. If you change this value, you must redraw the view by choosing *View – Redraw* from the menu.

Wire Display Threshold Sets the minimum number of pixels used to display a wire or via. This value works in conjunction with the *Apply Threshold in 2D* option.

At the chip level, set `1` for the *Wire Display Threshold* and turn off *Apply Threshold in 2D* to display all of the wires/vias in the design. If the display speed is too slow, then change either or both variables appropriately.

Vertical Violation and *Horizontal Violation*

Sets the range for vertical and horizontal route congestion display. The default value of `0.0` displays vertical and horizontal route-demand congestion values close to or greater than the vertical and horizontal route-resource value.

Vertical and horizontal violation values are the numbers in the diamond-shaped congestion symbols. Changing the value to a high value, such as `20.0`, can be used to display severe congestion symbols where the route-demand exceeds the route-resource by 20 or greater. Changing the value to a negative value, such as `-5.0`, will display several more congestion symbols where the route-demand is less than the route-resource by 5 or greater.

Apply Threshold in 2D Checks both width and height of a wire or via when used with *Wire Display Threshold*. When off, the wire or via is displayed if either its width or height meets the threshold. When on, both width or height must meet the threshold for the wire or via to be displayed.

Default: On

Percentage of Window to Pan

Specifies the percentage of display area that will be panned when you pan the display using the right or the left arrow keys.

Default: The default value is 95%.

Min. Floorplan Module Size

Filters out modules from the display in the Floorplan view that have an area less than the specified value. For example, a value of `100` displays all the modules that contain 100 or more instances. You can also add a small sized module to the Floorplan view by using the `addModuleToFPlan` text command.

Note: If modules or submodules contain at least one block, they are always displayed, regardless of the specified value.

Default: `100`

Number of Previous Zoom Saved

Specifies the number of zoom views that are saved. You can then view the previous zoom views by clicking the Zoom Previous icon or the bindkey `W`.

For example, if you set the number to 4, you can view four previous zoom views by clicking the Zoom Previous icon or the bindkey `W`.

Default: 1

Scale of Zoom In/Out Specifies the scale for the zoom in and zoom out feature. You can use a decimal number for the scale.

Show Floorplan Objects in Physical View

Enables the display and querying of floorplan objects in the physical view.

You can use this feature together with color groups to create a custom view. For example, you can create a color group that has a custom setting for block colors and use this color group while viewing floorplan objects in the physical view. For information on using color groups, see Creating and Editing Color Groups in the “Design Menu” chapter of this document.

Default: Off

Auto-redraw after Layer Change

Enables or disables auto-redraw when layers are changed.

Default: On

Honor Relative Floorplan Constraints

Determines whether interactive commands take into account the existing relative floorplan constraints.

For example, if you have two blocks called `blockA` and `blockB`, and `blockA` is relative to the right side of `blockB`:

- If *Honor Relative Floorplan Constraints* is enabled, when you move `blockB`, `blockA` also moves in such a way that it still stays on the right side of `blockB`. You cannot move `blockA` to another location because it must stay on the right side of `blockB`.
- If *Honor Relative Floorplan Constraints* is disabled, when you move `blockB`, `blockA` does not move with it, and can be freely moved to another location.

Default: On

Display Unplaced Instances

Displays unplaced cells in the Physical view.

Default: Off

Display Partition Pin

Displays partition pins.

Default: On

Show Lef Layer Name

Specifies that the layer name as specified in the LEF file should be displayed in the color bar.

Show LPDR Direction

Specifies that for designs that support X routing, the direction of the Local Preferred Direction Routing (LPDR) area should be displayed.

Show Attributes Popup

Specifies that the Context Pop-up Attribute Viewer, which is displayed when you place the mouse cursor over an object, should be displayed.

Show Delete Confirmation Box

Displays a dialog box that prompts for confirmation whenever you delete an object.

Default: Off

Related Text Commands

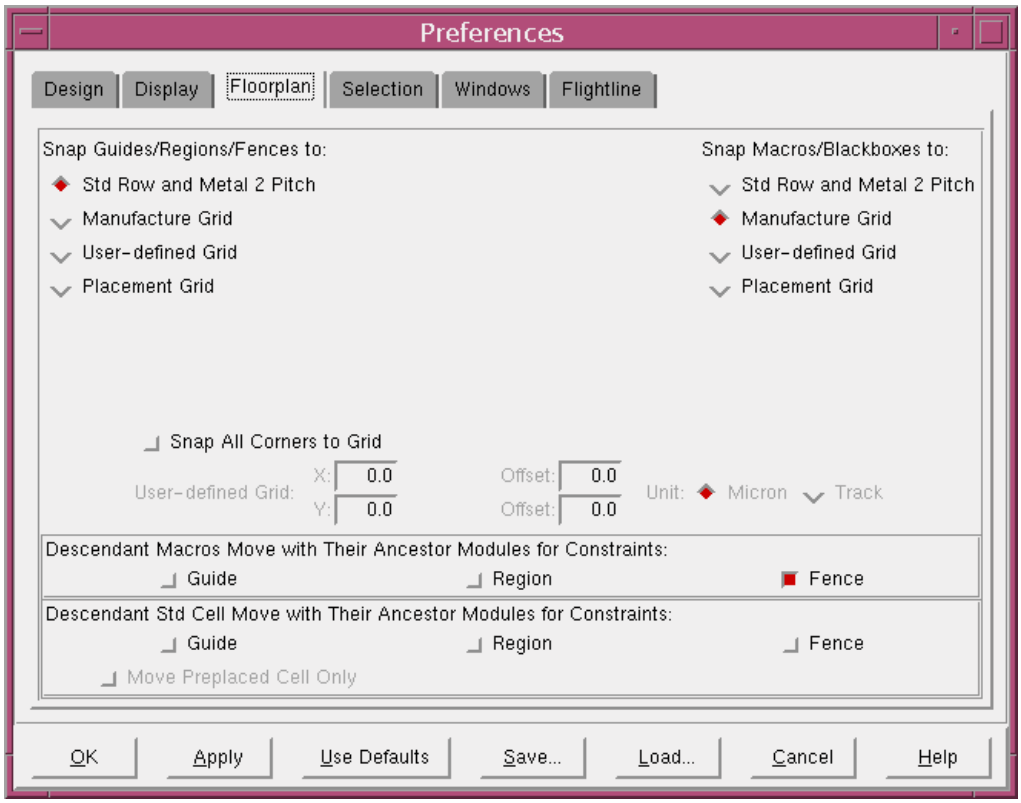
For information on the following commands, see “General Commands” in the *Encounter Text Command Reference*.

- `setLayerPreference`
- `setPreference`

Preferences – Floorplan

Use the *Floorplan* page of the Preferences form to set object behavior, including movement capabilities for guides regions, fences, snap macros, or blackboxes. The default settings are saved in the `enc.pref.tcl` file; custom settings can be saved with a different filename.

➤ Choose *Design – Preferences* and click the *Floorplan* tab.



Preferences – Floorplan Fields and Options

Snap Guides/Regions/Fences to and *Snap Macros/Blackboxes to*

Choose one of the following options:

Std Row and Metal 2 Pitch

(Default grid for modules) Snaps to a module guide. The default vertical snapping is the standard cell rows and the default horizontal snapping is the *metal2* pitch dimension, which is read from the technology file.

Manufacture Grid (Default grid for macros) Changes the default snapping to the manufacturing grid, which is read from the technology file. This is a finer grid snapping than the default.

User-defined Grid Optionally, you can change the default snapping to a grid defined in the *X* and *Y* location fields.

The *X* and *Y* fields are for the horizontal and vertical spacing between the user-defined snap grids. The *X* and *Y Offset* fields are for the distance values from the lower left corner of the design or die to the first x y grid, respectively.

By default, the *X* and *Y Offset* values are `0.0` microns. However, if you choose *User-defined Grid*, but do not provide the *X* and *Y* spacing values, you will get the error message: *User-defined grid should be greater than 0 for both X and Y direction*.

The user-defined grid is honored by the interactive move and stretch features in the *Snap Floorplan* menu command, and by the *Relative Floorplan* menu commands.

Placement Grid Changes the default snapping to the placement grid.

Descendant Macros Move with Their Ancestor Modules for Constraints

Guide Allows you to move guide objects with their descendant blocks (macros/blackboxes) when floorplanning.

Region Allows you to move region objects with their descendant blocks when floorplanning.

Fence (default) Allows you to move fence objects with their descendant blocks when floorplanning.

Note: If you move descendant blocks with a fence, blocks outside the fence boundary also move, but unplaced blocks will not move.

Descendant Std Cell Move with Their Ancestor Modules for Constraints

Guide Allows you to move guide objects with their descendant standard cells when floorplanning.

Region

Allows you to move region objects with their descendant standard cells when floorplanning.

Allows you to move objects with their descendant standard cells when floorplanning.

Note: If you move descendant standard cells with a fence, standard cells outside the fence boundary also move, do unplaced cells do not move.

Fence (default)

Allows you to move objects with their descendant standard cells when floorplanning.

Note: If you move descendant standard cells with a fence, standard cells outside the fence boundary also move, do unplaced cells do not move.

Move Preplaced Cell Only

Allows you to move only preplaced descendant cells with their group, region, and fence when floorplanning.

Note: When this option is not selected, all descendant cells, preplaced or not, move with the guide, region, and fence.

Related Text Commands

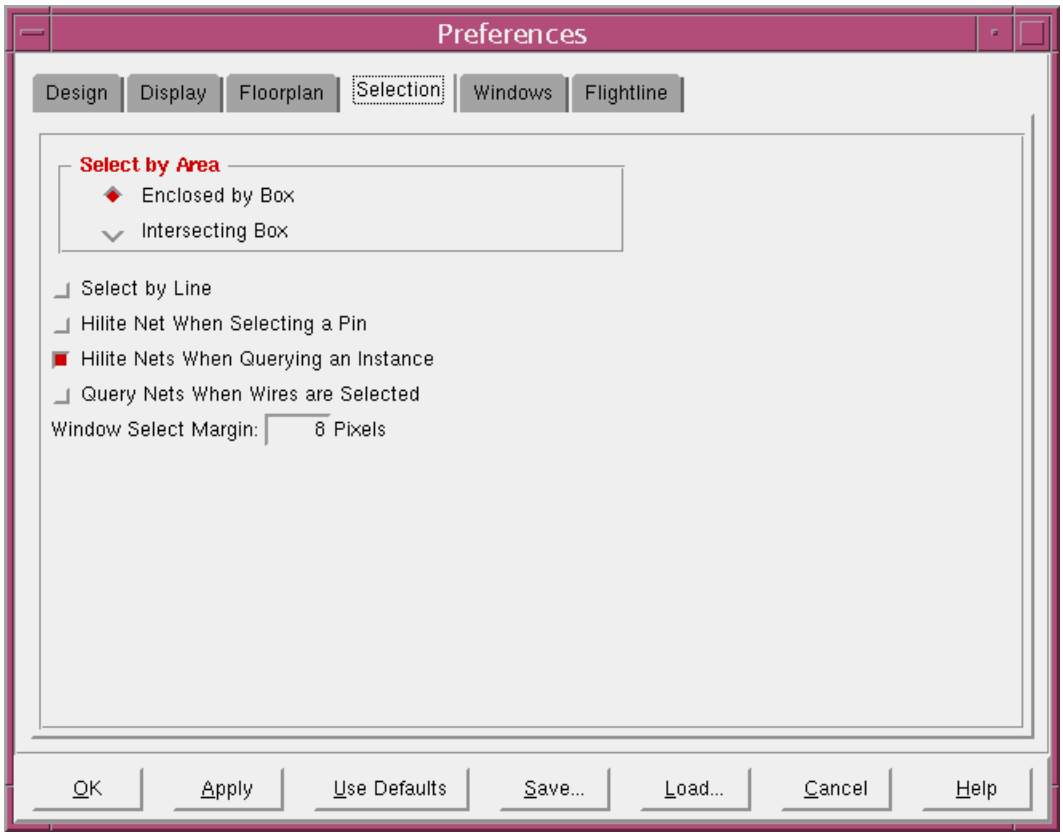
For information on the following commands, see “General Commands” in the *Encounter Text Command Reference*.

- `setLayerPreference`
- `setPreference`

Preferences – Selection

Use the *Selection* page of the Preferences form to select and display objects and determine their behavior within a selected area. The default settings are saved in the `enc.pref.tcl` file; custom settings can be saved with a different filename.

➤ Choose *Design – Preferences* and click the *Selection* tab.



Preferences – Selection Fields and Options

Enclosed by Box	Selects objects that are fully enclosed inside the specified area. Use the left mouse button to draw and define an area or bounding box. Any objects fully enclosed inside the drawing area are selected. *Default:* On

Intersecting Box
Selects objects that are fully enclosed or intersected within the specified area. Use the left mouse button to draw and define an area or bounding box. Any objects enclosed inside or intersected with the area bounding box are selected. This mode should be used to select wire or row.
Default: Off

Select by Line
Specified that objects can be selected by drawing a line that crosses the objects.

When you select this option and then choose the Select widget from the main menu, you can draw a line across several objects in the GUI; all the objects that the line crosses are selected.
Default: Off

Hilite Net When Selecting a Pin

Highlights a net through a pin selection. If this option is set when you select a pin, the corresponding net is highlighted.
Default: Off

Hilite Nets When Querying an Instance

Highlights nets that are connected to an instance when this instance is queried. For example, if you query a selected instance and this option is set, all nets that connect to this instance pin are also highlighted.
Default: On

Query Nets When Wires are Selected

Queries all nets that connect to the selected wires.
Default: Off

Window Select Margin
Specifies the number of pixels for the window margin.
Default: 8

Related Text Commands

For information on the following commands, see “General Commands” in the *Encounter Text Command Reference*.

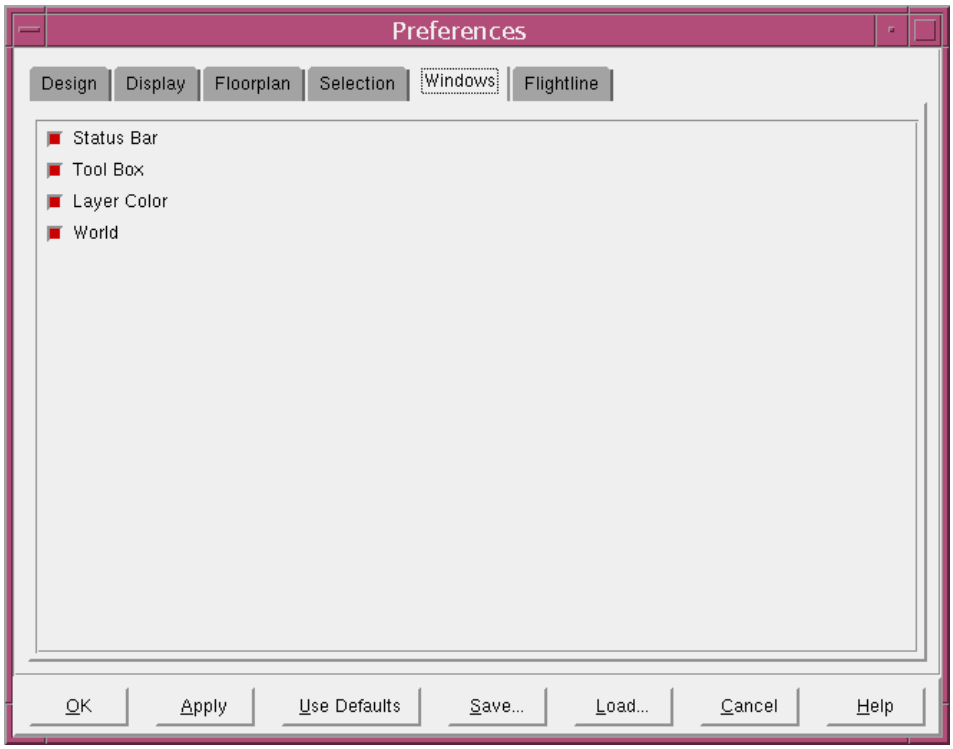
- `setLayerPreference`
- `setPreference`

Preferences – Windows

Use the *Windows* page of the Preferences form to show or hide Encounter main display windows. When you click the *OK* or the *Apply* button, the Windows settings are saved in the `.enc` file in your home directory. When you launch a new session, the settings in the `.enc` file are loaded automatically. The Windows settings are also saved in the `.enc` file when you click the Save button and save the other settings for Design, Display, Floorplan, and Selection in the `.enc.pref.tcl` or some other file.

Note: This page shows the same windows that are selected or deselected in the *Show/Hide* menu.

➤ Choose *Design – Preferences* and click the *Windows* tab.



Preferences – Windows Fields and Options

Properties

Controls the Attribute Viewer panel that appears when you place the cursor over an object. See Context Pop-up Attribute Viewer for more information.

Default: On

Status Bar	Controls the message bar display below of the main design display area, which shows object identifier or coordinate information. *Default:* On
Status Bar	Controls the message bar display below of the main design display area, which shows object identifier or coordinate information. *Default:* On
Tool Box	Controls the tool widget display above the design display area. See Tool Widgets on page 72 for more information. *Default:* On
Layer Color	Controls the visibility, selectability, and color display of various attributes at the top right side of the main window. *Default:* On
World	Controls the satellite window display at the lower right side of the main window. See Satellite Window for more information. *Default:* On

Related Text Commands

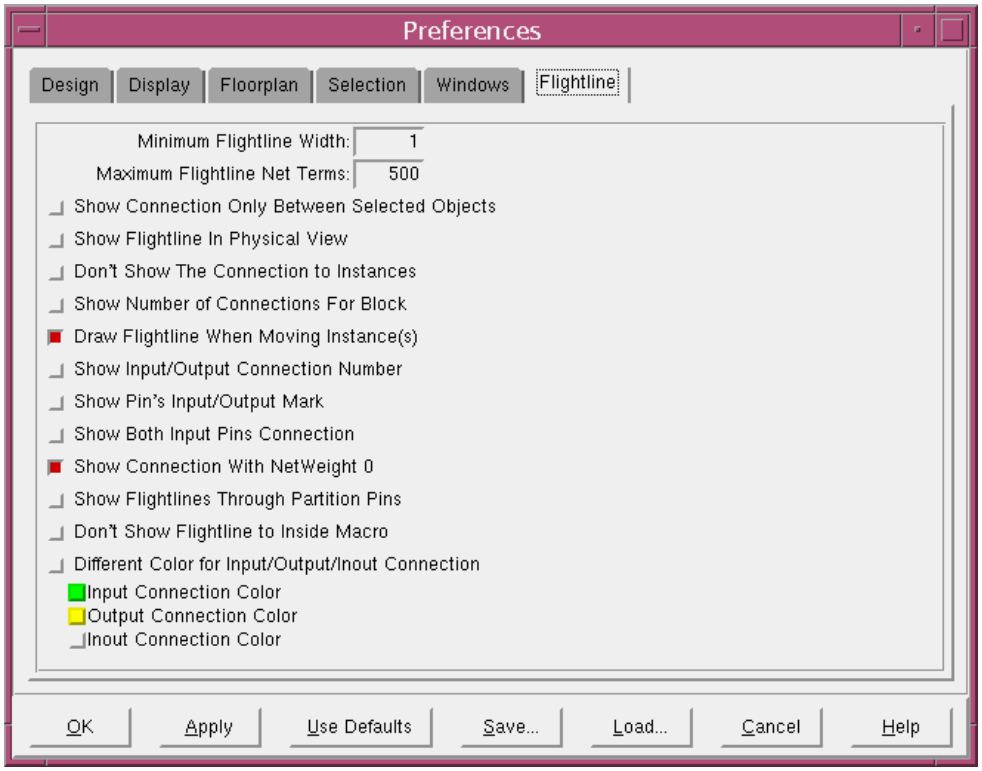
For information on the following commands, see “General Commands” in the *Encounter Text Command Reference*.

- `setWindowPreference`

Preferences – Flightline

Use the *Flightline* page of the Preferences form to set options for displaying net connections in the design.

➤ Choose *Design – Preferences* and click the *Flightline* tab.



Preferences – Flightline Fields and Options

Minimum Flightline Width

Sets the minimum connection threshold in order for flightlines to be displayed in the Floorplan view. For example, a threshold value of 5 displays flight lines that have 5 or more connections between modules and blocks.

Default: 1 (Displays all flight lines)

Maximum Flightline Net Terms

Sets the maximum connection threshold in order for flightlines to be displayed in the Floorplan view. For example, a value of `500` displays the flight lines for nets that have 500 terminals or less.

Default: `500`

Show Connection Only Between Selected Objects

Displays only the net connections between the selected objects.

Default: Off

Show Flightline In Physical View

Displays net connections in the Physical view.

Default: Off

Don't Show The Connection to Instances

Does not display net connections to instances, including blocks.

Default: Off

Show Number of Connections For Block

Displays the number of net connections from a selected block.

Default: Off

Draw Flightline When Moving Instance(s)

Displays net connections for instances when you move them.

Default: On

Show Input/Output Connection Number

Displays the total number net connections, the number of input connections, and the number of output connections for a selected block.

For example, if there are 23 total connections for the selected block and they are all output connections, the main window displays the following numbers: `23/0/23`.

Note: The software does not include I/Os in the total for output connections. Therefore, if the software displays a number such as: `10/5/4`, this indicates that one of the output connections is an I/O.

Default: Off

Show Pin's Input/Output Mark

Displays a symbol that distinguishes whether the pin is an input or an output pin on the block. The software displays an "o" for output pins, and an "x" for input pins.

Default: Off

Show Both Input Pins Connection

Displays net connections between inputs pins of two blocks or modules.

Default: Off

Show Connection With Netweight 0

Displays flightlines for nets that have a weight of `0`.

Default: On.

Show Flightlines Through Partition Pin

Displays net connections to partition pins. If this checkbox is off, the software displays net connections to instances inside partition blocks, but not does not display the connection to the partition pins.

This option can be useful for checking pin assignment results, especially for the un-committed partition pins.

Default: Off

Don't Show Flightlines to Inside Macro

Disables the display of the flightlines to macros that are embedded inside a module.

Default: Off

Different Color for Input/Output/Inout Connection

Displays the input, output, and inout net connections using different colors.

Default: Off

Input Connection Color

Specifies the color to use for input net connections. Click on the colored box to open the Color form.

Default: Green.

Output Connection Color

Specifies the color to use for output net connections. Click on the colored box to open the Color form.

Default: Yellow.

Inout Connection Color

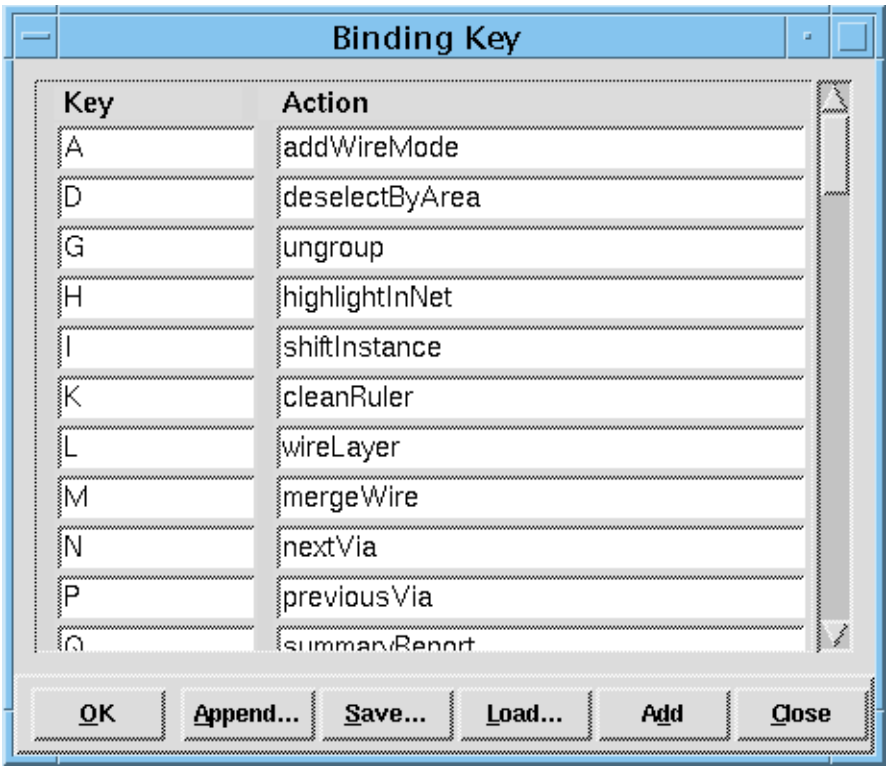
Specifies the color to use for inout net connections. Click on the colored box to open the Color form.

Default: Pink.

Binding Key

Use the Binding Key form to load, save, create, or define keyboard shortcut commands. You can sort either column by selecting the *Key* or *Action* label at the top of the form. For a description of these default binding keys, see "Default Binding Key Settings" on page 289.

➤ Choose *Design – Preferences* to open the *Design* page of the Preferences form and click the *Binding Key* button, or click the b key in the Encounter Main Window.



Binding Key Fields and Options

OK	Applies your changes to the design session and closes the window
Append	Opens the Append Binding Key to File form to appends the specified binding key to the selected Tcl file. **Note:** If a binding key is appended with conflicting Tcl file information, the last information read in the file takes precedence and is used.

Save	Opens the Append Binding Key to File form to save your changes to a Tcl file.
Load	Opens the Append Binding Key to File form to load binding key functionality from an existing Tcl file.
Add	Adds an new line to the end of the Binding Key table, where you can specify the key and the action. To create a new binding key shortcut, enter a new letter in the *Key* text field and add an action associated with the key by typing the new command in the text window. To edit an existing binding key shortcut, enter a letter associated with a shortcut command in the *Key* text field, and edit the action associated with the key by typing the new command in the text window.
Close	Closes the window without applying any changes.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `bindKey`

Default Binding Key Settings

The following table lists the default settings for the binding keys. In many cases, binding keys are context specific and behave differently depending on the mode that is active.

Important

You can modify these binding keys at any time; however, it is recommended that you use the default settings because some of the keyboard commands are not available through the GUI.

Key	Action	Default Behavior
A	addWireMode	Activates the Add Wire tool.
D	deselectByArea	Deselects the objects area
G	hierDown	

Key	Action	Default Behavior
H	highlightInternalNets	Highlights the internal net connections on a selected object.
I	shiftInstance	Opens the Shift Instances/Modules form to spaces instances horizontally or vertically.
K	cleanRuler	Removes all rulers from the display.
L	changeWireLayer	Changes the layer of selected power or signal wire segments.
M	mergeWire	Merges all wires of the same width, layer, and net that are collinear with, and electrically connected to, a selected wire.
N	nextVia	Displays the next via that has the same LEF rule as the selected via.
P	previousVia	Displays the previous via that has the same LEF rule as the selected via.
Q	summaryReport	Gives the summary report of the select object.
R	resizeMode	Sets the mode to resize an object in the design.
S	getWireInfo	Outputs information on the selected wire.
T	trimWire	Trims all selected special wires so that no antennas remain.
U	redo	Redoes the last action.
W	changeWireWidth	Changes the width of special wires.
X	cutWireMode	Activates the Cut Wire tool.
Z	zoomOut	Zooms out the display area by 2X.
a	selectMode	Activates the Select tool.
b	bindKeyForm	Opens the Binding Key form.
c	copySpecialWire	Copies the selected wire.
d	popUpDelete	Opens the Select/Delete Routes form
e	popUpEdit	Opens the Edit Route form
f	fit	Fits the design to the screen.
g	hierUp	

Key	Action	Default Behavior
h	highlightExternalNets	Highlights the external net connections of a selected object.
i	spaceInstance	Opens the Space Instances/Modules form to spaces instances horizontally or vertically.
k	createRuler	Activates the Ruler tool.
m	moveWireMode	Activates the Move Wire tool.
n	queryNext	Queries on the next overlapping object.
o	addViaMode	Activates the Add Via tool.
p	queryPrevious	Queries on the previous overlapping object.
q	attributeEditor	Opens the Attribute Editor on a selected object.
r	rotateInstance	Rotates an instance around its origin
s	stretchWireMode	Activates the Stretch Wire tool.
t	ciopReportTilePinStatus	Displays a report in the console window showing the Current Core Area, the Tile Signal Count, and the Driver Signal/Cell Count Summary.
u	undo	Undoes the last action.
w	previousView	Resets the display to its previous design view before a pan or zoom.
x	clearDrc	Clears all design rule checking (DRC) markers in your design.
z	zoomIn	Zooms in the display area.
F2	saveDesign	Saves the files for design import, floorplan, placement, and route.
F3	displayForm	Displays the appropriate form for an action, if available.
F8	printQuery	Prints *Auto Query* text messages to the Encounter console.
F9	metalBrightness	Sets the brightness for metal layer colors.
F11	metalLighter	Sets the brightness for metal layers in the Power-Grid Data Base (PGDB)

Key	Action	Default Behavior
`Up`	panUp	Pans up in the window.
`Down`	panDown	Pans down in the window.
`Left`	panLeft	Pans left in the window.
`Key-1`	toggleM1Visibility	Changes the visibility setting for the first metal layer.
`Key-2`	toggleM2Visibility	Changes the visibility setting for the second metal layer.
`Key-3`	toggleM3Visibility	Changes the visibility setting for the third metal layer.
`Key-4`	toggleM4Visibility	Changes the visibility setting for the fourth metal layer.
`Key-5`	toggleM5Visibility	Changes the visibility setting for the fifth metal layer.
`Key-6`	toggleM6Visibility	Changes the visibility setting for the sixth metal layer.
`Key-7`	toggleM7Visibility	Changes the visibility setting for the seventh metal layer.
`Key-8`	toggleM8Visibility	Changes the visibility setting for the eighth metal layer.
`Key-9`	toggleM9Visibility	Changes the visibility setting for the ninth metal layer.
`Right`	panRight	Pans right in the window.
`Space`	selectNext	Toggles object selections on top of each other.
`Delete`	deleteSelected	Deletes the selected instance.
`Escape`	cancel	Aborts the action during the an interactive command.
`Ctrl-a`	instAlignment	Opens the Align Instances/Modules form to align instances horizontally or vertically.
`Ctrl-c`	interrupt	If typed once, interrupts any process once within Encounter; if typed twice, exits out of Encounter.

Key	Action	Default Behavior
`Ctrl-d`	deselectAll	Deselects all selected object and object groups in the design display.
`Ctrl-h`	clearModuleNets	
`Ctrl-l`	legalizeFloorplan	Opens the Legalize Floorplan form.
`Ctrl-n`	snapFloorplan	Opens the Snap Loaded Floorplan form
`Ctrl-q`	queryCongest	Reports congestion on an area.
`Ctrl-r`	redraw	Redraws the window.
`Ctrl-s`	splitWire	Splits a single wire segment into multiple segments at points connected to other wires.
`Ctrl-w`	deleteQueryObj	Deletes the queried segment or via when in *Auto Query* mode.

Mode Setup

The Mode Setup form enables you to set global parameters for specific applications in the Encounter software.

The Mode Setup form contains the following pages:

- Mode Setup – Clock Mesh on page 295
- Mode Setup – CTS on page 303
- Mode Setup – Filler on page 314
- Mode Setup – NanoRoute on page 316
- Mode Setup – Optimization on page 338
- Mode Setup – Placement on page 343
- Mode Setup – ScanReorder on page 352
- Mode Setup – StreamOut on page 354
- Mode Setup – TieHiLo on page 357
- Mode Setup – Trial Route Mode on page 359

Mode Setup – Clock Mesh

The Mode Setup – Clock Mesh page enables you to set various global clock mesh parameters that are used for clock mesh synthesis, analysis, and optimization.

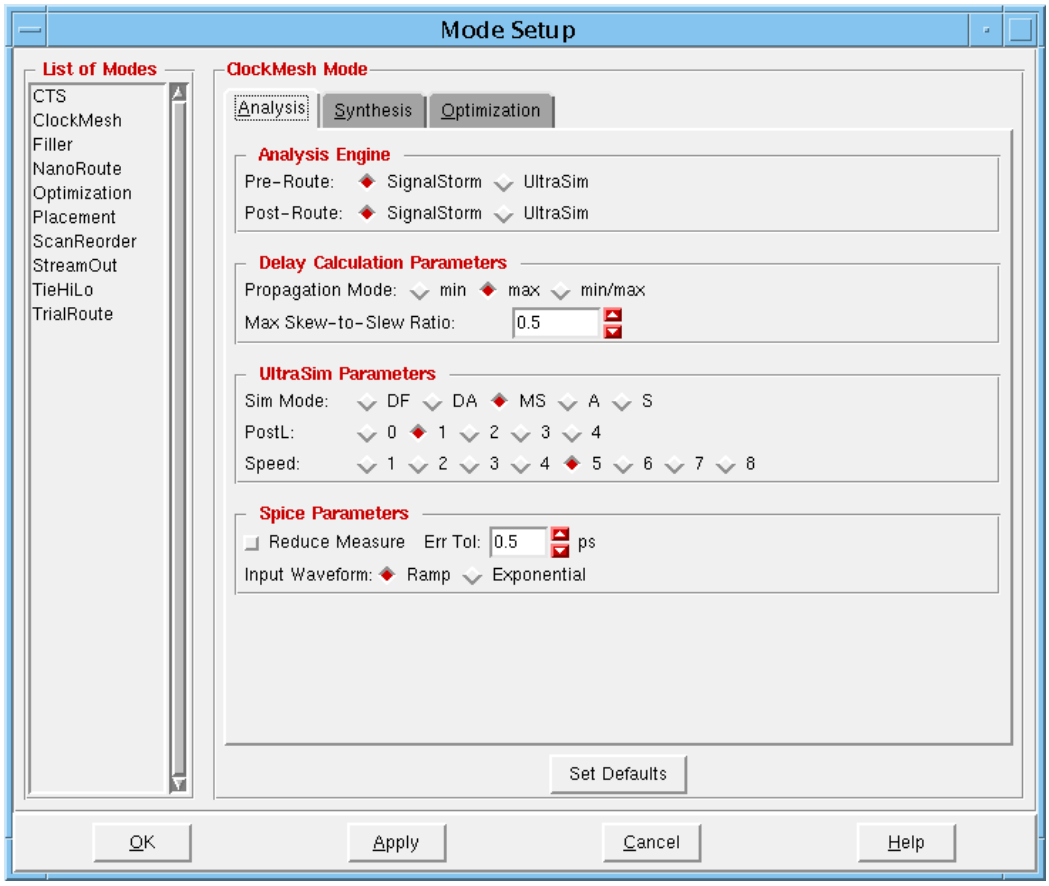
The Mode Setup – Clock Mesh page contains the following subpages:

- Clock Mesh – Analysis on page 296
- Clock Mesh – Synthesis on page 299
- Clock Mesh – Optimization on page 301

Clock Mesh – Analysis

Use the *Analysis* page to set global clock mesh analysis parameters used for defining the analysis engine, delay calculation parameters, and postroute simulation parameters.

➤ Choose *Design – Mode Setup* and select *Clock Mesh*.



Fields and Options

Pre-Route

Determines whether the clock mesh software uses integrated SignalStorm or the Virtuoso® UltraSim™ fast SPICE simulator for preroute mesh analysis.

Default: *SignalStorm*

Post-Route

Determines whether the clock mesh software uses integrated SignalStorm or the Virtuoso® UltraSim™ simulator for postroute mesh analysis.

Default: *SignalStorm*

Propagation Mode

Controls how the clock mesh delay calculator propagates timing through a net with multiple drivers.

Default: *max*

min	Specifies that each driver should take the minimum value for delay and transition among all driver inputs.
max	Specifies that each driver should take the maximum value for delay and transition among all driver inputs.
min/max	Specifies that each driver receives its actual transition and delay values.

Max Skew-to-Slew Ratio

Specifies a ratio of input skew to input slew (for parallel net drivers) above which the clock mesh software issues a warning.

Default: *0.5*

Sim Mode

Specifies the Virtuoso UltraSim simulator mode parameters that control simulation performance and accuracy.

See the *Virtuoso® UltraSim User Guide* for details on simulation modes.

Default: MS

DF	Specifies the *digital fast* simulation mode.
DA	Specifies the *digital accurate* simulation mode.
MS	Specifies the *mixed-signal* simulation mode.
A	Specifies the *analog* simulation mode.
S	Specifies the *SPICE* simulation mode.

PostL

Specifies the Virtuoso UltraSim simulator post-layout level.

Default: *1*

Speed

Specifies a Virtuoso UltraSim simulator speed/accuracy setting.

A setting of *1* represents the slowest simulation speed but produces the most accurate result.

A value of *8* represents the fastest simulation speed but produces the least accurate results.

Default: *5*

Reduce Measure

Eliminates SPICE measure statements for nodes that are likely to have timing that is very similar to other nodes.

Default: Off

Err Tol

Determines the threshold (in picoseconds) that controls which measure statements can be eliminated if *Reduce Measure* is selected. This value is an estimate.

Input Waveform

Controls the shape of the waveform provided as stimulus at the clock mesh root during netlist generation (and simulation).

Regardless of the shape, the waveform parameters are chosen so that the measured rise and fall times (between appropriate measuring voltages) match the specified root transition time.

The input waveform shape can be expected to have some impact on the cell delay (and to a lesser extent, output transition time) of the first logic level of the clock mesh (that is, the root cell, the first top-chain buffer, or the first pre-drive stage), but negligible impact overall. In terms of overall mesh timing, for most cases, the input waveform shape will have a small impact on total latency, and little or no impact on final skew.

Default: Ramp

Ramp

Generates a simple piece-wise linear ramp shape, using PWL function.

Exponential

Generates an exponential waveform, using EXP function.

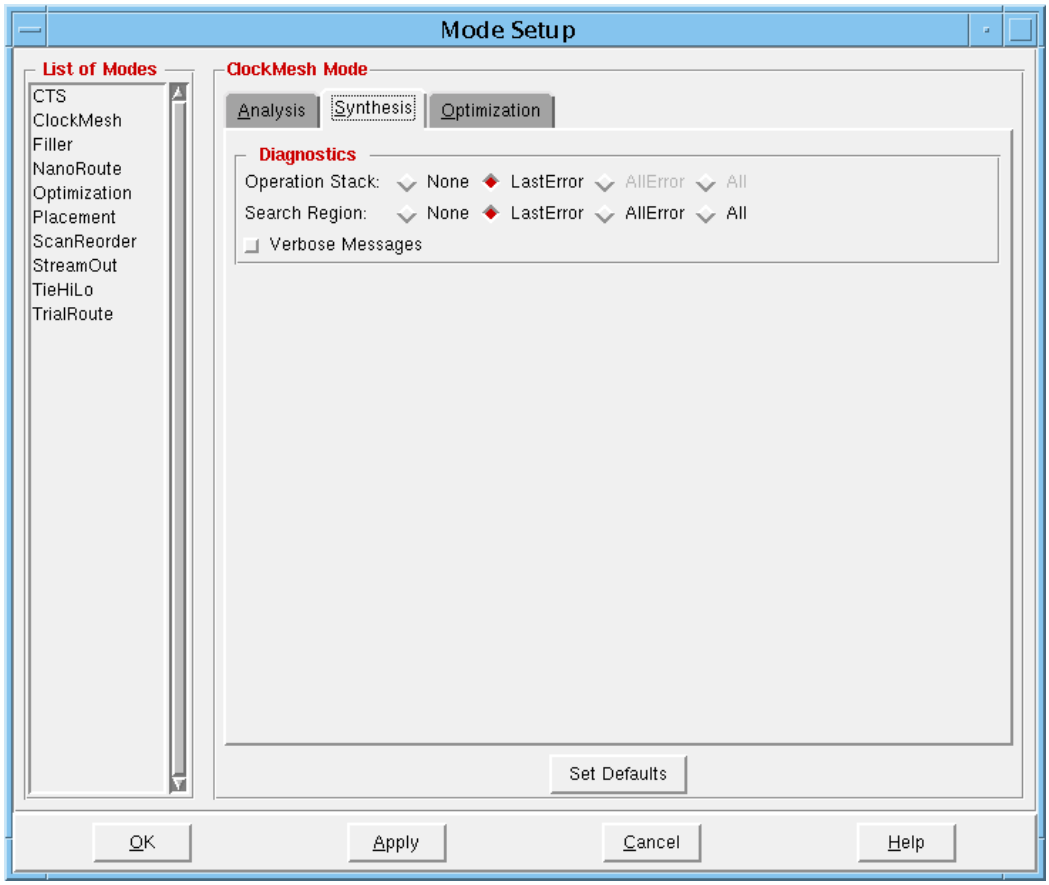
Related Text Commands

- `setClockMeshMode`
- `getClockMeshMode`

Clock Mesh – Synthesis

Use the *Synthesis* page to set global clock mesh diagnostic parameters.

➤ Choose *Design – Mode Setup*, then select *Clock Mesh*, then select *Synthesis*.



Fields and Options

Operation Stack

Specifies whether to create diagnostic stack information for failures during clock mesh synthesis.

Default: Last Error

None	No diagnostic stack information is created.
Last Error	Displays diagnostic stack information for the last failing synthesis step.

Search Region	Enables the temporary display of region markers for various wire and placement checks during clock mesh synthesis. *Default: Last Error*	
	None	No search regions are displayed.
	Last Error	Displays regions for the last failing search.
	All Error	Displays regions for all failing searches.
	All	Displays regions for all searches (successful and failing).
Verbose Messages	Generates more verbose messages during clock mesh synthesis. *Default*: Off	

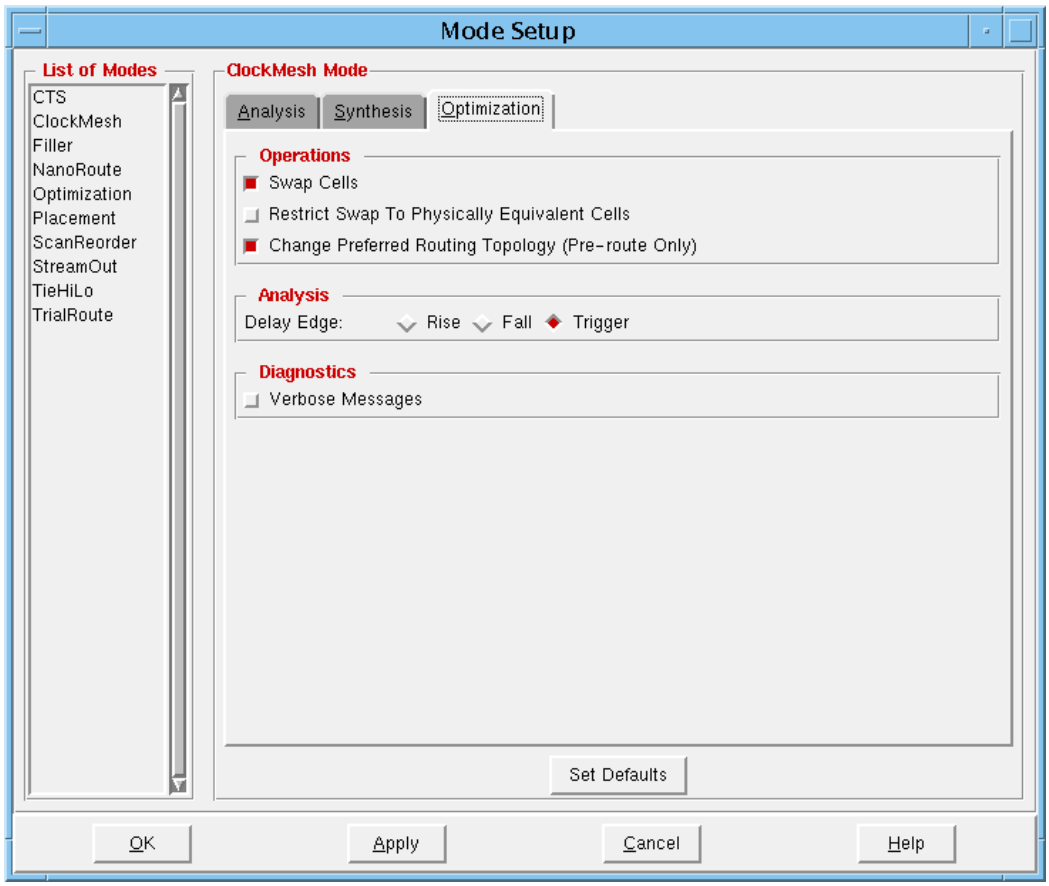
Related Text Commands

- `setClockMeshMode`
- `getClockMeshMode`

Clock Mesh – Optimization

Use the *Optimization* page to set global clock mesh optimization parameters. These parameters are used whenever the software optimizes local tree timing after local trees have been synthesized.

➤ Choose *Design – Mode Setup*, then select *Clock Mesh*, then select *Synthesis*.



Fields and Options

Swap Cells	Enables cell swapping. *Default:* On

Restrict Swap To Physically Equivalent Cells

Restricts cell swapping to only cells that are physically equivalent (same size, pin geometry, obstruction geometry). This feature can be useful during post-route optimization because it restricts the cell changes to those that do not require ECO place-and-route.

Default: Off

Change Preferred Routing Topology (Pre-route Only)

Changes the routing topology for local tree nets, in order to improve skew and transition.

Note: This option has no effect if the local trees already have been routed.

Default: On

Delay Edge

Specifies which edge to use for optimizing skew.

Default: Trigger

Rise	Minimizes skew based on the rising edge of the flops.
Fall	Minimizes skew based on the falling edge of the flops.
Trigger	Minimizes skew based on the trigger edge of the flops.

Verbose Messages

Generates more verbose messages during optimization.

Default: Off

Related Text Commands

- `setClockMeshMode`
- `getClockMeshMode`
- `optimizeClockMesh`

Mode Setup – CTS

The Mode Setup – CTS page enables you to specify global parameters for performing clock tree synthesis (CTS).

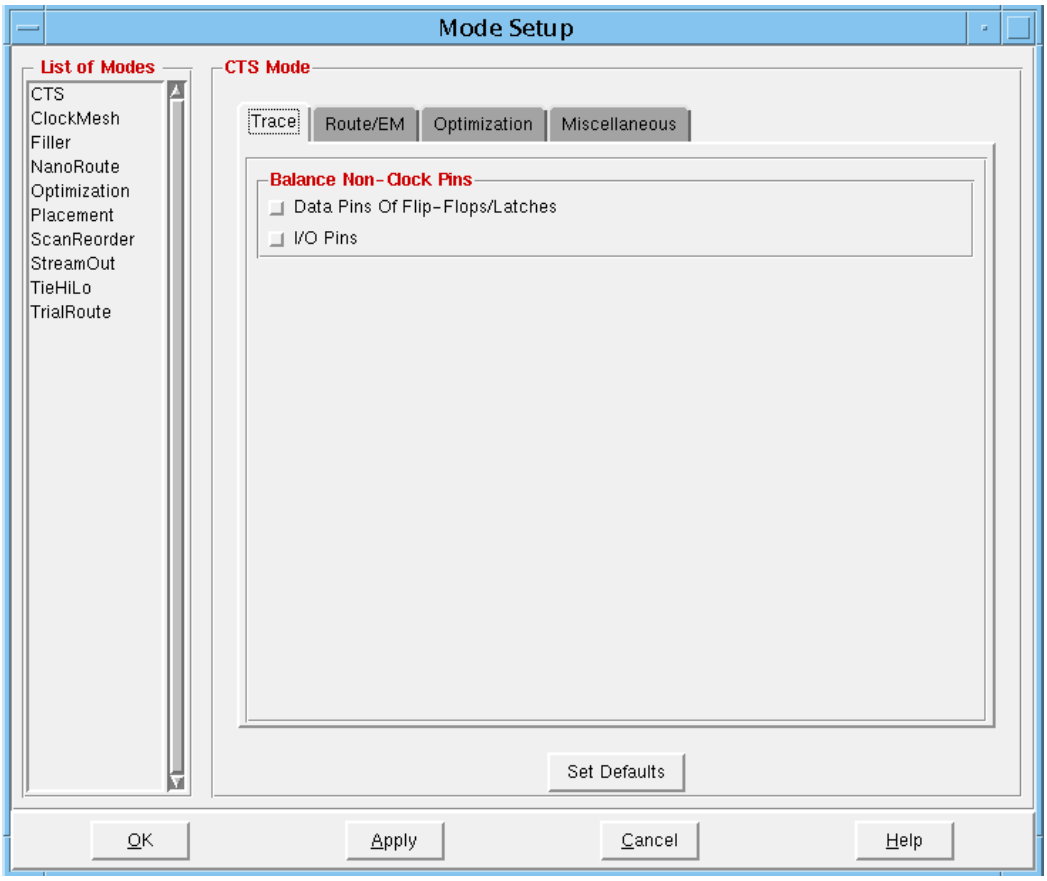
The Mode Setup – CTS page contains the following subpages:

- CTS – Trace on page 304
- CTS – Route/EM on page 306
- CTS – Optimization on page 309
- CTS – Miscellaneous on page 311

CTS – Trace

Use the *Trace* page to specify how CTS should treat pins when tracing through the clock tree.

➤ Choose *Design – Mode Setup* and select *CTS*.



Fields and Options

Data Pins of Flip-Flop/Latches

Treats Data pins of flip-flops and latches as synchronous pins, instead of as excluded pins. Data pins include:

- Data pins
- Enable pins
- Scan-in pins
- Scan-enable pins
- Synchronous set and reset pins

Default: Off

I/O Pins

Treats I/O pins as synchronous pins, instead of as excluded pins.

Default: Off

Related Text Commands

- `setCTSMode`
- `getCTSMode`

CTS – Route/EM

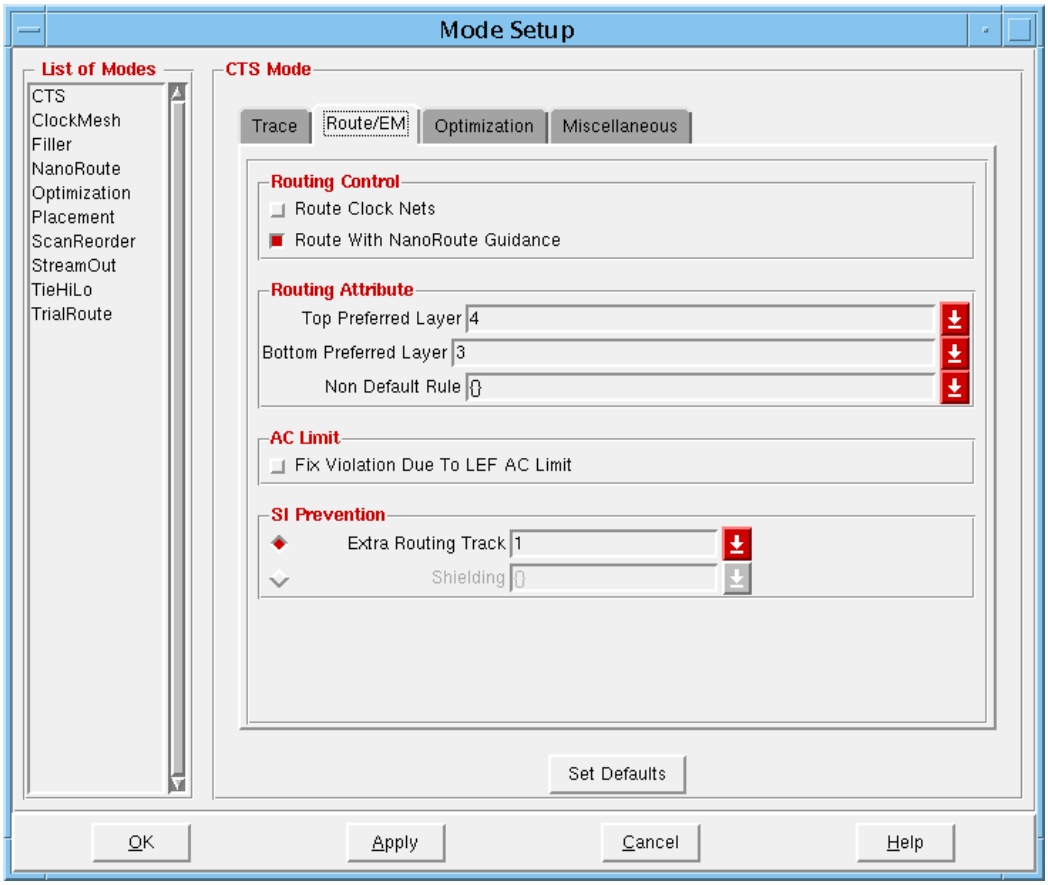
Use the *Route/EM* page to define routing attributes that CTS should use if no routing attribute section is specified for a clock tree in the clock tree specification file.

Note: CTS applies any routing constraints that you set using the *Route/EM* page globally to the design. However, any routing constraints that you set with the `RouteType` statement in the clock tree specification file take precedence over settings you make with this page.

Follow these general guidelines when you are considering routing constraints for your design:

- Use the `RouteType` statement in the clock tree specification file to set routing constraints on *particular clocks* in your design.
- Use the *Route/EM* page or the `setCTSMode` command to set routing constraints on *all other* clocks in your design.

➤ Choose *Design – Mode Setup* and select *CTS*, then select *Route/EM*.



Fields and Options

Route Clock Nets

Routes clock nets.

Default: Off

Route With NanoRoute Guidance

Specifies that Nanoroute should use the CTS-generated route guide file when routing clock nets.

The route guide marks routable gcells for the trunk portion of the net, and provides a list of pins per clock net that should be connected first, to maintain a balanced route topology.

Note: This option only takes effect if the *Route Clock Nets* option is selected.

Default: On

Top Preferred Layer

Specifies the top preferred metal layer for routing the clock tree.

Default: 4

Bottom Preferred Layer

Specifies the bottom preferred metal layer for routing the clock tree.

Default: 3

Non default Rule

Specifies the `LEF NONDEFAULTRULE` statement that the router should use.

Fix Violation Due To LEF AC Limit

Attempts to minimize EM violations during synthesis by resizing or inserting buffers to enhance the electrical current flow through the wires. If any wire exceeds the library value, CTS reports the violation in the standard CTS report.

Note: In order to perform EM analysis and optimization, your LEF file must contain an AC Limit table. You must also specify the `Period` statement in the clock specification file. You can use `clockDesign -genSpecOnly` to convert the period value from the SDC constraints.

Default: Off

Extra Routing Track	Specifies the extra space (in tracks) to add around clock wires, when routing the nets. *Default:* 1
Shielding	Specifies the ground net. *Default:* Off

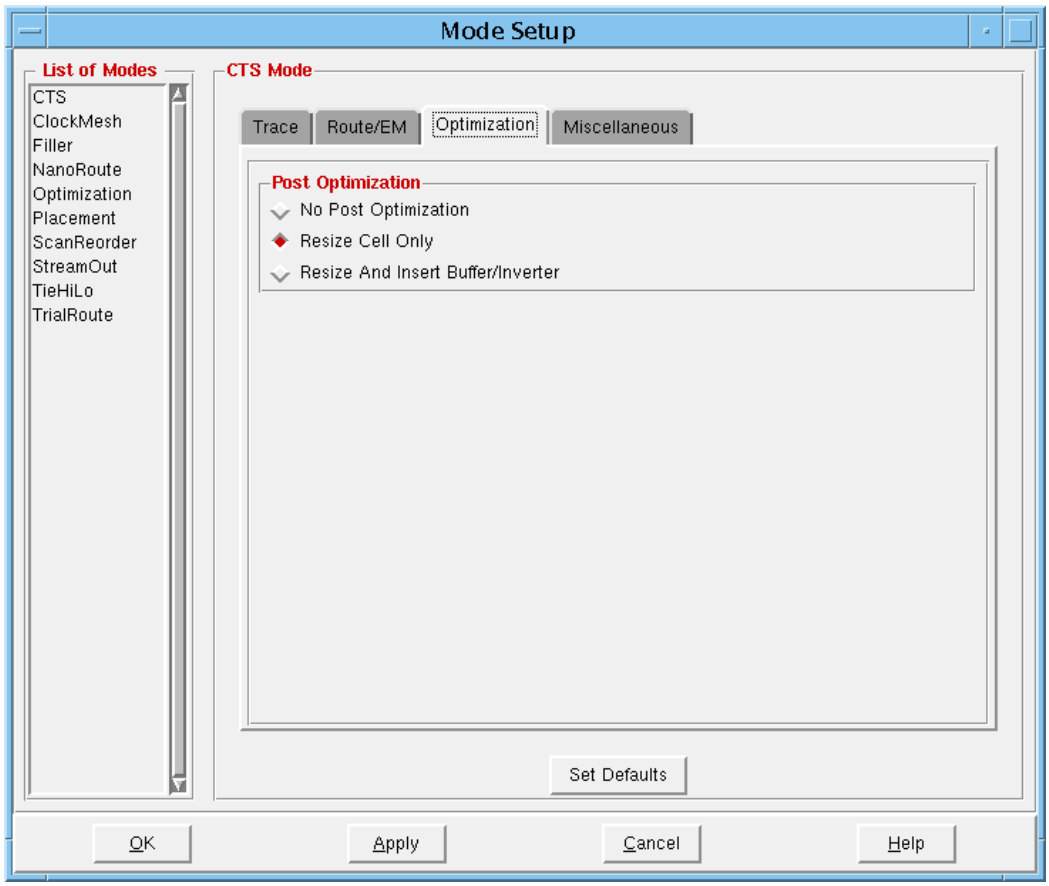
Related Text Commands

- `setCTSMode`
- `getCTSMode`

CTS – Optimization

Use the *Optimization* page to specify how CTS should handle post clock tree synthesis optimization.

➤ Choose *Design – Mode Setup* and select *CTS*, then select *Optimization*.



Fields and Options

No Post Optimization	Does not resize buffers or inverters, refine placement, or correct routing for signal and clock wires. *Default:* Off
Resize Cell Only	Resizes buffers or inverters only; the software does not refine placement or correct routing. *Default:* On

Resize And Insert Buffer/Inverter

Inserts and resizes buffers or inverters, refines placement, and corrects routing for signal and clock wires.

Default: Off

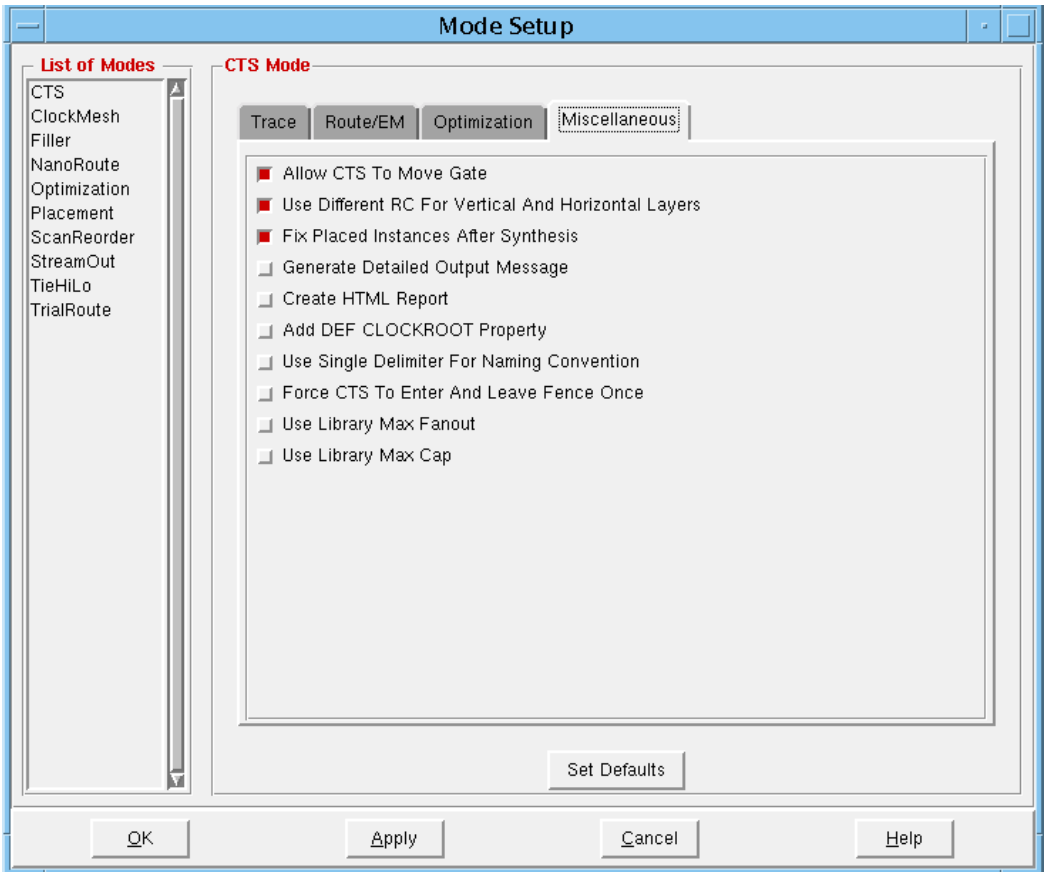
Related Text Commands

- `setCTSMode`
- `getCTSMode`

CTS – Miscellaneous

Use the *Miscellaneous* page to set various other global parameters for CTS.

➤ Choose *Design – Mode Setup* and select *CTS*, then select *Miscellaneous*.



Fields and Options

Allow CTS To Move Gate

Moves driving gates during clock tree synthesis.

Default: On

Use Different RC For Vertical And Horizontal Layers

Uses separate average RC values for horizontal and vertical layers. This is useful for when your design has very different R and C values for horizontal and vertical layers.

Default: On

Fix Placed Instances After Synthesis

Changes the placement status of instances from `PLACED` to `FIXED` after clock tree synthesis.

Default: On

Generate Detailed Output Message

Generates more detailed information in the Encounter console and the log files during CTS.

Default: Off

Create HTML Report Generates HTML versions of the CTS reports.

Default: Off

Add DEF CLOCKROOT Property

Adds the `CLOCKROOT` property to each clock that CTS inserts in a design.

Default: Off

Use Single Delimiter For Naming Convention

Uses single name delimiters after the first element in clock root and net names.

CTS normally inserts double (or, in some cases, multiple) name delimiters after the first element of clock root or net names. If you select this option, CTS inserts a single underscore (_) in clock root and net names.

Default: Off

Force CTS To Enter And Leave Fence Once

Forces CTS to enter only once into a fence in hierarchical designs. If you select this option, CTS will not enter into a fence more than once, and CTS will create only one clock port for each fence after partitioning.

Default: Off

Use Library Max Fanout

Uses the maximum fanout limit specified in the timing library.

If you do not select this option, the software uses the `MaxFanout` value from the clock tree specification file. If the clock tree spec file does not contain a `MaxFanout` value, the software uses a maximum fanout limit of 50.

Default: Off

Use Library Max Cap

Uses the maximum capacitance values in the timing library for buffers, inverters, or gating cells.

If you do not select this option, the software uses the `MaxCap` values from the clock tree specification file.

Default: Off

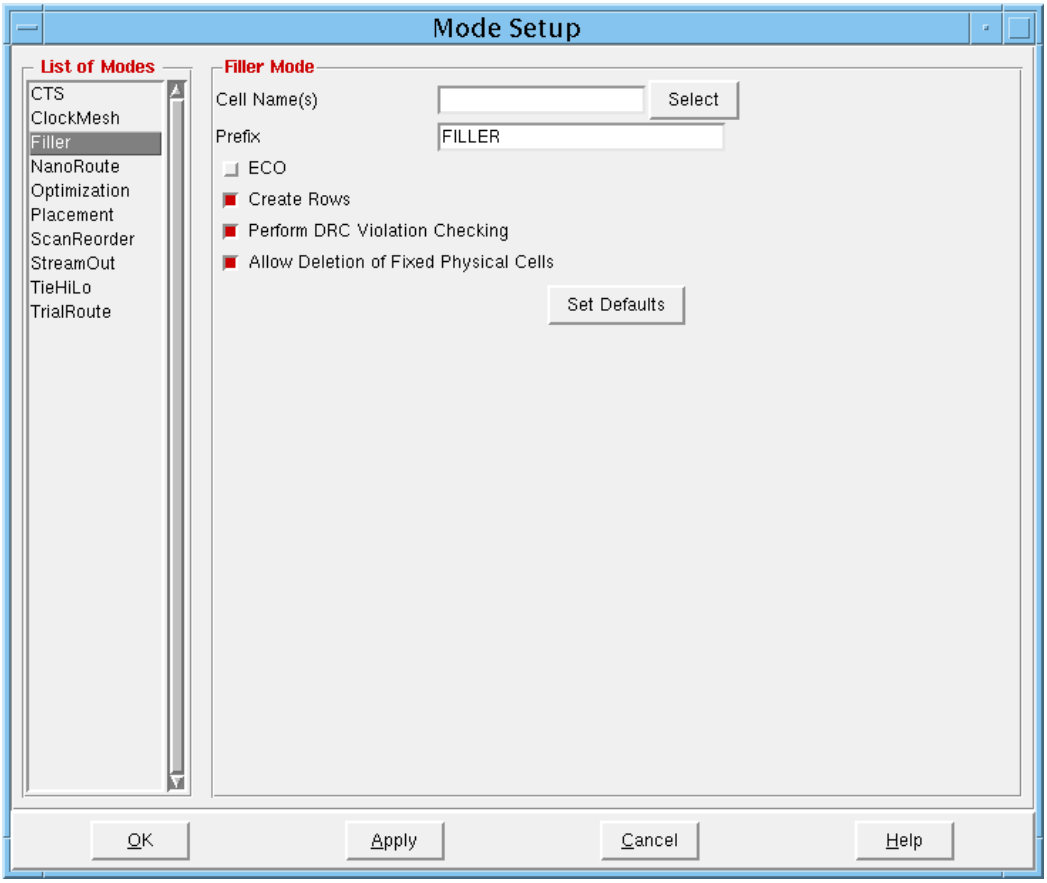
Related Text Commands

- `setCTSMode`
- `getCTSMode`

Mode Setup – Filler

Use the *Mode Setup – Filler* page to specify options for adding filler cells.

➤ Choose *Design – Mode Setup* and select *Filler*.



Fields and Options

Cell Name(s)	Specifies the filler cells to add.z *Default:* `""` (empty string)
Prefix	Specifies the prefix for the added filler cells. *Default:* `FILLER`
Create Rows	Creates rows in the floor plan. By default, if a cell's site does not have rows in the floor plan, `addFiller` creates the rows. *Default:* Selected

Perform DRC Violation Checking

When Add Filler is called after routing, instructs the software to run DRC checks of filler pins with signal net wires.
Default: Selected

Fill Boundary

Fills the space between the ending standard cell and the core area (box). If this option is not selected, the software adds filler cells between the standard cell instances only.
Default: Selected

Allow Deletion of Fixed Physical Cells

Allows the software to delete filler cells marked `FIXED` in the database.
Default: End-cap and well-tap cells are marked `FIXED`, and `deleteFiller` can delete them.

Set Defaults

Restores all the values of the options on this page to their default values.

Related Text Commands

- `getFillerMode`
- `setFillerMode`

Mode Setup – NanoRoute

The *Mode Setup – NanoRoute* page enables you to specify global parameters for the NanoRoute® router.

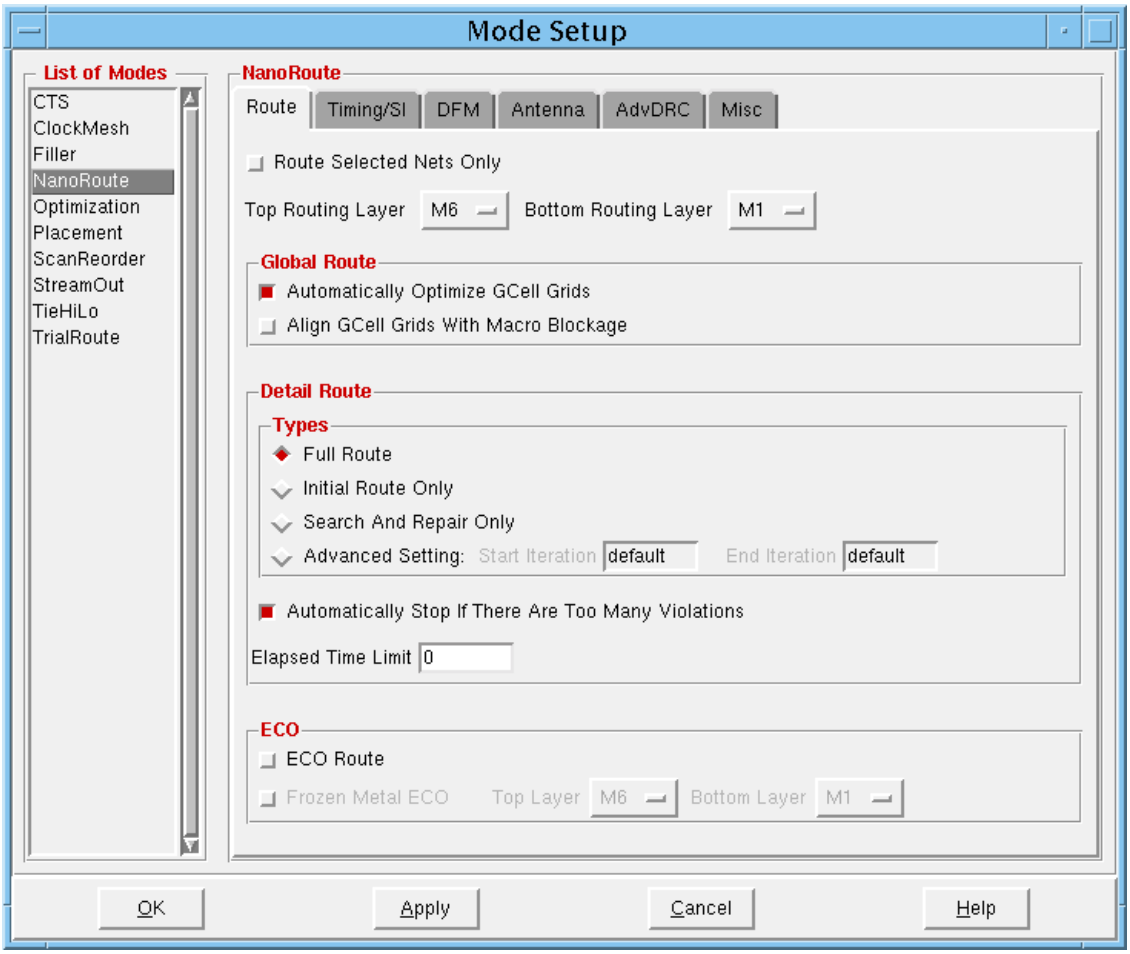
The *Mode Setup – NanoRoute* page contains the following subpages:

- NanoRoute – Route on page 317
- NanoRoute – Timing/SI on page 322
- NanoRoute – DFM on page 325
- NanoRoute – Antenna on page 330
- NanoRoute – AdvDRC on page 333
- NanoRoute – Misc on page 335

NanoRoute – Route

Use the *Route* page to specify options for global, detailed, and ECO routing.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *Route*.



Fields and Options

Route Selected Nets Only

Specifies whether NanoRoute routes all nets at once or routes selected nets only. To route critical nets as short as possible, select the critical nets and select this option.

When this option is selected, NanoRoute does the following:

- Removes incomplete nets unless they are marked `+ FIXED` or have a `-skip_routing` net attribute.
- Routes the remaining selected nets.

Default: Off

Top Routing Layer

Specifies the highest layer the router uses for global and detailed routing. This option sets a hard limit, that is, NanoRoute does not route nets above the specified layer.

Note: To set a soft limit, use the *Top Layer* attribute.

Default: The number of the highest routing layer specified in the LEF `LAYER` (Routing) statement.

Bottom Routing Layer

Specifies the lowest layer the router uses for global and detailed routing.

If the design has pins below the layer specified by this parameter, and if the tracks for the in-between layers are aligned to allow stacked vias to be dropped directly on top of the pins, the router uses stacked vias. However, if the tracks are not aligned, the router adds a short piece of wire before dropping a via to go to the next layer.

Note: To set a soft limit, use the *Bottom Layer* attribute.

Default: M1

Automatically Optimize GCell Grids

Overwrites the `GCELLGRID` defined in the DEF file with a grid that is optimized for the NanoRoute router. Selecting this option helps resolve congestion and over-the-macro violations if you see routability issues due to hot spots.

Default: On

Align GCell Grids With Macro Blockage

Generates global routing cells (gcells) aligned to blockages in macros. Select this option prior to global routing, to improve the alignment of gcells with pins.

Default: Off

Full Route

Runs all detailed routing steps.

Default: On

Initial Route Only

Runs initial detailed routing only. During initial detailed routing, the router builds the detailed routing database.

Default: Off

Search And Repair Only

Runs a search-and-repair step. During search and repair, the router locates shorts and spacing violations and reroutes the affected areas to eliminate as many of the violations as possible. You must have already run detailed routing in order to run search-and-repair.

Default: Off

Advanced Setting

Divides detailed routing into intermediate steps.

Default: Off

Start Iteration

Specifies the first pass in a detailed routing step.

Default: `default`

End Iteration Specifies the last pass in a detailed routing step or the beginning of postroute optimization.

Note: Setting *End Iteration* to a value higher than 20 generally does not improve results.

Default: `default`

Automatically Stop If There Are Too Many Violations

Controls whether NanoRoute continues routing if there are many violations. In highly congested designs, NanoRoute stops if the number of violations is too high. If you deselect this option, NanoRoute continues routing until there is no improvement. By default, this option is selected.

Default: On

Elapsed Time Limit Specifies a run-time limit for detailed routing. The time-limit is based on the elapsed time (the wall-clock time), not the CPU time. If the router reaches the limit during initial routing iteration, it stops when it finishes the routing iteration and keeps the routing result. If it reaches the limit during search and repair or postroute optimization, it stops immediately and keeps the routing result at that time.

Default: `0` (no time limit)

ECO Route Specifies engineering change order (ECO) mode. During ECO mode, NanoRoute completes partial routes with added logic, while maintaining the existing wire segments as much as possible.

Note: Select *ECO Route* only if you are running both global and detailed routing.

Default: Off

Frozen Metal ECO

Specifies the routing layers for ECO routing. Routing on all other layers is frozen.

Default: Off

Top Layer Specifies the top routing layer.

Bottom Layer Specifies the bottom routing layer.

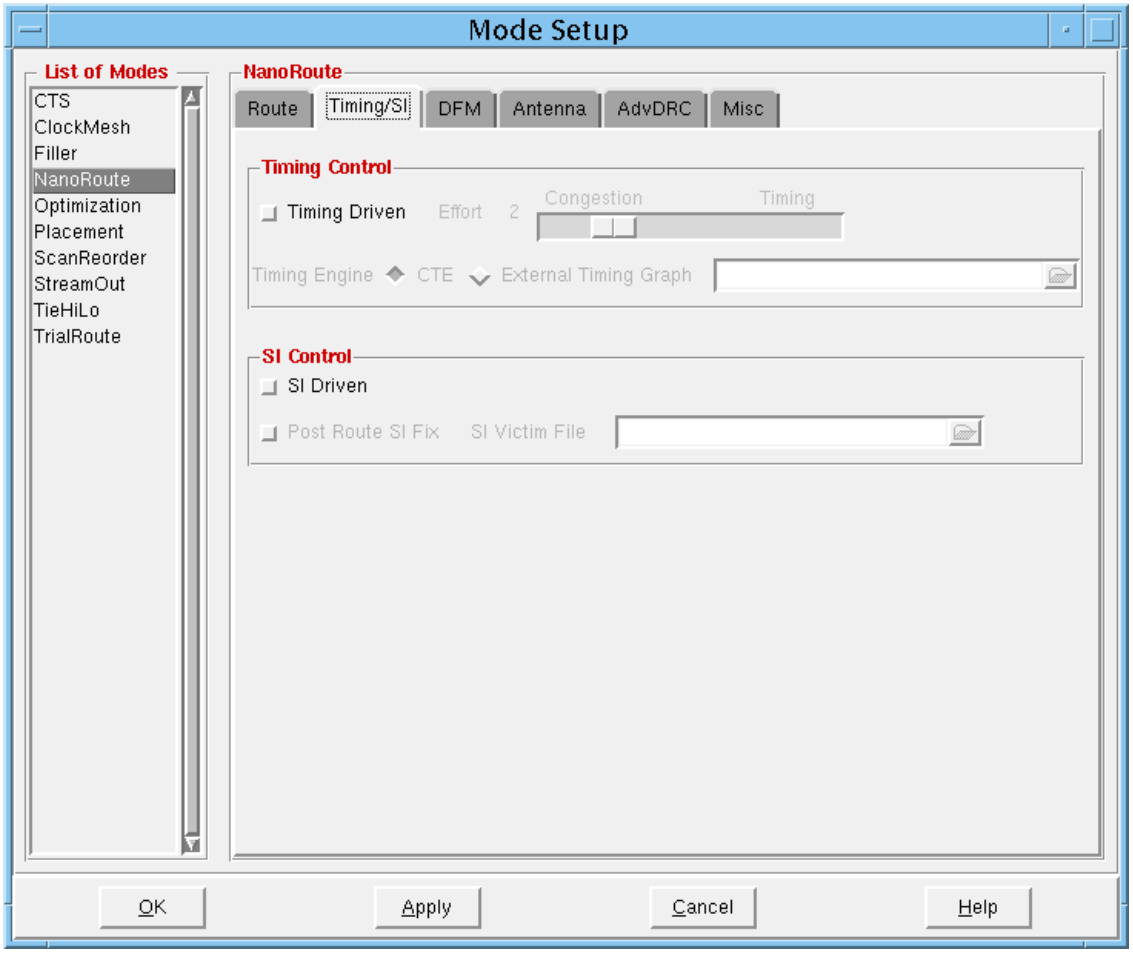
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute – Timing/SI

Use the *Timing/SI* page to specify options for timing-driven routing and signal-integrity-driven routing, and signal integrity repair.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *Timing/SI*.



Fields and Options

Timing Driven

Minimizes timing violations by analyzing the timing slack for each path, the drive strengths of each cell in the library, and the maximum capacitance and maximum transition limits. During timing-driven routing, NanoRoute routes multi-pin nets to the most critical sink first, performs wire optimization by reducing resistance and coupling, and continually adjusts detouring.

Default: Off

Effort Specifies how aggressively the router works to meet timing constraints. A higher value increases the effort toward meeting timing constraints and decreases the effort toward relieving congestion.
Range: 0 – 10

Timing Engine

Specifies the timing engine NanoRoute uses for timing analysis.

CTE Specifies the Encounter common timing engine.

Default: On

External Timing Graph

Specifies an externally generated timing graph.

Default: Off

SI Driven

Prevents or reduces crosstalk. Works in conjunction with timing-driven routing.

- When *Timing Driven* is selected, uses SMART routing to identify victim nets and minimize crosstalk by wire spacing, layer hopping, net ordering, and minimizing the use of long parallel wires.
- When *Timing Driven* is not selected, uses an older signal integrity engine to identify victim nets and minimize crosstalk by preventing or reducing the use of long parallel wires.

Default: Off

Post Route SI Fix

After routing and signal integrity analysis, uses information from a file that contains a list of victim nets to change the routing topology, including layer assignments, spacing, and location, to prevent coupling to other nets. Specify the file with *Use SI Victim File*. Postroute signal integrity repair requires both global and detailed routing.

Note: This option applies to nets with the *SI Post Route Fix* attribute set to *True*.

Default: Off

SI Victim File

Specifies a file from a crosstalk analysis tool, such as the CeltIC™ crosstalk analyzer for cell-based designs, that contains a list of nets with crosstalk problems.

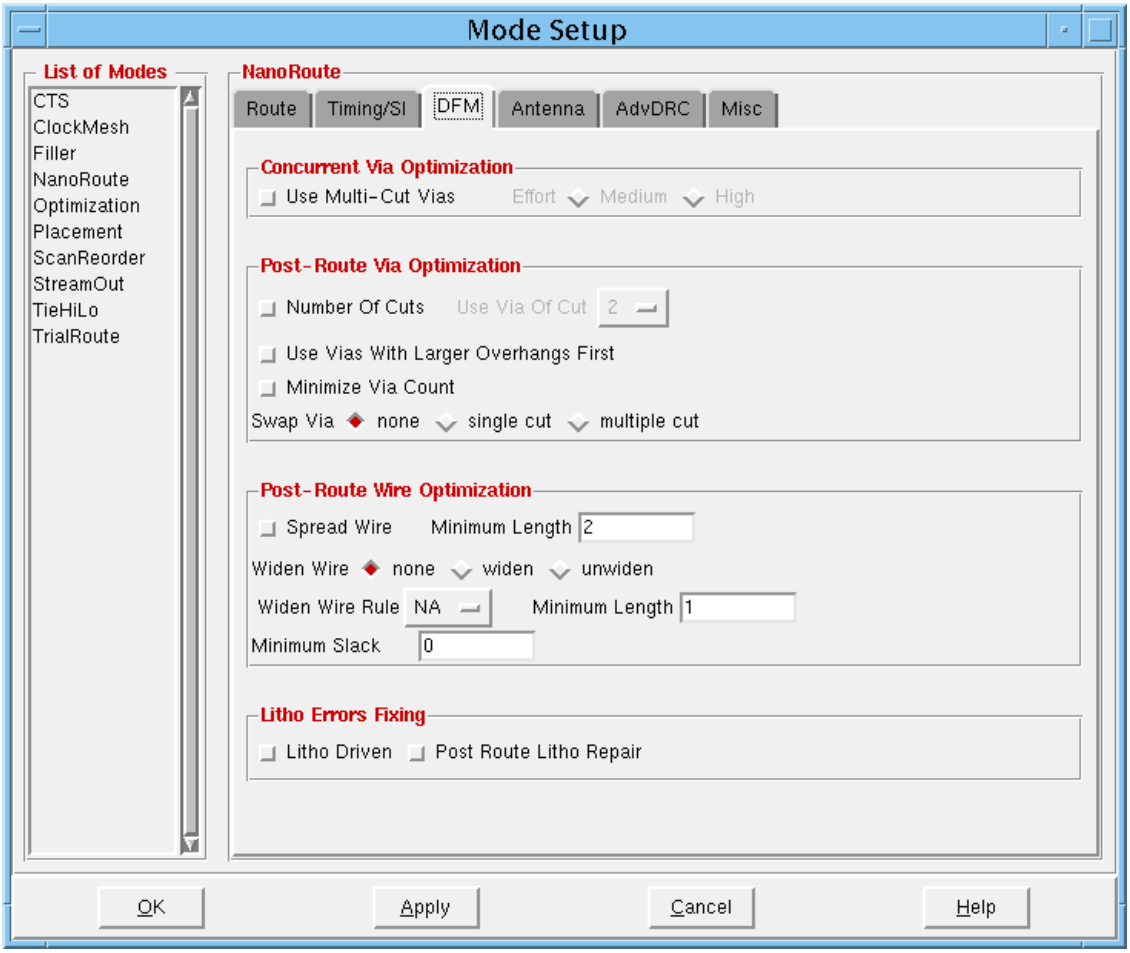
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute – DFM

Use the *DFM* page to set via optimization options.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *DFM*.



Fields and Options

Use Multi-Cut Vias Inserts multiple-cut vias concurrently with routing.

Default: Off

Effort Medium Specifies medium effort for using multiple-cut vias. Use medium effort for congested designs.

Default: Off

Effort High Specifies high effort for using multiple-cut vias. Use high effort for less congested designs to achieve the maximum multiple-cut via ratio, but with a higher run-time overhead.

Default: Off

Number Of Cuts Enables you to choose the number of cuts in the vias used to replace single-cut vias during postroute via optimization (via swapping). The router replaces only single-cut vias during via optimization; it does not replace multiple-cut vias.

Default: Off

Use Via Of Cut Specifies the number of cuts in the vias used to replace single-cut vias. For example, specify 4 to replace single-cut vias by quad-cut vias.

Default: 2

Use Vias With Larger Overhangs First

Specifies that the router choose vias with larger metal overhang first during via optimization. The router chooses from fat single-cut and fat multiple-cut vias. All vias must be predefined or automatically generated before via optimization.

Default: Off

Minimize Via Count Minimizes the number of vias in a fully routed design.

Default: Off

Swap Via

Swaps single-cut vias for multiple-cut vias or reverses swapping on critical nets in a fully routed design, so that multiple-cut vias are swapped for single-cut vias on those nets. Does not swap multiple-cut vias in nondefault rule routing.

A net with a pin on a critical path is considered a critical net if the pin slack, plus the value specified for *Minimum Slack*, is less than or equal to 0.
Default: none

none Does not swap vias.

single cut During timing-driven routing, swaps vias on critical nets only; otherwise, might swap any multiple-cut via for a single-cut via. Swapping multiple-cut vias for single-cut vias can improve timing and relieve congestion as a postroute process.

multiple cut Replaces single-cut vias with multiple-cut vias in a fully routed design without regard to timing.

Spread Wire

Turns on postroute wire spreading. Type the minimum length for wires to move in the text box next to *Minimum Length*.

The router moves the wires without moving the vias. Specifying `true` for this parameter might increase the overall routing run time but helps avoid yield lost caused by shorts.

Default: Off

Minimum Length

Specifies the minimum length for wires to move during wire spreading.

Widen Wire

Turns on postroute wire widening. Selecting this option might increase the overall routing run time, but helps avoid yield loss caused by opens. Select the nondefault rule for widening wires in the text box next to *Widen Wire Rule*.
Default: Off

none Turns off this option.

widen Turns on postroute wire widening.

unwiden Turns off postroute wire widening.

Widen Wire Rule

Specifies the nondefault rule for widening wires. The rule is specified in the LEF file.

Minimum Length

Specifies the minimum length in microns for a wire segment of a net before the segment is a candidate for widening. Wires are widened by an amount defined by a nondefault rule. They are not widened unless they meeting the following criteria:

- Timing is not adversely affected
- Routing resources are available
- No overflow is created
- No design rule or process antenna violations are created

Widening wires helps avoid design rule violations, signal integrity problems, and yield loss.

Minimum Slack

Specifies the minimum slack on pins associated with nets that are candidates for wire spreading or wire widening. Using this parameter reduces the timing impact of wire spreading, wire widening, and via swapping, and helps reduce congestion and the yield loss due to shorts and opens.

Litho Errors Fixing

Select one or both of the following options to minimize lithography problems.

Litho Driven

Avoids lithography problems during routing by avoiding certain routing patterns that might lead to the creation of lithography hotspots.
Default: Off

Post Route Litho Repair

Corrects bridging, necking, and line-end shortening problems caused by lithography. Prior to running the router with this parameter, import a hotspot interface format (HIF file) with the `loadViolationReport` command or by using the Load Violation Report form.

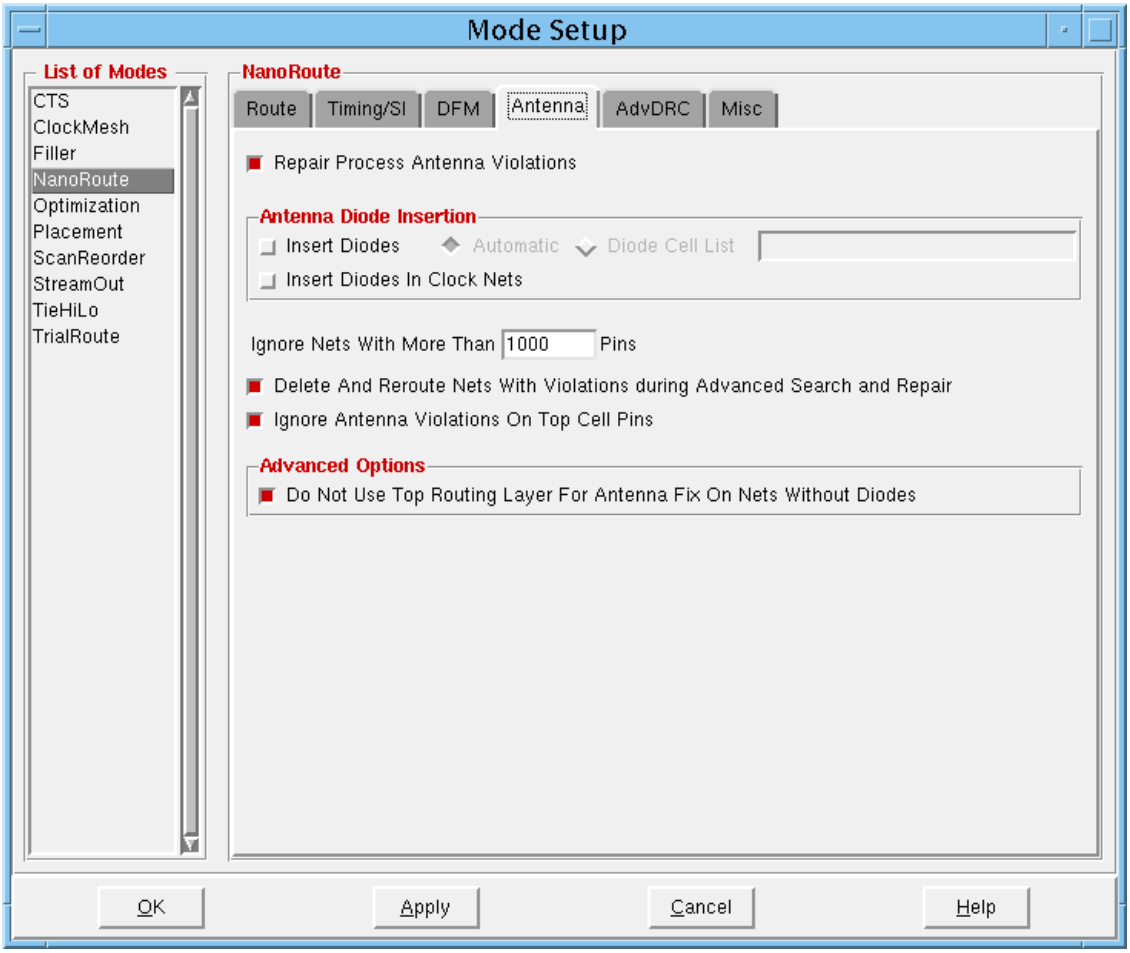
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute – Antenna

Use the *Antenna* page to specify when and how to repair process antenna violations.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *Antenna*.



Fields and Options

Repair Process Antenna Violations

Repairs process antenna violations by jumping layers (antenna stapling). The router repairs process antenna violations if it can do so without creating DRC violations. The router might need to make several passes before repairing all antenna violations.

Default: On

Insert Diodes

Inserts and places antenna diode cells during postroute optimization if there are available placement locations for the cells. By default, NanoRoute repairs antenna violations by changing layers (also called antenna stapling or layer hopping), but it can also repair antenna violations by inserting diodes as close as possible to input gates to discharge current.

Default: Off

Automatic

searches the LEF file and inserts the first `MACRO` with `CLASS CORE ANTENNACELL` it finds with the appropriate `SITE` definition.

Default: On

Diode Cell List

Routes antenna diode cells with the specified name during postroute optimization. The antenna diode cells must have the same LEF `SITE` definition as the standard cells.

Default: Off

Insert Diodes In Clock Nets

Inserts diodes to repair process antenna violations on clock nets that are in the regular net section of the DEF file.

Default: Off

Ignore Nets With More Than number Pins

Specifies the maximum number of pins to consider on any net during process antenna violation repair.

Default: `1000`

Delete And Reroute Nets With Violations during Advanced Search and Repair

Deletes and reroutes nets with process antenna violations. This option is not enabled if you are using LEF 5.3 or older, or if the design has more than 100 DRC violations.

Default: On

Ignore Antenna Violations On Top Cell Pins

Ignores antenna violations on top-level I/O block pins, but repairs antenna violations elsewhere. Do not select this option when you route a block whose top level is going to have diodes inserted.

Default: On

Do Not Use Top Routing Layer For Antenna Fix On Nets Without Diodes

Reserves the top routing layer for repairing process antenna violations. The NanoRoute router globally routes nets that do not have diode protection, such as nets without output pin protection, without using the top routing layer. During detailed routing, it repairs antenna violations by jumping to the highest layer. This is useful for routing feedthrough nets.

Default: On

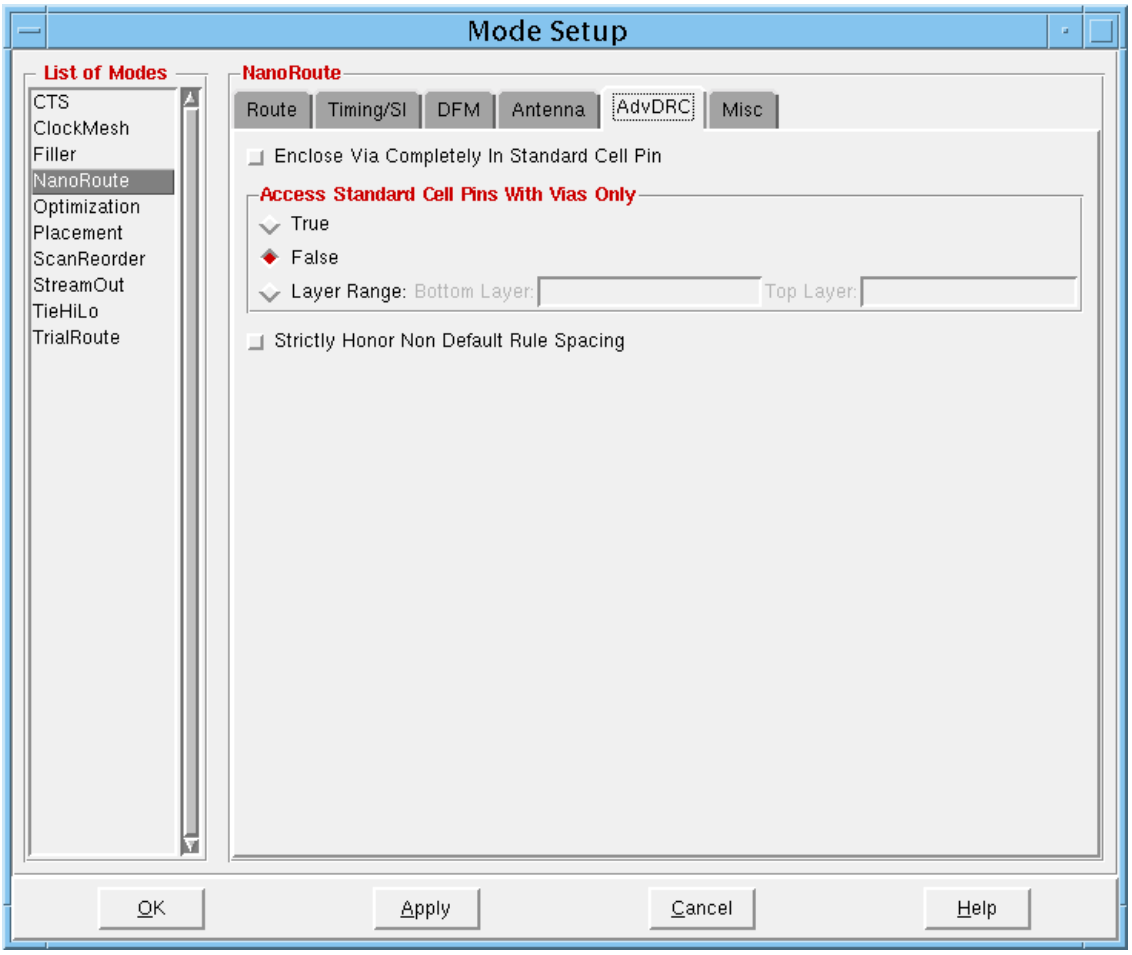
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute – AdvDRC

Use the *AdvDRC* page to specify advanced options for checking design rules.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *AdvDRC*.



Fields and Options

Enclose Via Completely In Standard Cell Pin

Encloses via geometries completely inside standard cell pins. Select this option to avoid `MINSTEP` violations for standard cell pin access.

Default: Off

Access Standard Cell Pins With Vias Only

Allows via access only to standard cell pins. Does not allow planar access.

Default: False

True	Allows via access only. Does not allow planar access.
False	Allows both via and planar access.
Layer Range:	Lets you specify the layer range for limiting via access.

Strictly Honor Non Default Rule Spacing

Uses nondefault spacing rules for wide wires. If vias are tapered, still uses default vias.

By default, the router treats nondefault rule spacing as a soft attribute; that is, when routing resources are available, it honors the nondefault rule. If the area is too congested, and resources are not available, the router might not honor nondefault spacing rules. You can override this behavior by selecting this option.

You define nondefault routing rules in the `NONDEFAULTRULE` statement of the LEF file.

Default: Off

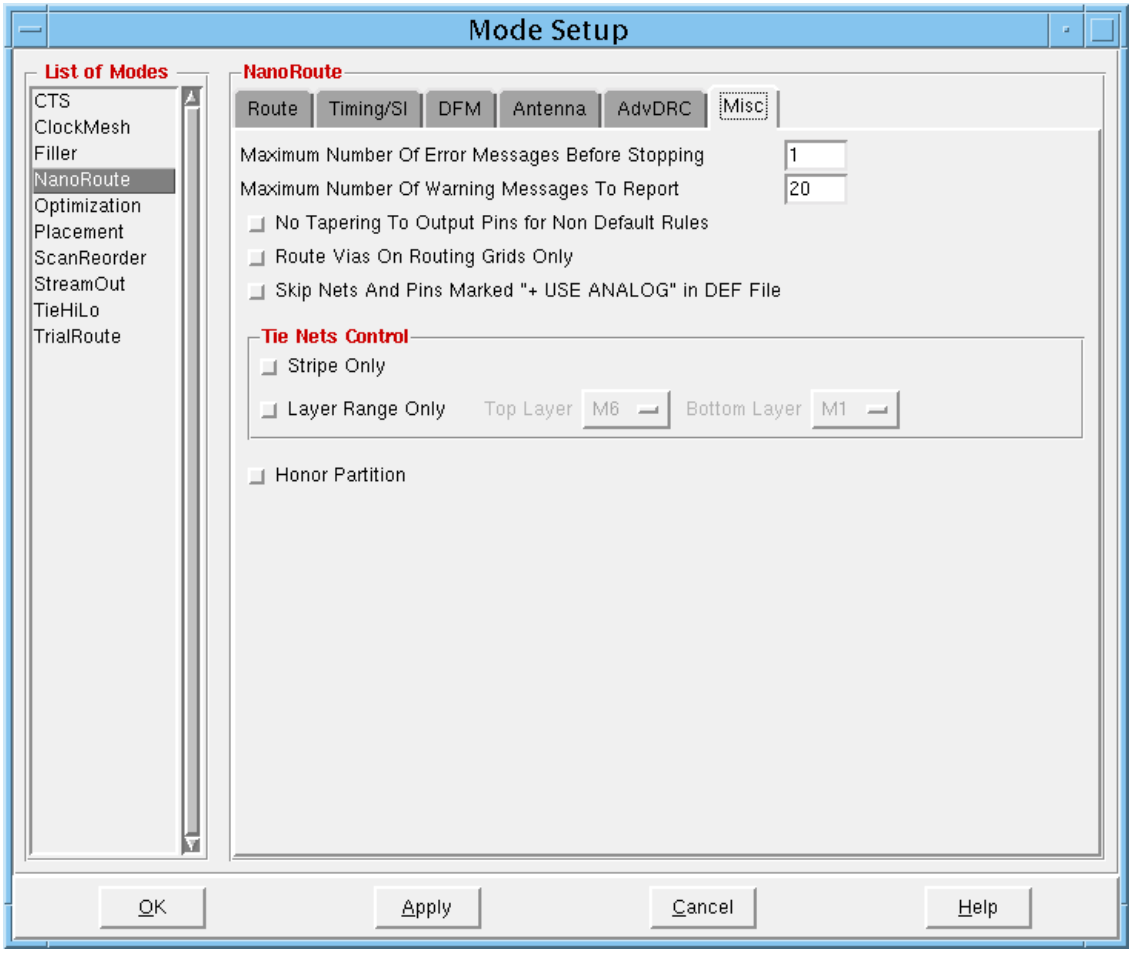
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

NanoRoute – Misc

Use the *Misc* page to specify additional NanoRoute options.

➤ Choose *Design – Mode Setup* and select *NanoRoute*, then select *Misc*.



Fields and Options

Maximum Number Of Error Messages Before Stopping

Specifies the maximum number of error messages for any one command written to the log file before stopping processing.
Default: 1

Maximum Number Of Warning Messages To Report

Specifies the maximum number of warning messages for any one command reported to the log file. After reaching this number, the router continues processing, but does not report warnings for this command.
Default: 20

No Tapering to Output Pins for Non Default Rules

Prohibits the router from tapering at standard cells, macro cells, and block output pins.
Default: Off

Route Vias On Routing Grids Only

Centers vias on routing grids by dropping them at track intersections.
Default: Off

Skip Nets And Pins Marked "+ USE ANALOG" in DEF File

Skips routing nets or pins marked + `USE ANALOG` in the DEF file.
Default: Off

Stripe Only

Specifies targets for tie-high and tie-low nets.

- When off, connects tie nets to nearby stripes, ring pins, or core rings.
- When on, connects tie nets to the same targets as when on, plus macro (power and ground) pins, cover macro pins, and standard cell followpins. I/O pad pins and pad ring pins are excluded from tie-net connections.

Default: If the design contains stripes, the behavior is the same a when off. If the design does not contain stripes, the behavior is the same as when on.

Layer Range Only

Specifies the range of routing layers for stripes.

Honor Partition

Routes nets belonging to a partition completely inside that partition and nets that are part of the top-level glue logic completely within the top-level channels.
Default: Off

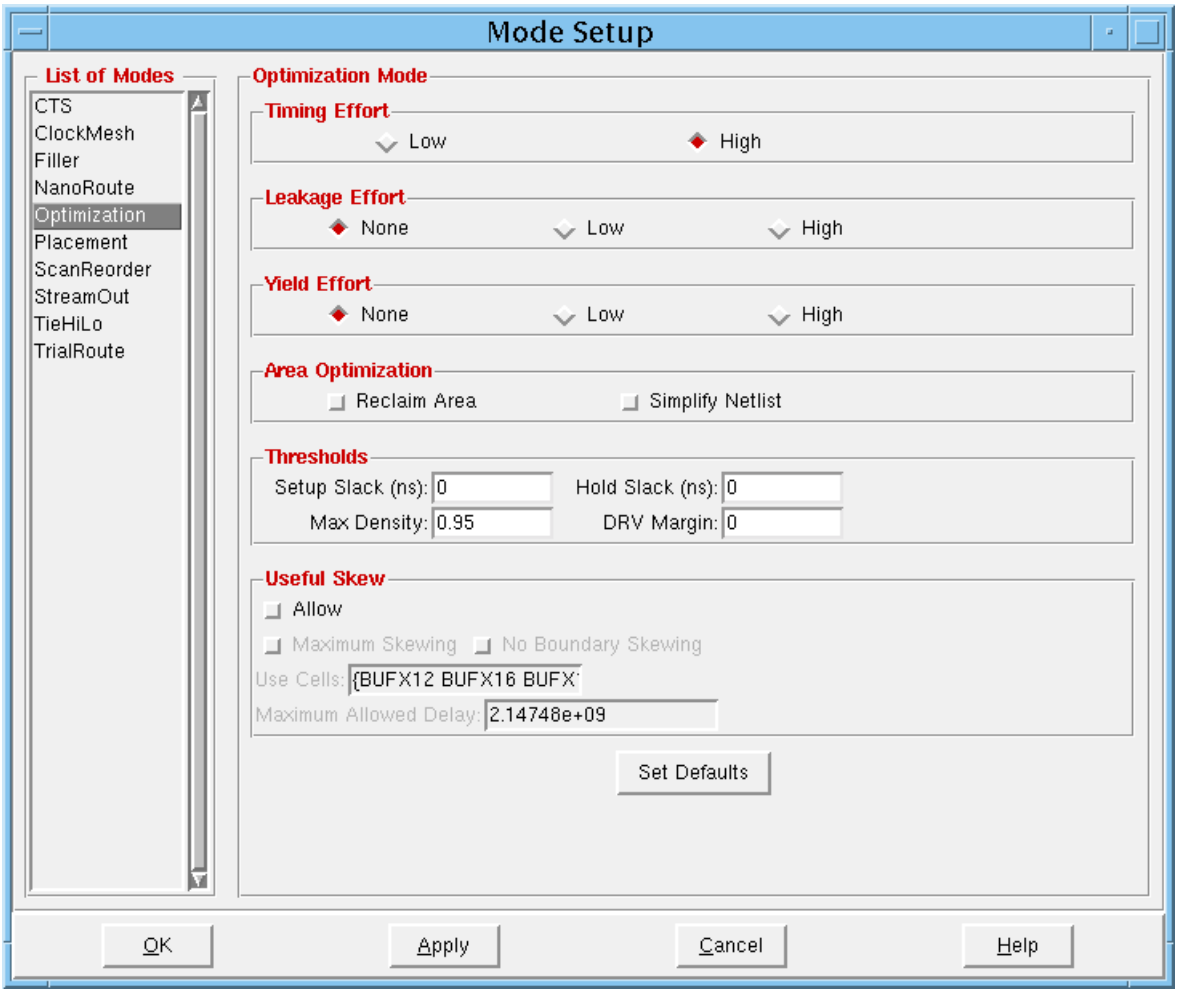
Related Text Commands

- `getNanoRouteMode`
- `setNanoRouteMode`

Mode Setup – Optimization

Use the *Mode Setup – Optimization* page to set effort levels for timing, leakage, and yield; specify area optimization options, thresholds for slack and density and a margin for DRV; and set useful skew options.

➤ Choose *Design – Mode Setup*, then select *Optimization*.



Optimization Fields andOptions

Timing Effort	Specifies the effort level the software uses for timing optimization. *Default: High*

Low — Specifies low effort level. Use this level for design prototyping. This level triggers global resizing and buffering steps in order to obtain a good timing result in the fastest run time.

High — Specifies high effort level. Use this level to reach timing closure for challenging designs. This level activates all the physical synthesis optimization transforms.

Leakage Effort

Enables optimization to run in a power leakage-aware mode. In this mode, the software reduces the total amount of leakage power in addition to optimizing timing and area, and minimizes the number of design rule violations. During library set up, you must load all the Vth libraries. The software sorts the cells—you do not need to declare the high Vth library.
Default: None

None — Disables power leakage-aware mode.

Low — Reduces leakage power only in the post-route stage. The software does not insert high-leakage cells during hold fixing.

High — Reduces leakage in pre-route and postroute stages. The software does not insert high leakage cells during hold fixing. This mode is more aggressive than low-effort mode, and might affect run time and timing closure.

Yield Effort

Specifies the level of effort for performing yield optimization. This parameter applies during preCTS, postCTS, and post-route modes of optimization. It does not apply during incremental optimization.

- Low-effort yield optimization improves the yield while maintaining the timing. This effort is recommended for timing-critical designs.
- High-effort yield optimization achieves the maximum yield, but could lead to a small degradation in timing. If that occurs, an incremental optimization can be performed to recover the timing.

Default: *None*

None — Does not optimize for yield.

	Low	Improves the yield while maintaining the timing. This effort level is recommended for timing-critical designs.
	High	Words to achieve the maximum yield, but could lead to a small degradation in timing. If that occurs, an incremental optimization can be performed to recover the timing.
Area Optimization		
	Reclaim Area	Creates additional space in the design by downsizing gates or deleting buffers, while maintaining worst slack and total negative slack. *Default:* On **Note:** This option is not enabled when *Timing Effort* is set to *Low*.
	Simplify Netlist	Determines whether to simplify the netlist during timing optimization. The software recovers area, decreases congestion, and improves runtime by simplifying the netlist in the following ways: ■ Removing dangling output instances ■ Propagating constants ■ Removing unobservable logic ■ Remapping useless logic The software respects the `set_dont_touch` constraint, so it does not remove the constrained flip-flops, and does not touch non-uniquified modules. *Default:* Off **Note:** This option is not enabled when *Timing Effort* is set to *Low*.

Thresholds	
Setup Slack (ns)	Specifies a target slack value in nanoseconds for setup analysis. During setup violation repair, the setup target slack is `setupTargetSlack` and the hold target slack is set to 0. Generally, you use both *Setup Slack* and *Hold Slack* for hold analysis. If you specify *Hold Slack* only, the *Setup Slack* value is 0. *Default:* `0`
Hold Slack (ns)	Specifies a target slack value in nanoseconds for hold analysis only. During setup violation repair, the setup target slack is `setupTargetSlack` and the hold target slack is set to `0`. Generally, you use both *Setup Slack* and *Hold Slack* for hold analysis. If you specify *Hold Slack* only, the *Setup Slack* value is 0. *Default:* `0`
Max Density	Specifies the maximum area of utilization during timing optimization. *Default:* `0.95`
DRV Margin	Scales the maximum capacitance and maximum transition constraints according to the `margin` specified decimal value. For example, a margin of `0.2` (20 percent) multiplies the constraints by `0.8`. The margin can be positive or negative. Introducing this margin of pessimism improves correlation between the number of DRC violations before and after routing. *Default:* `0.0`
UsefulSkew	
Allow	Enables useful skew and lets you select usefule skew options. *Default:* Off
Maximum Skewing	Advances sequential elements more aggressively than by default, without degrading the worst negative slack. This option and the *Maximum Allowed Delay* option are complementary: If you select both options, the software uses the aggressive algorithm while respecting the *Maximum Allowed Delay* limit. *Default:* Off
No Boundary Skewing	
	Excludes boundary sequential cells in useful skew calculations. *Default:* Off
Use Cells	Specifies the cells for useful skew to use during post-CTS buffer insertion. *Default:* The software uses any cells.

Maximum Allowed Delay

Limits the amount of slack (in nanoseconds) the software can borrow from neighboring flip-flops when performing useful skew operations. The Encounter delay calculation and RC extraction methods might differ from those of sign-off tools, so other setup violations might occur if the software borrows too much slack. By having control over slack borrowing, you can prevent these setup violations. Limiting borrowed skew also limits the clock tree skew and avoids large hold violations. This option and the *Maximum Skewing* option are complementary: If you select both options, the software uses the aggressive algorithm while respecting the *Maximum Allowed Delay* limit.
Default: The software borrows the amout of slack needed to reduce setup violations—there is no maximum.

Related Text Commands

- `getOptMode`
- `setOptMode`

Mode Setup – Placement

Use the *Mode Setup – Placement* page to set global parameters for placing standard cells and refining placement.

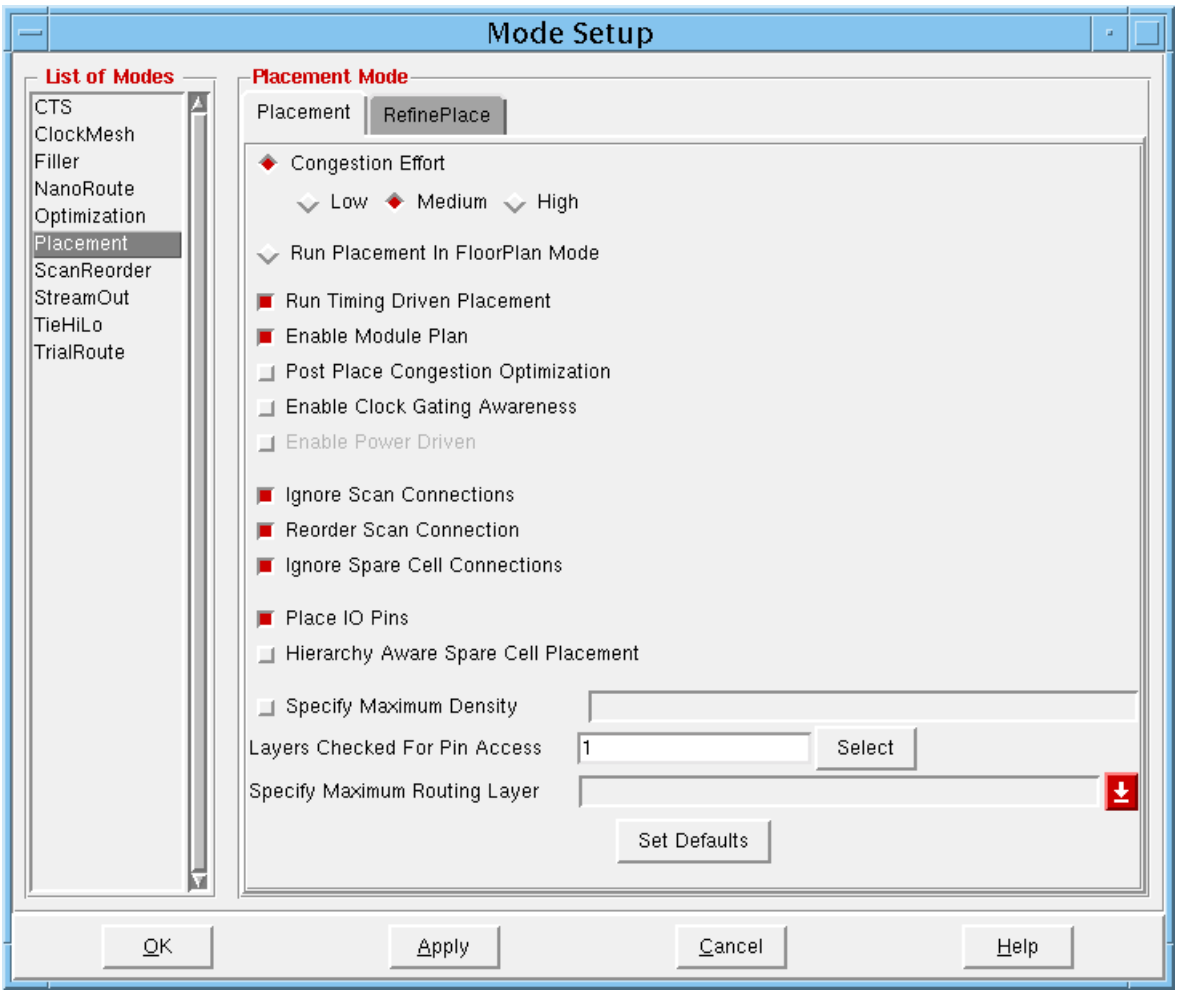
The Mode Setup – Placement page contains the following subpages:

- Placement on page 344
- RefinePlace on page 350

Placement

Use the *Placement* page to set global parameters for placement of standard cells .

➤ Choose *Design – Mode Setup*, then select *Placement*.



Fields and Options

Congestion Effort	Specifies the effort level for decreasing congestion. In general, a congestion effort increases the run time. *Default: Medium*

Low	Runs fewer iterations of placement to arrive quickly at a legal placement. This parameter might decrease placement quality.
Medium	Runs placement on designs in a normal effort level.
High	Runs more iterations of placement in an effort to achieve better congestion results. This parameter increases the run time.

Run Placement in Floorplan Mode

Runs a quick placement to gauge the feasibility of the netlist, but might not place components in legal locations. This mode assumes non-timing-driven placement.

Run Timing Driven Placement

Takes timing into account during placement to improve the placement of instances on timing critical paths. Before using this parameter, make sure the timing constraints are loaded in the design.

This option is disabled if you select *Run Placement in Floorplan Mode*.

Enable Module Plan

Improves wire length, timing, relative module location, and congestion results during the early phase of global placement for most designs. This option has the following features:

- It supports multi-threading. If this option is not selected, multi-threading is disabled during placement.
- It is compatible with full and incremental placement, prototyping mode, and the in-place optimization flow.
- It supports fences, regions, and guides.

  Consider removing legacy guides when *Enable Module Plan* is specified: As *Enable Module Plan* works to produce the best possible relative module location for a design, these guides may no longer be required for optimum timing results.
- It supports spare cells distribution, MSV flow, and is clock-gate aware.

Default: On

Note: Cadence recommends deselecting this option for designs with more than 1,000 floorplan constraints or other types of complex floorplan constraints.

Post Place Congestion Optimization

Runs congestion optimization after placement is complete in the detailed placement stage.

Before running post-placement congestion optimization, the design must be legally placed. If the placement is not legal, the software does not run the refinement step during congestion optimization, and instead exits.

Enable Clock Gating Awareness

Specifies that placement is aware of clock gate cells in the design.

Load the clock tree specification file before running the placement command with this option selected.

Default: Off

Enable Power Driven

Identifies and constrains power-critical nets to reduce switching power. In most cases, timing is not degraded. However, in some cases, a trade-off between power and timing is required.

Note: This option is not enabled if *Run Placement in Floorplan Mode* is selected or if you have not loaded an activity file (TCF or VCD) to supply the net switching information.

Load the activity file using the `readActivityFile` command.

Ignore Scan Connections

Disregards the scan connections while placing the scan groups. Before you place the design, you must already have specified the scan cells with the `specifyScanCell` command, or the scan cell information must be in the timing library.

Default: On

Reorder Scan Connections

Ignores the scan chain connectivity during placement and performs scan chain reordering after placement.

If this option is not selected, the software considers scan chain connectivity during placement and does not perform scan chain reordering after placement.

Default: On

Ignore Spare Cell Connections

Does not consider spare cell connections when placing spare cells. Before you place the design, you must already have specified the spare cells with the `specifySpareGate` command, or the spare cell information must be in the timing library.

Default: On

Note: The placer disconnects high-fanout (nets with more than 75 terminals) from spare cells, even when this option is not selected.

Place IO Pins

Moves placed and unplaced I/O pins, based on the placement of connected instances in an attempt to find a better I/O pin placement than the one specified in the I/O pin placement or floorplan file. At the end of global plaqcement, the I/O pin location is legalized.

When this option is off, I/O pins are ignored during global placement and no legalization is done at the end.

Default: On

Hierarchy Aware Spare Cell Placement

Places spare cells in the netlist within a hierarchical module, even if no region or fence constraints are specified.

- If you select this option, spare cells in a hierarchical module are placed within the bounds of the hierarchy.
- If you do not select this option, spare cells are spread out within the placement area, and are not bound to the hierarchy.

Default: Off

Specify Maximum Density

Controls local density during global placement. Sets the maximum placement density of the core area so that the placement engine aggressively minimizes the wirelength, while satisfying the maximum density constraint. This helps to achieve better timing results in low utilization designs. After global placement, the density control is removed.

Use a value between 0 (zero percent) and 1 (100 percent). For example, a value of 0.5 indicates that the maximum utilization of the entire design will be 50% or less.

Layers Checked For Pin Access

Specifies the layers to check for pin access. Click the *Select* button to open the Select Layer form to add or delete layers.

Specify Maximum Routing Layer

Constrains placement up to the specified layer for congestion and routability estimation.

Set Defaults

Resets the values of the options on this page to the default values.

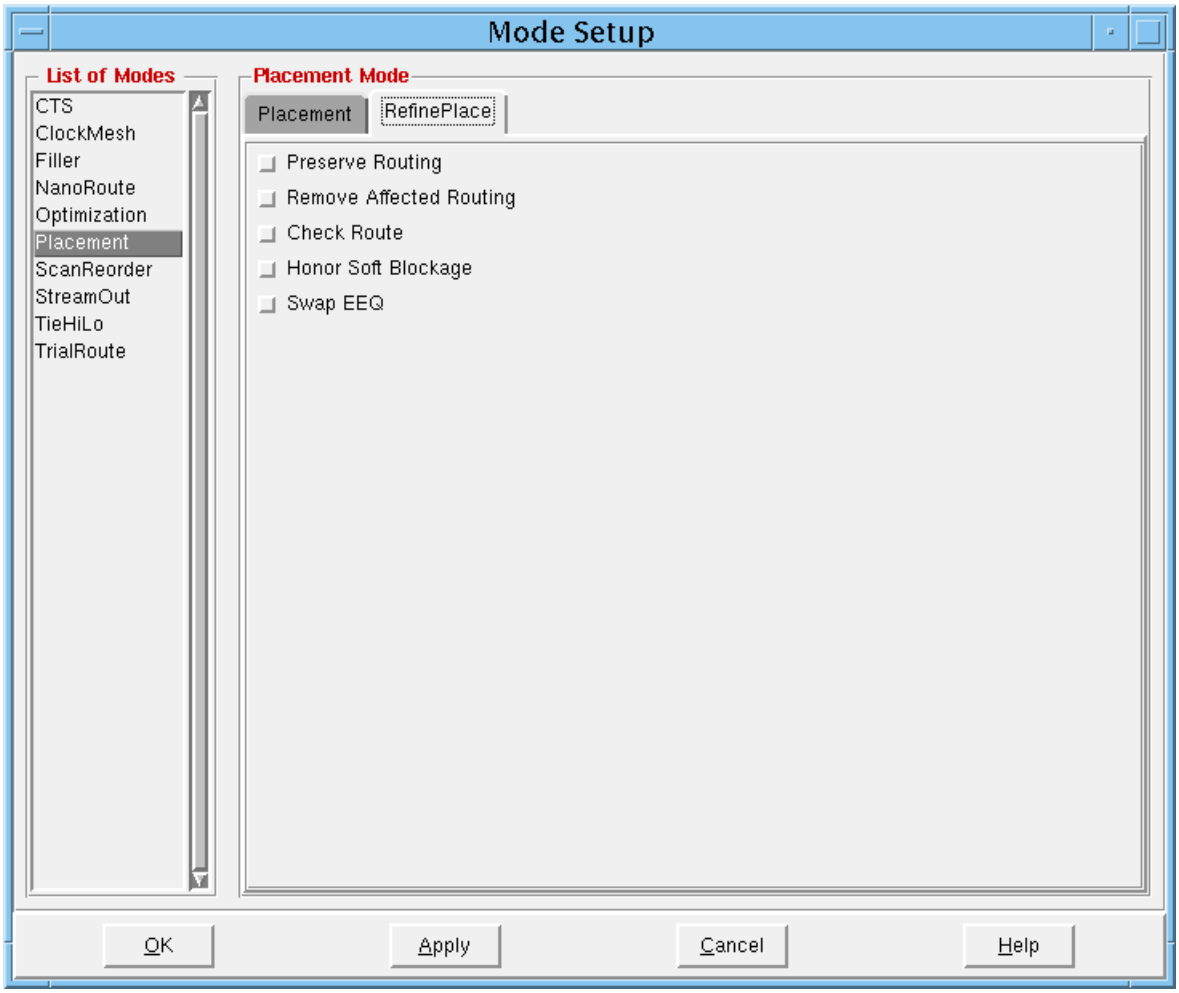
Related Text Commands

- `getPlaceMode`
- `setPlaceMode`

RefinePlace

Use the *RefinePlace* page to set global parameters for correcting and reporting flawed cell locations and instance overlap problems.

➤ Choose *Design – Mode Setup* and select *Placement*, then select *RefinePlace*.



Fields and Options

Preserve Routing	Preserves all routed wires. *Default:* Off

Remove Affected Routing

Removes all wires connected to moved cells.

Default: Off

Check Route

Considers pre-routed `FIXED` signal wires and avoids creating DRC violations between `FIXED` signal wires and instance pins. When this parameter is not specified, `refinePlace` ignores `FIXED` signal wires.

Using this option might result in longer run time.

Default: Off

Honor Soft Blockage

Specifies that soft blockage will be considered when running the command. By default, the soft placement blockage is only considered during global placement, and is ignored in refinePlace and optimization stages.

Default: Off

Swap EEQ

Allows replacement of master cells by EEQ cells during detailed placement to improve routability. After detailed placement, the software reports the number of replacements. EEQ cells are defined in the LEF file.

Default: Off

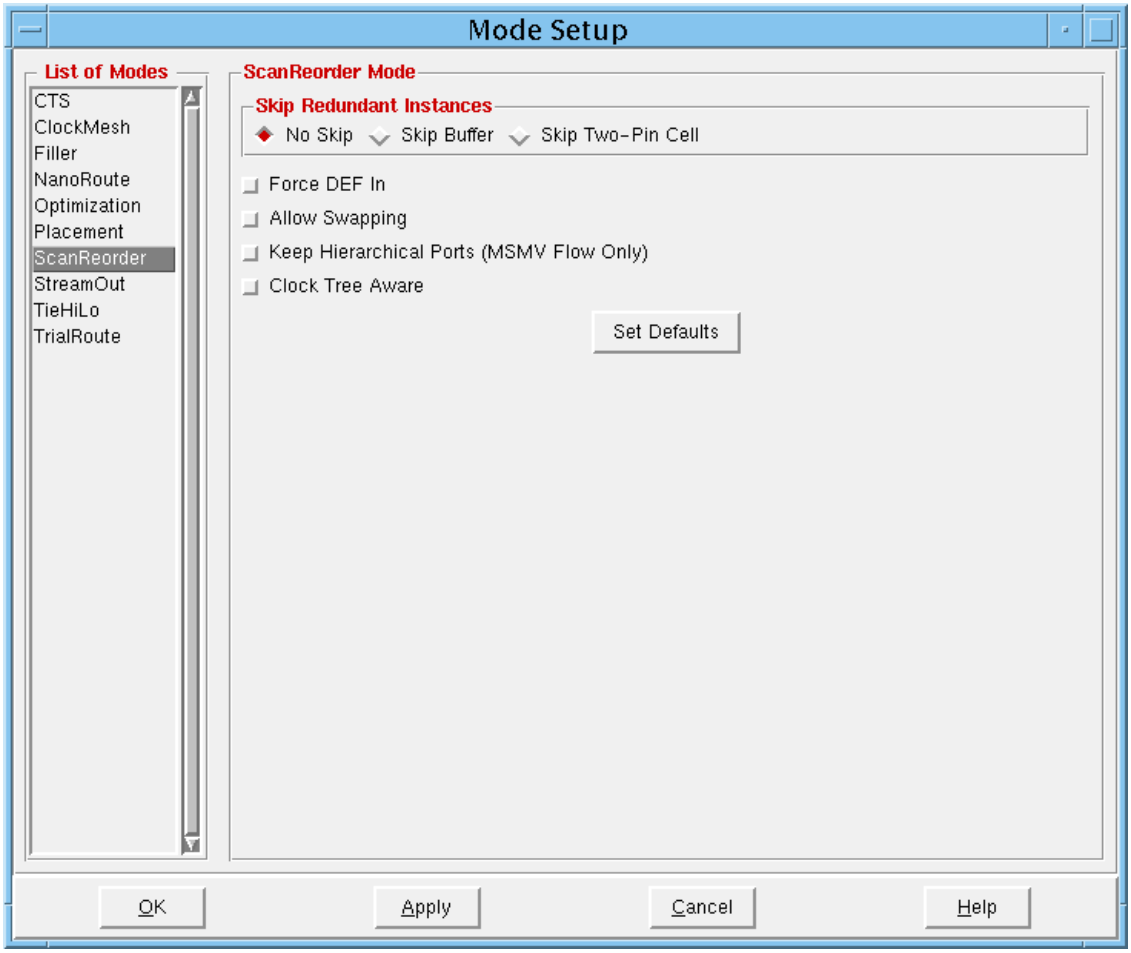
Related Text Commands

- `getPlaceMode`
- `setPlaceMode`

Mode Setup – ScanReorder

Use the *Mode Setup – ScanReorder* page to set global parameters for scan reordering.

➤ Choose *Design – Mode Setup*, then select *ScanReorder*.



Fields and Options

Skip Redundant Instances

Specifies how scan reordering handles buffers and inverters in the scan chain.
Default: No Skip

No Skip	Specifies that buffers and inverters remain after the scan chain reorder.

Skip Buffer Ignores buffers in the scan chain. If a buffer or inverter is not connected elsewhere in the design, `scanReorder` removes the buffer.

Skip Two-Pin Cell

Ignores buffers and inverters in the scan chain. If a buffer or inverter is not connected elsewhere in the design, `scanReorder` removes the buffer or inverter.

Allow Swapping Allows the software to swap scan elements between scan chains.
*Default:*Off

Keep Hierarchical Ports (MSMV Flow Only)

Maintains or corrects the hierarchical ports without deleting or inserting shifters, and reorders the remaining scan chain.

Default: Off

Clock Tree Aware Specifies whether scan reordering is clock tree aware.

If this parameter is not specified, or if 0 is specified for this parameter, scan reordering is not clock tree aware and is completely wirelength driven.

If a value is specified, the value must be a floating point number between 0 and 1, where 0 means scan reordering is completely wirelength driven and 1 means it is completely clock tree driven. The closer the value is to `1`, the more importance is given to clock trees over wirelength.

Value: Specify a floating number between `0` and `1`. Specifying a value is optional.

Default: Off (The software is not clock tree aware.) If this option is selected, the default value is `1`.

Set Defaults Resets the options on this page to the default values.

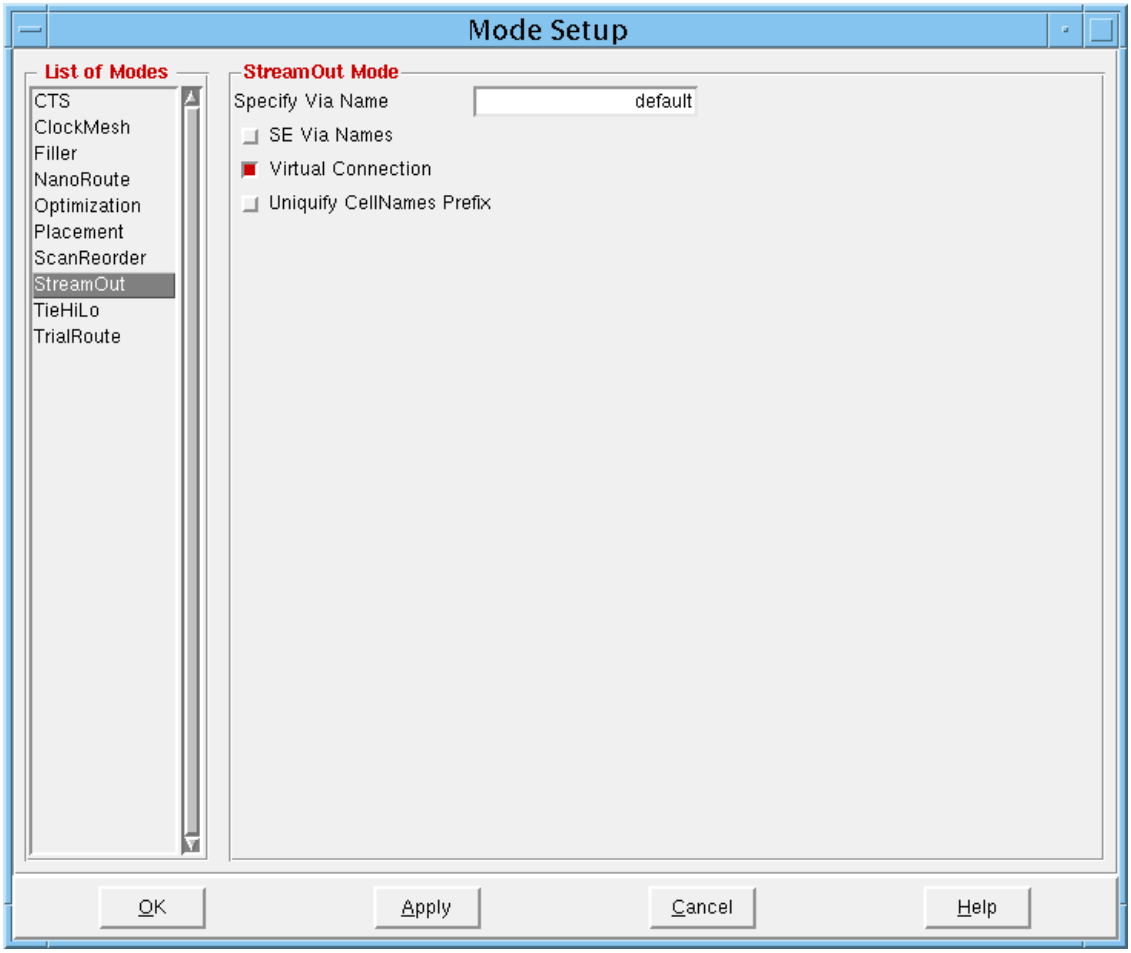
Related Text Commands

- `getScanReorderMode`
- `setScanReorderMode`

Mode Setup – StreamOut

Use the *Mode Setup – StreamOut* page to set the global options for creating a GDSII Stream file of the current database.

➤ Choose *Design – Mode Setup* and select *StreamOut*.



Fields and Options

Specify Via Name

Specifies the naming convention that the software uses for via cells declared in the DEF file.

Note: When the version of the GDS file is 3 (this is the default version), via names are truncated if they are longer than 32 characters. The software automatically appends a unique identifier to names if there is a name conflict.

You can use any of the following characters to specify a format string to generate names that give you information about the cell contents. Separate the characters with underscores (_) to improve readability. You can list them in any order.

- `%c`

  Specifies the number of columns.

- `%l(lcu)`

  Specifies the via layers. For the lower layer, use `%l` or `%l(l)`. For the cut layer, use `%l(c)`. For the upper layer, use `%l(u)`. You can specify one, two, or all three layers. You must enclose the `l`, `c`, and `u` in parentheses, as in the following examples: `%l(c)`, `%l(lu)`.

- %n

  Specifies the number of cut rows and columns that make up a cut array.

- `%r`

  Specifies the number of cut rows.

- `%t`

  Specifies the top structure name.

- %v

  Specifies the via name in the DEF file.

SE Via Names

Determines the naming convention used for vias declared in the LEF file. If you select this option, the software creates unique names. If you do not select this option, the software retains the LEF via names.

Default: Off

Virtual Connection

Appends a colon (:) label to pin names for DEF pins with the `.extra`*N* syntax and to LEF pins with multiple ports (if *Output Macros* is selected for LEF pin ports that have disjoint shapes).

Default: On

Uniquify CellNames Prefix

Adds a prefix, instead of a suffix, to uniquified cell names. The prefix is the source filename.

Default: Off (The software adds a suffix (also the source filename) to uniquified cell names)

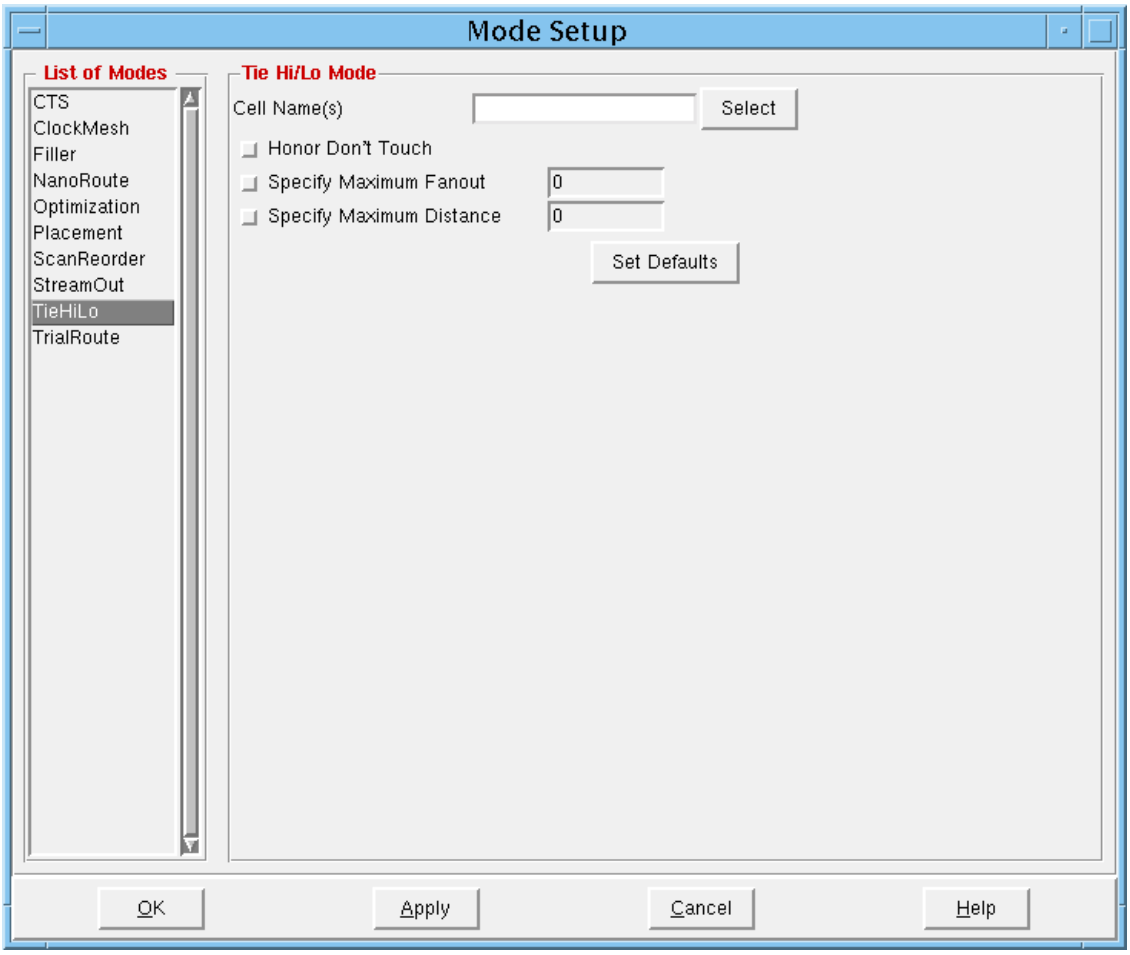
Related Text Commands

- `getStreamOutMode`
- `setStreamOutMode`
- `streamOut`

Mode Setup – TieHiLo

Use the *Mode Setup – TieHiLo* page to set global parameters for the Tie HI/LO commands.

➤ Choose *Design – Mode Setup* and select *TieHiLo*.



Fields and Options

Cell name(s)

Specifies the tie cell names to be used by the `addTieHiLo` command.

You can specify a maximum of two tie-cells, where one cell must be a tie-high driver, and the other a tie-low driver. The two tie-cell names must be in quotation marks.

Default: `""` (empty string)

Honor Don't Touch

Allows both `addTieHiLo` and `deleteTieHiLo` commands to honor the `dont_touch` property set on instances, nets, cells, and modules. For instances that need to be tied off, the `dont_touch` property has no effect, because the operation is on the net connected to one of its terms.
Default: Off

Specify Maximum Fanout

Specifies the number of tie-pins a tie-net can drive. A value of `0` implies no fanout constraint.
Default: `0`

Specify Maximum Distance

Specifies the distance, in microns, between the tie-cell driver and the tie-pins. A value of `0` implies no distance constraint.
Default: `0`

Set Defaults

Specifies the distance, in microns, between the tie-cell driver and the tie-pins. A value of `0` implies no distance constraint.
Default: `0`

Related Text Commands

- `getTieHiLoMode`
- `setTieHiLoMode`

Mode Setup – Trial Route Mode

The Mode Setup – Trial Route Mode page enables you to set global parameters for the Trial Route program. Parameters that you specify with this form are then used automatically whenever you run Trial Route, either explicitly through the `trialRoute` command or Trial Route form, or internally during in-place optimization, partitioning, or placement.

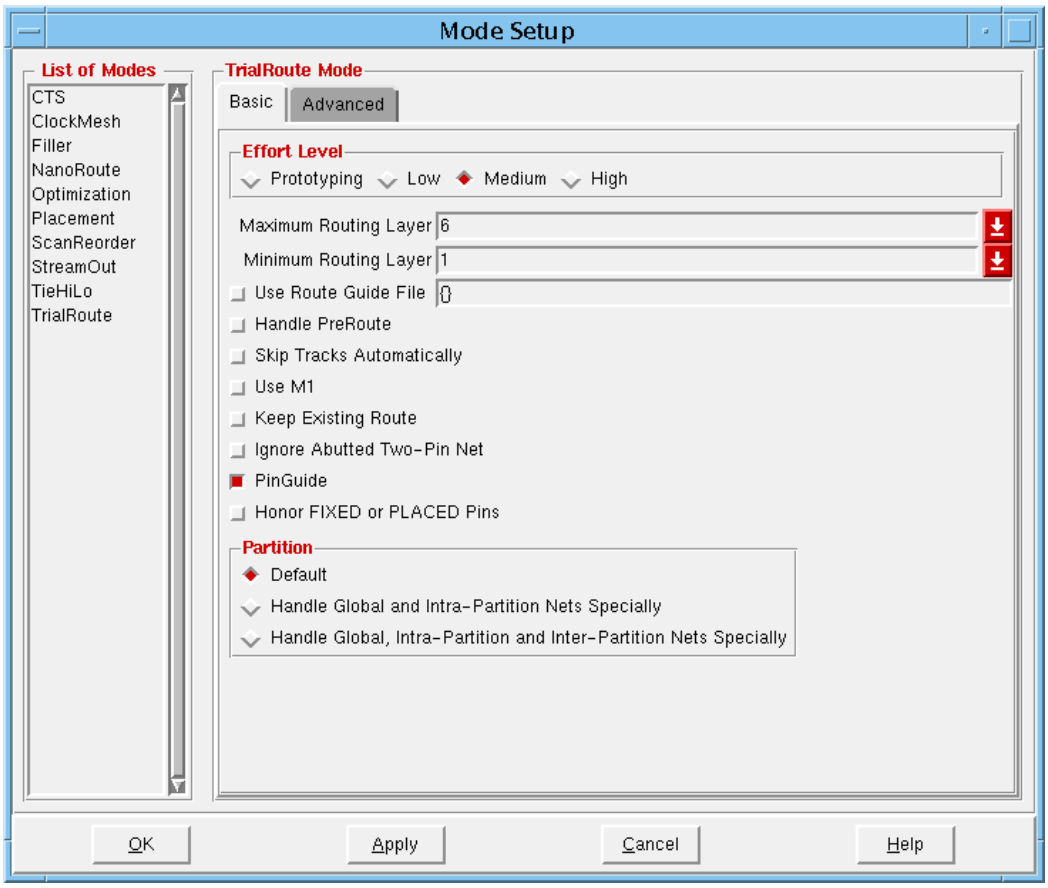
The Mode Setup – Trial Route Mode page contains the following subpages:

- Trial Route Mode – Basic on page 360
- Trial Route Mode – Advanced on page 366

Trial Route Mode – Basic

Use the *Basic* page of the Trial Route Mode page to set

➤ Choose *Design – Mode Setup* and select *TrialRoute*, then select *Basic*.



Fields and Options

Prototyping

Runs quickly to gauge the feasibility of your netlist, but components in your design might not be routed at legal locations.

The corresponding text command parameter is `-floorplan`.

Default: Off

Low

Completes a quick routing through all congested areas. Use this option only when routing a poorly designed netlist in which a part of the design is good and needs to be analyzed.

The corresponding text command parameter is `-noDetour`.

Note: If you use this option, the routing of the design might not be accurate because some nets might be routed through congested areas or over blockages in order to complete the routing.

Default: Off

Medium

Runs the default effort level of Trial Route. This level is used for most routing, including the final version of placement that is the input for detailed routing in a third-party tool.

Default: On

High

Runs additional iterations for resolving difficult routing congestions.

The corresponding text command parameter is `-highEffort`.

Default: Off

Maximum Routing Layer

Limits routing to layers at and below the specified layer. All metal layers above the specified metal number are not routed.

The corresponding text command parameter is `-maxRouteLayer`.

Minimum Routing Layer

Limits routing to layers at and above the specified layer. However, layers below the specified layer can still be used for routing if necessary, such as for short connections to pins.

You must specify a number greater than 1. Select the *Use M1* option to use layer m1 for routing.

The corresponding text command parameter is `-minRouteLayer`.

Use Route Guide File

Specifies a routing guide file to use. Guide files help control the routing topology by dividing the design into routing regions in which Trial Route then creates wires.

Guide files are generated when there are partially routed nets with `FIXED` wires in the design, and contain the following wire information: the coordinates of the wire ends, whether it is a horizontal or vertical wire, the width of the wire, and the layer number. The following example shows a section of a guide file:

```
routeGuideNet clk
wire 32.89 50 32.89 45.715 V 0.5 L 3
wire 32.89 45.715 32.89 10.045 V 0.5 L 5
wire 32.89 45.715 43.47 45.715 H 0.5 L 4
wire 32.89 10.045 7.13 10.045 H 0.5 L 4
wire 7.13 10.045 7.13 35.465 V 0.5 L 3
endRouteGuideNet
```

The corresponding text command parameter is `-guide`.

Default: Off

Handle PreRoute

Ignores pre-routed nets that have a status of Ignore in the database. You can use the `dbIsNetIgnoreInRoute` database command to check if a net has a database status of Ignore. To set the status of a net to Ignore, use the `dbSetIsNetIgnoreInRoute` database command.

The corresponding text command parameter is `-handlePreRoute`.

Note: Trial Route automatically maintains completely routed nets marked as `FIXED` or `COVER`.

Default: Off

Skip Tracks Automatically

Classifies nets by default rule, then route the nets for each rule, using the track constraints specified with the *Skip Tracks* option. Trial Route routes nets from the rule with the largest pitch first, then the second largest pitch, and so forth. After routing the nets for a rule, Trial Route marks them as pre-routed before routing the nets of the next rule.

The corresponding text command parameter is `-autoSkipTracks`.

Note: Wire overlap can occur if a gcell is only partially covered by a routing blockage or pre-routed wires.

Default: Off

Use M1

Uses layer *m1* to route the design rather than using *m1* for connecting to pins. This provides better route congestion results.

The corresponding text command parameter is `-useM1`.

Default: Off

Keep Existing Route

Maintains existing pre-routed nets, even if they are not marked `FIXED`.

The corresponding text command parameter is `-keepExistingRoute`.

Note: Trial Route automatically maintains completely routed nets marked as `FIXED` or `COVER`.

If your DEF file contains partially-routed nets with `FIXED` or `COVER` wires, Trial Route completes the routing for the nets. Trial Route cannot maintain the exact location of the wires; however, they are accurate within the gcell area.

Also, if you write out a DEF file after routing, all wires for the net are marked `FIXED`. You can no longer identify the original `FIXED` wires.

Default: Off

Ignore Abutted Two-Pin Net

Does not route nets that have two pins on the same layer whose pin geometries abut (that is, touch each other).

The corresponding text command parameter is `-ignoreAbutted2TermNet`.

Default: Off

Pin Guide

Uses the pin guide statements in the floorplan file (if they exist). If pin guide statements exist, Trial Route runs three times (similar to the *Handle Partition* option). If there are no existing pin guide statements, Trial Route runs once, which is its default behavior.

Trial Route also honors any pre-assigned pins (that is, pins marked `FIXED`)

The corresponding text command parameter is `-pinGuide`.

Default: On

Honor FIXED or PLACED Pins

Honors pre-assigned pins (pins marked `FIXED`) and assigned pins (pins marked `PLACED`). If these pins exist, Trial Route runs three times (similar to the *Handle Partition* option). If there are no existing pre-assigned or assigned pins, Trial Route runs once, which is its default behavior.

The corresponding text command parameter is `-honorPin`.

Default: Off

Default

Ignores partition specifications during routing.

Default: On

Handle Global and Intra-Partition Nets Specially

Routes intra-partition and global nets using the specifications of the partitions, such as area and the number of layers. This routing is based on the resources available after the chip is partitioned.

Use this option to gauge the congestion at the full chip level for the chip to be partitioned.

The corresponding text command parameter is `-handlePartition`.

Note: You can select this option in flat partitioned designs to simulate channel-based routing. For channelless designs, you must perform feedthrough insertion before you can select this option. For more information, see "Routing a Partitioned Design" in the *Encounter User Guide*.

Default: Off

Handle Global, Intra-Partition and Inter-Partition Nets Specially

Routes a net belonging to more than one partition so that the routing does not violate partition boundaries, in addition to routing intra-partition and global nets using the specifications of the partitions. For example, if a net belongs to partitions `P1` and `P3`, but not `P2`, the net is routed without going over the `P2` partition boundary.

The corresponding text command parameter is `-handlePartitionComplex`.

Note: You can use this option in flat partitioned designs to simulate channel-based routing. For channelless designs, you must perform feedthrough insertion before you can select this option. For more information, see "Routing a Partitioned Design" in the *Encounter User Guide*.

Default: Off

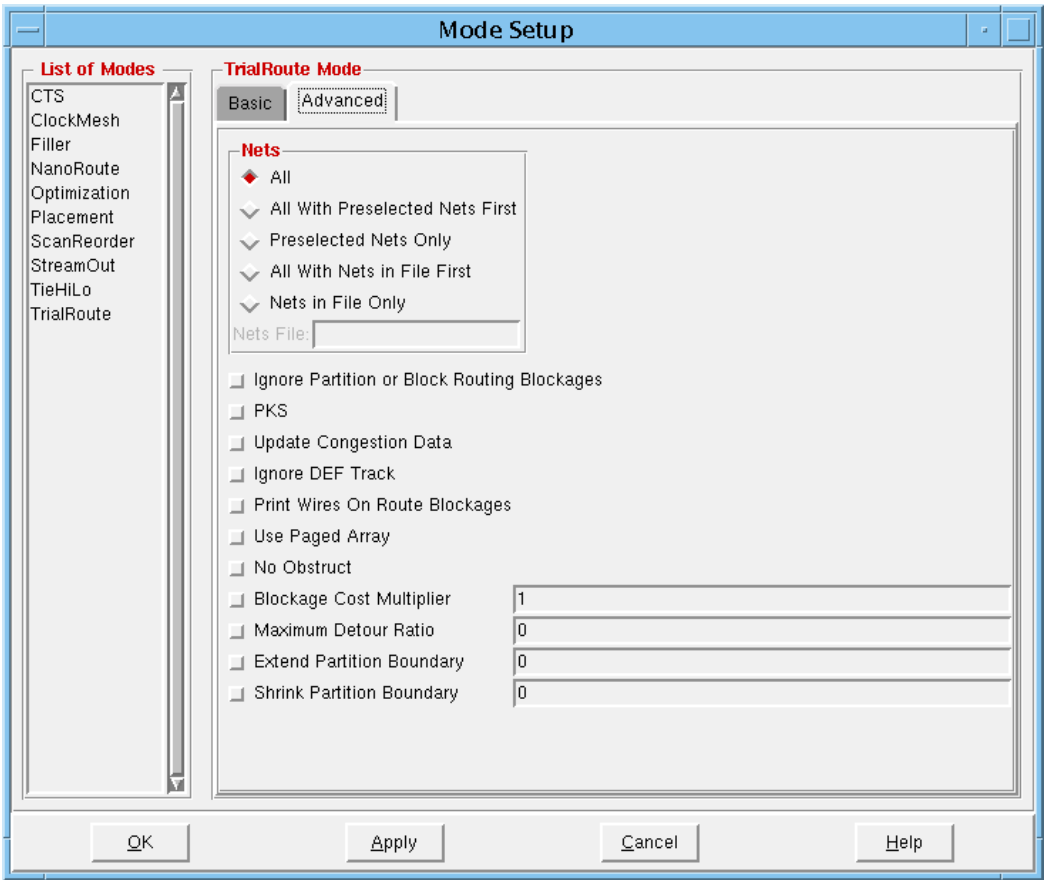
Related Text Commands

- `setTrialRouteMode`
- `trialRoute`

Trial Route Mode – Advanced

Use the *Advanced* page of the Trial Route Mode page to specify additional Trial Route options.

➤ Choose *Design – Mode Setup* and select *TrialRoute*, then select *Advanced*.



Fields and Options

All	Routes all nets, in no specific order. *Default:* On

All With Preselected Nets First

Routes the preselected nets first, then all remaining nets.

The corresponding text command parameter is `-selMarkedNet`.

Default: Off

Preselected Nets Only

Routes only the preselected nets.

The corresponding text command parameter is `-selMarkedNetOnly`.

Default: Off

All With Nets in File First

Routes the nets in the file specified in the *Nets File* option file first, then all remaining nets.

The corresponding text command parameter is `-selNet`.

Note: If you select this option and *Minimum Routing Layer*, Trial Route routes the nets in the file first on the layers at and above the specified minimum routing layer, then routes the remaining nets on all layers.

If you select this option and *Maximum Routing Layer*, Trial Route routes the nets in the file first. However, all nets are routed at and below the specified maximum routing layer.

Default: Off

Nets in File Only

Routes only the nets in the file specified in the *Nets File* option.

The corresponding text command parameter is -selNetOnly.

Default: Off

Nets File:

Specifies a net file containing net names. The file contains a list of net names, each on a separate line. You cannot specify wild cards.

Ignore Partition or Block Routing Blockages

Routes over all blocks and partitions.

The corresponding text command parameter is `-ignoreObstruct`.

Default: Off (Only routes over blocks and partitions that do not have routing blockages specified in their LEF files. Routing blockages for partitions are specified in a LEF file created by the Encounter software. This LEF file contains information set with the Specify Partition form, and is created when the partition is saved either with the Save Partition form or with the `savePartition` command.)

PKS

Generates net routes using a Steiner routing algorithm. These net routes are used for estimating routing congestion and determining net loading and delays for timing analysis.

The corresponding text command parameter is `-PKS`.

Default: Off

Update Congestion Data

Updates congestion data after the layer assignment phase of Trial Route mode. This displays congestion that is closer to the actual Trial Route result.

The corresponding text command parameter is `-updateRemainTrks`.

Default: Off

Ignore DEF Track

Ignores the track definitions specified in the `TRACKS` statement of the DEF file and defines its own tracks. Improperly defined tracks can cause Trial Route to take a long time to complete, and to sometimes crash.

The corresponding text command parameter is `-ignoreDEFTrack`.

Default: Off

Print Wires On Route Blockages

Prints the names of all wires that overlap routing blockages on the same layer to the log file. When used with the *Handle Partition* option, Trial Route also prints the names of wires that overlap temporary routing blockages derived from partition specifications.

The corresponding text command parameter is `-printWiresOnRTBlk`.

Default: Off

Use Paged Array

Breaks large linear arrays into chunks, or paged arrays for better memory usage.

You should only select this option for large jobs (that is, jobs with approximately one million cells or more) that are running out of memory. This feature works best when Trial Route is run in default mode.

The corresponding text command parameter is `-usePageArray`.

Default: Off

No Obstruct

Allows partial routing over routing obstructions and blocks. You can use this parameter when trial routing takes a long time to complete due to blocked terminals.

The corresponding text command parameter is `-noObstruct4`.

Default: Off

Blockage Cost Multiplier

Specifies the value by which to multiply the cost of the wire in order to avoid overlapping with a routing blockage in an area that is not completely blocked. The higher the wire number, the more Trial Routes attempts to avoid overlapping the wire with a blockage.

Specify a number between `2` and `10`.

The corresponding text command parameter is `-blockageCostMultiple`.

Default: Off

Maximum Detour Ratio

Attempts to re-route two-pin nets to reduce wire length when the wire length is greater than:

value x half the net bounding box perimeter

Trial Route reduces the wire length by relaxing the cost for congested gcells; therefore, reducing wire length can increase congestion.

Use this option when there are two-pin nets with long detours that slow timing.

The corresponding text command parameter is `-maxDetourRatio`.

Default: Off

Extend Partition Boundary

Specifies the spacing, in microns, between partition boundaries and wires outside of the partitions for top-level nets. Use this option to prevent outside wires from routing inside of partition boundaries.

Note: You can use this option only if you select the *Handle Partition* and *Handle Partition Complex* options.

The corresponding text command parameter is `-ptnBdryExt`.

Default: Off

Shrink Partition Boundary

Specifies the spacing, in microns, between partition boundaries and wires inside of the partitions when routing intra partition nets. Use this option to prevent inside wires from routing outside of partition boundaries.

The corresponding text command parameter is `-ptnBdryShr`.

Note: You can use this option only if you select the *Handle Partition* and *Handle Partition Complex* options.

Default: Off

Related Text Commands

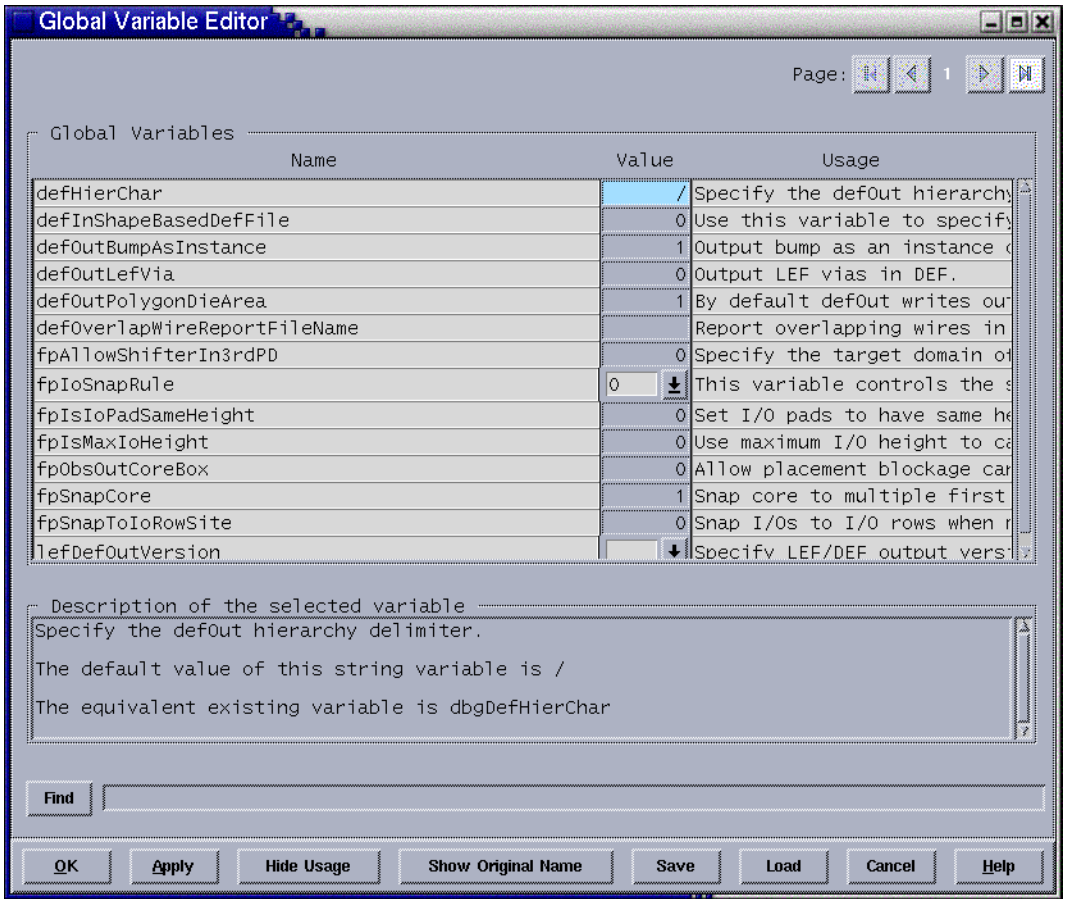
- `setTrialRouteMode`
- `trialRoute`

Global Variables

Opens the Global Variable Editor form. You can use this form to set and view the values of the global variables.

Currently, the Global Variable Editor supports global variables for the following areas: Floorplanning, DEF, and Power.

➤ Choose *Design – Global Variables*.



Global Variable Editor – Fields and Options

Name	Displays a selectable list of the global variables.
Value	Specifies the value of the global variable.
Usage	Displays a brief description of how the variable is used.

Description of the selected variable

	Displays a detailed description of the global variable currently selected in the *Name* field.
Find	Finds a global variable and displays it at the top of the Name field. To find a variable, type the name in the text field next to the *Find* button, and the click *Find*. **Note:** The variable name is case-sensitive.

Related Text Commands

For information on the following related text commands, see the *Encounter Text Command Reference*:

- `getUserDataValue`
- `getUserDataDesc`
- `getUserDataType`
- `getUserDataDefaultValue`
- `getUserDataAlias`
- `getUserDataRange`
- `saveUserDataFile`
- `loadUserDataFile`
- `getUserDataName`

Multiple CPU Processing

Use the *Design* menu's Multiple CPU Processing form to set options for multi-threading, distributed processing, and Superthreading.

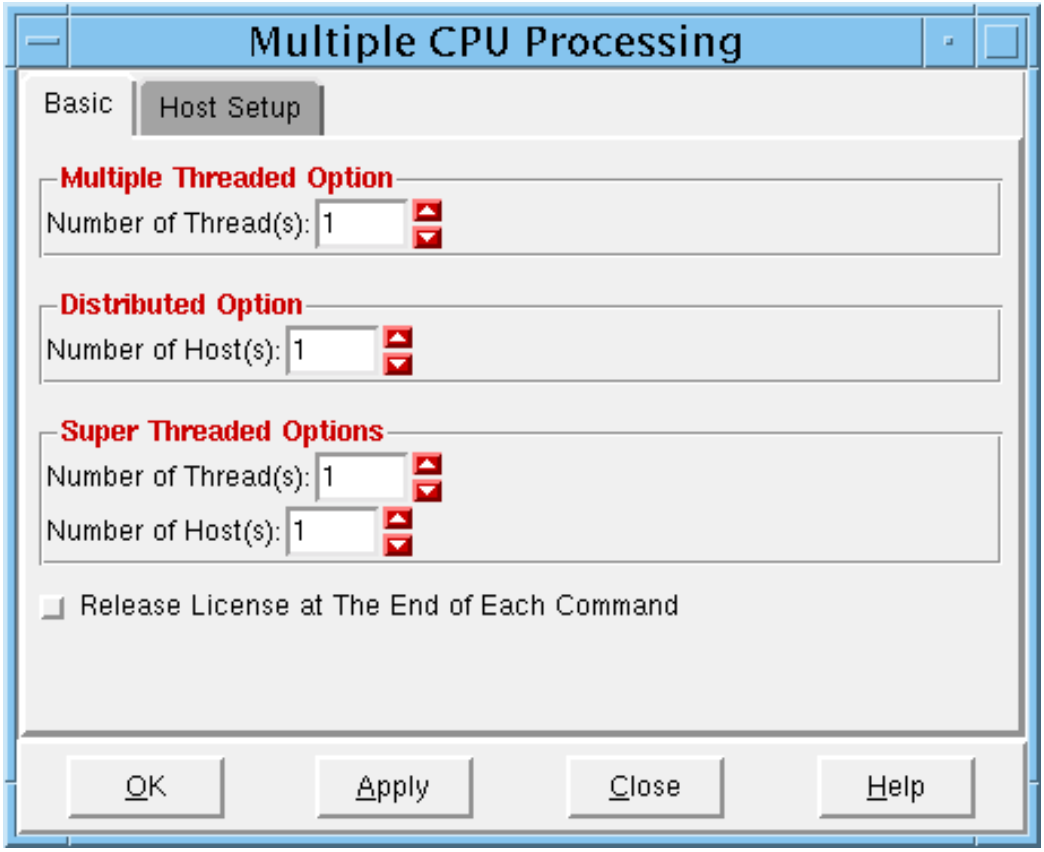
The Multiple CPU Processing form contains the following pages:

- Multiple CPU Processing – Basic on page 374
- Multiple CPU Processing – Host Setup on page 377

Multiple CPU Processing – Basic

Use the *Basic* page of the Multiple CPU Processing form to specify options for multi-threading, distributed processing, and Superthreading.

➤ Choose *Design – Multiple CPU Processing* and click the *Basic* tab.



Multiple CPU Processing – Basic Fields and Options

Multiple Threaded Option
Number of Threads

Specifies the maximum number of threads in one machine to use for multi-threaded processing.

Default: 1

Distributed Option
Number of Hosts

Specifies the maximum number of machines to use for distributed processing.

Default: 1

Super Threaded Options

Number of Threads

Specifies the maximum number of threads in one machine to use for Superthreading.

Default: 1

Important

This option is enabled for the NanoRoute router only.

Number of Hosts

Specifies the maximum number of machines to use for distributed processing.

Default: 1

Important

This option is enabled for the NanoRoute router only.

Release License at The End of Each Command

Releases the additional licenses used for multiple-CPU processing as soon as the current multi-thread, distributed processing, or Superthread process completes.

Default: All licenses remain checked out for the duration of the session.

Related Text Command

- `releaseMultiCpuLicense`
- `setMultiCpuUsage`
- `setReleaseMultiCpuLicense`

Related Topics

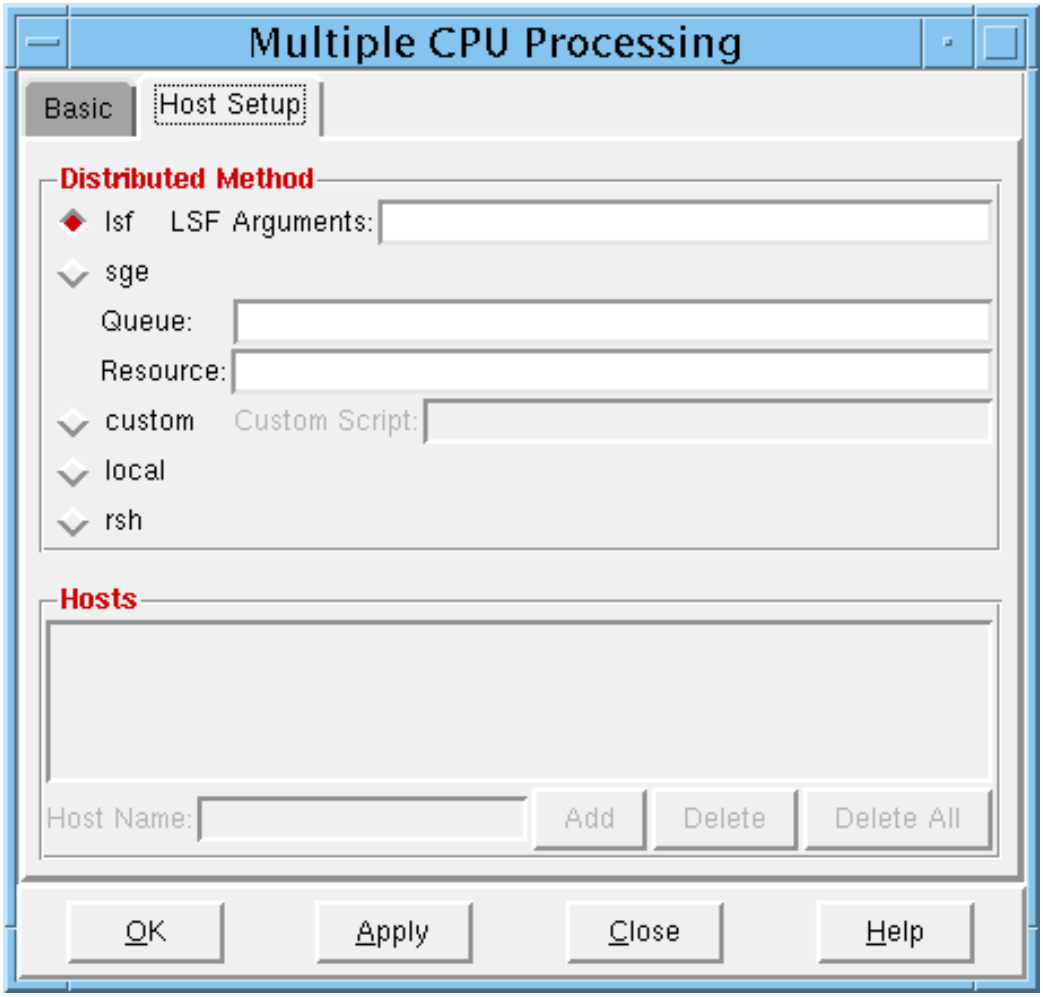
- Getting Started Chapter in the *Encounter User Guide*

- “Running Multiple-CPU Processing”

Multiple CPU Processing – Host Setup

Use the *Host Setup* page of the Multiple CPU Processing form to specify options for distributed processing and Superthreading.

➤ Choose *Design – Multiple CPU Processing* and click the *Host Setup* tab.



Multiple CPU Processing – Host Setup Fields and Options

Distributed Method	Specifies the type of distributed processing to run. Select one of the following options:

lsf

Specifies a Load Sharing Facility configuration. If you do not specify any values in the *LSF Arguments* text entry box, the software uses default settings.

Important

To use this option, LSF must already be set up (typically by specifying the `LSF_ENVDIR` and `LSF_SERVERDIR` environment variables) and `bsub` must be in your search path. Contact your LSF administrator for details.

LSF Arguments

Specifies the `bsub` options. For information, see the LSF documentation.

sge

Specifies a Sun Grid Engine configuration. For more information, see the SGE documentation.

Queue

Specifies the queue. The software uses the default queue name you do not specify one.

Resource

Specifies a resource string for the LSF queue.

Important

The correct resource string is specific to your installation. Contact your LSF administrator for the appropriate parameters and values.

custom

Specifis a custom configuration.

Custom Script

Specifies a custom script to run distributed processing.

local

Runs all distributed processing jobs on the master machine.

rsh

Creates or modifies a remote shell (rsh) configuration.

Hosts

Specifies remote hosts to use for distributed processing.

Host Name

Specifies the hosts to add or remove.

Related Text Command

- `setDistributeHost`

Related Topics

- Getting Started Chapter in the *Encounter User Guide*
  - "Running Multiple-CPU Processing"

Show/Hide

Use the *Show/Hide* menu to show or hide any the following display options:

Menu Buttons	Controls the shortcut menu button display at the top of the GUI.
Status Bar	Controls the message bar display below of the main design display area, which shows object identifier or coordinate information.
Tool Box	Controls the tool widget display above the design display area. See Tool Widgets on page 72 for more information.
Object Color	Controls the visibility, selectability, and color display of various attributes at the top right side of the main window.
World View	Controls the satellite window display at the middle right side of the main window. See Satellite Window on page 98 for more information.
Hints	Activates the help system.
Help Automatically	Activates the help system.

Note: To save windows selected or deselected in the *Show/Hide* menu, you can save it to the `enc.pref.tcl` file from the *Preferences – Windows* form. See Preferences – Windows on page 282 for more information.

Exit

Use the *Exit* menu command to end an Encounter session.

3

Edit Menu

- Find/Select Object on page 385
- Deselect All on page 394
- Highlight Selected on page 395
- Clear Highlight on page 396
- Edit Highlight Color on page 397
- Clear Ruler on page 398
- Pin Editor on page 399
  - Reorder Pin List on page 405
  - Pin Alignment on page 407
- Wire Editor on page 409
  - Edit Route– Route on page 410
  - Edit Route – Nets on page 412
  - Select A File (for Net Names) on page 415
  - Edit Route – Override on page 417
  - Select A File (for Override Values) on page 419
  - Edit Route – Shielding on page 421
  - Edit Route – Snap on page 423
  - Edit Route – Via on page 425
  - Edit Route – Wire Group on page 427
  - Edit Route – Miscellaneous on page 433
  - Special Route Options on page 437

- Select/Delete/Deselect Routes on page 439
- Edit Via on page 442
- Edit Via – Viacell on page 446
- Edit Route Widgets on page 447

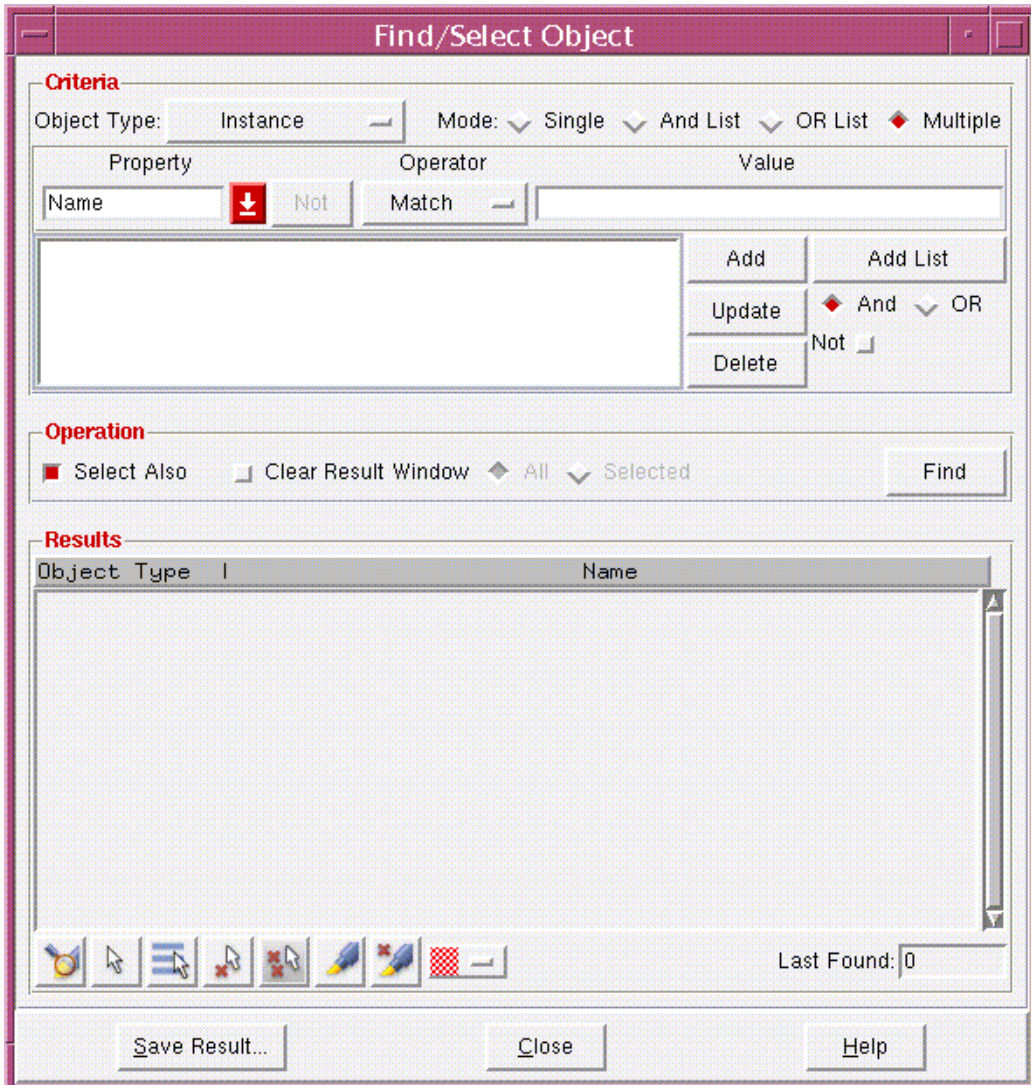
- Object on page 449
  - Edit Pin Group on page 450
  - Edit Net Group on page 454
  - Create Non Default Rules on page 458
    - Add Via Cell on page 460
- Custom Object Editor on page 461

Find/Select Object

Use the Find/Select Object form to find and select specific object types in the design display area.

Note: The Select operations are recorded in the command file and the log file with the `selectObjByProp` command.

➤ Choose *Edit – Find/Select Object*.



Find/Select Object Fields and Options

Object Type

Specifies the type of object to find. Choose from: *Instance*, *Pin, Net, Module, Instance Group*, or *Bump*.

The `Pin` object type pin can be used for I/O pins, partition pins, and instance pins. Names of instance pins and/or partition pins should be specified with the full path name. For example, pin A of instance DTMF_CHIP/alu should be specified as:

```
DTMF_CHIP/alu/A
```

You can use the *Net* option to find/display bus names.

Mode

Specifies the type of find/select operation. Select one of the following:

- *Single*: Performs a simple search for a Property/Value combination.
- *And List*: Performs a find/select operation that matches an AND list of two or more multiple Property/Value combinations.
- *OR List*: Performs a find/select operation that matches an OR list of two or more multiple Property/Value combinations.
- *Multiple*: Performs a find/select operation that matches multiple lists of Property/Value combinations; these lists can be a combination of AND lists and OR lists.

For more information, see Mode Settings on page 389

Property

Displays the available properties for the object that you selected in the Object Type field.

You can use the pre-defined property `Connection` to find/select objects by connectivity. The `Connection` property supports connectivity search for the following objects:

- Instance
- Pin
- Net
- Module
- Selected objects

NOT

Inverses the value of the operator in the Operator field. For example, If the value in the Operator field is `<,` clicking the NOT button effectively changes the value to `NOT <`

Operator

Specifies the relationship between the property and its value.

This field is dynamically populated based on the specified object type.

Value

Specifies the value of the property.

This field is dynamically populated based on the specified object type. In some cases, you may have to manually specify a value, for example, the name of a cell.

Add

Adds the search criteria based on the values of Property, Operator, and Value fields. The search criteria are displayed in the form.

This button is not available if you select the *Single* mode.

Delete

Deletes the currently selected search criteria.

This button is not available in the *Single* mode.

Update

Updates the currently selected search criteria based on the values of Property, Operator, and Value fields.

This button is not available in the *Single* mode.

Add List	Adds a blank list to the search criteria. This button is available only in the *Multiple* mode. ■ If the And button is selected, an AND list is added ■ If the OR button is selected, an OR list is added. You can then add search criteria to the list by specifying values in the Property, Operator, and Value fields, selecting the list in the search criteria, and clicking the *Add* button. You can create a NOT AND list or a NOT OR list by selecting the *Not* button before you click the *Add List* button.
And	Specifies that the list added through the *Add List* button is an AND list. This button is available only in the *Multiple* mode.
OR	Specifies that the list added through the Add List button is an OR list. This button is available only in the *Multiple* mode.
Not	Creates a NOT AND list or a NOT OR List when the Add List button is clicked.
Select Also	Finds all objects that meet the specified criteria, reports them in the *Results* window, and selects them in the design display area. *Default:* The objects are reported in the results window but are not selected in the design display area.
Clear Result Window	Clears objects previously listed in the *Results* list, then finds the objects that meet the specified criteria and reports them in the Results list. *Default:* The objects previously listed are retained in the results window along with the results of the current search.
All	Clears all objects previously listed in the Results list.
Selected	Clears those objects previously listed in the Results list that are currently selected in the *Results* list.
Find Only	Finds all objects that meet the specified criteria and reports them in the *Results* window.

Zoom in Highlighted

Zooms in the highlighted object(s). You can highlight object(s) by selecting them in the results window and clicking the *Highlight* button

Select

When you click *Select*, the objects selected in the Results window are selected in the design display area.

Select All

When you click *Select All*, all the objects in the Results window are selected in the design display area.

Deselect

When you click *Deselect*, the objects selected in the Results window are deselected in the design display area.

Deselect All

When you click *Deselect All*, all the objects in the Results window are deselected in the design display area.

Highlight

When you click *Highlight*, the objects selected in the Results window are highlighted in the design display area.

Dehighlight

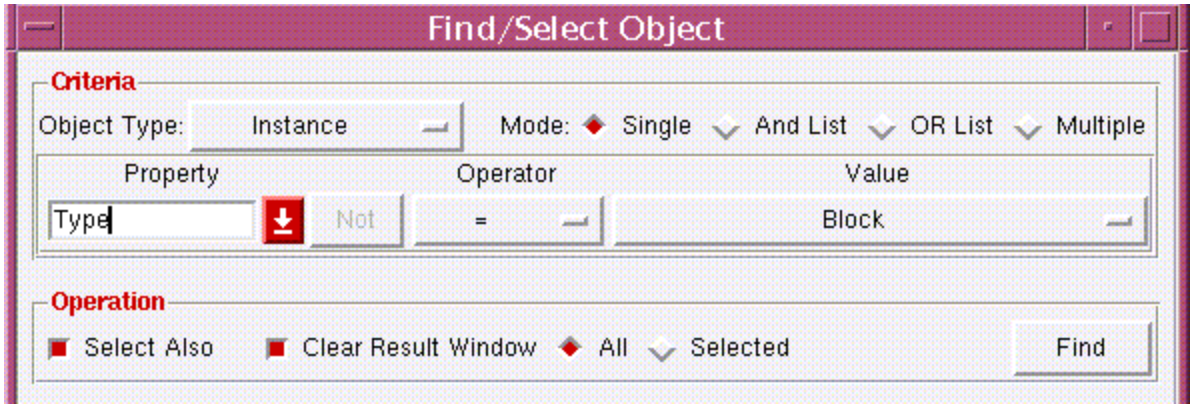
When you click *Dehighlight*, the objects selected in the Results window are dehighlighted in the design display area.

Mode Settings

The Mode field in the Find/Select Object form provides the following options:

Single

Performs a simple search for a Property/Value combination. The following example illustrates the search for all instances of the type BLOCK.



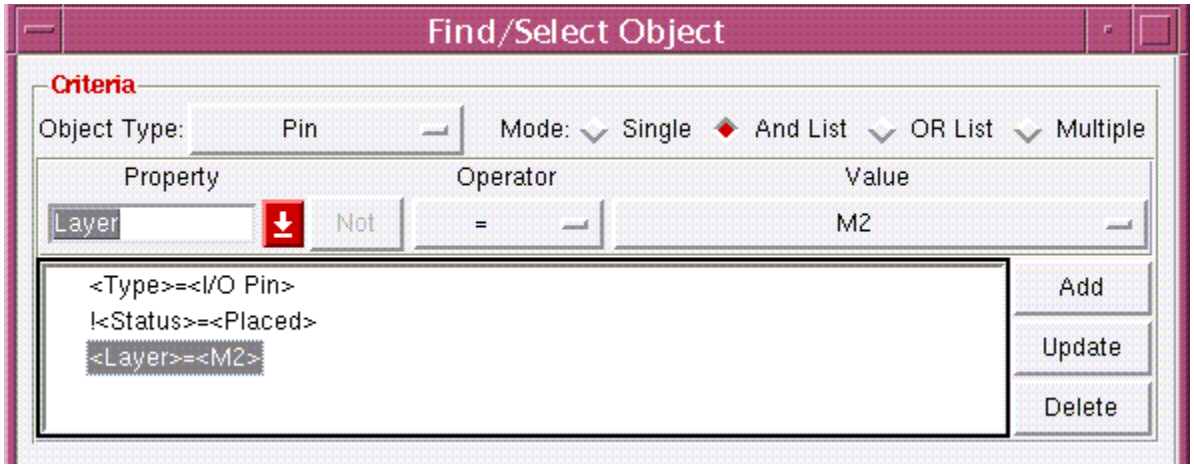
The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Instance <Type>=<Block>
```

And List

Performs a find/select operation that matches an AND list of two or more Property/Value combinations. The following example illustrates the search for all pins that match *all* of the following criteria:

- type is I/O
- layer is M2
- status is not *placed*

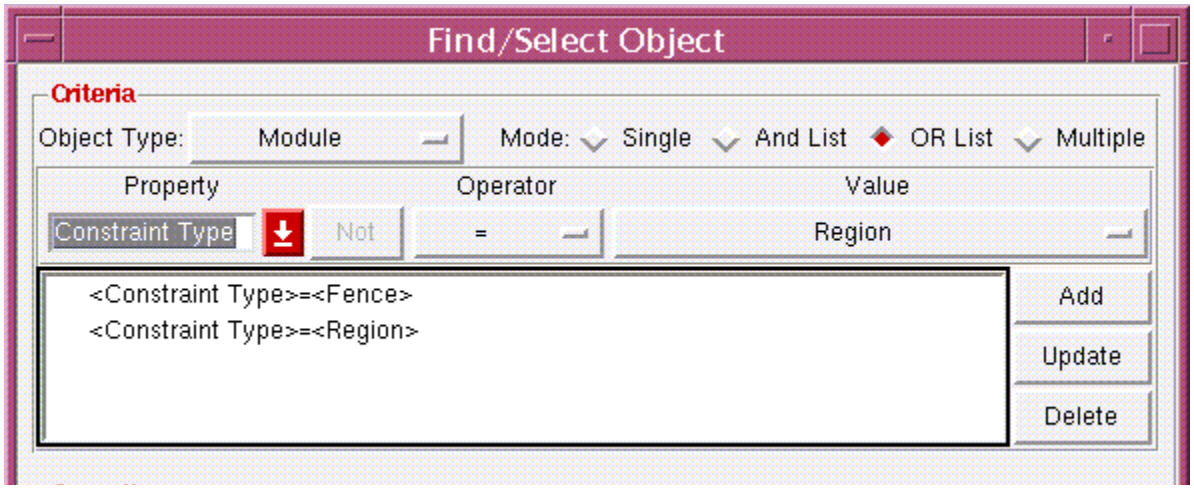


The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Pin {And(<Type>=<I/O Pin>,!<Status>=<Placed><layer>=<M2>)}
```

OR List

Performs a find/select operation that matches an OR list of two or more Property/Value combinations. The following example illustrates the search for all modules whose constraint type is Fence or Region



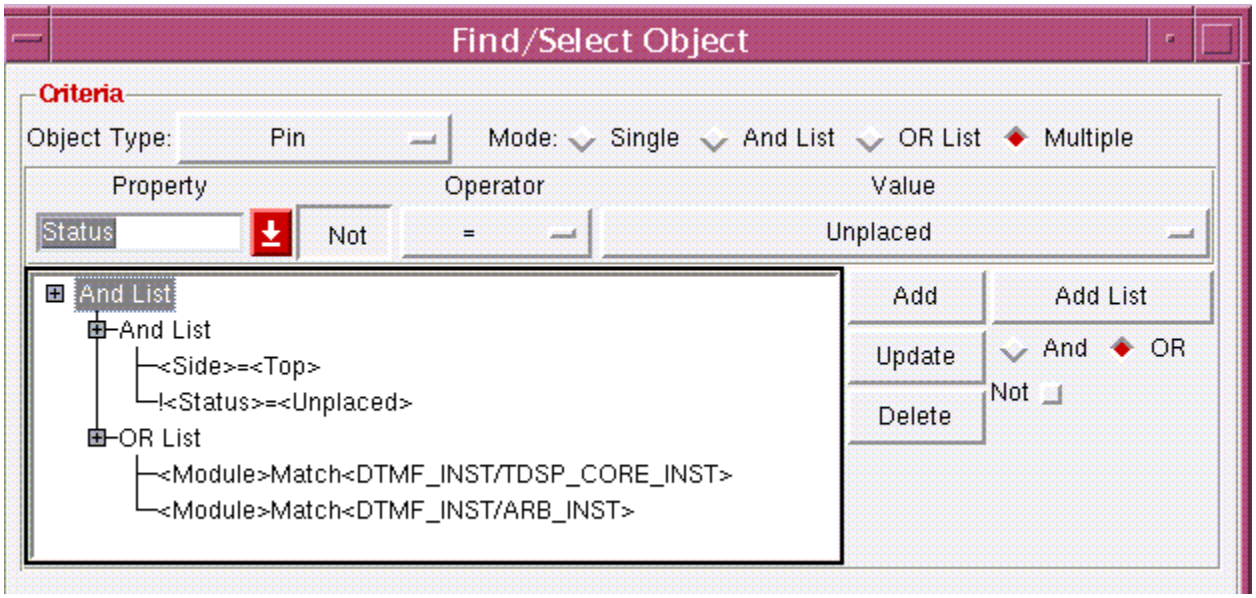
The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Module {OR(<Constraint Type>=<Fence>,<Constraint Type>=<Region>)}
```

Multiple List

Performs a find/select operation that matches multiple lists of Property/Value combinations; these lists can be a combination of AND lists and OR lists. The following example illustrates the find/select operation for all pins of the modules DTMF_INST/TDSP_CORE_INST and

DTMF_INST/ARB_INST that are on the top side and have a status of *placed*, *fixed*, or *cover*.



The select operation logged in this case by the `selectObjByProp` command would be:

```
selectObjByProp Pin
And(And(!<Status>=<Unplaced>,<Side=<Top>),OR(<Module>Match<DTMF_INST/
TDSP_CORE_INST>,
<Module>Match<DTMF_INST/ARB_INST>))
```

Related Text Commands

The following text command provides equivalent or additional functionality:

- `selectObjByProp`
- `selectGroup`
- `deselectGroup`
- `selectInstByCellName`
- `deselectInstByCellName`
- `selectInstOnNet`
- `deselectInstOnNet`
- `selectIOPin`
- `deselectIOPin`

For more information, see “Floorplan Commands” in the *Encounter Text Command Reference.*

Deselect All

Use the *Deselect All* menu command to deselect all selected nets.

➤ Choose *Edit – Deselect All*.

Highlight Selected

Use the *Highlight Selected* menu command to highlight the object sets, and choose the highlight color, that are selected with the Find by Name form.

➤ After selecting an object set, choose *Edit – Highlight Selected*.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `highlight`
- `selectGroup`
- `deselectGroup`
- `selectInstByCellName`
- `deselectInstByCellName`
- `selectInstOnNet`
- `deselectInstOnNet`
- `selectIOPin`
- `deselectIOPin`

For more information, see “Floorplan Commands” in the *Encounter Text Command Reference.*

Clear Highlight

Use the *Clear Highlight* menu command to clear the design display area of the highlighted objects that were selected with the *Highlight Selected* menu command.

➤ Choose *Edit – Clear Highlight*.

Related Text Commands

The following text command provides equivalent or additional functionality:

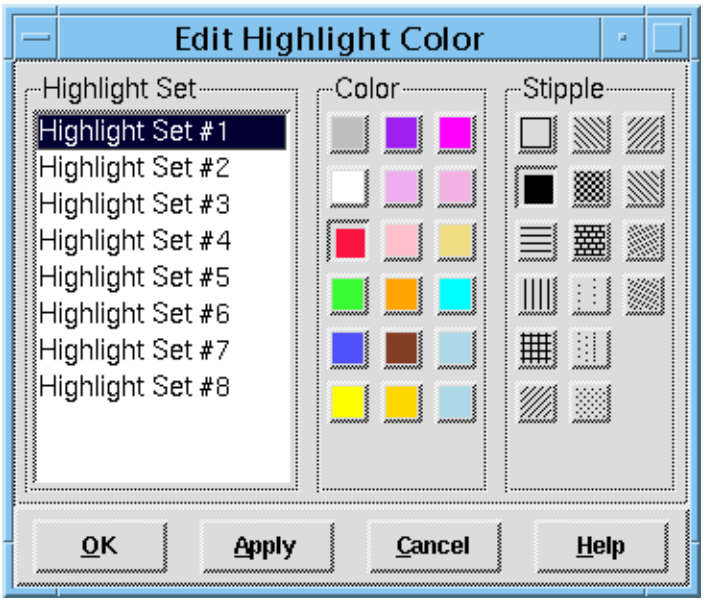
- `selectGroup`
- `deselectGroup`
- `selectInstByCellName`
- `deselectInstByCellName`
- `selectInstOnNet`
- `deselectInstOnNet`
- `selectIOPin`
- `deselectIOPin`

For more information, see “Floorplan Commands” in the *Encounter Text Command Reference.*

Edit Highlight Color

Use the Edit Highlight Color form to further customize the highlight color and pattern of selected object sets in the design display area.

➤ Choose *Edit – Edit Highlight Color*.



Edit Highlight Color Fields and Options

Highlight Set	Specifies the highlight set.
Color	Specifies the highlight color.
Stipple	Specifies the highlight pattern.

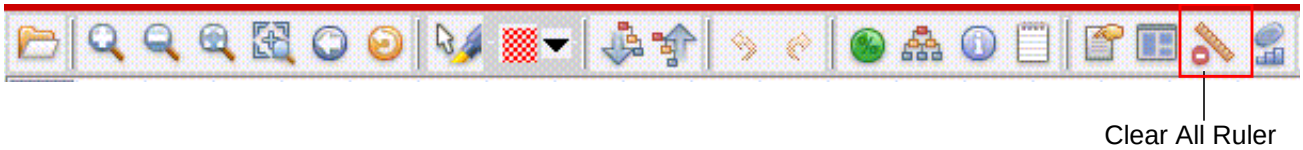
Related Text Commands

There are no related text commands. This feature is available only through the Encounter *Edit* menu.

Clear Ruler

Select Edit – Clear Ruler to clear all ruler lines.

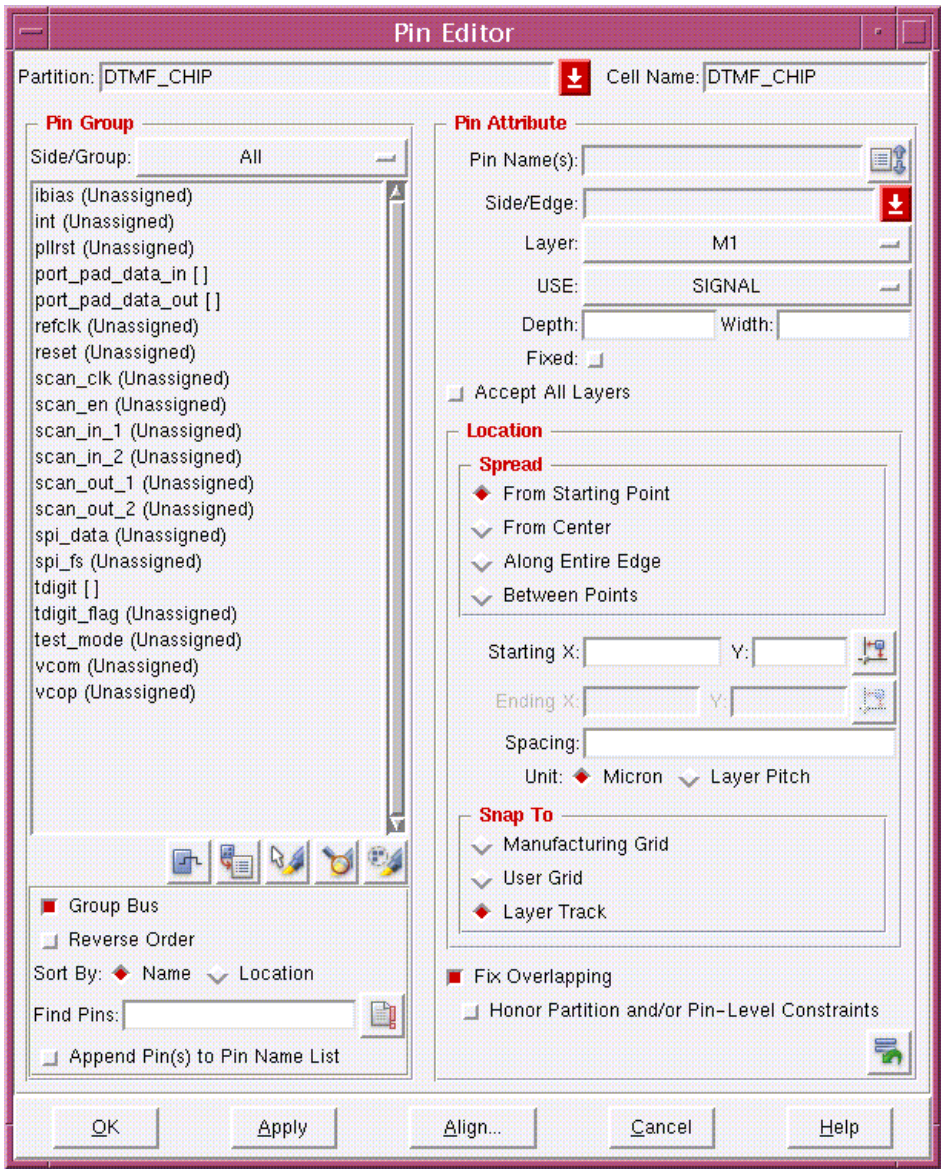
You can also clear the ruler lines with the Clear All Ruler icon in the main window.



Pin Editor

Use the Pin Editor to display and edit pin and pin groups.

➤ Choose *Edit – Pin Editor*.



Pin Editor Fields and Options

Partition

Specifies the partition name to display the pin group for all the pins in a partition, and the cell name (module name) of the currently specified partition. Pins are grouped alphabetically if they are unassigned.

Side/Group

Displays pins by side or group. For the pin group list, you can select a side or group criteria of *Top*, *Bottom*, *Left*, *Right*, *Inside*, *Unassigned*, *All*, or *Other*.

Inside: The group of pins that are assigned but not on boundary.

Other: The pins that you bring in from the artwork window by clicking the Get Selected Pin icon.

Pin Group

The *Pin Group* panel provides the following widgets and options:

Timing Budget Info.—Displays timing budgeting justification information for the highlighted pins, if timing information is available. For more information on timing budgeting, see "Timing Budgeting" on page 305.

Get Selected Pin—In the *Pin Group* panel, lists pins that you have selected in the design display area.

Select Highlighted in Display—In the design display area, selects the pins that you have highlighted in the *Pin Group* panel.

Zoom in Highlighted in Display—In the design display area, zooms in on the pins that you have highlighted in the *Pin Group* panel.

Group Highlighted—Creates a temporary subgroup list of the original pin group.

Group Bus

Groups bus bits with their respective pins for ease in reordering the pin list.

Reverse Order

Reverses the pin ordering in the pin list.

Sort by

Sorts according to one of the following options:

Name: Sorts in alphabetical order.

Location: Sorts left to right, and bottom to top.

Find Pins Searches for pins by name. You can use the asterisk (*) as a wildcard character for this field.

Click the *Update* icon, or press `Return` to start the search.

Update Updates the list of pins after the Find operation.

Append Pin(s) to Pin Name List

Allows you to add multiple pins to the *Pin Name(s)* list. You can select multiple pins in the Pin Group list by clicking SHIFT + pin name (contiguous selection) or CTRL + pin name (non-contiguous selection). These pins are added to the pin name list.

If the Append Pin(s) to Pin Name List option is selected, any new pins that you select from the Pin Group will be appended to the pin name list. If this option is off, any new pins that you select from the Pin Group will replace the previous list of pins.

Pin Name(s) Displays the pin or pin group names as selected from the pin group list. Click the widget to the right of the field.

This opens the Pin Editing List form. For more information, see "Reorder Pin List" on page 405.

Side/Edge Displays the side. For rectilinear partitions, also displays the edges. Use the pull-down menu to assign a side or an edge. You can select *Top*, *Bottom*, *Left*, *Right*, *Inside*, or *Unassigned* for side, or the edge number for a particular edge.

Layer Displays the layer. Use the pull-down menu to assign a new layer.

USE Specifies one of the following +USE properties:

- SIGNAL
- CLOCK
- ANALOG

Depth Displays the depth of the edited pin in microns.

Width Displays the width of the edited pin in microns.

Fixed

If selected, sets pin status to *fixed*.

Default: The pin status is set to *placed*.

Accept All Layers

Includes all layers specified in the technology file, regardless of layers specified for *Partition Pin Layer Used* in the *Specify Partition* form.

If you do not use this option, the Encounter software shows only the preferred routing layers selected in the *Specify Partition* form.

Spread

Defines how to position pins along a block's edge.

Choose one of the following options:

From Starting Point

Uses the coordinates of the first pin in the *Pin Name* list as the starting point (anchor) for spreading a group of pins.

From Center

Spreads pins beginning at the starting x and y coordinates of the center of the block's edge or side.

Along Entire Edge

If you had selected an Edge in the Side/Edge option, the pins are spread evenly along the entire specified edge, using the limits of the edge as the starting and ending points.

If you had selected a side in the Side/Edge option, the pins are spread evenly along all the edges belonging to the specified side. The pins are spread from left to right and from top to bottom.

The Pin Editor determines the appropriate spacing.

Between Points

Spreads pins evenly along the block edge between points you specify with *Starting X/Y* and *Ending X/Y*. The ending coordinates become the coordinates of the last pin in the pin group. The Pin Editor determines the appropriate spacing.

For rectilinear partitions, if the start and/or end points are not on the specified side, the start and/or end points are snapped to the nearest correct location on the specified side.

Starting X/Y Specifies the x and y starting location. Use the mouse widget to get the coordinates from the design display area.

Ending X/Y Specifies the x and y ending location. Use the mouse widget to get the coordinates from the design display area.

Spacing Displays the spacing between pins for multi-pin editing. The spacing is either in micrometers or by layer track, as specified by *Unit*.

Positive spacing values spread pins to the right along a horizontal block edge, or up along a vertical block edge.

Negative spacing values spread pins to the left along a horizontal block edge, or down along a vertical block edge.

Unit Specifies the units used for pin spacing: micrometers or layer tracks.

Snap To Indicates the grid or layer to which the pins should snap:

Manufacturing Grid

Specifies that the pins should snap to the manufacturing grid.

User Grid Specifies that the pins should snap to a user-defined grid.

Layer Track

Specifies that pins should snap to the layer tracks.

Fix Overlapping If selected, automatically moves the pin to the closest acceptable position. When deselected, allows a pin to be placed in the selected position, overriding overlap rules.

Note: This option applies only to *Snap To Layer Track*.

Honor Partition and/or Pin-Level Constraints

If selected, the user-defined partition-level and/or pin-level constraints will be followed.

The following constraints are honored when this option is selected: pin spacing, pin size, pin-to-corner distance, and partition-allowed pin layers.

If not selected, the user-defined constraints are not applied to the affected pins. in this case, the pins are assigned exactly as per the attributes you specify in the Pin Editor form.

	Reset Pin Info—Resets the pin editing entries to their original values.
Align	Opens the Pin Alignment form. For more information, see "Pin Alignment" on page 407

Related Command

For information on the following command, see "Partition Commands" in the *Encounter Text Command Reference.*

- `editPin`

Related Topics

For information on the following topics, see "Floorplanning the Design" in the *Encounter User Guide*.

- Using the Pin-Spreading Feature
- Using a Pin as the Starting Point for Spreading Pins
- Using the Center of a Block Edge as the Starting Point for Spreading Pins
- Spacing Pins Evenly Using the Block Edge Ends as Limits
- Spacing Pins Evenly Using Explicit Starting and Ending Points

Reorder Pin List

Use the Reorder Pin List form to display and manage your pin editing session.

Complete the following steps:

1. Choose *Edit – Pin Editor*, or click the *Design Browser* widget on the toolbar.
2. Click on a pin or group of pins from the *Pin Group* panel.
3. Click the widget to the right of the *Pin Name(s)* text field.

Click this widget to open the Reorder Pin List form

The Reorder Pin List form appears.

Reorder Pin List Fields and Options

Pin Names

Highlight a pin and use the up or down arrow keys at the right side of the Reorder Pin List form to move the pin to a different place in the pin list.

You can also select a pin and drag-and-drop it to the new location.

Group Bus / Expand Bus	*Group Bus*: Groups bus pins.
	Expand Bus: Ungroups bus pins.
Reverse	Reverses the order of the selected pins.
Delete	Deletes selected pins from the list.

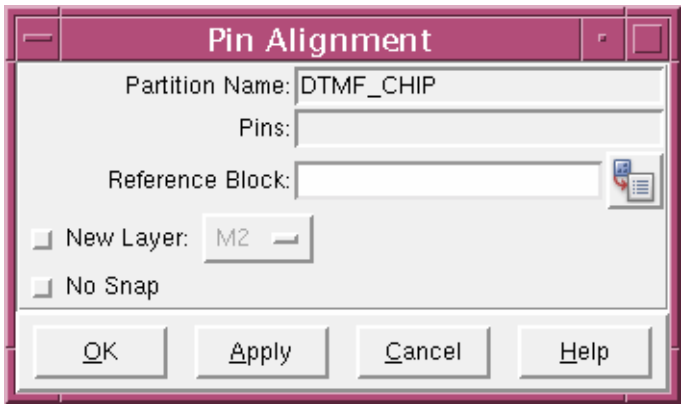
Pin Alignment

Use the Pin Alignment form to align pins between blocks on their facing edges. By default, this command snaps pins to the routing grid.

Note: Specified pins will not be aligned if they do not have the reference connections on the reference block, or if the reference pins are not assigned prior to running this command.

Complete the following steps:

1. Choose *Edit – Pin Editor*, or click the *Pin Editor* widget on the toolbar.
2. Click the *Align* button at the bottom of the Pin Editor.



Pin Alignment Fields and Options

Partition Name	Specifies the name of the partition for which you want to align pins.
Pins	Specifies the pin(s) to be aligned between the facing edges of the target block and reference block. This field contains the same value(s) as *Pin Name(s)*. When you select a pin group in the Pin Editor, those pins appear in the *Pins* field of this form.
Reference Block	Specifies the instance name of the reference block to which the specified pins will be aligned.

New Layer	Specifies whether to keep the current pin layer or specify a new pin layer. *Default*: If you do not specify this option, the new pin layer will be the same as the referenced layer to reduce wire routing.
No Snap	Prevents pins from being snapped to the routing grid.

Related Text Command

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `pinAlignment`

Wire Editor

Use the Edit Route form (Edit – Wire Editor) to edit wires and vias. The information you specify on the form applies only to wires and vias that you add or change with the wire editor—it does not affect wires or vias added by the NanoRoute router, the WRoute router, power route, or other routing commands.

Tip

For quick access to this form, use the e bindkey.

The Edit Route form contains the following pages:

- Edit Route– Route on page 410
- Edit Route – Nets on page 412
- Edit Route – Override on page 417
- Edit Route – Shielding on page 421
- Edit Route – Snap on page 423
- Edit Route – Via on page 425
- Edit Route – Wire Group on page 427
- Edit Route – Miscellaneous on page 433

The Edit Route form provides access to the following additional forms and widgets:

- Select A File (for Net Names) on page 415
- Select A File (for Override Values) on page 419
- Special Route Options on page 437
- Select/Delete/Deselect Routes on page 439
- Edit Via on page 442
- Edit Route Widgets on page 447

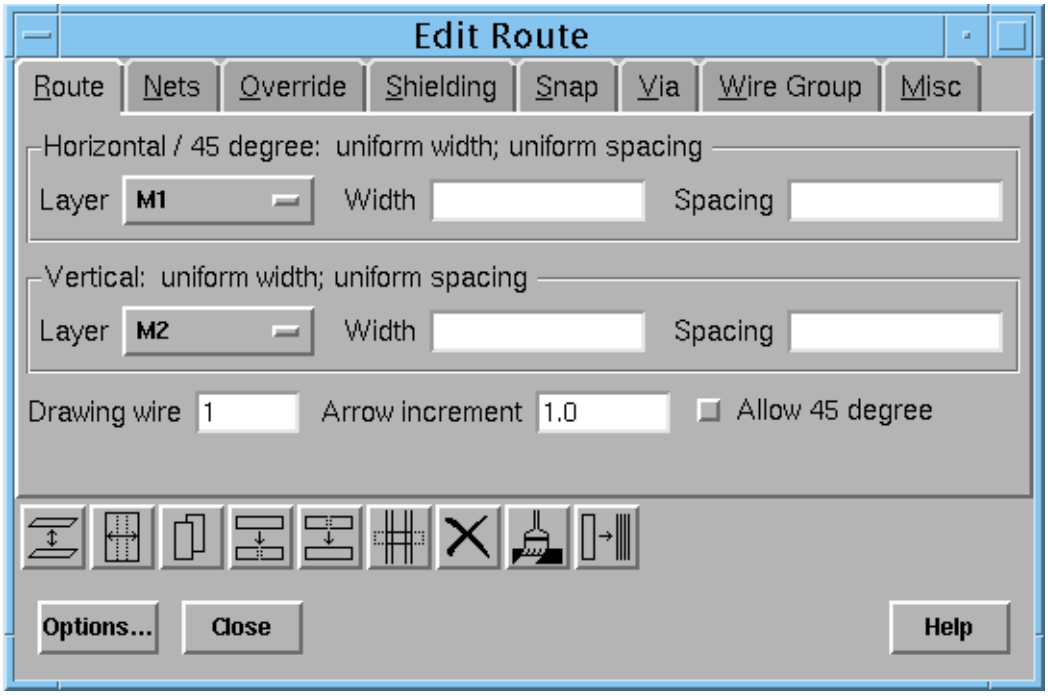
Note: The main Encounter window also has a set of widgets you can use for wire editing. For information, see “Wire Editing Widgets” on page 75.

Edit Route– Route

Use the *Route* page of the Edit Route form to specify the layers, width, and spacing of the wires to add or modify.

Use one of the following methods to open the Edit Route form:

- Choose *Edit – Wire Editor*, then click the *Route* tab.
- Use the e keyboard shortcut.



Edit Route – Route Fields and Options

Horizontal / 45 degree: uniform width; uniform spacing

Specifies uniform width and spacing, in microns, for 45-degree or horizontal wires. You can specify different values for each metal layer.

Vertical: uniform width; uniform spacing

Specifies uniform width and spacing, in microns, for vertical wires. You can specify different values for each metal layer.

The values for the width and spacing are used when you select *Force Special* on the *Nets* page. For more information, see "Force Special (to allow arbitrary widths)" on page 414.

Drawing wire

Specifies the position of the net listed on the *Nets* page that corresponds to the mouse pointer location when you add an array of wires. This net is also used as the reference net when changing direction. All other nets around this net are lengthened or shortened accordingly.

When you change directions, the value of the *Drawing wire* changes—so that the wire that corresponds to the mouse pointer location remains unchanged.

- For horizontal wires, a value of `1` indicates the bottom-most net.
- For vertical wires, a value of `1` indicates the left-most net.

Arrow increment

Specifies the step increments, in microns, to move wires. *Default:* `1.0`

You can move a selected wire incrementally by using the arrow keys. The wire moves the specified increment distance in the direction of the arrow. Wire movement is subject to snap constraints. For more information on wire snapping, see "Edit Route – Snap" on page 423.

Allow 45 degree

Lets you draw a 45-degree wire using the mouse. The wire direction is determined by the mouse position. This option has the following limitations:

- It can be used for special nets only.
- You can draw only one net at a time.
- It is limited to on-line design rule checking.

Related Text Commands

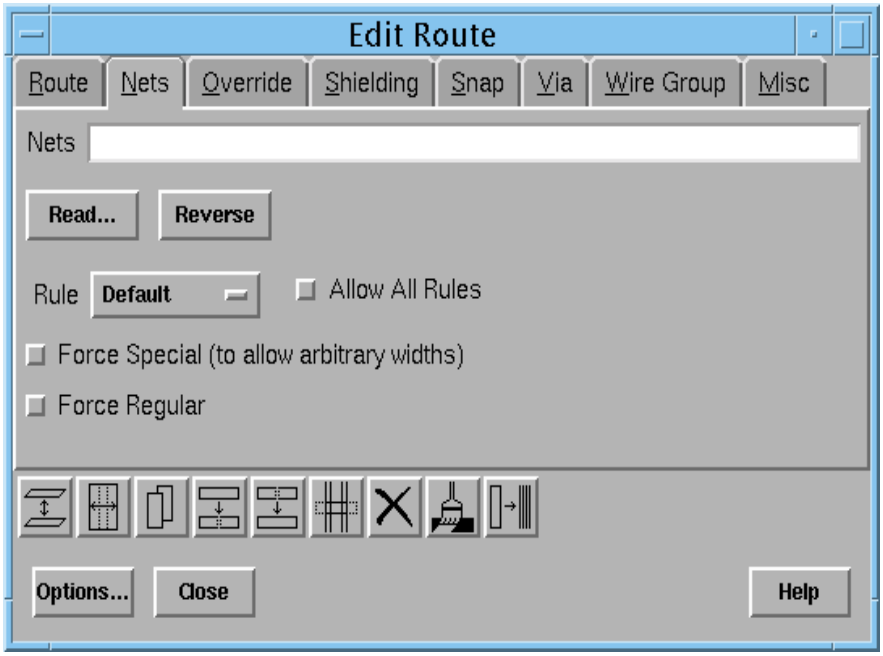
For information on the following commands, see "Wire Edit Commands" in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

Edit Route – Nets

Use the *Nets* page of the Edit Route form to specify the net names of the wires to edit. In addition, you can specify the way that LEF default and nondefault rules are applied.

➤ Choose *Edit – Wire Editor*, then click the *Nets* tab.



Edit Route – Nets Fields and Options

Nets

Specifies the nets to edit. The order of the net names determines the drawing arrangement of the wires.

Use the following format to specify a bus:

`netName [x:y]`

For example, to draw eight wires for a bus, type the following:

`-nets netName[7:0]`

This is equivalent to specifying `netName[7], netName[6], ... netName[0]`. Specifying `-nets netName[0:7]` reverses the order.

- For horizontally drawn wires, the first net name entered is drawn as the top-most wire, followed by the next net name, and so on. The last-entered net name is drawn as the bottom-most wire.
- For vertically drawn wires, the first net name entered is drawn as the left-most wire, followed by the next net name, and so on. The last-entered net name is drawn as the right-most wire.

The *Drawing wire* option on the *Route* page determines which wire follows the mouse motion. This wire remains the same length when making a turn. Other wires are lengthened or shortened to accommodate the drawing wire. For more information, see "Edit Route– Route" on page 410.

Tip

When auto query is enabled, you can use the `s` keyboard shortcut to populate the *Nets* field with the net name of the selected wire. For more information, see "Auto Query" on page 101.

Read

Loads a file that contains a list of net names. In the file, each net name must be on a separate line. For more information, see "Select A File (for Net Names)" on page 415.

Reverse

Reverses the order of the names displayed in the *Nets* field. For example, if the *Nets* field contains the net names `VDD1 VSS1 VDD2 VSS2` and you click *Reverse*, the order of the net names changes to `VSS2 VDD2 VSS1 VDD1`.

Rule

Specifies the rule for assigning the width, minimum allowed spacing, and extension if you are adding regular (signal) wires. The added wire segments use the width and extension defined in LEF file for that rule.

The specified rule applies only when you add signal wires with the *Force Special* option deselected or when you add power or ground wires with the *Force Regular* option selected.

Allow All Rules

Specifies that any rule can be used. That is, if a net does not have a nondefault rule attached to it, its wires and vias can be created with any LEF rule when this option is selected.

If a net has a nondefault rule attached to it, its wires and vias can only be created with that nondefault rule or with the default rule when this option is not selected.

Force Special (to allow arbitrary widths)

Lets you specify any width for signal wires using the *Width* field on the *Route* tab.

Note: *Force Special* and *Force Regular* options cannot be selected at the same time, but they can both be deselected at the same time.

Force Regular

Creates regular wires and vias, even if special (power or ground) nets are specified.

Note: *Force Special* and *Force Regular* options cannot be selected at the same time, but they can both be deselected at the same time.

Related Text Commands

For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

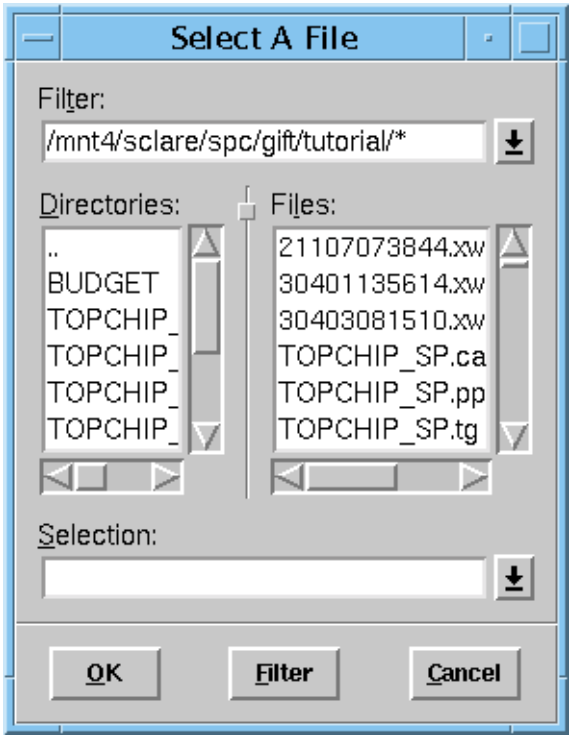
Select A File (for Net Names)

Use the Select A File form to load a net name file in the *Nets* field of the *Edit Route – Nets* page. The net name file can contain only one net name per line. Net names for a bus must be listed as individual net names.

The following example shows the contents of a file with a list of net names:

```
VDD1
VSS1
VDD2
VSS2
```

➤ Choose *Edit – Wire Editor*, then click the *Read* button on the *Nets* page of the Edit Route form.



Select A File (for Net Names) Fields and Options

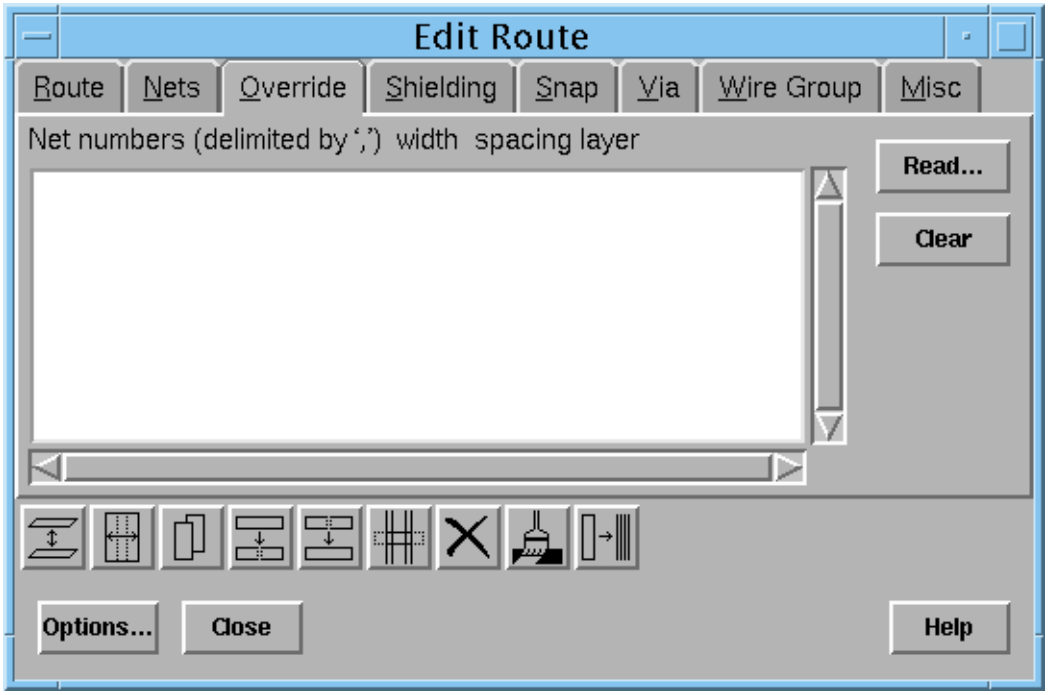
Filter	Specifies the filter for selecting the directory to use.
Directories	Displays the list of directories.
Files	Displays the list of files in the selected directory.

Selection	Displays the selected file.

Edit Route – Override

Use the *Override* page of the Edit Route form to specify different values for the width and spacing of specified wires.

➤ Choose *Edit – Wire Editor*, then click the *Override* tab.



Edit Route – Override Fields and Options

Net numbers

Specifies the override width and space values. Enter values in this text entry field manually or populate it with values from a file. If you enter values manually, use the same format you used for creating a file. For more information, see "Select A File (for Override Values)" on page 419.

Important

An entry highlighted in red has a syntax error and will be ignored.

Read

Opens the Select A File form, which you can use to load a file with override values. For more information, see "Select A File (for Override Values)" on page 419.

Clear	Removes all entries from the *Override* page.

Related Text Commands

For information on the following commands, see “Wire Editing Commands” in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

Select A File (for Override Values)

Use the Select A File form to load a file with override values into the *Edit Route – Override* page.

Use the following format for entering values into the text box:

```
Net#,Net# Width Spacing
```

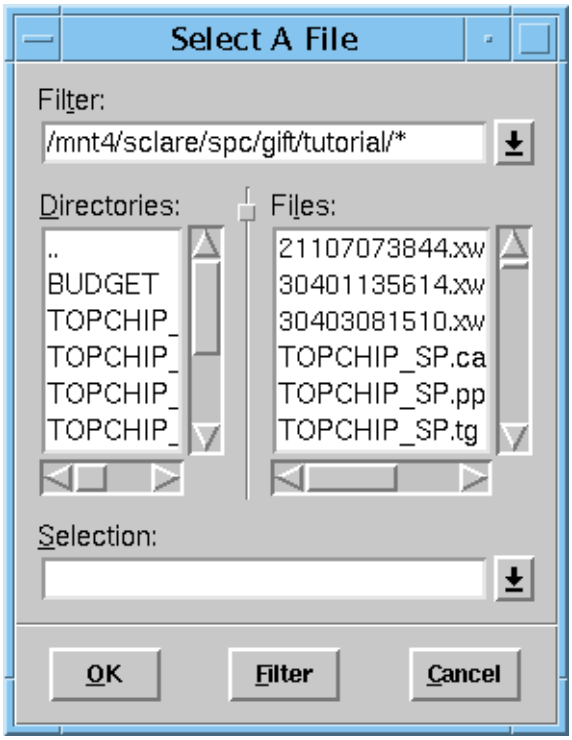
where `Net#` is the position of the net name in the *Nets* field of the *Nets* page.

The following example shows the contents of an override file in which four nets are specified on the *Nets* page:

```
1,2 20 30
4 10 30
```

In the example, nets `1` and `2` have override values of `20` for width and `30` for spacing, and net `4` has an override value of `10` for width and `30` for spacing. Net `3` has the width and spacing specified on the *Route* page.

➤ Choose *Edit – Wire Editor*, click the *Override* tab, then click the *Read* button on the *Override* page of the Edit Route form.



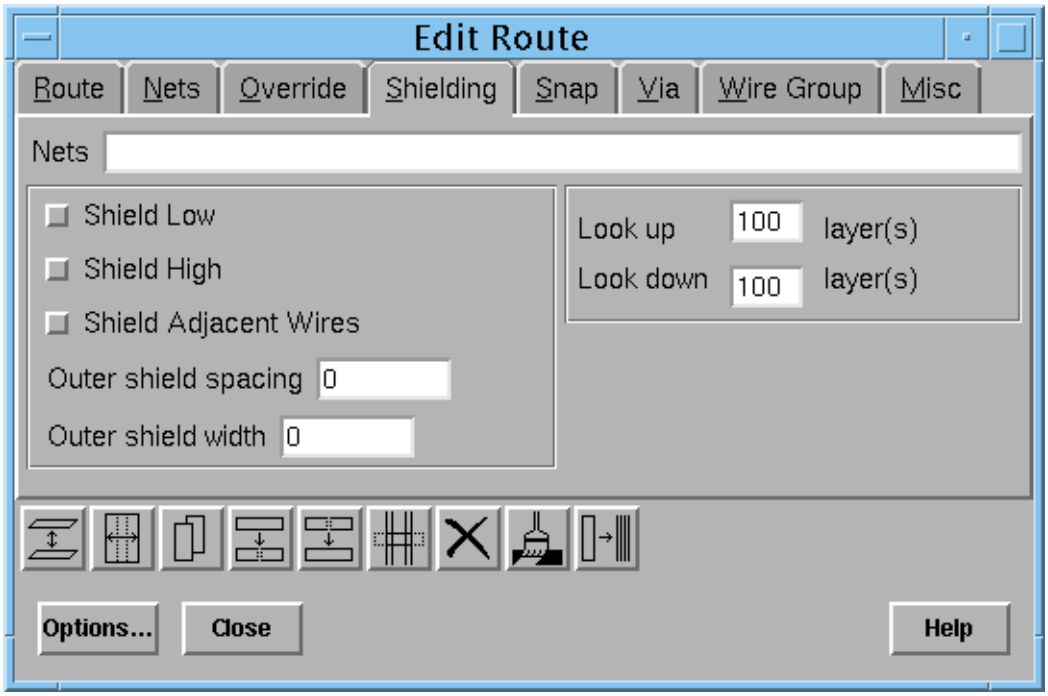
Select A File (for Override Values) Fields and Options

Filter	Specifies the filter for selecting the directory you want to use.
Directories	Displays the list of directories.
Files	Displays the files in the selected directory.
Selection	Displays the selected file.

Edit Route – Shielding

Use the *Shielding* page of the Edit Route form to specify that added wires should be shielded by other wires that are added at the same time.

➤ Choose *Edit – Wire Editor*, then click the *Shielding* tab.



Edit Route – Shielding Fields and Options

Nets	Specifies the nets for the shield wires, usually power or ground names. Separate multiple net names with spaces.
Shield Low	Adds a minimum-width shield wire at the bottom (Low) side of horizontal routes or at the left side of vertical routes. The spacing of the added shield wire is determined by the design rules in the technology file.
Shield High	Adds a minimum-width shield wire at the top (High) side of horizontal routes or at the right side of vertical routes. The spacing of the shield wire is determined by the design rules in the technology file.

Shield Adjacent Wires	Adds minimum-width shield wires centered between two adjacent wires.
Outer shield spacing	Specifies the spacing, in microns, to the outer shield wires. Entering a value in this field is optional.
Outer shield width	Specifies the width, in microns, of the outer shield wires. Entering a value in this field is optional.
Look up ___ layer(s)	
	Specifies the number of layers above the current layer that an added shield wire connects to using a via. *Default:* `100` (all metal layers)
Look down ___ layer(s)	
	Specifies the number of layers below the current layer that an added shield wire connects to using a via. *Default:* `100` (all metal layers)

Related Text Commands

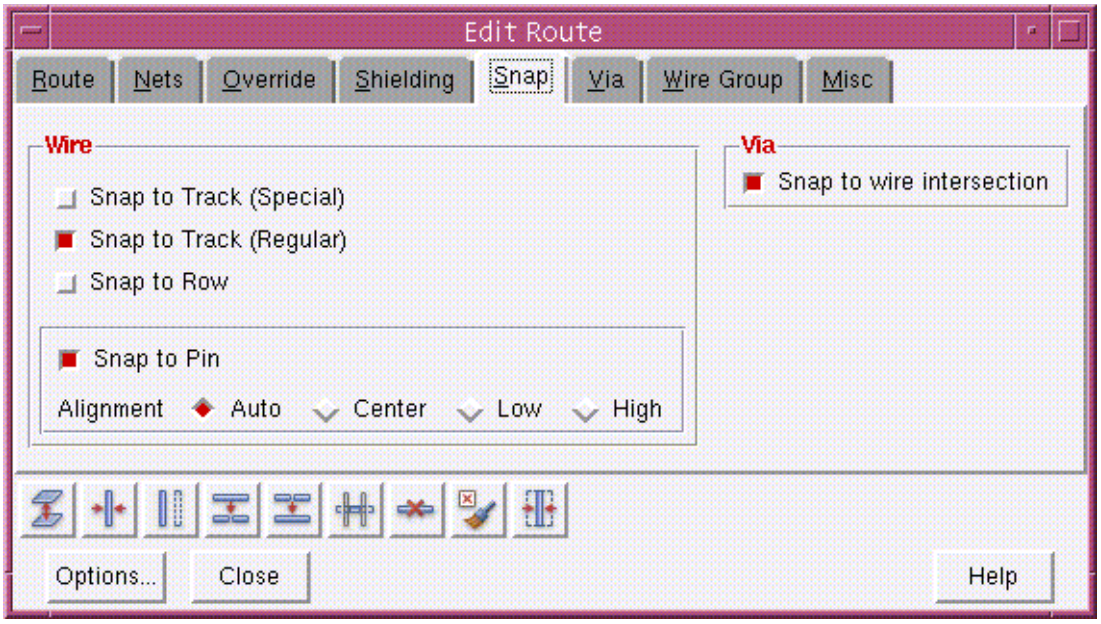
For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

Edit Route – Snap

Use the *Snap* page of the Edit Route form to specify how new or changed wires snap to pins or existing wires and whether they snap to a routing track.

➤ Choose *Edit – Wire Editor*, then click the *Snap* tab.



Edit Route – Snap Fields and Options

Snap to track (Special)

Automatically snaps added or moved special wires to the closest routing track in the preferred direction for the layer. By default, this option is not selected.

Snap to track (Regular)

Automatically snaps added or moved regular wires to the closest routing track in the preferred direction for the layer. By default, this option is not selected.

Snap to Row

Automatically snaps added or moved wires to the nearest standard cell row. Use this option to create followpins.

Note: *Snap to Track* has priority over *Snap to Row* if both are selected.

Snap to pin

Automatically snaps added wires to the pin. Select one of the following *Alignment* options to control the part of the pin to which the wire snaps:

Auto	Snaps the wire to the pin at a location on the pin that is determined by the software.
Center	Snaps the center of the wire to the center of the pin.
Low	Snaps the bottom edge of the wire to the bottom-most part of the pin for a horizontal wire, or the left edge of the wire to the left edge of the pin for a vertical wire.
High	Snaps the top edge of the wire to the top-most part of the pin for a horizontal wire, or the right edge of the wire to the right edge of the pin for a vertical wire.

Snap to wire intersection

Enables or disables the snapping of vias to wire intersection.

Default: On

Related Text Commands

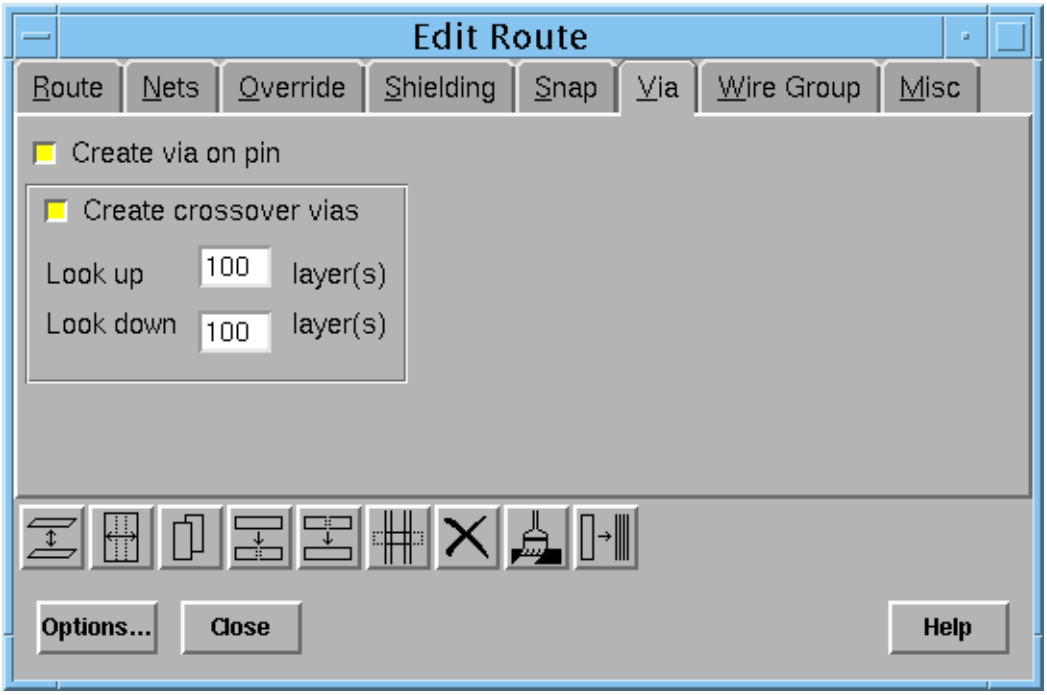
For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

Edit Route – Via

Use the *Via* page of the Edit Route form to control whether vias are created when an added wire crosses a same-net wire on a different layer.

➤ Choose *Edit – Wire Editor*, then click the *Via* tab.



Edit Route – Snap Fields and Options

Create via on pin	Creates vias at pins. You might need to deselect this option for bump pins that are not square-shaped. By default, this option is selected.
Create crossover vias	

Creates a via when you draw a wire that crosses a wire or pin of the same net that is on a different layer.

Note: Vias are not created if the minimum or maximum layer constraints prevent the creation of a via.

If you deselect this option, the tool does not create vias at crossovers. For example, if you draw a wire from left to right, the tool begins creating a via at the left edge of the vertical target. This via is removed as soon as the drawing wire moves past the right edge of the vertical target.

Note: If you draw a wire between two pins, the tool creates vias on the pins as needed, regardless of whether this option is selected or deselected.

Look up ___ layer(s)

Specifies the number of layers above the current layer that an added wire connects to using a via.
Default: `100` (all metal layers)

Look down ___ layer(s)

Specifies the number of layers below the current layer that an added wire connects to using a via.
Default: `100` (all metal layers)

Related Text Commands

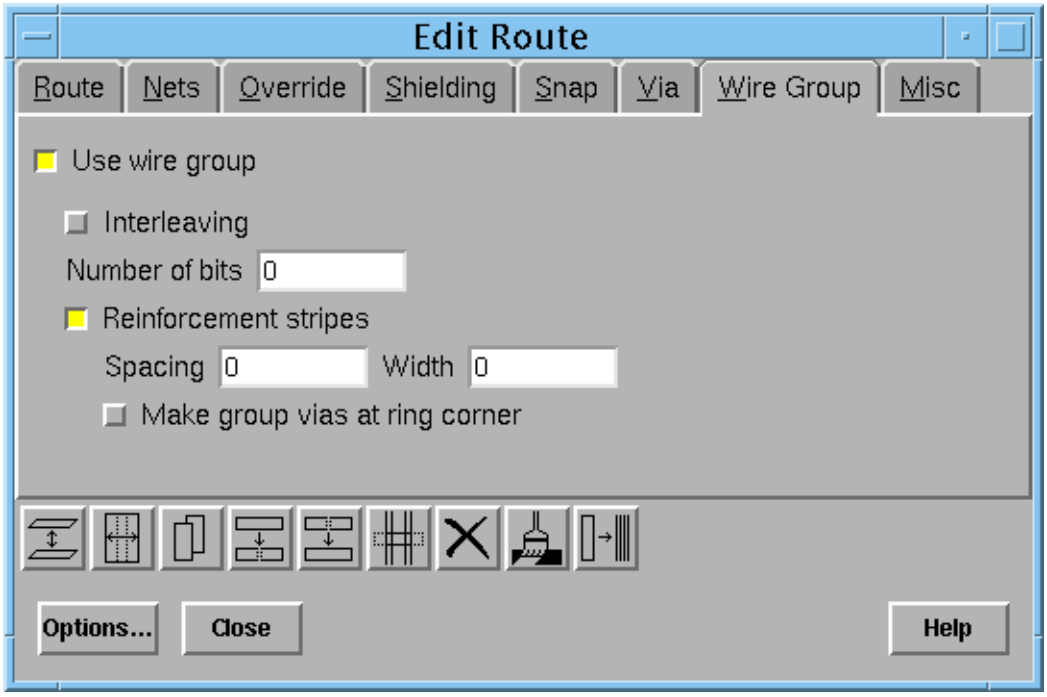
For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- `editAddRoute`
- `setEdit`

Edit Route – Wire Group

Use the *Wire Group* page of the Edit Route form to group multiple wires from the same net. Use wire groups to decrease resistance and provide stronger connections.

➤ Choose *Edit – Wire Editor*, then click the *Wire Group* tab.



Note: By default, *Use wire group* and *Reinforcement stripes* are not selected. They are selected in the above figure to make the text in the form easier to read.

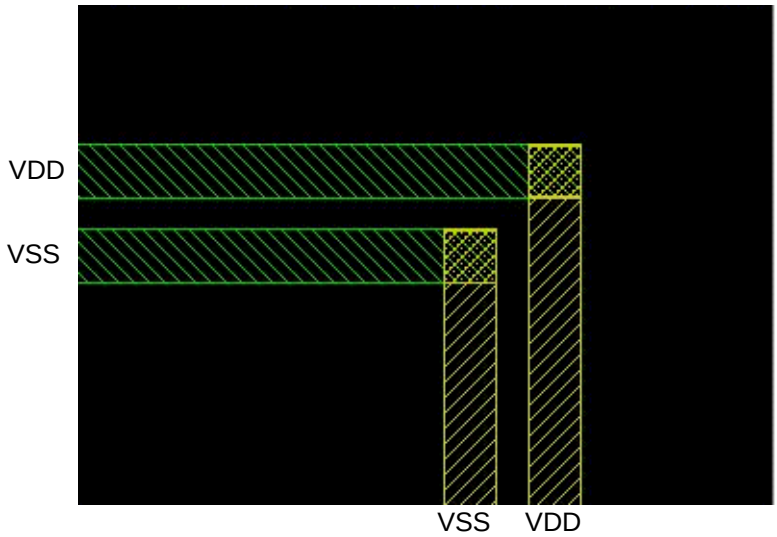
Edit Route – Wire Group Fields and Options

Use wire group

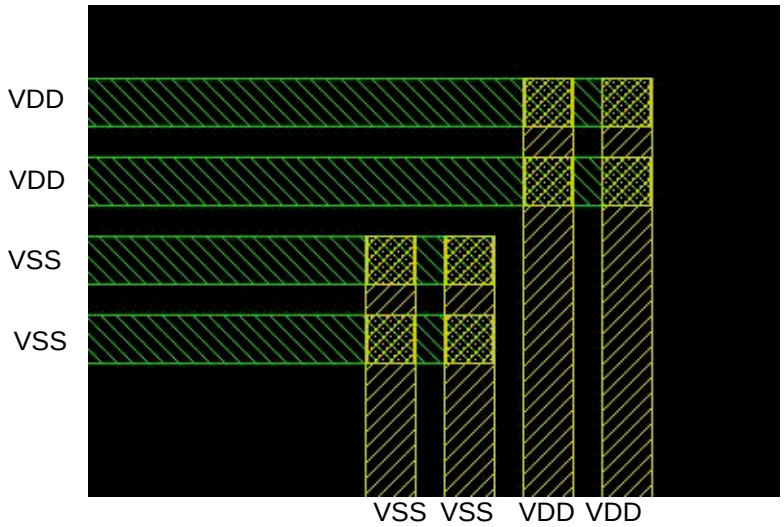
Groups multiple wires from the same net.
Default: Off

> **Note:** You must select *Use wire group* and specify 2 or more for *Number of bits* to enable wire groups.

The following figure shows a power and ground wire that do not form a wire group.



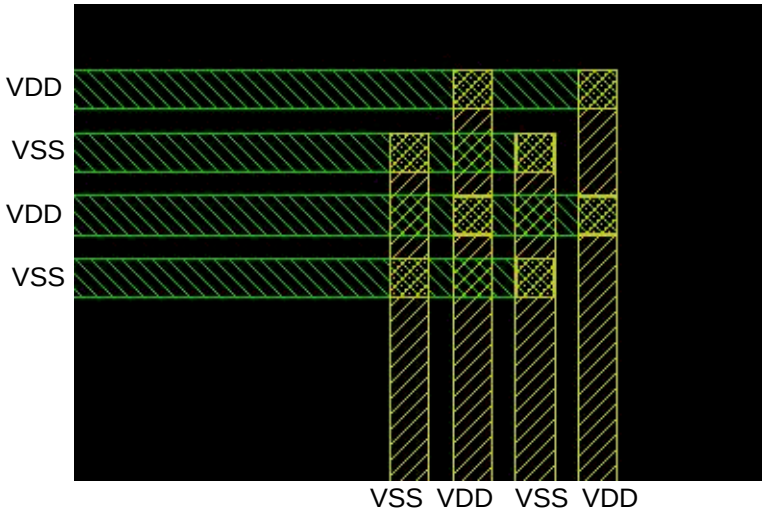
The following figure shows power and ground wires that form a wire group.



Interleaving

Alternates the specified wires in the wire group. For example, if you specify VDD and VSS on the *Nets* page and select this option, the software alternates the power and ground wires in the wire group.
Default: Off

When *Interleaving* is specified, the Encounter software draws a wire group like the following:



Note: Do not select both *Interleaving* and *Reinforcement Stripes*—doing so creates shorts in the wire groups.

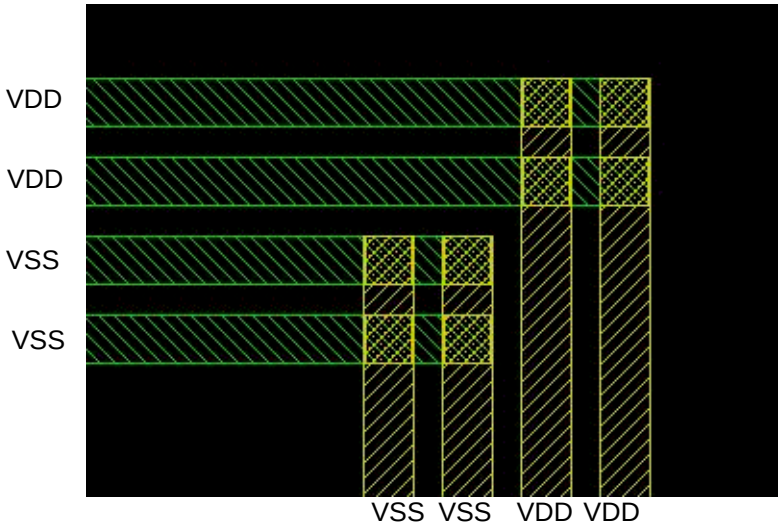
Number of bits

Specifies the number of times to replicate a wire in the wire group. For example, if you specify VSS and VDD on the *Nets* page, and specify 2 for this option, the software creates a wire group with two power wires and two ground wires.
Default: 0 (disabled)

Important

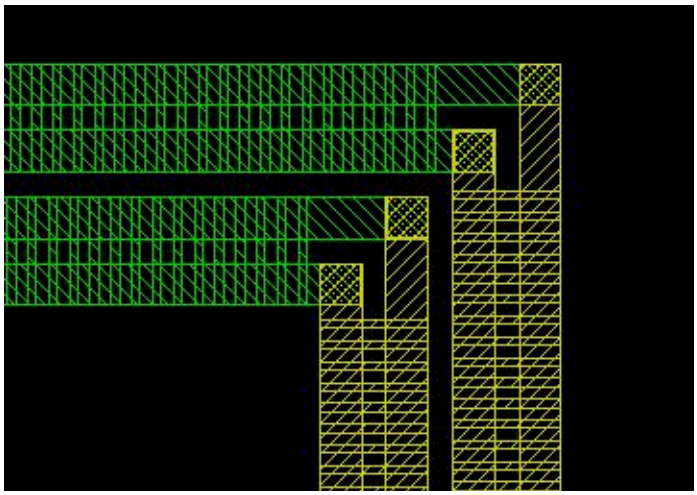
The value of this option must be greater than 1 to enable wire groups.

When *Number of bits* 2 is specified, the Encounter software draws a wire group like the following:



Reinforcement stripes Creates slots in the wire group by creating wires that connect the wires in the wire group, but are orthogonal to them. Slots help to reduce resistance in power networks.
Default: Off

When *Reinforcement stripes* is specified, the Encounter software draws a wire group like the following:



Note: Do not select both *Reinforcement stripes* and *Interleaving*—doing so creates shorts in the wire groups.

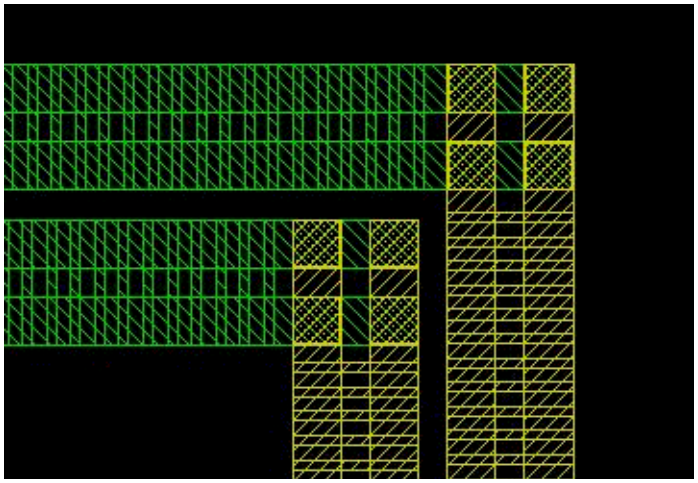
Spacing Specifies the spacing for the reinforcement stripes.

Width Specifies the width of the reinforcement stripes.

Make group vias at ring corner

Specifies that the wire group uses group vias. Group vias are connected vias in a wire group. Using group vias ensures that the contact is maintained if one of the vias in the wire group produces a void.
Default: Off

In the following figure, the wire group has group vias:



Note: The figures that follow *Interleaving* and *Reinforcement stripes* show wire groups that do not have group vias.

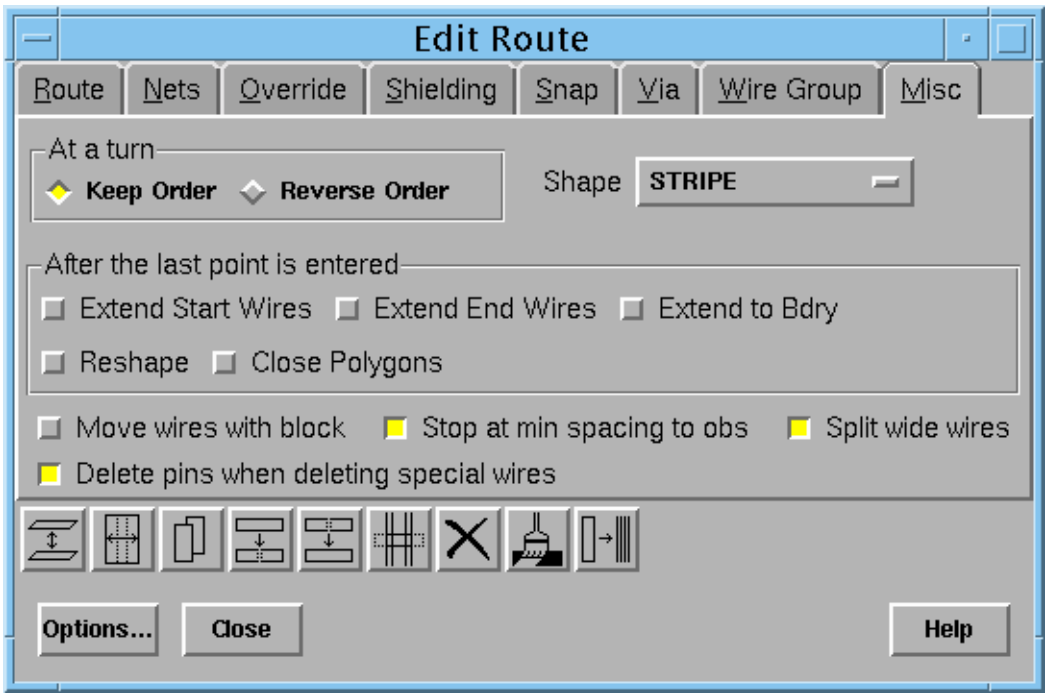
Related Text Commands

- `setEdit`

Edit Route – Miscellaneous

Use the *Misc* page of the Edit Route form to specify the shape and behavior of wires that are added or modified.

➤ Choose *Edit – Wire Editor*, then click the *Misc* tab.



Edit Route – Miscellaneous Fields and Options

At a turn

Specifies whether the order of the wires changes when the wire makes a 90-degree turn. Select one of the following options:

Keep Order

Follows the placement order of the net names specified in the *Nets* field of the *Nets* page. This is the default.

Reverse Order

Reverses the placement order of the net names specified in the *Nets* field of the *Nets* page.

Shape

Select one of the following shapes for each wire created in Add Wire mode:

- *None*
- *RING*
- *STRIPE*
- *FOLLOWPIN*
- *IOWIRE*
- *COREWIRE*
- *BLOCKWIRE*
- *FILLWIRE*
- *FILLWIREOPC*
- *PADRING*
- *BLOCKRING*
- *DRCFILL*

After the last point is entered

Specifies the behavior of the wires when the route is completed. Select any of the following options:

Extend Start Wires

After completing a special route, the start of the route segment extends and connects to wires on the same net. If there is no such wire to extend to, then the startpoint is not changed.

Extend End Wires

After completing a special route, the end of the route segment extends and connects to wires on the same net. If there is no such wire to extend to, then the endpoint is not changed.

Extend to Bdry Requires selection of *Extend Start Wires*, *Extend End Wires*, or both. After completing a special route, the start or the end of the segment always extends to the cell boundary. Via connections are made to the extended route at places where there are wires on the same nets. In addition, pins are created at the boundary.

Reshape Automatically trims redundant wires when new wires are added.

Close Polygons Closes a special route structure toward itself. For the closing to complete, the ending route segments must be drawn toward (but do not need to touch) the starting route segments.

Move wires with block Moves wires that are connected to a block when the block moves. By default, this option is not selected.

Stop at min spacing to obs

Checks DRC rules and stops moving or stretching wires before causing a violation. To ignore DRC rules when moving or stretching wires, deselect this option.
By default, this option is selected.

Note: If you select this option, you cannot move a wire to the desired destination if that wire passes through a location where a DRC violation occurs. Deselect this option to permit the wire to pass through to the desired location.

Split wide wires Splits wires automatically when the width of a wire exceeds the maximum width specified in the LEF file.
By default, this option is selected.

Delete pins when deleting special wires

Removes pins when deleting special wires. To keep pins, deselect this option.
By default, this option is selected.

Related Text Commands

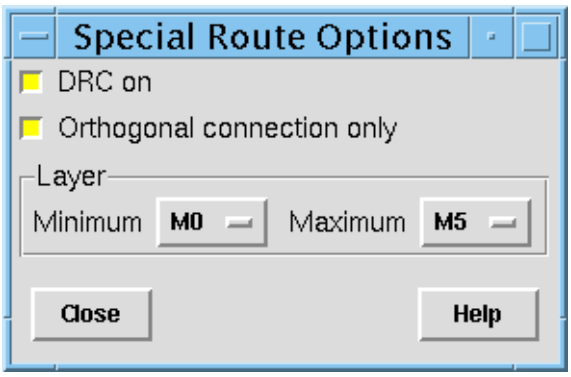
For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- editAddRoute
- setEdit

Special Route Options

Use the Special Route Options form to specify design-rule checks and to control the stacking depth of vias or the layers used in special routing.

➤ Choose *Edit – Wire Editor*, then click the *Options* button.



Special Route Options Fields and Options

DRC on

Performs design-rule checking while routing. If a check does not pass, a DRC marker appears on the screen.
By default, this option is selected.

Orthogonal connection only

Does not consider wires and pins that are in the same direction as a target for connection when creating vias. For example, if you extend a wire to the left, any horizontal wire it meets is not considered a target. However, a vertical wire is considered a target.

Layer

Specifies the layer range for added or moved wires and vias. Choose a layer from each of the following pull-down menus:

Minimum — The bottom-most layer on which to create or move wires and vias.

Maximum — The top-most layer on which to create or move wires and vias.

Related Text Commands

For information on the following text command, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

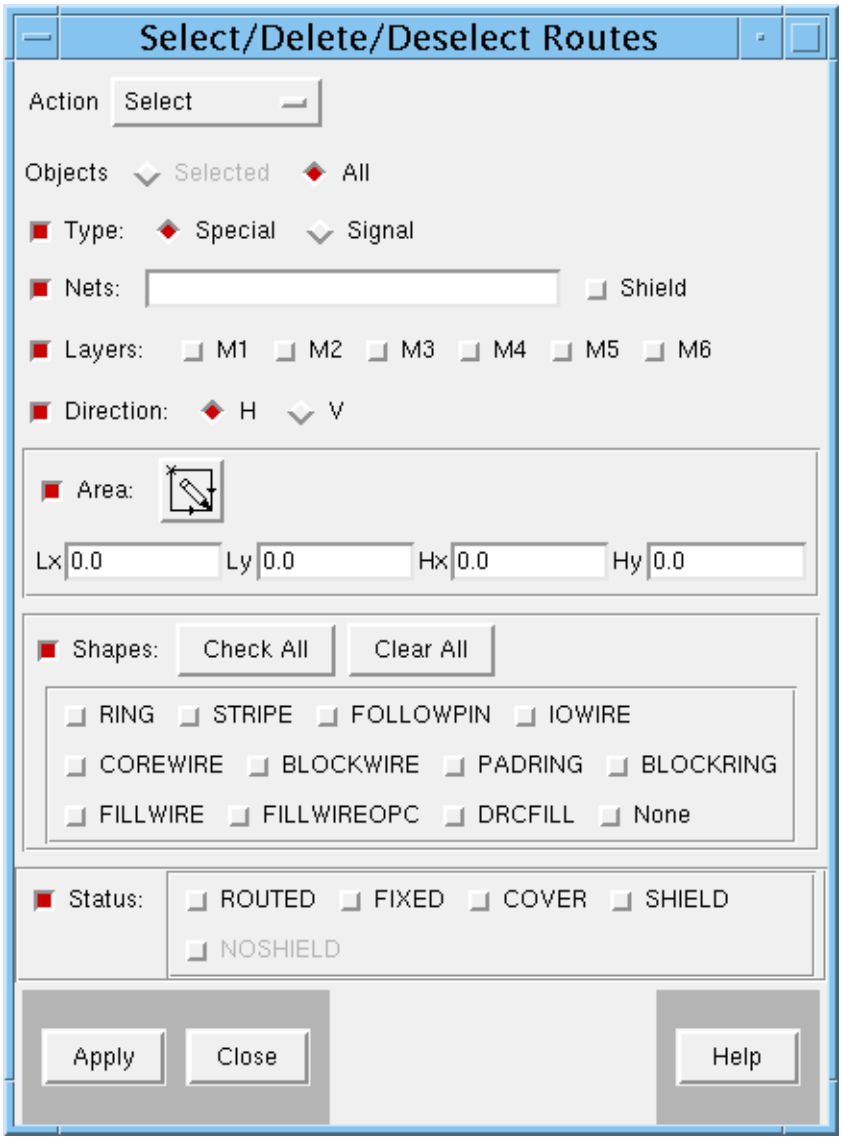
- `setSpecialRouteOption`

Select/Delete/Deselect Routes

Use the Select/Delete/Deselect Routes form to select, delete, or deselect wires.

Use one of the following methods to open the Select/Delete/Deselect Routes form:

- Choose *Edit – Wire Editor*, then click the *Delete Wires* (*X*) widget at the bottom of the Edit Route form.
- Use the d keyboard shortcut.



Select/Delete/Deselect Routes Fields and Options

Action

Specifies whether to select, deselect, or delete wires when you click the *Apply* button. Select one of the following options from the pulldown menu:

Select — Selects wires with attributes selected with other options on this form when you click the *Apply* button. This is the default.

Deselect — Deselects wires with attributes selected with other option on this form when you click the *Apply* button.

Delete — Deletes wires with attributes selected with other options on this form when you click the *Apply* button.

Objects

Specifies whether to delete all objects or selected objects. This option is available only for the *Delete* action.
Default: Selected

Type

- If selected, you must specify the type of wire to be selected, deselected, or deleted.
- If deselected, both wire types can be selected, deselected, or deleted. This is the default.

Select one of the following:

Special — Selects or deletes only special (power or ground) wires.

Signal — Selects or deletes only regular (signal) wires.

Nets

If selected, objects are selected, deselected, or deleted from only the nets specified in the text entry field. You can use wildcard values in this field. For example, if you specify `V*`, wires can be selected, deselected, or deleted from nets `VDD` and `VSS`. If deselected, objects can be selected, deselected, or deleted from any net.

Tip

When auto query is enabled, you can use the `s` keyboard shortcut to populate this field with the net names of the selected objects.

Shield Selects, deselects, or deletes the shield wire associated with the specified net.

Layers Selects, deselects, or deletes objects from the specified layers only. By default, objects are selected, deselected, or deleted from all layers.

Direction Selects, deselects, or deletes objects with specified orientation only. By default, this option is selected.

- *H* Only horizontal objects can be selected, deselected, or deleted
- *V* Specifies that only vertical objects can be selected, deselected, or deleted

Area Specifies the area in which to perform the action. Use the area button or specify the coordinates in the text boxes.

Shapes Enables you to specify the shapes to select, deselect, or delete. If not selected, you can select, deselect, or delete all shapes.

For shape definitions, see Shapes, in the “DEF Syntax” chapter of the *LEF/DEF Language Reference*.

- *Check All* Makes all shapes on the list available to select, deselect, or delete.
- *Clear All* Makes all shapes on the list unavailable to select, deselect, or delete.

Status Enables you to specify the status of the object to select, deselect, or delete. Select one or more of the following: *ROUTED*, *FIXED*, *COVER*, *SHIELD*, *NOSHIELD*.

Note: If you select *Type Special* and *Status NOSHIELD* or *Type Signal* and *Status SHIELD*, the software generates an error message.

Related Text Commands

For information on the following commands, see “Wire Edit Commands” in the *Encounter Text Command Reference*.

- `editDelete`
- `editDeselect`
- `editSelect`

Edit Via

Use add via mode to add and modify vias. Use one of the following methods to place the software in add via mode:

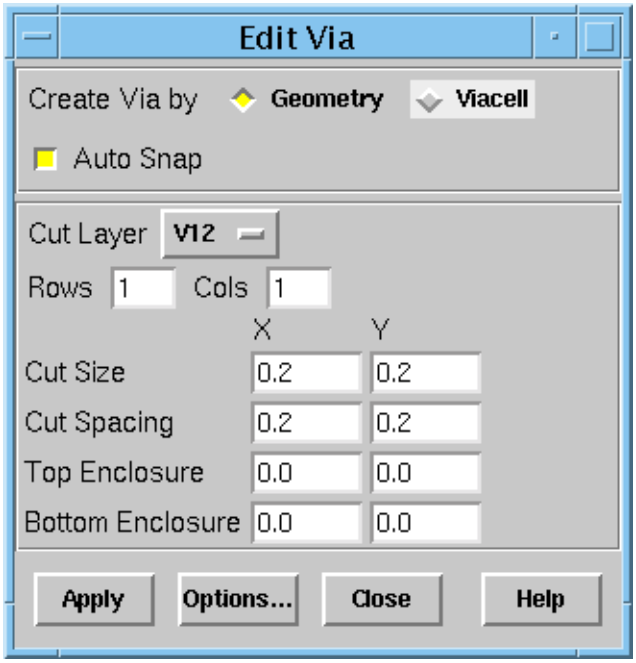
- Click the *Add Via* widget on the Tools list.
- Use the o keyboard shortcut.

The Edit Via form has two versions, depending on which via creation option you select:

- "Edit Via – Geometry" on page 442
- "Edit Via – Viacell" on page 446

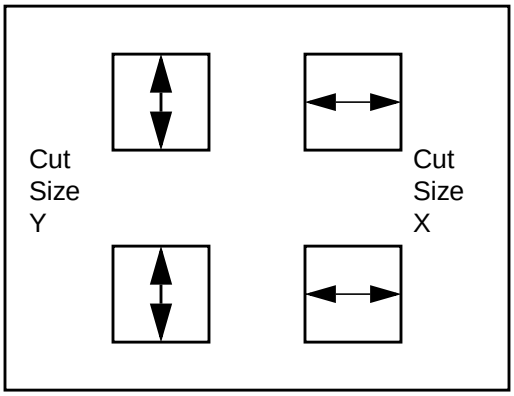
Edit Via – Geometry

➤ Click the *Add Via* widget, then press the F3 key.



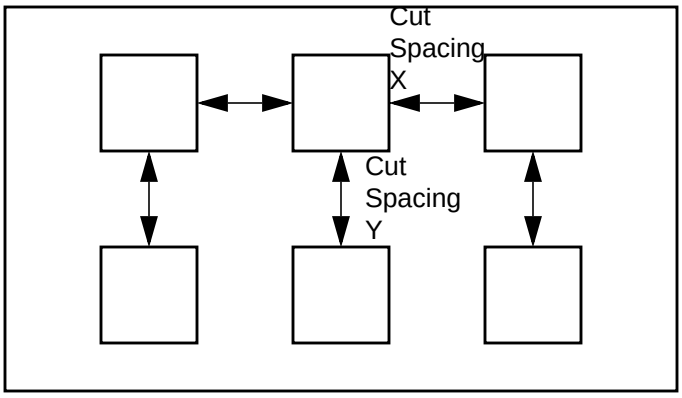
Edit Via – Geometry Fields and Options

Auto Snap	Snaps vias to the center of the intersection of wires on the same net. This is the default. If deselected, the via stays in the location where it is added or moved, snapping only to the manufacturing grid.
Cut Layer	Specifies the layer for the via. Choose a cut layer name from the pull-down menu.
Rows	Specifies the number of horizontal cuts for the via.
Cols	Specifies the number of vertical cuts for the via.
Cut Size	Specifies the length and width, in microns, for each via cut. The following figure shows *Cut Size X* and *Y* for a via with two rows and two columns.



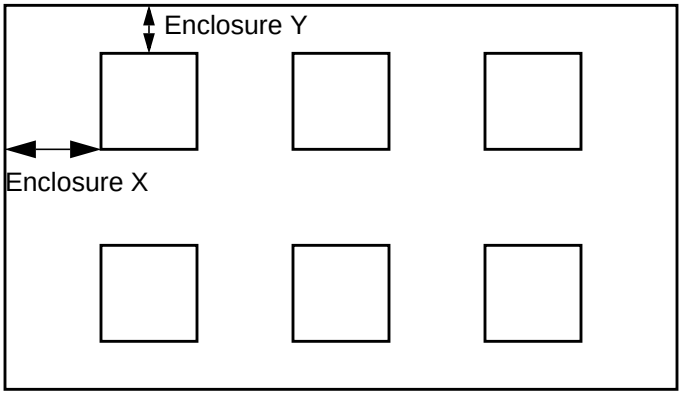
Cut Spacing

Specifies the length and width, in microns, of the spacing between each cut. The following illustration shows the *Cut Spacing X* and *Y* for a via with two rows and three columns.



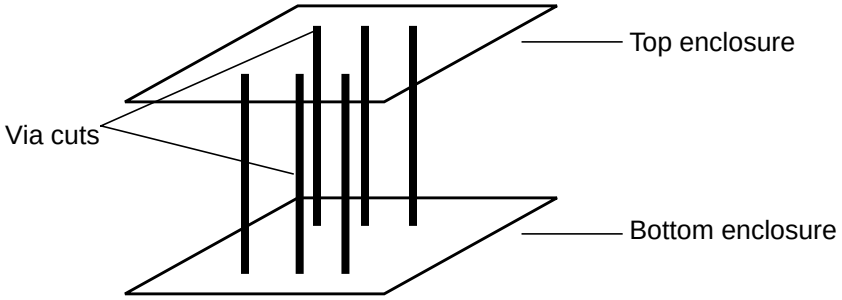
Top Enclosure

Specifies the length and width, in microns, of the metal overhang for the layer at the top of the via. The following figure shows the *Top Enclosure* and *Bottom Enclosure* for a via with two rows and three columns.



Bottom Enclosure

The length and width, in microns, of the metal overhang for the layer at the bottom of the via. The following figure shows a three-dimensional view of the *Top Enclosure* and *Bottom Enclosure* layers.



Origin

Specifies the X and Y offset for all the via shapes. For more information, see "Via" in the *LEF/DEF Language Reference*.

Related Topics

For information on the following topics, see "Wire Editing" in the *Encounter Text Command Reference*.

- Adding Vias

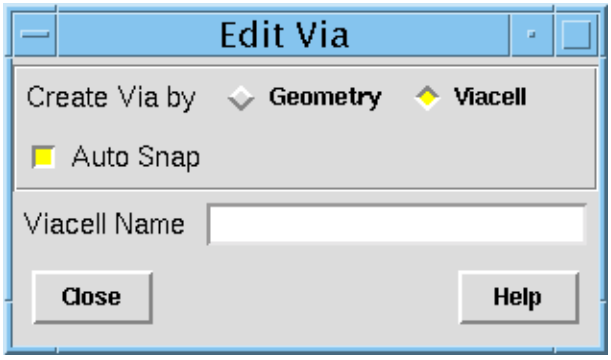
Related Text Commands

For information on the following commands, see "Wire Edit Commands" in the *Encounter Text Command Reference*.

- `editAddVia`
- `editChangeVia`
- `editDeselectVia`
- `editSelectVia`
- `setViaEdit`

Edit Via – Viacell

➤ Click the *Add Via* widget, then press the F3 key and select *Create Via by Viacell*.



Edit Via – Viacell Fields and Options

Auto Snap	Snaps vias to the center of the intersection of wires on the same net. This is the default. If deselected, the via stays in the location where it is added or moved and snaps to the manufacturing grid.
Viacell Name	Specifies the via cell from the LEF or DEF file.

Related Topics

- Adding Vias
- `setEditVia`
- `editAddVia`

Edit Route Widgets

The bottom of each page of the Edit Route form contains the following widgets. Select the wires to edit before clicking a widget or pressing the equivalent keyboard shortcut.

Change wire layer
Equivalent keyboard shortcut: `L`
Select wires to change to the layer specified by the *Layer* button on the *Route* page and click this widget. Changes horizontal wires to the layer specified by the *Horizontal Layer* button and vertical wires to the layer specified by the *Vertical Layer* button.

Change wire width
Equivalent keyboard shortcut: `W`
Select special wires to have the width specified in the *Width* field on the *Route* page, and click this widget.

Duplicate wires
Equivalent keyboard shortcut: `c`
Select wires and click this widget to duplicate the wires on the layer specified by the *Layer* button on the *Route* page. Press the `Shift` key and click to select multiple wires. The duplicated wires are in the same location as the original. The duplicated wires are selected and the original wires are deselected, allowing you to move the duplicated wires without disturbing the original wires.

Split wires
Equivalent keyboard shortcut: `Control-s`
Select wires and click this widget to break the wires into segments. Wire splits occur at the intersections of wires on the same net. If you delete a section of the split wire so that the remaining wire is only partially connected to another wire, the remaining wire is automatically repaired so it extends to the appropriate edge of the wire it connects to.

Merge wires
Equivalent keyboard shortcut: `M`
Select wires and click this widget to join all wires of the same width, layer, and net that are collinear with and electrically connected to a selected wire. Does not merge signal wires that contain branches.

Trim wires
Equivalent keyboard shortcut: `T`
Select a wire and click this widget to remove any portion of the wire that extends beyond another wire or pin of the same net. Trims the selected wire back to the intersection with the other wire or pin.

Delete wires
Equivalent keyboard shortcut: d
Opens the Select/Delete Routes form. For more information, see "Select/Delete/ Deselect Routes" on page 439.

Note: To delete wires without opening the form, use the `D` keyboard shortcut.

Clear DRC markers
Equivalent keyboard shortcut: x
Click this widget to clear DRC markers from the design display area.

Split wires wider than maximum width
No equivalent keyboard shortcut.
Click this widget to check for wires that violate the `maxWidth` rule and split them (and the associated vias) as minimally as possible while maintaining the same footprint.

Object

The Object menu contains the following forms:

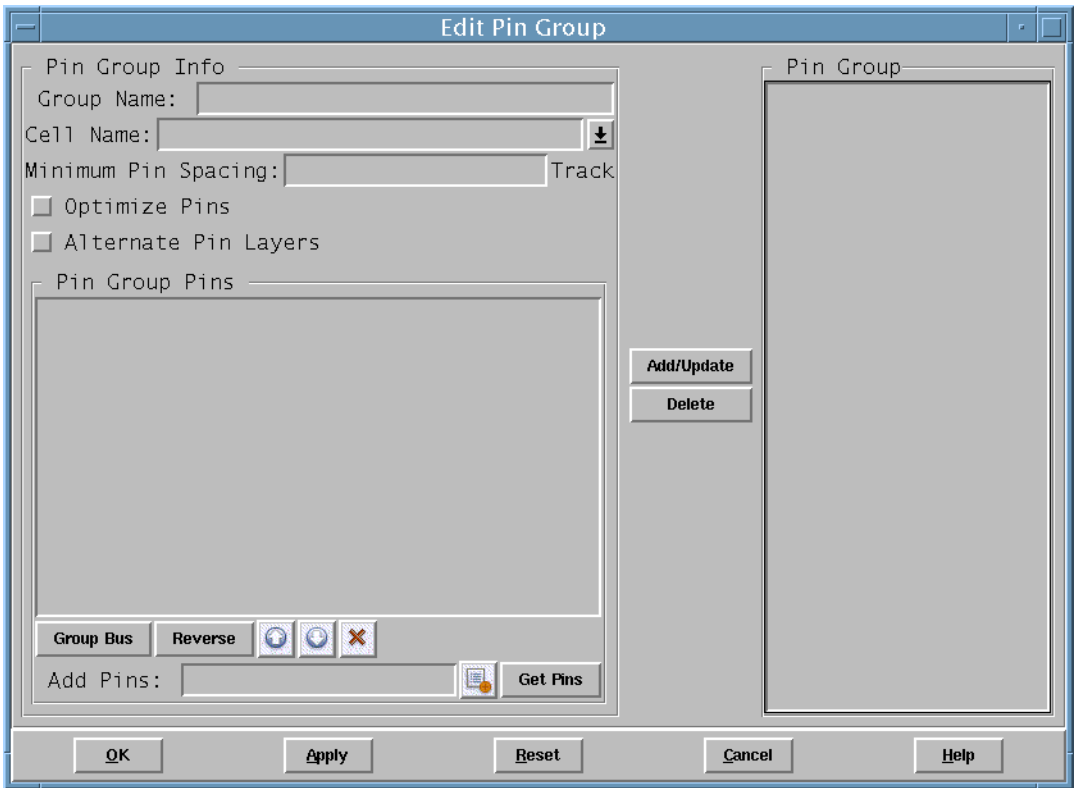
- Edit Pin Group
- Edit Net Group
- Create Non Default Rules

Edit Pin Group

Use the Edit Pin Group form to create a new pin group, add or delete pins to an existing pin group, delete all or specific pin groups, list all pins of the specified partition or block-level design, and change pin orders within a pin group.

You can use this form in conjunction with the Pin Editor.

➤ Choose *Edit – Object – Pin Group*.



Edit Pin Group Fields and Options

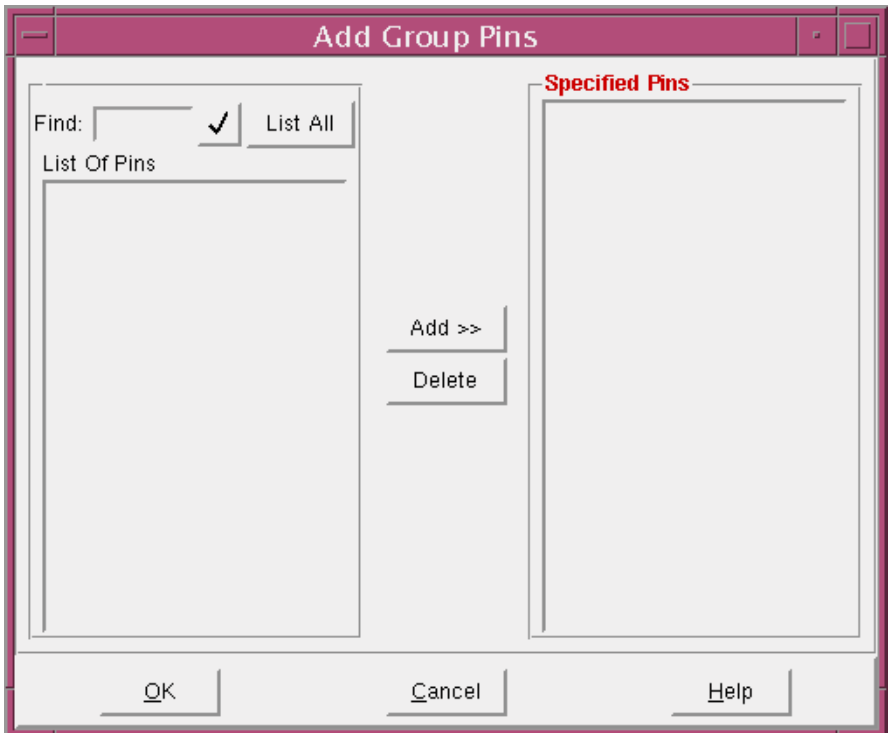
Group Name	Specify an existing or new pin group name in the field, specify a partition in the *Cell Name* field, and click the Add/Update button to add it to the *Pin Group* list.
Cell Name	Specify the partition name to associate with the pin group.
Minimum Pin Spacing	Specify the minimum spacing between the members of the net group.

Optimize Pins	Use this option to specify that pins in the group should be reordered to optimize wire length. *Default*: Off. The pin order is exactly as specified in the pin group.
Alternate Pin Layer	Use this option to specify that pins in the group should be assigned to alternate layers. *Default*: Off.
Pin Group Pins	Lists the pin names in the pin group. To add a pin to the list, use the *Add Pins* field. To delete pins, highlight them in the list and click the X button.
Group/Expand Bus	The Group Bus option specifies that all bus bits should be displayed as one bus in the *Pin Group Pins* list. The Expand Bus option specifies that all bus bits should be displayed individually in the *Pin Group Pins* list. Consider a bus named A that contains the bits A1, A2, A3, and A4. The *Group Bus* option displays them as one bus, bus A, in the Pin Group Pins list. The *Expand Bus* option displays them as individual bus bits A1, A2, A3, and A4, in the *Pin Group Pins* list.
Reverse	Reverses the order in which the pins are listed in the *Pin Group Pins* list.
Add Pins	Specify the name of the pin(s) and click the check button to include it in the *Pin Group Pins* list. You can use the wildcard (*) character to select a set. To select from a list of the available nets, click the Get Pins button.
Pin Group List	Displays all pin groups. Highlighting a group adds the name to the left side of the form where you can display and edit the group. To delete pin groups, highlight them in the list and click the Delete button.

Add Group Pins

Use the Add Group Pins form to add nets from a list of available pins.

➤ In the Edit Pin Group form, click the *Get Pins* button.



Add Group Pin Fields and Options

Find	Type the name of pin to find. You can specify wildcard (*) with pin names. To start the search, click the check icon next to the Find field or press Enter.
List All	Lists all available pins.
List of Pins	Displays the available pins.
Add	Adds the pins selected in the List of Pins window to the Specified Pins window. The pins listed in the Specified Pins window are added to the Edit Pin Group form when you click OK.
Delete	Deletes the pins selected in Specified Pins window.

Related Text Commands

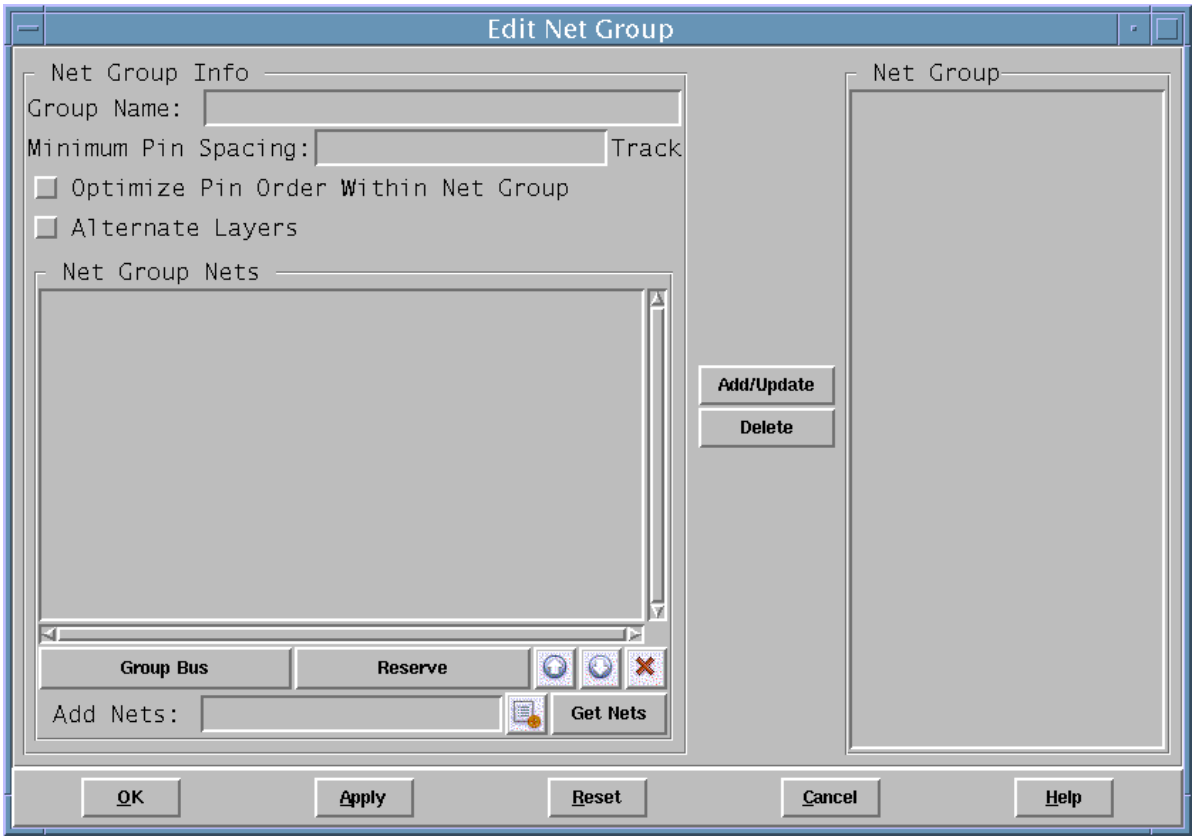
For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `addPinToCellPinGroup`
- `createCellPinGroup`
- `deleteAllCellPinGroups`

Edit Net Group

Use the Edit Net Group form to create a new net group, add or delete nets to an existing net group, delete all or specific net groups, select nets based on a list of all the nets that connect to a specified partition or block-level design, and change net orders within a net group.

➤ Choose *Edit – Editing – Net Group*.



Edit Net Group Fields and Options

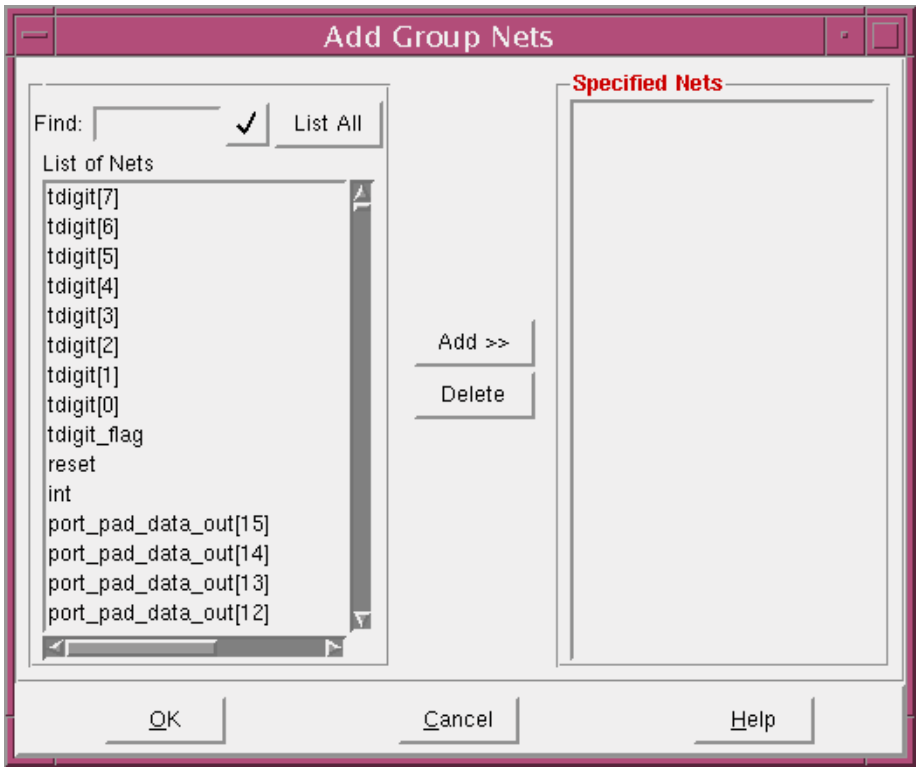
Group Name	Specify an existing or new net group name in the field and click the Add/Update button to add it to the *Net Group* list.
Minimum Pin Spacing	Specify the minimum spacing between the members of the net group.

Optimize Pin Order Within Net Group	Use this option to specify that pins in the group should be reordered to optimize wire length. *Default*: Off. The pin order is exactly as specified in the pin group.
Alternate Layers	Use this option to specify that pins in the group should be assigned to alternate layers. *Default*: Off.
Group/Expand Bus	The Group Bus option specifies that all bus bits should be displayed as one bus in the *Net Group Nets* list. The Expand Bus option specifies that all bus bits should be displayed individually in the *Net Group Nets* list. Consider a bus named A that contains the bits A1, A2, A3, and A4. The *Group Bus* option displays them as one bus, bus A, in the *Net Group Nets* list. The *Expand Bus* option displays them as individual bus bits A1, A2, A3, and A4, in the *Net Group Nets* list.
Reverse	Reverses the order in which the pins are listed in the *Net Group Pins* list.
Net Group Nets	Lists the net names in the net group. To add a net to the list, use the *Add Nets* field. To delete nets, highlight them in the list and click the X button.
Add Nets	Specify the name of the net(s) and click the Add Nets icon to include it in the *Net Group Nets* list. You can use the wildcard (*) character to select a set. To select from a list of the available nets, click the *Get Nets* button. For more information, see Add Group Nets on page 455.
Net Group	Displays all net groups. Highlighting a group adds the name to the left side of the form where you can display and edit the group. To delete net groups, highlight them in the list and click the Delete button.

Add Group Nets

Use the Add Group Nets form to add nets from a list of available nets.

➤ In the Edit Net Group form, click the *Get Nets* button.



Add Group Net Fields and Options

Find	Type the name of net to find. You can specify wildcard (*) with net names. To start the search, click the check icon next to the Find field or press Enter.
List All	Lists all available nets.
List of Nets	Displays the available nets.
Add	Adds the nets selected in the List of Nets window to the Specified Nets window. The nets listed in the Specified Nets window are added to the Edit Net Group form when you click OK.
Delete	Deletes the nets selected in Specified Nets window.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

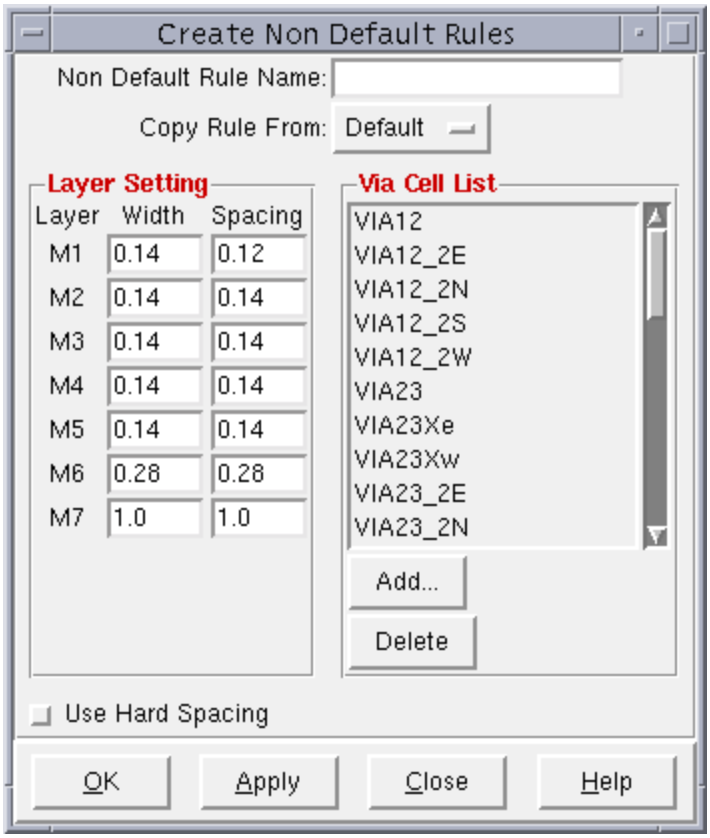
- `createNetGroup`
- `addNetToNetGroup`

Create Non Default Rules

Use the Create Non Default Rules form to define non-default rules for objects.

Note: You cannot create non-default rules for diagonal width, wire extension, via rule and minimum cuts.

➤ Choose *Edit – Object – Non Default Rules.*



Note: You cannot specify a non-default rule for creating a new via.

Fields and Options

Non Default Rule Name	Specifies the name of the non default rule.
Copy Rule From	Specifies the default rule that is copied from an existing LEF technology.
Layer	Displays the names of the metal layers.
Width	Specifies the width, in microns, of each metal layer.

Spacing	Specifies the spacing, in microns, between two metal layers.
Via Cell List	Displays the list of the via cells from the current editing rule.
Add	Opens the Add Via Cell form to add via cells in the *Via Cell List.* See Add Via Cell on page 460 for more information.
Use Hard Spacing	Specifies hard spacing between the metal layers.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

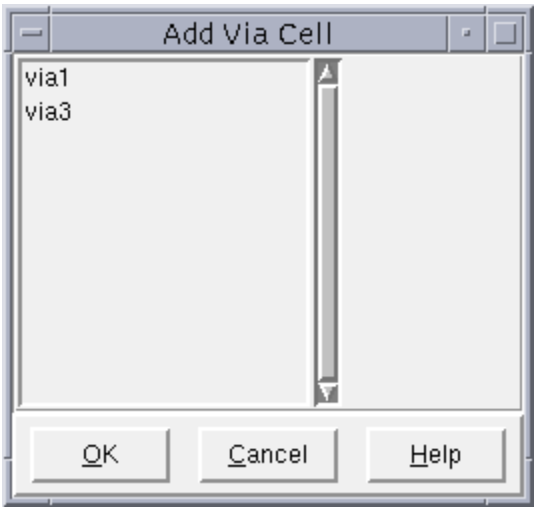
- `createNdr`
- `exportNdr`
- `initNdr`
- `modifyNdrViaList`
- `setNdrSpacing`
- `setNdrWidth`

Add Via Cell

Use the Add Via Cell form to add new vias to the current non-default rule that you are editing. The Add Via Cell form contains the list of LEF and DEF vias. To add a new via, select the via name in the Add Via Cell form.

You can add multiple vias, by clicking SHIFT + via name (contiguous selection) or CTRL + via name (non-contiguous selection). These vias are added to the via cell list.

Clicking the *Add* button in the Create Non Default Rules form opens the Add Via Cell form.



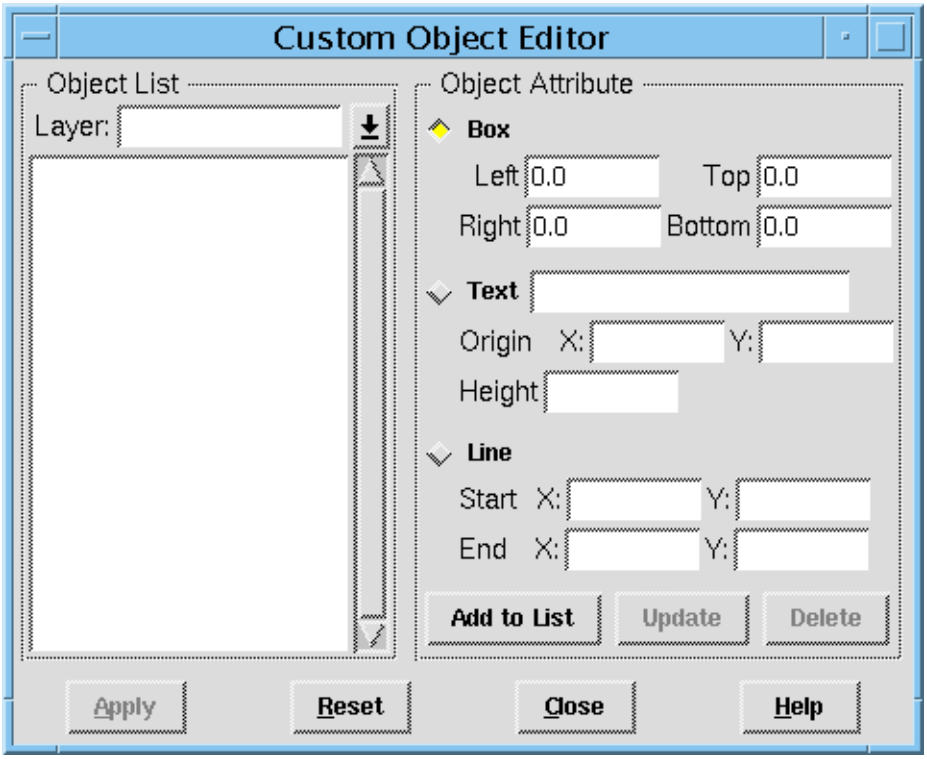
Add Via Cell Fields and Options

OK	Confirms adding the selected via cells to the Via Cell List.
Cancel	Cancels the changes made to the Add Via Cell form.

Custom Object Editor

Use the Custom Object Editor to add, update, and delete custom objects.

➤ Choose *Edit – Custom Object Editor*.



Custom Object Editor Fields and Options

Layer	Specifies a layer. You can use the pull-down menu to select an existing layer, or type a new layer name in Layer field, then press Return or Enter.
Box	Specifies a custom box object type. Use the *Left*, *Right*, *Top*, and *Bottom* fields to specify the coordinates.
Text	Specifies a custom text object type. Use the *Origin X* and *Origin Y* fields to specify the location, and *Height* fields to specify the text size.

Line	Specifies a custom line object type. Use the *Starting X* and *Y* fields to specify the coordinates of the line's starting point, and the *Ending X* and *Y* fields to specify the coordinates of the line's ending point.
Add to List	Adds a new custom object to the *Object List*.
Update	Applies any modification to an existing custom object that was loaded into the editor.
Delete	Deletes the current custom object.
Apply	Adds the custom object to the design.
Reset	Clears all actions since the last applied update, clicking the *Apply* button.

4

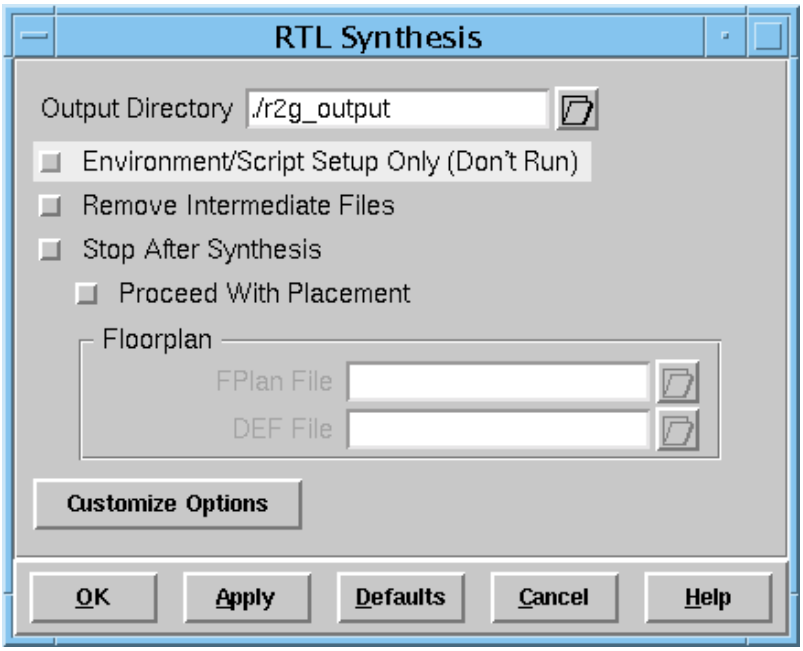
Synthesis Menu

- RTL Synthesis on page 464
- Gates Synthesis on page 475

RTL Synthesis

Use the *RTL Synthesis* menu command to specify the options for setting up and controlling the synthesis run.

➤ Choose *Synthesis* from the main menu and then select *RTL Synthesis* from the pull-down menu.



RTL Synthesis Fields and Options

Output Directory	Specifies the output directory for RC results. Click on the file icon to display a form for selecting the output directory.
Environment/Script Setup Only (Don't Run)	Creates directories and files as needed to prepare the RC synthesis run, without actually running it.
Remove Intermediate Files	Removes all intermediate files, including the RC script, after synthesis is done.
Stop After Synthesis	Runs RC synthesis and generates the gate-level netlist, but does not reload the synthesized netlist. This allows you to iterate synthesis runs to refine the netlist results.

Proceed With Placement	Automatically launches placement after RTL synthesis when either the floorplan or a DEF files is provided.	
Floorplan	Allows you to specify a floorplan file or a DEF file to use for placement.	
	FPlan File	Specifies the name of the floorplan file.
	DEF File	Specifies the name of the DEF file.
Customize Options	Displays the RTL Synthesis Basic Options and RTL Synthesis Advanced Options forms for configuring the RTL synthesis options.	

Related Text Commands

The following text command provides equivalent or additional functionality:

- `compileDesign`

For more information, see the *Command Reference for Encounter RTL Compiler Ultra.*

Supported Subforms

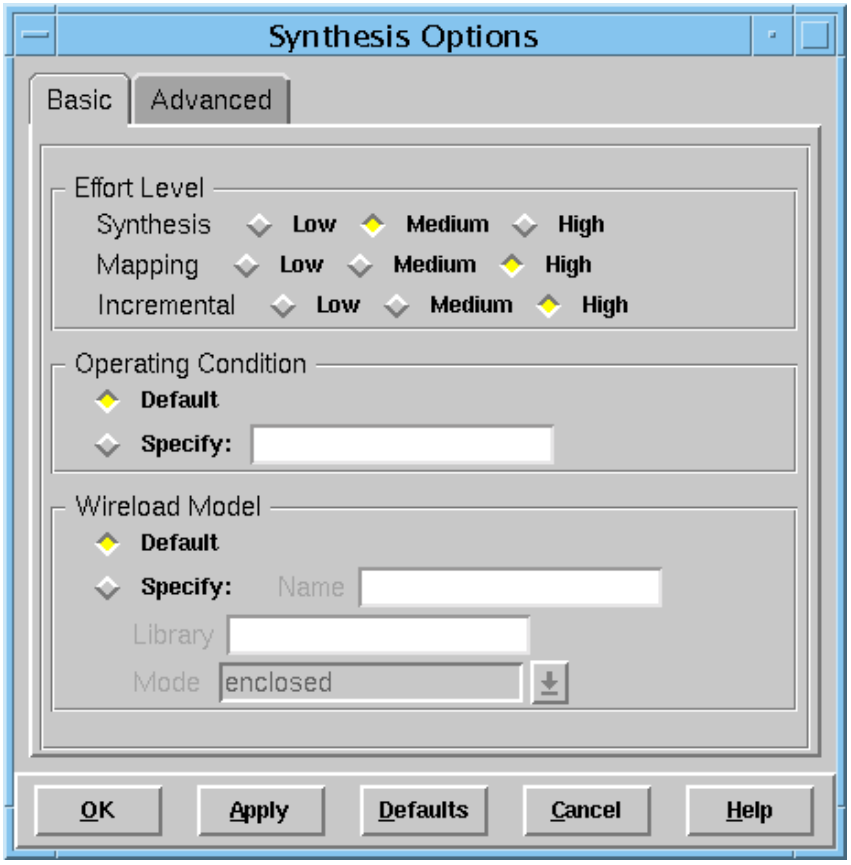
The RTL Synthesis form supports the following subforms:

- RTL Synthesis Basic Options
- RTL Synthesis Advanced Options
- RTL Synthesis Variables Setting
- RTL Synthesis Attributes Setting

RTL Synthesis Basic Options

Use the *Synthesis Options – Basic* form to specify the options for configuring RTL synthesis.

1. Choose *Synthesis – RTL Synthesis.*
2. Select the *Customize Options* button and click on the *Basic* tab.



RTL Synthesis Options – Basic Fields and Options

Effort Level	Specifies the level of effort for RTL optimization, mapping, and incremental optimization.

	Low	The design is mapped to gates, but RTL Compiler does very little optimization, incremental clean up, or redundancy identification and removal. The low setting is generally not recommended.
	Medium	Performs better timing-driven structuring, incremental synthesis, and redundancy identification and removal on the design. Medium is the default.
	High	Performs the timing-driven structuring on larger sections of logic and spends more time and makes more attempts on incremental clean up. This effort level involves very aggressive redundancy identification and removal.
Synthesis	Select whether to use high, medium, or low effort for generic RTL optimization. The default effort level is medium.	
Mapping	Specifies the level of effort for mapping and logic optimization. The aim of optimization is to provide the smallest possible implementation of the synthesized design that still meets the supplied timing goal. The default level is medium.	
Incremental	Specifies the level of effort for incremental synthesis. Incrementally optimizes mapped gates. Allows the mapper to preserve the current implementation of the design and perform incremental optimizations only if the procedure guarantees an improvement in the overall cost of the design. The default level is medium.	
	This parameter only works with an already mapped design.	
Operating Condition	Specifies the default operating condition. If no default is defined, this parameter needs to be specified.	
	Default	Uses the default operating condition.
	Specify	Specifies the operating condition, and overwrites the default. This field is required if a default operating condition is not used.
Wireload Model	Specifies various options for the use of wireload models during synthesis.	

Default	Uses the default wireload model.
Specify	Specifies the name of the wireload model to be used during synthesis.
Library	Specifies the library containing the wireload model.
Mode	Specifies how the wireload model is applied.
enclosed	Uses the wire-load model of the smallest block that fully encloses the net to compute the load of the net. Hierarchical boundary pins are not counted as fanouts.
top	Uses the wire-load model of the top-level design for all nets in all subdesigns. Hierarchical boundary pins are not counted as fanouts.
segmented	Divides nets that cross hierarchical boundaries into segments with one segment for each level of hierarchy. Separate load values are computed for each segment (counting the hierarchical boundary pins as individual fanouts) and the load values are added together.

Related Text Commands

The following text command provides equivalent or additional functionality:

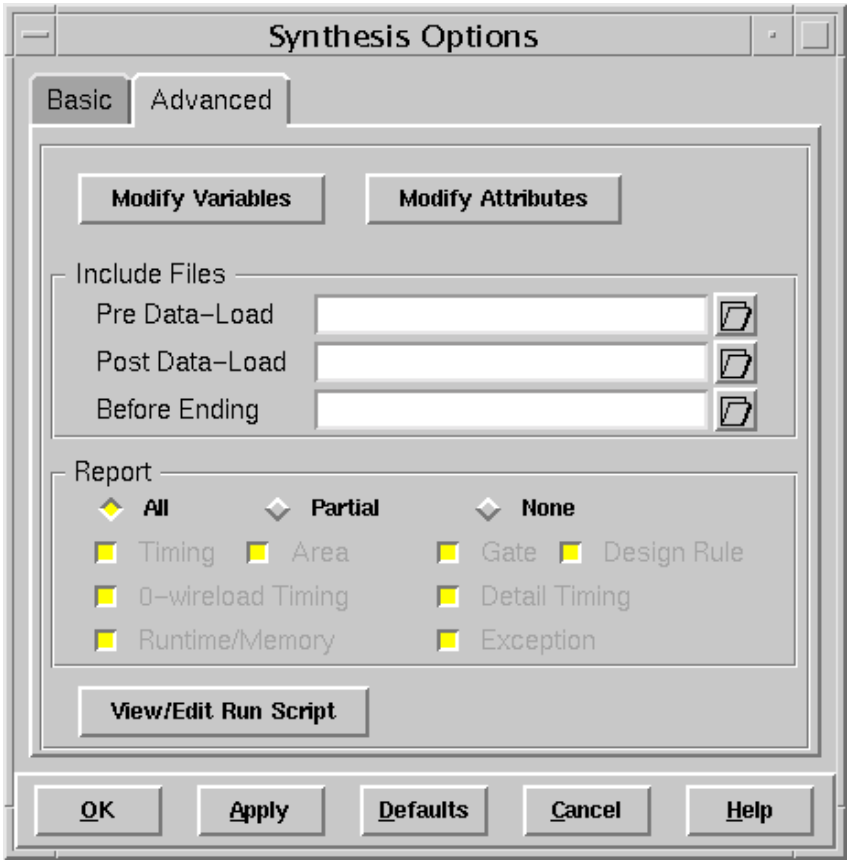
- `setCompileMode`

For more information, see the *Command Reference for Encounter RTL Compiler Ultra.*

RTL Synthesis Advanced Options

Use the *Synthesis Options – Advanced* form to specify the options for configuring advanced aspects of RTL synthesis.

1. Choose *Synthesis – RTL Synthesis.*
2. Select the *Customize Options* button and click on the *Advanced* tab.



RTL Synthesis Options – Advanced Fields and Options

Modify Variables	Allows you to create and edit a list of RC variables. See RTL Synthesis Variables Setting on page 471.
Modify Attributes	Allows you to create and edit a list of RC attributes. See RTL Synthesis Attributes Setting on page 473.

Include Files	These options allow you to specify various files to be used during the synthesis run.	
	Pre Data-Load	Specifies the name of a file to be included prior to loading the design. For example, you can create files for variable and attribute definitions.
	Post Data-Load	Specifies the name of a file to be included after loading the libraries, RTL, and constraints. For example, you can create a file with commands to report specific timing paths before synthesis.
	Before Ending	Specifies the name of a file to be included after synthesis and optimization. For example, you can create a file to report on timing paths after synthesis to compare with pre-synthesis data.
Report	Specifies the type of the reports to be written during the synthesis run. The report options are `all`,	
	All	Generates all the available types of reports.
	Partial	Allows you to select from the following report options: `Timing, Area, Gate, Design Rule, 0-wireload Timing, Detail Timing, Runtime/Memory, Exception`.
	None	Runs the synthesis without generating any reports.
View/Edit Run Script	Displays the synthesis run script in a text editor window where you can view or modify the script and save any changes.	

Related Text Commands

The following text command provides equivalent or additional functionality:

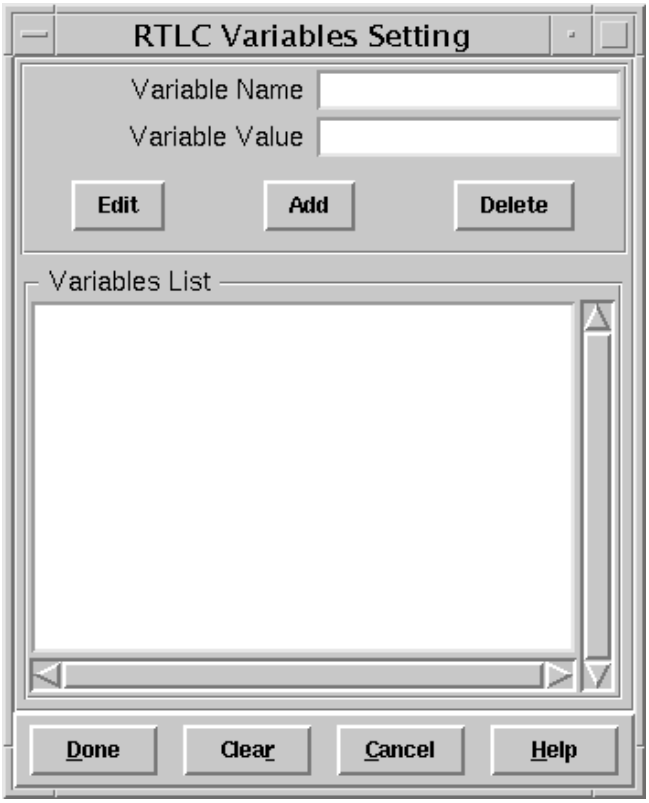
- `setCompileMode`

For more information, see the *Command Reference for Encounter RTL Compiler Ultra.*

RTL Synthesis Variables Setting

Use the *RTLC Variables Setting* form to create and modify the list of RTL synthesis variables.

1. Choose *Synthesis – RTL Synthesis.*
2. Select the *Customize Options* button and click on the *Advanced* tab.
3. Click on the *Modify Variables* button.



RTLC Variables Setting Fields and Options

Variable Name	Specifies the name of an RC variable to be added to the list.
Variable Value	Specifies the value to be assigned to the variable
Edit	Allows you to edit the list of defined variable/value pairs.

Add	Allows you to add the specified variable and value to the list of defined variables.
Delete	Allows you to delete selected variable/value pairs from the list of defined variables.
Variables List	Displays the list of defined variable/value pairs.
Done	Indicates that you have completed modifying the variables list and commits your changes.
Clear	Removes all existing variable/value pairs from the list of defined variables.
Cancel	Cancels any uncommitted changes made to the list of defined variable.

Related Text Commands

The following text command provides equivalent or additional functionality:

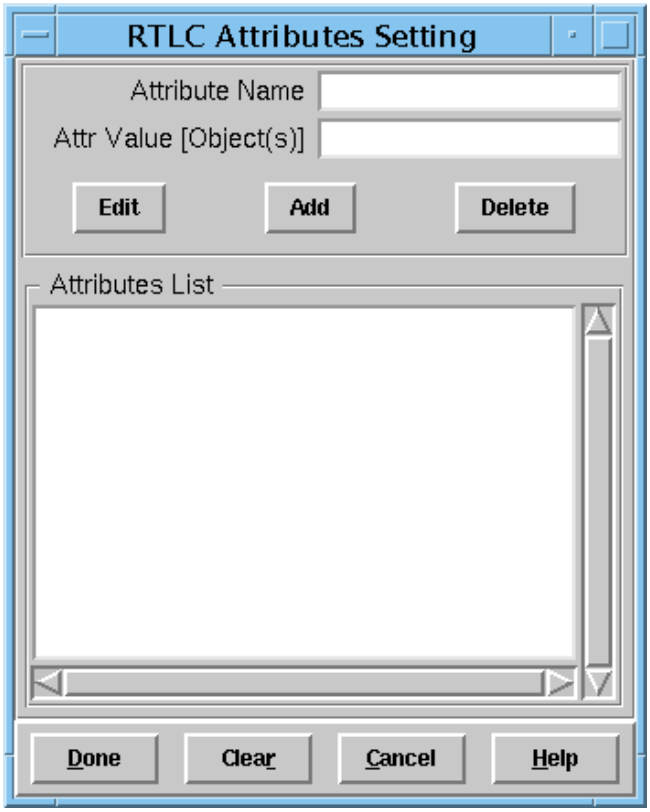
- `setCompileMode -rcVar`

For more information, refer to the manual, *Using Encounter RTL Compiler Ultra*.

RTL Synthesis Attributes Setting

Use the *RTLC Attributes Setting* form to create and modify the list of RTL synthesis attributes.

1. Choose *Synthesis – RTL Synthesis.*
2. Select the *Customize Options* button and click on the *Advanced* tab.
3. Click on the *Modify Attributes* button.



RTL Attributes Setting Fields and Options

Attribute Name	Specifies the name of an RC attribute to be added to the list.
Attribute Value	Specifies the value to be assigned to the attribute.
Edit	Allows you to edit the list of defined attribute/value pairs.
Add	Allows you to add the specified attribute and value to the list of defined variables.

Delete	Allows you to delete selected attribute/value pairs from the list of defined variables.
Variables List	Displays the list of defined attribute/value pairs.
Done	Indicates that you have completed modifying the attributes list and commits your changes.
Clear	Removes all existing attribute/value pairs from the list of defined variables.
Cancel	Cancels any uncommitted changes made to the list of defined attributes.

Related Text Commands

The following text command provides equivalent or additional functionality:

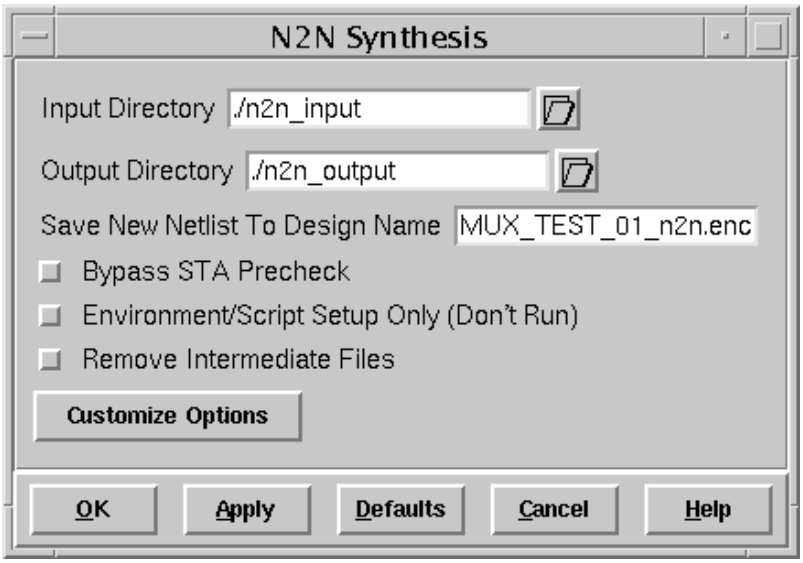
- `setCompileMode -rcAttr`

For more information, see the *Attribute Reference for Encounter RTL Compiler.*

Gates Synthesis

Use the *Gates Synthesis* menu command to specify the options for configuring netlist synthesis and optimization.

➤ Choose *Synthesis – Gates Synthesis.*



N2N Synthesis Fields and Options

Input Directory — Specifies the name of the input directory for all input files to RTL Compiler. The default is `./n2n_input`.

Output Directory — Specifies the name of the directory for output files from RTL Compiler. The default is `./n2n_output`.

Save New Netlist to Design Name

Specifies the FE database name in which to store FE input and output files. The default is *`top_module`*`_n2n.enc`

Bypass STA Precheck — Bypass the zero-load timing check to save run time.

Environment/Script Setup Only (Don't Run)

Creates directories and files as needed to prepare the RC synthesis run, without actually running it.

Remove Intermediate Files	
	Removes all the transferring files, including the script and log files
Customize Options	Displays the Gates Synthesis Basic Options and Gates Synthesis Advanced Options forms for configuring the Gates synthesis options.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runN2NOpt`

Supported Subforms

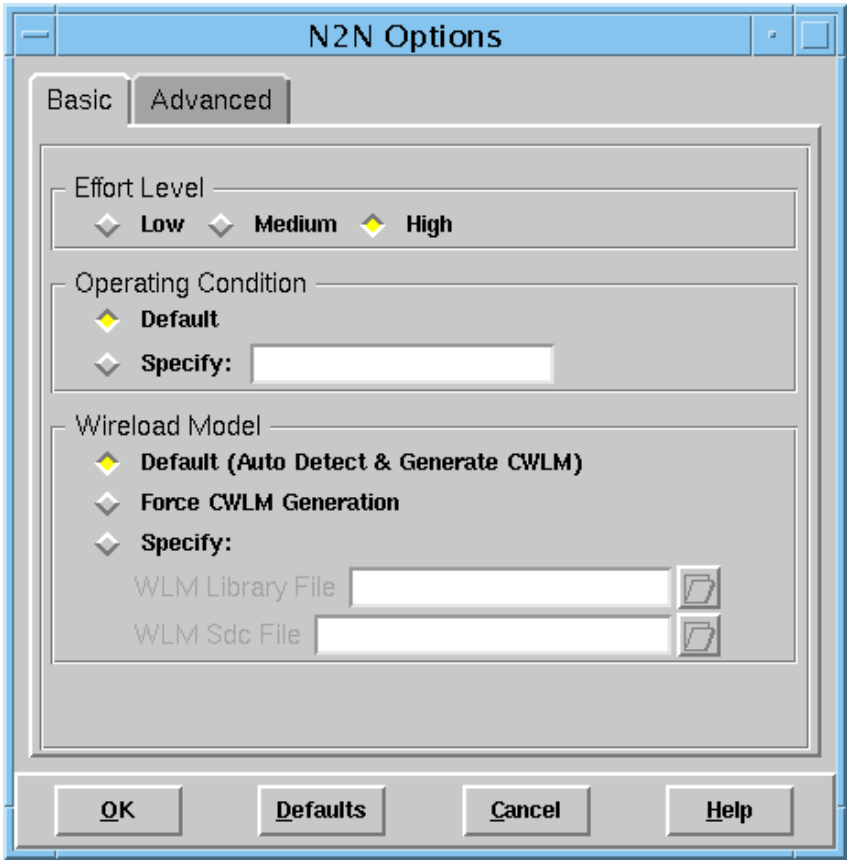
The N2N Synthesis form supports the following subforms:

- Gates Synthesis Basic Options
- Gates Synthesis Advanced Options

Gates Synthesis Basic Options

Use the *N2N Options – Basic* form to specify the options for configuring netlist synthesis and optimization.

1. Choose *Synthesis – Gates Synthesis.*
2. Select the *Customize Options* button and click on the *Basic* tab.



N2N Options – Basic Fields and Options

Effort Level Specifies the level of effort for the optimization run.

	Low	Best choice when you want quick feedback with a minimal number of changes, such as when the netlist is already in good shape and near the final stage. Use this option when you do not want to fully re-synthesize the netlist. No re-mapping is done; critical paths are restructured, area reclaim is done, and incremental optimization is done to minimize changes to the netlist.
	Medium	Provides the best balance of QoR vs. runtime. Use this option when the netlist is reasonable but is not ready for timing closure and tape-out, or long logics on critical paths. This effort level re-maps and restructures critical paths only, followed by incremental optimization. It also changes more of the global netlist and reduces area.
	High	(The default) Performs the most transformations in the netlist. Use this option when the netlist contains long logic chains, does not meet target timing and area objectives, or if you want to improve the timing and area from the current target. This option completely re-maps and restructures the global netlist and then performs incremental optimization. Expect the longest runtimes and a bigger area reduction if the original netlist synthesized poorly.
Operating Condition	Allows you to specify either the default or a user-defined operating condition.	
	Default	Uses the default operating condition.

	Specify:	Specifies the name of the user-defined operating condition. This option overwrites the default.
Wireload Model	The following options control the generation of the custom wireload model.	
	Default (Auto Detect & Generate CWLM)	
		Generates a custom wireload model and applies it to the current synthesis run if no usable wireload model is defined in the library. Creates the wireload model description and the constraint file for the custom wireload model.
	Force CWLM Generation	
		Always generates a custom wireload model and applies it to the current synthesis run regardless of an existing wireload model files in the library.
	WLM Library File	Specifies the name of an existing file containing the description of the custom wireload model.
	WLM Sdc File	Specifies the name of an existing custom wireload constraints file.

Related Text Commands

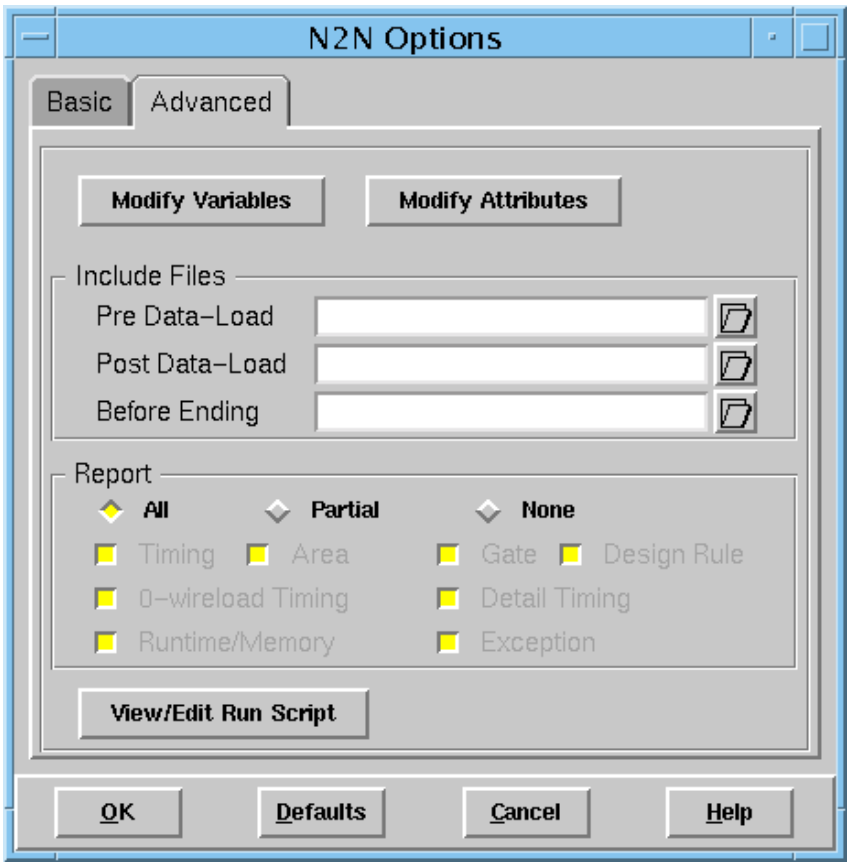
The following text command provides equivalent or additional functionality:

- `runN2NOpt`

Gates Synthesis Advanced Options

Use the *N2N Options – Advanced* form to specify the options for configuring advanced aspects of netlist synthesis and optimization.

1. Choose *Synthesis – Gates Synthesis.*
2. Select the *Customize Options* button and click on the *Advanced* tab.



N2N Options – Advanced Fields and Options

Modify Variables	Allows you to create and edit a list of RC variables. See RTL Synthesis Variables Setting on page 471.
Modify Attributes	Allows you to create and edit a list of RC attributes. RTL Synthesis Attributes Setting on page 473.

Include Files — These fields allow you to specify files to be included before, during, and after the synthesis run.

- *Pre Data-Load* — Specifies any one or more files to be included prior to loading data, including libraries, netlist, and constraint files.
- *Post Data-Load* — Specifies any one or more files to be included prior to the optimization/synthesis run.
- *Before Ending* — Specifies any one or more files to be included after the optimization run.

Report — Specifies the type of the reports to be written during the synthesis run. The report options are:

- *All* — Generates all the available types of reports.
- *Partial* — Allows you to select from the following reports: `Timing`, `Area`, `Gate`, `Design Rule`, `0-wireload Timing`, `Detail Timing`, `Runtime/Memory`, `Exception`.
- *None* — Runs the synthesis without generating any reports.

View/Edit Run Script — Displays the synthesis run script in a text editor window where you can view or modify the script and save any changes.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runN2NOpt`

5

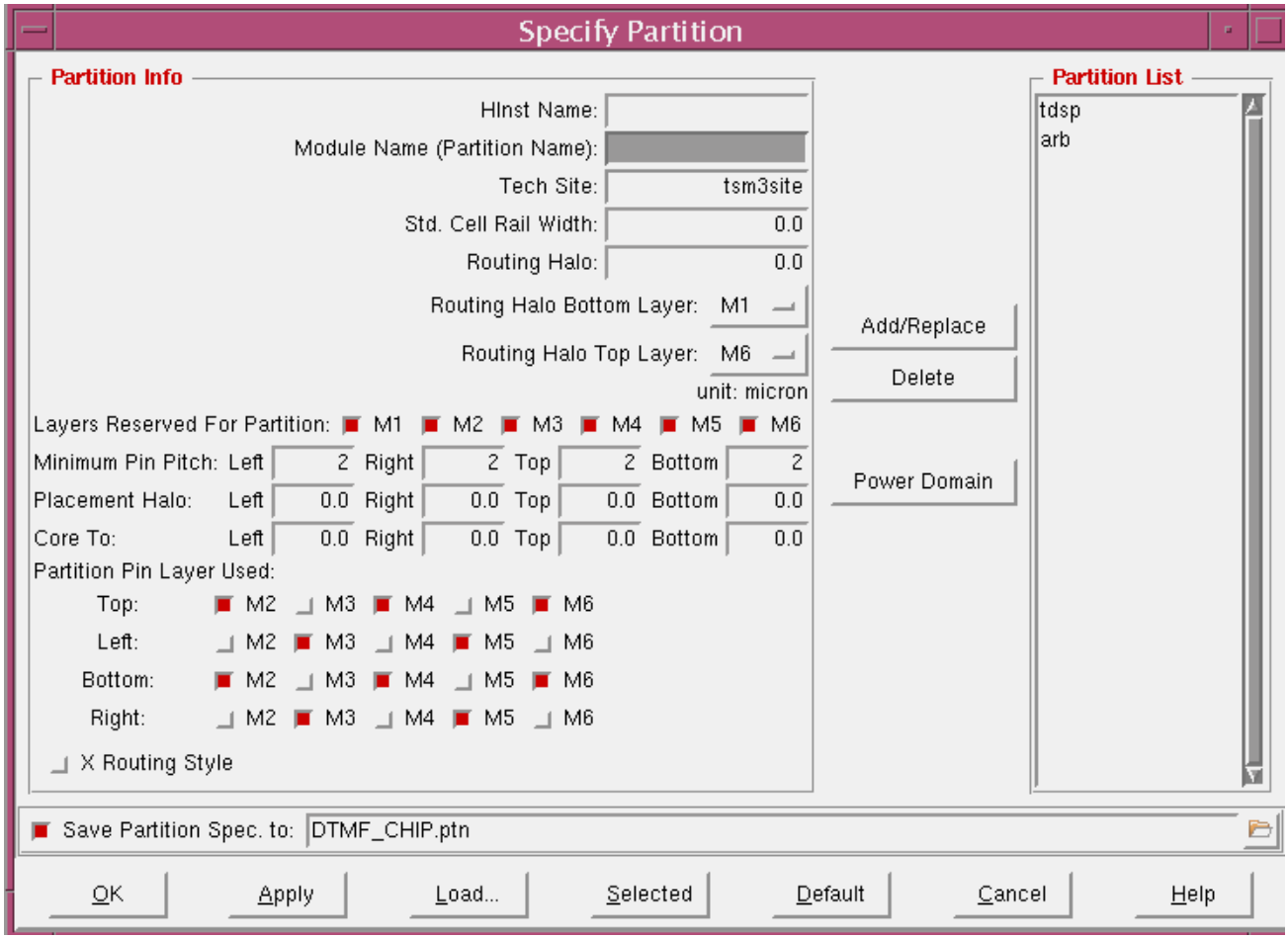
Partition Menu

- Specify Partition on page 484
- Specify Black Box on page 493
- Create Physical Feedthrough on page 498
- Show Wire Crossing on page 500
- Insert Feedthrough Buffer on page 508
- Channel Estimation/FPlan Adjustment on page 511
- Assign Partition Pins on page 513
- DeriveTimingBudget on page 519
- Commit Partition on page 526
- Run Parallel on page 529
- Unpartition on page 531
- Check Pin Assignment on page 532
- Change Partition View on page 533

Specify Partition

Use the Specify Partition form to designate partitions. Before specifying a module or submodule as a partition, you must move the module into the core area.

➤ Choose *Partition – Specify Partition*.



Specify Partition Fields and Options

Note: For a graphical example of how some of these fields relate to a partition, see Defining Partitions in the *Encounter User Guide*.

HInst Name

Specifies the instance name of a module that is to become a partition. A module must correspond to a single module, regardless of its level in the netlist hierarchy.

Important

A partition cannot have another partition as its ancestor or descendant. For the case where more than one module is instantiated with the same cell type, see Specifying Multiple Instantiated Partitions and BlackBoxes in Chapter 6, “Partitioning the Design” of the *Encounter User Guide*.

Module Name (Partition Name)

The name of the hierarchical instance module is taken as the name of the partition.

Tech Site

Specifies the technology site name. The partition will have the same site as the top-level design. If the specified hierarchical instance is also a power domain, then the corresponding power domain row structure is displayed.

Std. Cell Rail Width

Specifies the standard cell power rail width, in micrometers. If partition pins are not allowed above power or ground rail width, enter the dimension of the power rail width. If a value of 0.0 is entered (the default), the width from the Technology file will be used.

If partition pins are not allowed above power and ground rails, select *Disallow pins above power/ground rails* in the Partition form.

Routing Halo

Specifies routing spacing, in micrometers, around the sides of the partition. Routing on the specific routing layers in this area will be considered as high cost. The router can, however, perform routing perpendicular to the pins.

You can specify a positive or a negative value for the routing halo. A positive value means that the halo will be outside the partition. A negative value means that the halo will be applicable during block implementation, inside of the partition.

The same value is used for all sides of the partition.

Note: For instance blocks— blackboxes, hard macros or block-level designs—specify the routing halo through the Edit Halo form or through the `addRoutingHalo` command. Also, for bottom- up hierarchal flow, specify routing halo for a block at the top-level design or at the block-level design through the Edit Halo form or through the `addRoutingHalo` command.

Routing Halo Bottom Layer

Specifies the bottom partition layer for which routing halo will be created.

Default: By default, the bottom layer reserved for the partition is used

Routing Halo Top Layer

Specifies the top partition layer for which routing halo will be created.

Default: By default, the top layer reserved for the partition is used.

Layers Reserved for Partition

Specifies the selected metal layers that are used for routing in the partition and generating partition pins. Any unselected metal layers, usually the top-most metal layers, are allowed to route over the partition.

A normal six-metal layer selection process is `M1`, `M2`, `M3`, `M4` and `M5` selected, and `M6` unselected. When saving the partition, the LEF generated for this partition will have routing blockages on their layers so that the top-level router is aware of which metal layers are being used in the partition

Minimum Pin Pitch

Specifies the pin pitch dimension for the *Left*, *Right*, *Top*, and *Bottom* partition sides. The default is 2, which places one pin for every two metal tracks. The actual pin pitch depends on the pin's metal layer.

Note: The Partition Pin Guide floorplan object will supersede this entry and use the *Min. Space* entry in the object's Attribute Editor.

Placement Halo

Specifies extra spacing, in micrometers (around the left, bottom, right and top sides respectively) of the partition that should not be used for placement. The placement program will not place standard cells in the area for partition placement. This spacing is called *placement halo.*

At the top-level design, this information is saved as part of the partition section in a floorplan file. This information is also saved in a partition floorplan file when saving partitions. By default, the value is 0 for all the sides.

If the hierarchical instance was earlier defined as a power domain, then this field corresponds to the minimum gap parameter of the power domain.

Core to Left
Core to Right
Core to Top
Core to Bottom

Specifies the space, in micrometers, between the module boundary and core design area of the partition module. The partition pins will be located at the partition instance boundary and the core area. The placement program will not place standard cells in this area for partition placement.

If the specified hierarchical instance is also a power domain, then these fields will have the same value as the power domain.

Partition Pin Layer Used

Specifies the metal layers from the defaults. The default metal layers correspond to the sides of the partition, where the vertical metal layers (for example, *M2*, *M4*, and so on) are for the Top and Bottom sides, and horizontal metal layers (for example, *M3*, *M5*, and so on) are for the Left and Right sides of the partition.

Deselecting all metal layers for a side of a partition prevents pins from being created for the entire side of that partition. These deselected layers overwrite the *Partition Pin Layer* selection, used when clicking *Add/Replace*.

Note: The initially displayed pin layers are the layers that are specified in the LEF or technology file.

Add/Replace

Updates the partition constraint information and adds it to the *Partition List*.

Delete

Removes highlighted entries in the *Partition List*.

Power Domain

Opens the Power Domain form to designate a power domain as a partition. If the specified hierarchical instance is also a power domain, the corresponding power domain information will be available.

See Power Domain on page 490 for more information.

Partition List

Lists the specified partitions. To change the order of the partitions in the list, click the left mouse button on the partition name and drag it to its new area.

X Routing Style

Specifies that the design has X routing.

Important

X Routing Style is obsolete and will be removed in the next major release of the software.

Save Partition Spec. to

Outputs the partition assignment to the partition specification file. The default filename is `designName`.ptn.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `definePartition`
- `specifyPartition`

Related Topics

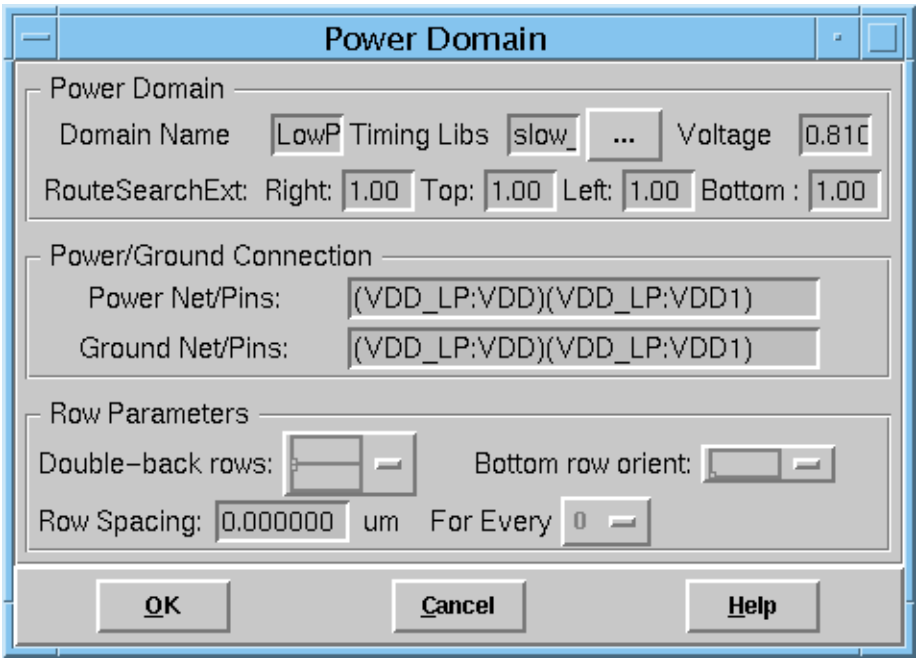
For information on the following topics, see “Partitioning the Design” in the *Encounter User Guide*.

- Defining Partitions
- Specifying Multiple Instantiated Partitions and Blackboxes
- Changing Partition Clone Orientation
- Specifying Rectilinear Partitions and Blackboxes
- Specifying Core-to-I/O Distance for Partition Cuts
- Specifying Nested Partitions
- Creating a Blackbox Inside a Partition

Power Domain

Use the Power Domain form to designate a power domain as a partition.

Clicking the *Power Domain* button opens the Power Domain form.



Power Domain Fields and Options

Domain Name	Specifies the name of the partition to become a power domain.
Timing Libs	Specifies the name of one or more timing libraries to associate with the power domain. To choose a timing library, use the Specify Timing Libraries form. For information about using this form, see "Power Menu" on page 683.
Voltage	Specifies the voltage information for the power domain. **Note:** You cannot enter a value in this field. This field is populated with values obtained when you use the Specify Timing Libraries form. For more information, see "Power Menu" on page 683.

RouteSearchExt

(Optional) Specifies a distance, in microns, that limits the search for legal targets by the power planning and routing software beyond the power domain boundary. This prevents unwanted connections to targets of the same net that are not associated with the power domain.

Power Net/Pins

A list of power net and power pin connections to be included in the power domain. These must be specified in the following format:

(*power_net1*: *power_pin1 power_pin2* ...)
(*power_net2*: *power_pin3 power_pin4* ...)
...

Ground Net/Pins

A list of ground nets and ground pin connections to be included in the power domain. These must be specified in the following format:

(*ground_net1*: *ground_pin1 ground_pin2* ...)
(*ground_net2*: *ground_pin3 ground_pin4* ...)
...

Double-back rows

Allows the selection of standard cell row pair orientations. The orientation selections for the row pair are bottom-to-bottom or top-to-bottom. The default is bottom-to-bottom orientation.

Bottom row orient

Specifies the orientation of the bottom row in the core area. The default is an `R0` orientation, or you can choose the `MX` orientation (mirrored through the x axis).

Row Spacing for Every # rows

Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pulldown menu, specify *1* for every row, or *2* for every other row.

Related Text Commands

For information about the following text commands, see “Multiple Supply Voltage (MSV) Commands” in the *Encounter Text Command Reference*.

- `createPowerDomain`
- `createPowerDomainCut`

- `modifyPowerDomainAttr`
- `modifyPowerDomainMember`

Related Topics

For information on the following topics, see “Low Power Design” in the *Encounter User Guide*.

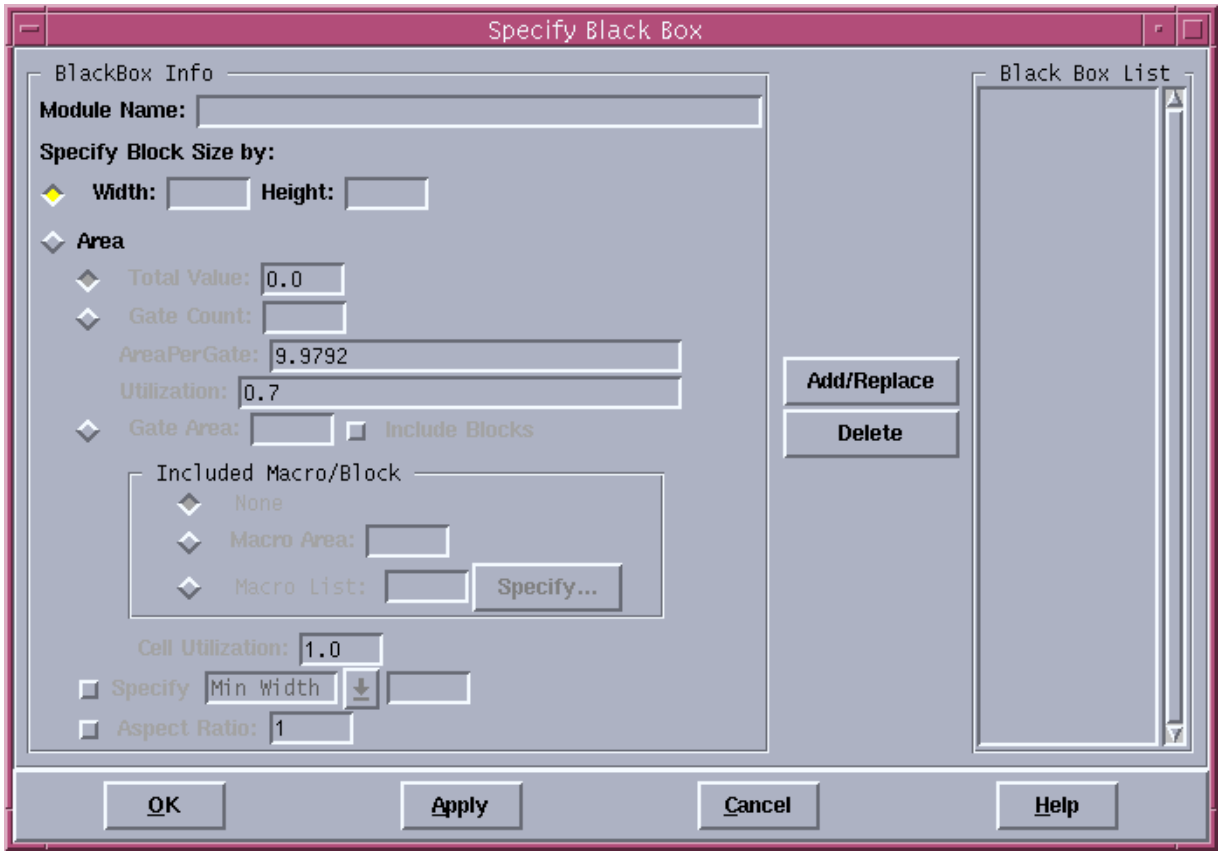
- Mulitple Suppy Voltage Flat Flow
- Creating a Rectilinear Power Domain

Specify Black Box

Use the Specify Black Box form to specify which modules will be regarded as blackboxes.

➤ Choose *Partition – Specify Black Box*

.



Specify Black Box Fields and Options

Module Name	Specifies a module name or leaf cell name that is defined in the netlist to be treated as a blackbox. For the modules that are not empty, the content information of this module is not expanded in the data structure to reduce the used memory.
Width, Height	Specifies fixed width and height of a specified module, in micrometers.

Area

Specifies that the blackbox will be sized by area.

Value

Specifies area value in square micrometers. If you specify the block size area, the default created block aspect ratio is 1.

Gate Count

Specifies a gate count value. The total cell area is equal to the specified gate count multiplied by the specified area per gate. This field has no default value.

AreaPerGate

Specifies an area per gate value in square micrometers. The default value is three times (3x) the area of the standard cell site.

Utilization

Specifies the cell utilization. This value derives the area that is reserved for routing. The final block size is equal to the total cell area plus the routing area. The default value is 0.7 (70 percent).

Gate Area

Specifies the gate area.

Include Blocks

Specifies that the gate area includes the macro area.

If the *Include Blocks* option is not selected, the final gate area for the blackbox is derived by adding the area of the hard macro(s) to the gate area specified in the *Gate Area* field.

If the *Include Blocks* option is selected, the specified gate area also includes the area of the specified hard macro(s).

Default: Off.

Included Macro/Block

None

Specifies that no macros or blocks are included.

Macro Area

Specifies the total area of the macro(s) in square microns. This value is added to the total gate area.

Macro List

Specifies the hard macro(s) to include in the blackbox. Enter the name of the macro followed by the number of times the macro will be instantiated in the blackbox. You can specify more than one blackbox. For example, to specify the macro `RAM_128x16A` two times and the macro `pllclk` one time, enter the following in the *Macro List* field:

```
RAM_128x16A 2 pllclk 1
```

You can also select the macros from a list of available macros. For this, click the *Specify...* button and enter the details in the Specify Macros form that appears. For more information, see Specify Macros on page 496.

Cell Utilization

Specifies the cell utilization. This value is used to derive the area of the blackbox, which is calculated using the following formula:

Blackbox area = (standard cell area / cell utilization) + macro area

Default: The default value of cell utilization is `1` (100%).

Aspect Ratio

Specifies the aspect ratio value of its width divided by its height (x/y). This value combined with the specified related area information determines the necessary width and height of a blackbox.

Add/Replace

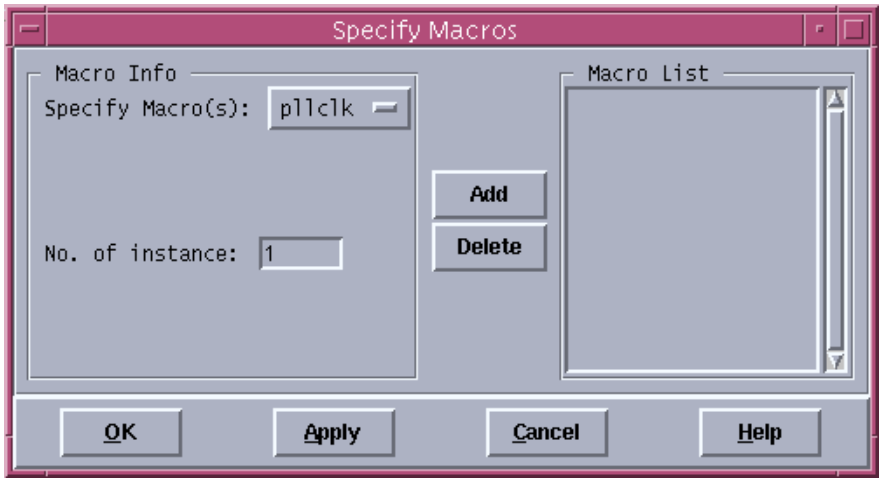
Adds the new specified module as a blackbox with its block size information to the *Black Box List*. If you modify the block size of a given module that is already specified as a blackbox, click the *Add/Replace* button to update the block size information.

Delete	Deletes a selected blackbox in the *Black Box List* and its specified constraints. **Note:** You cannot delete a blackbox if it is an empty module in the netlist, or a cell that has no physical macro definition.
Black Box List	Lists all the blackbox modules, if available. You can highlight a module entry field name to populate the *Module Name* and block size information. For a blackbox that already has pin assignment, if you change its size, the Encounter software will change the blackbox size and un-assign all the pins.

Specify Macros

Use the Specify Macros form to select the hard macro(s) whose area(s) will be included while calculating the total gate area of the blackbox.

➤ Choose *Partition – Specify Black Box*, and then click the *Specify...* Button, which is located next to the *Macro List* option.



Specify Macros Fields and Options

Specify Macro(s)	Displays the macros from a list of the available macros. To specify a macro whose area should be included while calculating the total area of the blackbox, select the macro and click the Add button.
No. of Instances	Specifies the number of times the macro is referenced. Thus, by specifying a value for count, you avoid repeating the macro names for macros that are referenced multiple times. *Default*: The default value is 1.
Add	Adds the macro selected in the Specify Macro field to the Macro List field.
Delete	To remove a macro from the Macro List field, select the macro in the Macro List field and click the Delete button.
Macro List	Displays the list of macro(s) whose area(s) will be included while calculating the total gate area of the blackbox.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `resizeBlackBox`
- `specifyBlackBox`
- `unspecifyBlackBox`

Related Topics

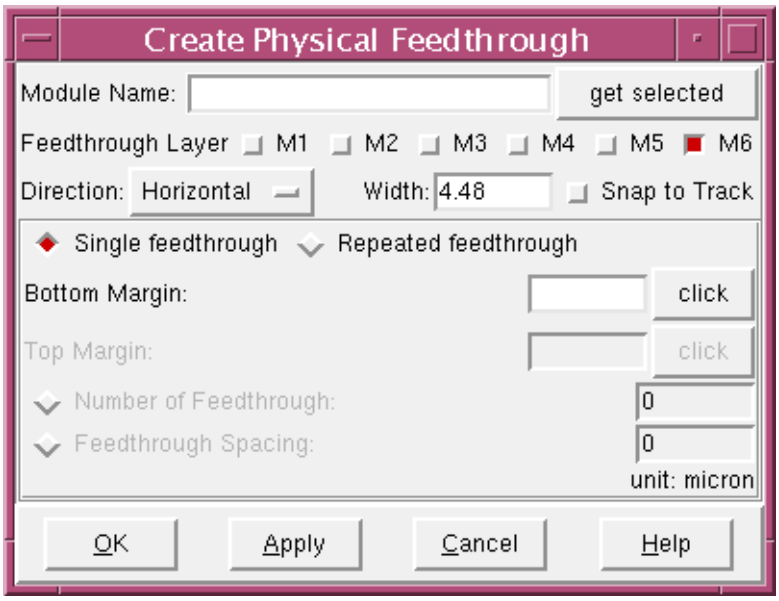
For information on the following topics, see “Partitioning the Design” in the *Encounter User Guide*.

- Defining Blackboxes
- Specifying Multiple Instantiated Partitions and Blackboxes
- Specifying Rectilinear Partitions and Blackboxes

Create Physical Feedthrough

Use the Create Physical Feedthrough form to specify a feedthrough or several feedthroughs on a partition. You can insert feedthroughs in partitions to satisfy timing requirements or accommodate physical constraints. Use this form after specifying the partition(s), but before running the Partition program.

➤ Choose *Partition – Create Physical Feedthrough*.



Create Physical Feedthrough Fields and Options

Module Name	Type the module name in the field or highlight the module in the design display area and click *get selected*.
Feedthrough Layer	Specifies the metal layer(s) that can be routed over the feedthrough area. The default is metal layer 6 (M6), the top-most metal layer.
Direction	Specifies either a *Horizontal* or *Vertical* direction.
Width	Specifies the width of the feedthrough, in micrometers.
Snap to Track	Snaps the feedthrough to a routing track.
Single feedthrough	Creates one feedthrough.
Repeated feedthrough	Creates repeated feedthroughs.

Bottom Margin	With the *Direction: Horizontal* option selected, this specifies the bottom margin for a single feedthrough or repeated feedthroughs.
Top Margin	With the *Direction: Horizontal* option selected, this specifies the top margin for repeated feedthroughs.
Left Margin	With the *Direction: Vertical* option selected, this specifies the left margin for a single feedthrough or repeated feedthroughs.
Right Margin	With the *Direction: Vertical* option selected, this specifies the right margin for repeated feedthroughs.
Number of Feedthrough	Specifies the number of feedthroughs when selecting *Repeated feedthrough*.
Feedthrough Spacing	Specifies the spacing, in micrometers, between the feedthroughs when selecting *Repeated feedthrough*.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `createPtnFeedthrough`
- `deleteAllPtnFeedthroughs`

Related Topics

For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Inserting Feedthroughs

Show Wire Crossing

Use the Show Wire Crossing form to display all the nets that have cross-partition routing. The nets that have wire crossing are highlighted in the artwork window. You can use this feature to help you decide whether a net should be a feedthrough net or not.

The Show Wire Crossing form consists of the following two pages:

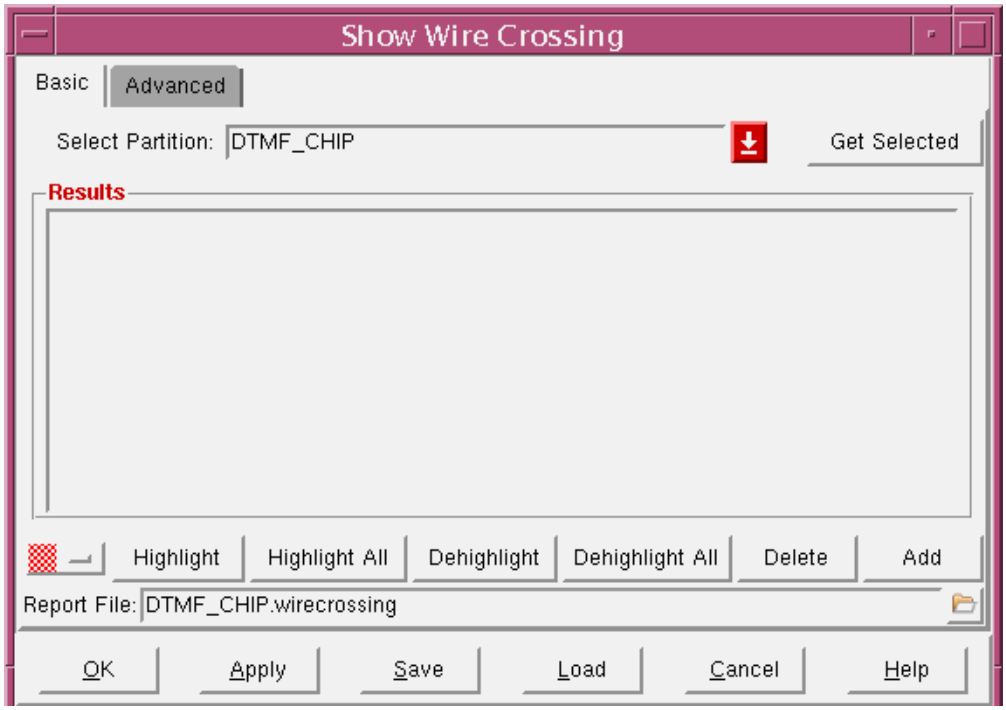
- Show Wire Crossing – Basic
- Show Wire Crossing – Advanced

Show Wire Crossing – Basic

Use the Show Wire Crossing – Basic form to display all the nets that have cross-partition routing. The nets that have wire crossing are highlighted in the artwork window.

You can save the list of nets that have wire crossing in a file, and later use this file as an input file while inserting feedthrough buffers. You can thus use this feature to help you decide which nets should be used as feedthrough nets.

➤ Choose *Partition – Show Wire Crossing,* and then click on the *Basic* tab.



Show Wire Crossing - Basic Fields and Options

Select Partition	Displays a list of partitions in the design. Select the partition for which you want to display the nets that cross the partition.
Get Selected	Gets the names of the currently selected partition in the artwork. By default, the current-level design name is displayed.

Results	Displays the nets for the selected partitions. The nets displayed are considered part of the current editing list of nets, which will be saved in the file specified in the *Report File* field.
Highlight	Displays nets that have wire crossing over the specified partition. If the specified partition is a design, the *Results* window displays those nets that have wire crossing over all the partitions in this design.
Highlight All	When you click *Highlight All*, all nets in the Results window are highlighted in the design display area.
Dehighlight	When you click *Highlight*, the nets selected in the Results window are dehighlighted in the design display area.
Dehighlight All	When you click *Highlight All*, all nets in the Results window are dehighlighted in the design display area.
Delete	Deletes the net selected in the Results Window from the Results Window. The deleted net will not be saved in the file specified in the *Report File* field.
Add	Displays the Add Net Names form, which you can use to add nets to the current editing list displayed in the Results Window. The added nets will be saved in the file specified in the *Report File* field. For more information, see Add Net Names on page 504.
Report File	Specifies the file in which the current editing list displayed in the Results Window is saved. You can later use this file as an input file while inserting partition feedthrough buffers. You can thus choose which nets should be feedthrough nets.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `showPtnWireX`

Related Topics

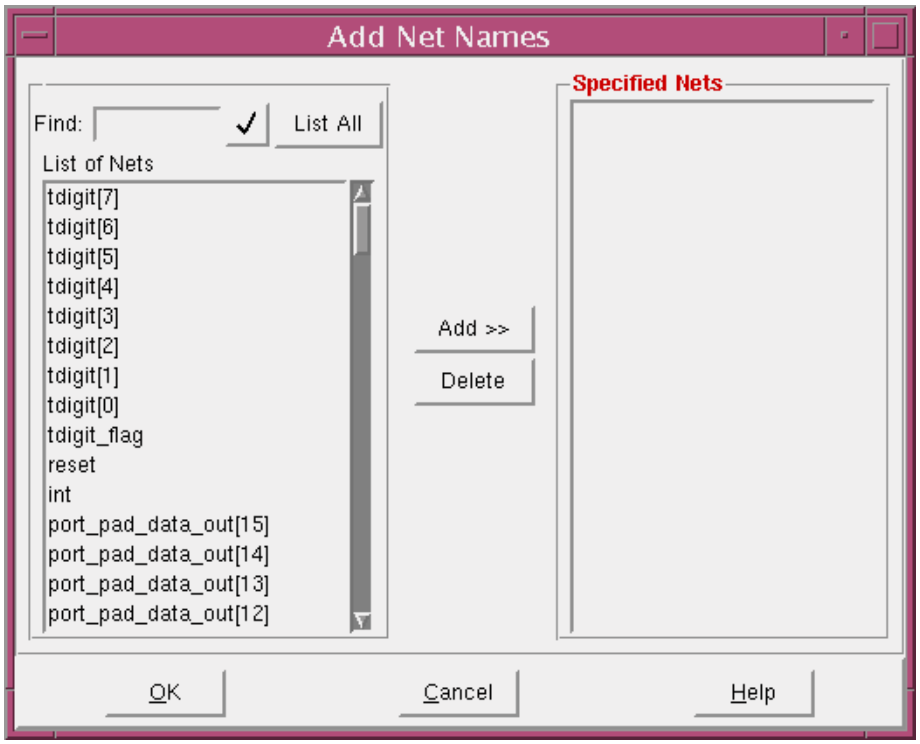
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Generating the Wire Crossing Report

Add Net Names

Use the Add Net Names form to add nets to the current editing list displayed in the Results Window of the *Show Wire Crossing - Basic* form. The added nets will be saved in the file specified in the *Report File* field of the *Show Wire Closing - Basic* form

➤ Choose *Partition – Show Wire Crossing,* and in the *Basic* tab, click *Add*.



Add Net Names - Fields and Options

Find	Type the name of the net that you want to include in the list of specified nets and click the button next to the field. The selected net is displayed in the *List of Nets* field. You can also specify wildcards(*). The names are case-sensitive.
List All	Displays all the nets in the design for the selected partitions.
Specified Nets	Displays the list of the nets that will be added to the Results window of the *Show Wire Crossing – Basic* form when you click *OK* or *Apply*.

Add	Add the selected net in the *List of Nets* field to the list displayed in *Specified Nets*.
Delete	Removes the net selected in *Specified Nets*.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `showPtnWireX`

Related Topics

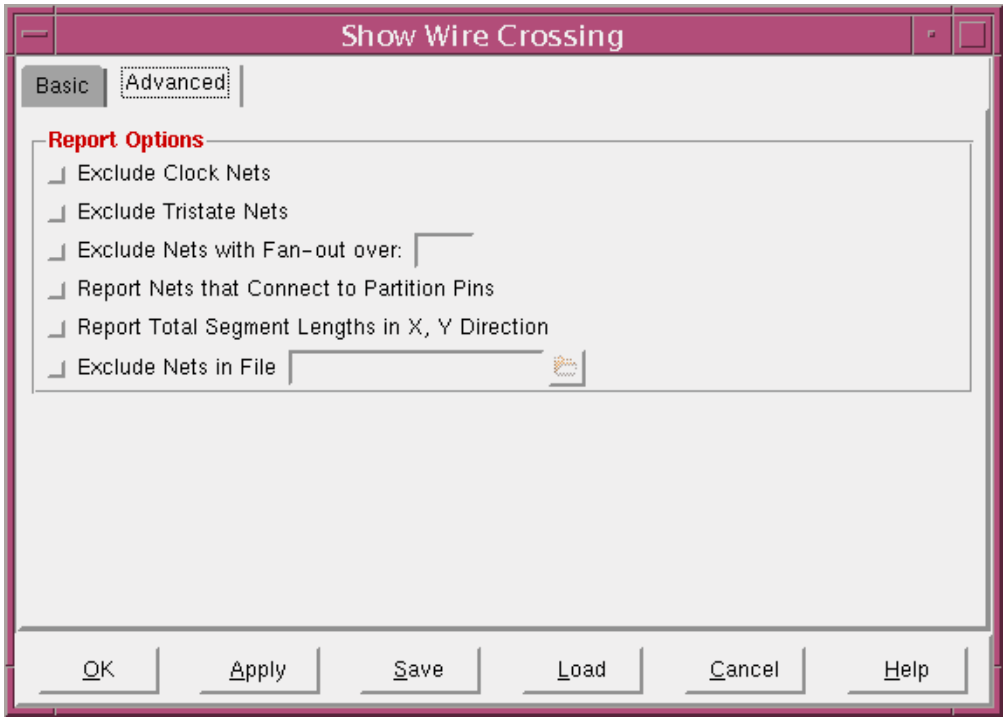
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

Generating the Wire Crossing Report

Show Wire Crossing – Advanced

Use the Show Wire Crossing – Advanced form to customize the list of nets that will be highlighted. For example, you can specify whether clock nets should be highlighted.

➤ Choose *Partition – Show Wire Crossing,* and then click on the *Advanced* tab.



Show Wire Crossing - Advanced Fields and Options

Exclude Clock Nets	Specifies that clock nets should not be displayed in the Results window and highlighted. Default *Off*
Exclude Tristate Nets	Specifies that tristate nets should not be displayed in the Results window and highlighted. Default *Off*
Exclude Nets with fan-out over	Specifies that nets that have a fan-out value greater than the specified value should not be displayed in the Results window and highlighted. Default *Off*

Report Nets also Connect to Partition Pins	Specifies that nets that connect to partition pins should be reported and highlighted. Default *Off*
Report Total Segment Lengths in the X, Y Direction	Specifies that the segment length in the X, Y direction should also be displayed in the artwork window.
Exclude Nets in File	Specifies that the nets in the specified file should not be included in the Results window and highlighted.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `showPtnWireX`

Related Topics

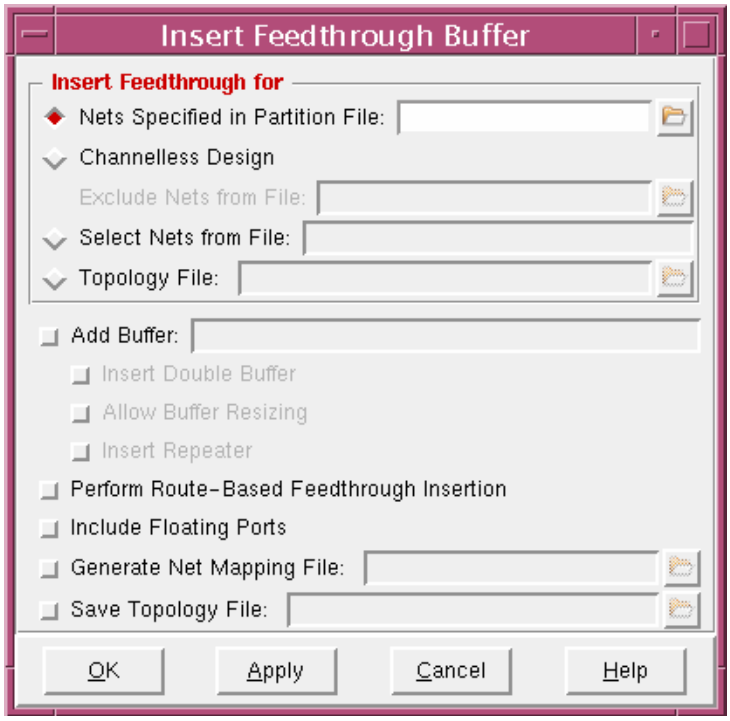
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

Generating the Wire Crossing Report

Insert Feedthrough Buffer

Use the Insert Feedthrough Buffer form to insert feedthrough buffers into the partitions to avoid routing a net over a block area. This automatically runs ECO placement and changes the original netlist.

➤ Choose *Partition – Insert Feedthrough Buffer*.



Insert Feedthrough Buffer Fields and Options

Nets Specified in PtnFile	Specifies a file that contains net names to be feedthrough nets for a partition and feedthrough buffers inserted.
Channelless Design	Specifies that the design is pure channelless, having no channel available for routing, and therefore all nets will be considered for buffer insertion.
Exclude Nets from File	Specifies the file that contains net names to be excluded from being a feedthrough net for a partition.

Select Nets from File

Specifies the file that contains net names to be feedthrough nets for a partition and inserted feedthrough buffers.

Topology File

Specifies the file that has the topology tree information. This information is used to create feedthrough buffers for the netlist.

Note: If you specify a topology file, only those nets that are specified in the topology file are considered for feedthrough buffer insertion.

Note: If a net does not exist in the design, it should not be in the topology file. For example, if ECO changes remove a net, that net should be removed from the topology file.

Add Buffer

Specifies the name of the feedthrough buffer cell type.

Insert Double Buffer

Specifies that two buffers are added: one close to the feedthrough input pin, and the other close to the feedthrough output pin.

Allow Buffer Resizing

Specifies that inserted feedthrough buffer(s) are resized to optimize timing.

Note: If this option is specified with *Insert Repeater*, then resizing is done before repeater insertion, regardless of the order they are specified.

Important

You must load the timing library and timing constraint file before selecting this option.

Insert Repeater

Specifies that buffers and inverters are inserted to optimize timing along the path of feedthrough buffers.

Note: If this option is specified with *Allow Buffer Resizing*, then resizing is done before repeater insertion, regardless of the order they are specified.

Important

You must load the timing library and timing constraint file before selecting this option.

Do Route Based	Derives the feedthrough topology based on the routing results.
Include Floating Ports	Specifies that floating ports are included in the feedthrough buffer insertion. Without this option, floating ports are not considered.
Generate Net Mapping File	Generates a file that maps the original net name to the new net name created for the feedthrough buffers.
Save Topology File	Saves a file with feedthrough buffer topology tree information from an existing floorplan.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `deleteAllPtnFeedthroughs`
- `insertPtnFeedthrough`

Related Topics

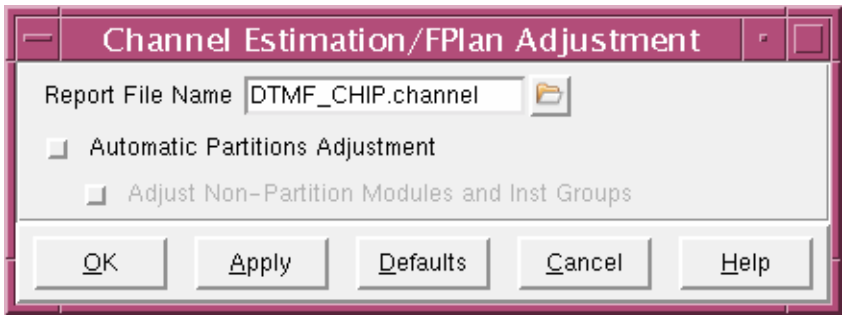
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Inserting Feedthroughs

Channel Estimation/FPlan Adjustment

Use the Channel Estimation/FPlan Adjustment form to generate a report on the required spacing between partitions, blackboxes, and hard macros, and automatically adjust the partition shapes to allow for the calculated channel width. This feature automatically assigns pins for uncommitted partitions and blackboxes to get more accurate channel width estimations.

➤ Choose *Partition – Estimate Routing Channel*.



Channel Estimation/FPlan Adjustment Fields and Options

Report File Name
Specifies the report output file. The default is `topCellName.channel`.

Automatic Partitions Adjustment
Includes the adjustment of blackboxes, hard macros, and modules that are specified as partitions.

Adjust Non-Partition Modules and Inst Groups
Includes the adjustment of non-partition modules and instance groups (guides, regions, or fences).

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

■ `estimatePtnChannel`

Related Topics

For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Estimating the Routing Channel Width

Assign Partition Pins

Use the Assign Partition Pins form to assign partition pins. You can assign pins for a partition without having to commit the partition.

The Assign Partition Pins form consists of the following two pages:

- Assign Partition Pins – Basic
- Assign Partition Pins – Advanced

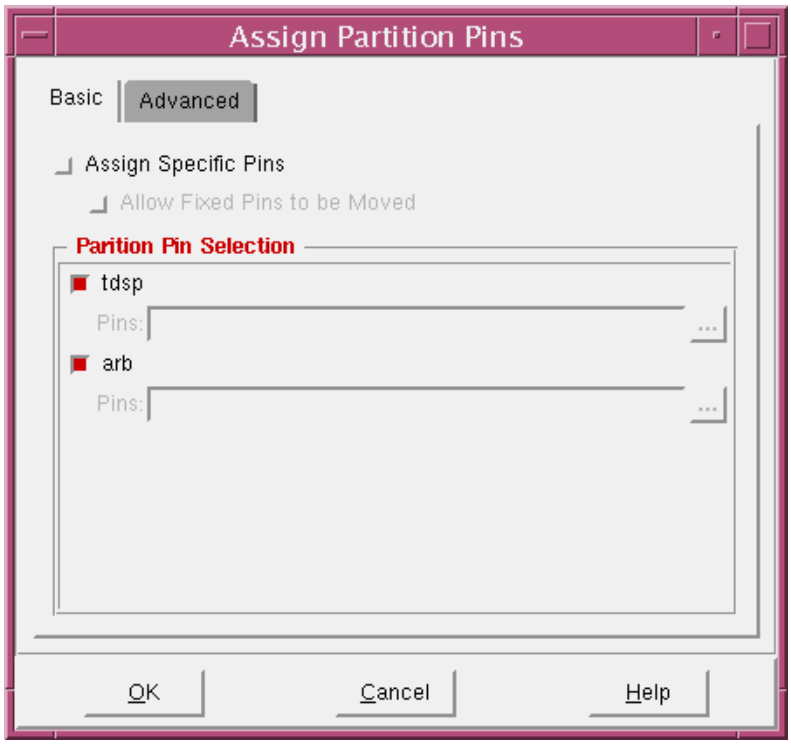
Assign Partition Pins – Basic

Use the Assign Partition Pins – Basic form to create pins for the partitions.

Important

You should route the design before assigning partition pins.

➤ Choose *Partition – Assign Pins*, and click the *Basic* tab.



Partition Fields and Options

Assign Specific Pins — Specifies that only the specified pins should be assigned. If you do not select this check box, all pins for all partitions are assigned.

Allow fixed Pins to be Moved

If you select this checkbox, the specified pins with a *Fixed* status can also be moved.

Note: Pins that are not specified but have a *Fixed* status are *not* moved.

Default: The specified pins with a *Fixed* status are *not* moved.

Partition Pin selection

If you select the *Assign Specific Pins* checkbox, specify the pins to assign for each partition, in the corresponding *Pins* field next to the name of the partition.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `assignPtnPin`

Related Topics

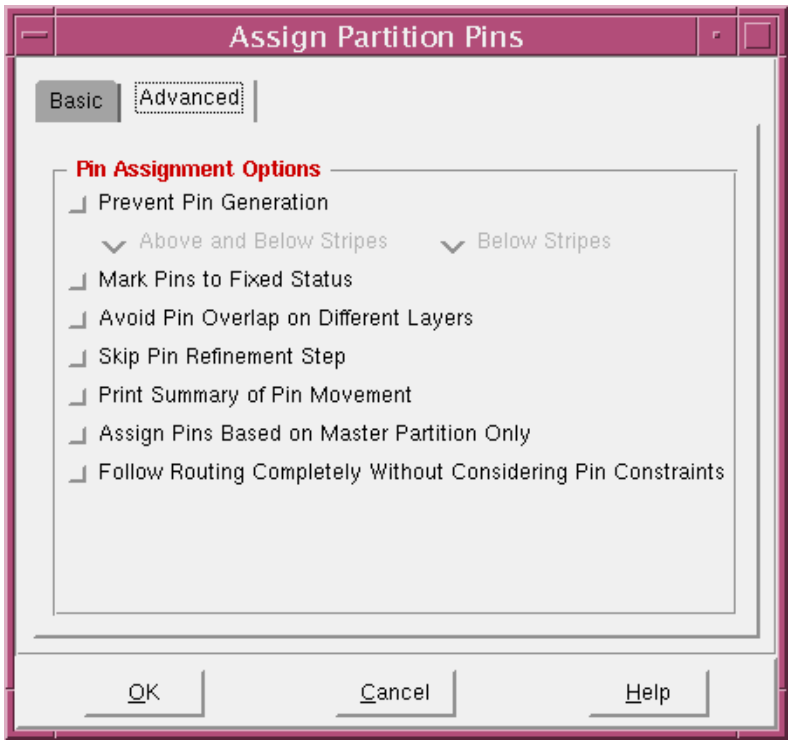
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Assigning Pins

Assign Partition Pins – Advanced

Use the Advanced Partition Pins – Advanced form to customize the pin assignment options. For example, you can specify that the status of the assigned pins should be changed to *Fixed*.

➤ Choose *Partition – Assign Pins*, and click the *Advanced* tab.



Assign Partition Pins – Advanced Fields and Options

Prevent Pin generation

Above and Below Stripes	Prevents the generation of pins on all metal layers, above and below the power and ground strips.
Below Stripes	Prevents the generation of pins below power and ground strips.

Mark Pins to Fixed Status

Specifies that all pins will have a Fixed status.

Default: *Off*

Avoid Pin Overlap on Different Layers

Specifies the following:

- There are no pins above or below any pin, across layers. That is, if a pin on a layer has co-ordinates x and y, there are no pins on co-ordinates x and y on any other layer. This applies to all pins on all layers.
- If the value of the pin pitch is 1 (instead of the default value of 2 or any other value), adjacent pins are not placed on the same layer.

Default: *Off*

Skip Pin Refinement Step

Does not allow topology-based pin refinement. Pin refinement refines the pin locations to reduce the top-level congestion or top-level wire length. Pin location assignment is only based on connectivity or trial routing.

Default: *Off*

Print Summary of Pin Movement

Prints a summary report of the deviation (in micrometers) of the final pin locations from the point of intersection of the net and the partition edge.

For details of the report, see the description of the `assignPtnPin` command in the *Encounter Text Command Reference*.

Default: *Off*

Assign Pins Based on Master Partition Only

Specifies that for designs that have partition clones, the command should consider only the partition master and use the master assignment for all the clones.

Default: *Off*

Follow Routing Completely Without Considering Pin Constraints

Specifies that the pin assignment completely follows the routing results generated by Trial Route, without taking into consideration any pin constraints.

The option can be useful when, for example, you want to compare pin locations based purely on Trial Route results with pin locations that honor the specified pin constraints.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `assignPtnPin`

Related Topics

For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Assigning Pins

DeriveTimingBudget

The Derive Timing Budget form enables you to generate timing budgets.

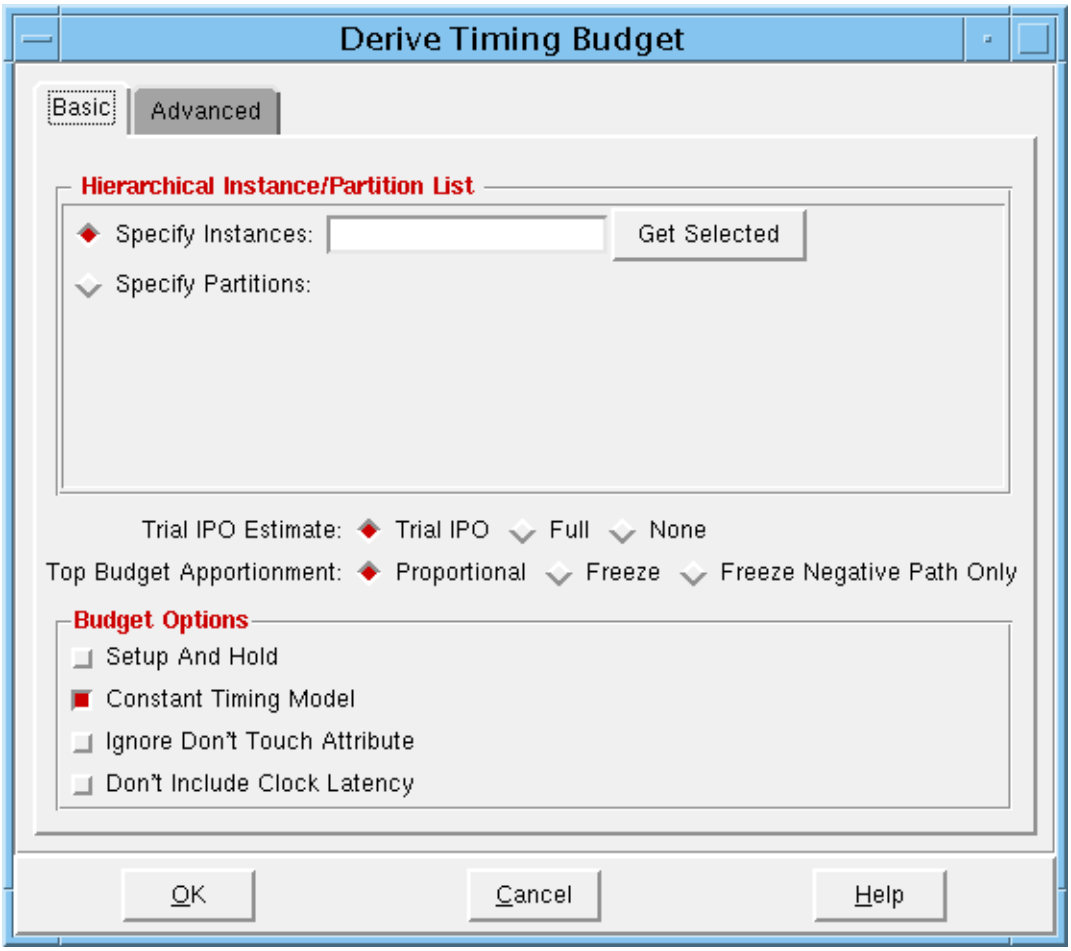
The Derive Timing Budget form has the following pages:

- Derive Timing Budget – Basic on page 520
- Derive Timing Budget – Advanced on page 523

Derive Timing Budget – Basic

Use the *Basic* page of the Derive Timing Budget form to select partition pins and set budgeting options.

➤ Choose *Partition — Derive Timing Budget* and click the *Basic* tab.



Derive Timing Budget – Basic Fields and Options

Hierarchical Instance Solution

Specify Instances	Performs budgeting for the hierarchical instance(s). This instance could be a black box. You can derive timing budgets for black boxes and other instances in the same run. If you select *Merge Master and Clone* from the Derive Timing Budget – Advanced page, the software worst-case budgets based on worst-case data per-pin for specified instances in a master/clone set. If you specify instances from more than one master/clone set, the tool derives separate worst-case timing budgets for the specified instances in each set.
Specify Partitions	Performs budgeting for the specified partition(s). If you select Merge Master and Clone from the Derive Timing Budget – Advanced page, the software obtains worst-case budgets based on worst-case data per-pin for all partitions in the master/clone set containing the partition.
Trial IPO Estimate	Inserts trial IPO fixes when generating the timing budget files. These parameters are used only for trial IPO operation, and the Encounter software does not make actual changes in the design.
Trial IPO	Runs trial IPO operations on all the top-level nets and the section of the path that is within the partition.
Full	Runs trial IPO operations on all the nets in the design.
None	Does not run trial IPO operations.

Top Budget Apportionment

Proportional	Proportions the timing budget for the top-level and the partitions.
Freeze	Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions.
Freeze Negative Path Only	Fixes the top-level timing budget, and proportions the remaining timing budget only for the partitions when the slack is negative.

Budget Options

Constant Timing Model	Creates load-dependent timing models.

Ignore Don't Touch Attribute	Handles don't touch objects as fixed.
Don't Include Clock Latency	Does not include the clock latency in the `set_input_delay` and `set_output_delay` constraints. **Note:** The clock latency is always included if the design has propagated clock(s) irrespective of this option.

Related Text Commands

For information on the following commands, see "Timing Budgeting Commands" in the *Encounter Text Command Reference*.

- `deriveTimingBudget`

Related Topics

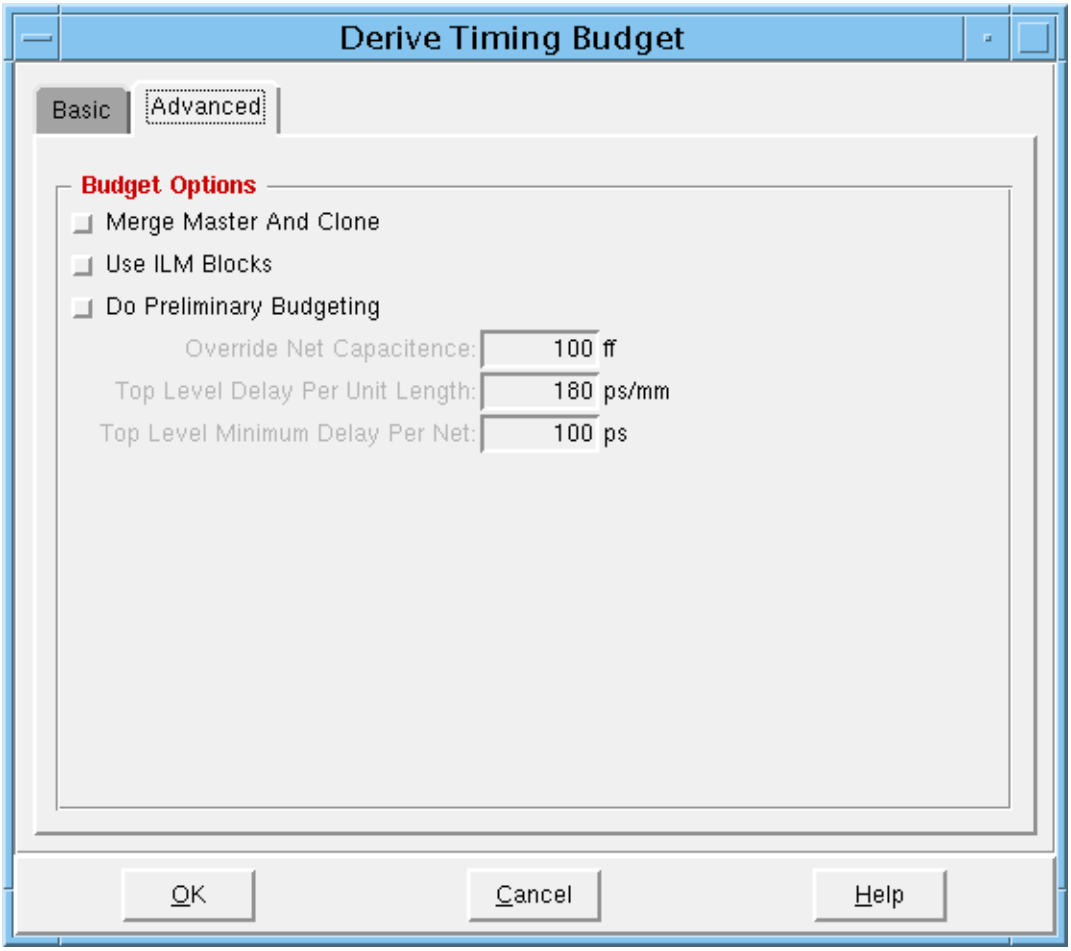
For information on the following topics, see "Timing Budgeting" in the *Encounter User Guide*.

- Deriving Timing Budgets

Derive Timing Budget – Advanced

Use the *Basic* page of the Derive Timing Budget form to specify pin assignment options.

➤ Choose *Partition — Derive Timing Budget* and click the *Advanced* tab.



Derive Timing Budget – Advanced Fields and Options

Merge Master and Clone	Derives a timing budget for hierarchical partitions based on the worst-case data per-pin on the master/clone set containing the partitions. The timing data for the partitions in the master/clone set will be identical, reflecting the worst case among the corresponding pins on the master/clones. You can use this option with the *Specify Instances* or *Specify Partitions* options on the Derive Timing Budget – Basic page. When used with instances, this option derives worst-case budgets for specified instances in a master/clone set. For example, in a master/clone set that includes `instA`, `instB`, and `instC`, if `pin1` has the worst case data on `instA` among pins on `instA`, `instB,` and `instC`, then the software uses the data from `instA/pin1` for `instB/pin1 and instC/pin1`. Similarly, if `pin2` has the worst case data among `instA`, `instB,` and `instC`, then the software uses the data from `instA/pin2` for `instB/pin2` and `instC/pin2`. When used with partitions, this parameter derives worst-case budgets for all partitions in the master/clone set that contains the specified partition.
Use ILM blocks	Derives the timing budget for ILM blocks.
Do Preliminary Budgeting	Derives timing budgets in the early stages of the design to get a preliminary estimate of the budgets. When you use this parameter the software uses the net delays and net loads that you specify using the `setThresholdBudgetThreshold` command. The software does not perform calculations to derive the values for net delay and net load, and does not use trial IPO operations for calculating budgets. The software distributes the positive slack equally between source block, destination block, and top-level. For negative slack, the *Freeze Negative Path Only* option on the Derive Timing Budget – Basic form. For more information, see "Deriving Preliminary Budgets in Early Design Phase" in the "Timing Budgeting" chapter of the *Encounter User Guide*.
Override Net Capacitance	Specifies the lump capacitance value.
Top Level Delay Per Unit Length	Specifies the top-level estimated delay per mm length.

Top Level Minimum Delay Per Net	Specifies the top-level minimum delay per net value.

Related Text Commands

For information on the following commands, see “Timing Budgeting Commands” in the *Encounter Text Command Reference*.

- `deriveTimingBudget`

Related Topics

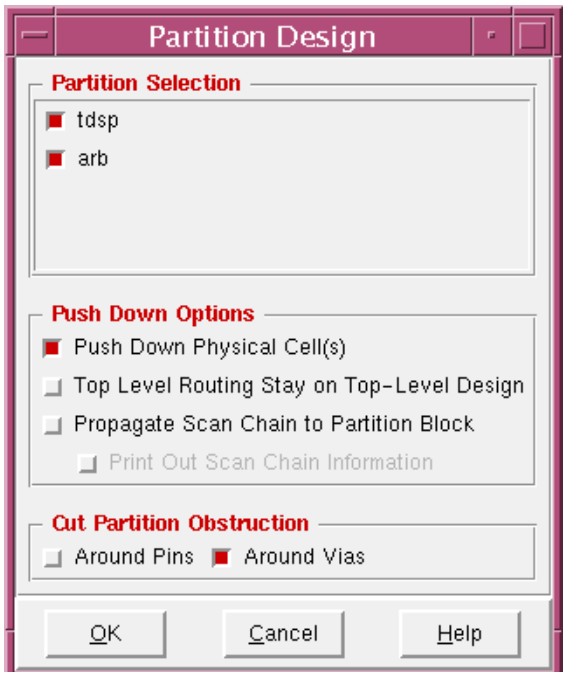
For information on the following topics, see “Timing Budgeting” in the *Encounter User Guide*.

- Deriving Timing Budgets

Commit Partition

Use the Commit Partition form to push down the physical cells to the partition-level design(s).

➤ Choose *Partition — Commit Partition*.



Partition Design – Fields and Options

Partition Selection Specifies the modules to convert to a partition.

Push Down Physical Cells

Specifies that physical only (filler) cells are pushed down into the partition; they are not retained. at the top level.

Default: *Off*

Top Level Routing Stay on Top-Level Design

Specifies that stripes that are not on a layer reserved by the partition are retained at the top level and are also copied into the partition

For more information, see the How Top-level Stripes Are Pushed Down section in the *Encounter User Guide*.

Default: *Off*

Propagate Scan Chain to Partition Block

Specifies that scan chains should be propagated to the partition blocks.

Default: *Off*

Print Out Scan Chain Information

Displays detailed information about the scan chain on the screen and also prints it in the log file.

Default: *Off*

Cut Partition Obstructions Around Pins

Specifies that there are no cuts in the obstructions around pins. You can use this parameter when you want to ensure that the top-level routing can connect the pins without using the space between the pins and the corresponding cover blockages.

Default: *On*

Cut Partition Obstructions Around Vias

Specifies that there are no cuts in the obstructions around vias. You can use this parameter when you want to ensure that the top-level routing can connect the vias without using the space between the vias and the corresponding cover blockages.

Default: *On*

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `Partition`
- `savePartition`

Related Topics

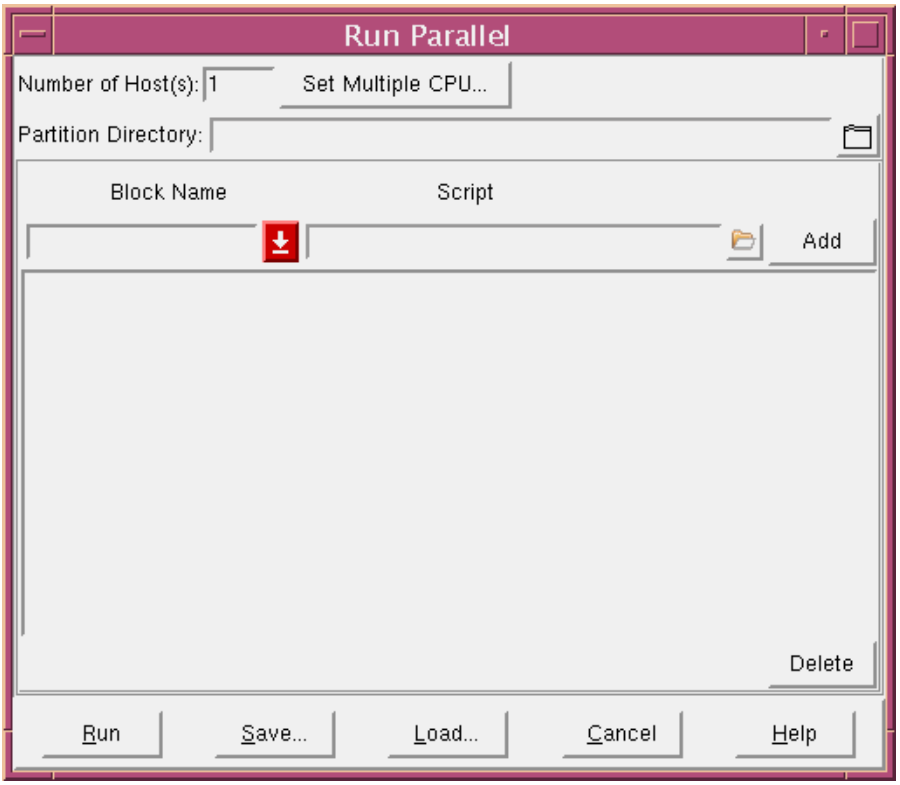
For information on the following topics, see “Partitioning the Design” in the *Encounter User Guide*.

- Running the Partition Program

Run Parallel

Use the *Run Parallel* form to specify job information for parallel runs, such as block working directories and their run scripts. You can also bring up the *Multiple CPU Processing* Form from the *Run Parallel* form.

➤ Choose *Partition — Run Parallel*.



Run Parallel – Partition Fields and Options

Number of Hosts	Displays the currently specified number of hosts.
Set Multiple CPU	Bring up the Multiple CPU Processing form that you can use to set options for multi-threading, distributed processing, and Superthreading. For more information on this form, see Multiple CPU Processing in the “Design Menu” chapter of this document.
Partition Directory	Specifies the directory of the partition.

Block Name	Specifies the block name. Use the pull-down menu to select an available block.
Script	Specifies the location and name of the run script.
Add	Adds the block name and run script to the list.
Delete	Deletes the highlighted block name and run script from the list.

Related Text Commands

For information on the following commands, see “Partition Commands” in the *Encounter Text Command Reference*.

- `setDistributeHost`

Related Topics

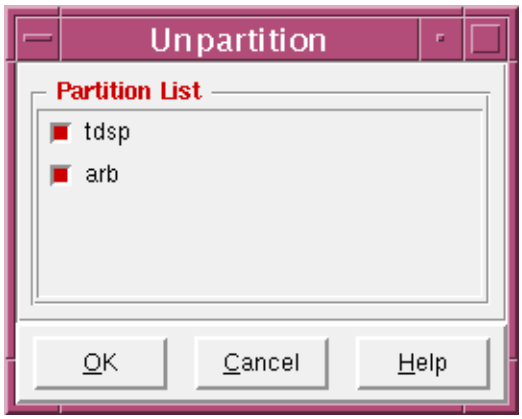
For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

- Parallel Job Distribution

Unpartition

Use the Unpartition form to convert selected partitions in a design back to soft modules. You can use this in sequence with the Partition program to fine tune partition size and shape for top-level routing or block-level implementation.

➤ Choose *Partition – Unpartition*.



Unpartition Fields and Options

Partition List	Specifies the partition(s) to convert back to soft modules. By default, all are selected

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

- `flattenPartition`

Related Topics

For information on the following topics, see “Partitioning the Design” in the *Encounter User Guide*.

- Running the Partition Program
- Unpartitioning with Routing Data

Check Pin Assignment

Use the *Check Pin Assignment* menu command to check whether pin assignment results are valid. A report is output to the Encounter console window. For each partition, it reports whether it has passed the pin checking. If it does not pass, the report indicates the number of pins that are unassigned. This is useful when working with the Pin Editor.

➤ Choose *Partition – Check Pin Assignment*.

Related Text Commands

For information on the following command, see “Partition Commands” in the *Encounter Text Command Reference*.

■ `checkPinAssignment`

Related Topics

For information on the following topic, see “Partitioning the Design” in the *Encounter User Guide*.

■ Assigning Pins

Change Partition View

Use the *Change Partition View* menu command to toggle the design display area view between the selected partition and the top-level design.

Tip

This command is only for viewing and examining into the partition. Real work that is to be done in a partition must be done in the created partition directories, which were created when saving the partitions.

➤ Highlight a partition in the design display area and choose *Partition – Change Partition View*.

Related Text Commands

There are no related text commands. This feature is available only through the *Partition* menu.

6

Floorplan Menu

- Specify Floorplan on page 536
- Specify BlackBlob on page 543
- Automatic Floorplan on page 554
- Resize Floorplan on page 582
- Relative Floorplan on page 588
- FlipChip on page 581
- Create Physical Hierarchy on page 614
- Connect Global Nets on page 616
- Edit Floorplan on page 620
- Check Floorplan on page 646
- Generate FP Guide on page 648
- Generate Regrouped Netlist on page 650
- Group Pin(s) Move on page 652
- Swap Two Selected I/O Cells on page 654
- View Relative Floorplan Through Context Menu on page 655
- Flip Hierarchical Instances on X-axis or Y-axis on page 656

Specify Floorplan

Use the Specify Floorplan form to view or change your floorplan specifications after importing the design. Use this form to specify the dimensions by size; or by die, I/O, or core coordinates.

When you use the Specify floorplan form (or specify the floorplan through the `floorplan` command), the floorplan is resized automatically—relatively floorplan constraints are automatically derived on the fly for blocks, fixed standard cells, fixed pre-routes, and blockages.

The floorplan is linearly adjusted as follows:

- Spacing among blocks is evenly adjusted.
- The size of the modules and black boxes is evenly adjusted.
- The fixed pre-routes and I/Os are automatically adjusted.

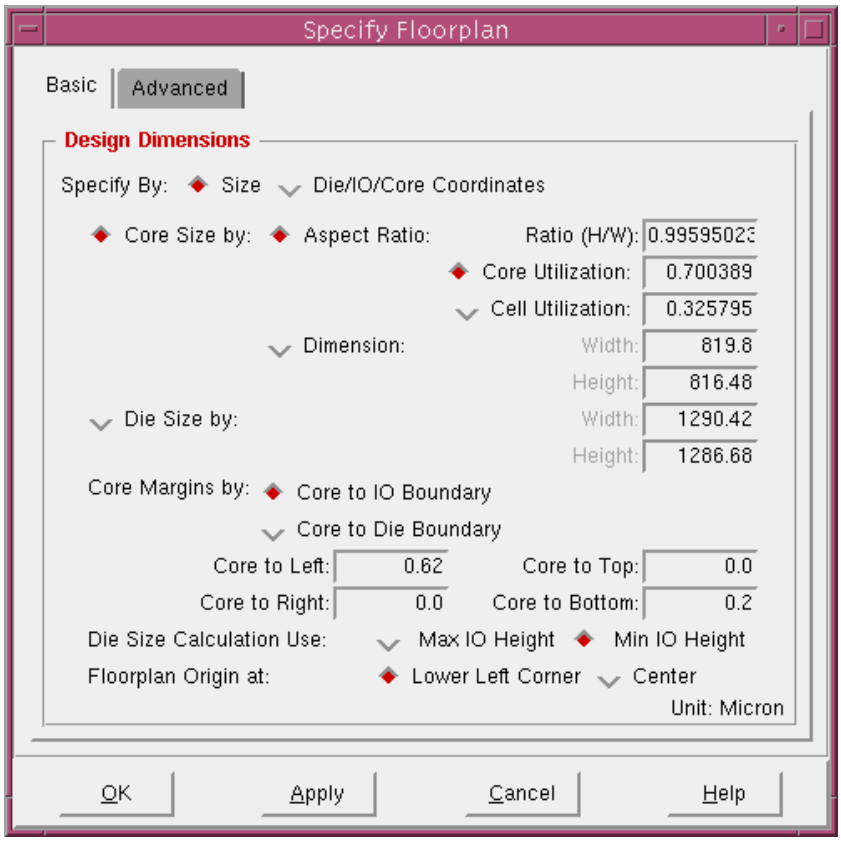
The Specify Floorplan Plan consists of the following two pages:

- Specify Floorplan – Basic
- Specify Floorplan – Advanced

Specify Floorplan – Basic

Use the *Specify Floorplan – Basic* form to specify the design dimensions.

➤ Choose *Floorplan – Specify Floorplan*, and then click the *Basic* tab.



Specify Floorplan – Fields and Options

Size	Specifies that the design dimensions are specified by size. If you select this option, specify the details in *Core Size* or *Die Size* fields.
Die/IO/Core coordinates	Specifies that the design dimensions are specified by die, I/O, or core coordinates. Specify the Die/IO/Core lower left (ll) and upper right (ur) coordinates in the fields that are displayed if you select this option.

Core Size by

Specifies the core size dimension definition.

Aspect Ratio defines the chip's core dimensions as the ratio of the height divided by the width. If a value of 1.0 is used, a square chip is defined. A value of 2.0 will define a rectangular chip with height dimension that is twice the width dimension.

Choose one of the following ways of determining core and module sizes:

Core Utilization determines the core and module sizes by total standard cells and macros density.

Cell Utilization determines the core and module sizes by standard cell density.

For more information on total density versus standard cell density calculation, see Calculating Density in the *Encounter User Guide*.

Width and Height specifies the core's width and height values, in micrometers.

Die Size by: Width and Height

Specifies the design's die size, in micrometers.

Core Margins by

Specifies the core margin dimension definition. Choose one of the following:

Core to IO Boundary uses the spacing, in micrometers, between the core edge and the I/O box, which is the margin between the outside edge of the core box and the inside edge of the I/O box. The margin values and the height of the I/O pad instances determines the die size. You can specify the margins on all four sides: *Core to Left*, *Core to Bottom*, *Core to Right*, and *Core to Top*.

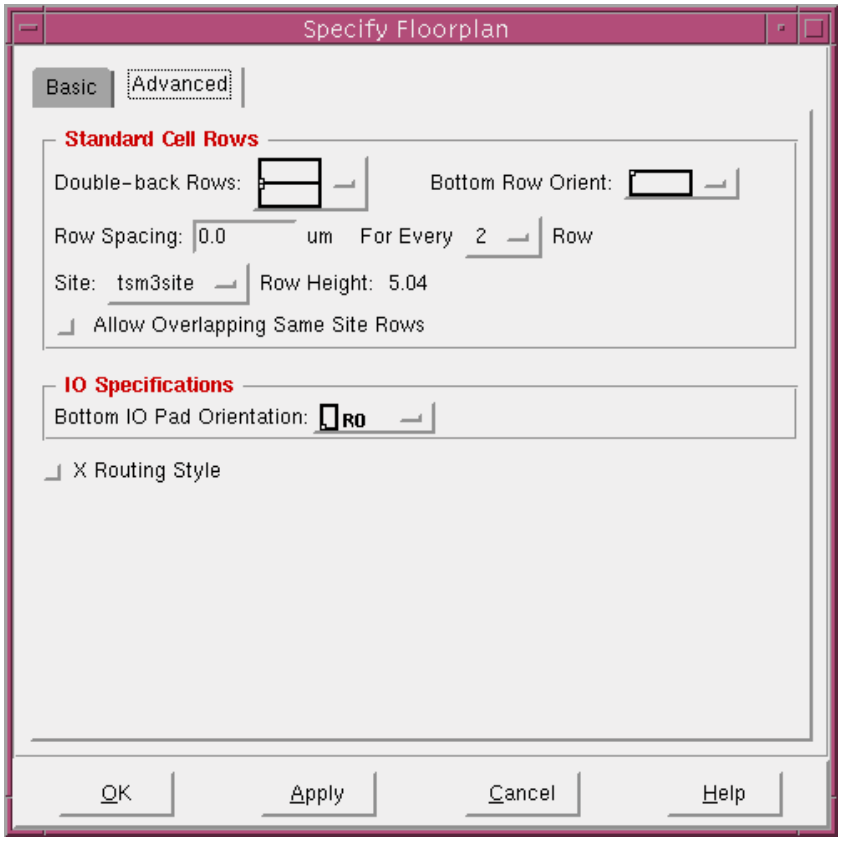
Core to Die Boundary uses the spacing, in micrometers, between the core edge and the die edge, which is the margin between the outside edge of the core box and the inside edge of the die (head) box. This sets the die size once the core size is calculated. You can specify the margins on all four sides: *Core to Left*, *Core to Bottom*, *Core to Right*, and *Core to Top*.

Die Size Calculation Use	Specifies the die size and I/O box calculation when using *Core Margins by*. The height of the I/O pad instance determines the final die size calculation. Choose one of the following: *Max I/O Height* uses the tallest height I/O pad instance dimension to calculate the die size. *Min I/O Height* uses the shortest I/O pad instance dimension to calculate the die size.
Floorplan Origin at	Specifies the floorplan's origin. Choose one of the following: *Lower Left Corner* when loading a design that has its origin at the lower left. All files saved or output will reference the origin selection. *Center* when loading a design that has its origin at the center of the core.

Specify Floorplan – Advanced

Use the *Specify Floorplan – Advanced* form to specify the standard cell rows and bottom I/O pad orientation.

➤ Choose *Floorplan – Specify Floorplan*, and then click the *Advanced* tab.



Specify Floorplan – Advanced Fields and Options

Row Direction

Specifies whether the rows are horizontal or vertical.

Note: Support for vertical rows is a beta feature. Usage and support of this beta feature are subject to prior agreement with Cadence. Contact your Cadence representative if you have any questions.

Double-back Rows

Allows the selection of standard cell row pair orientations. The orientation selections for the row pair are bottom-to-bottom or top-to-bottom. The default is bottom-to-bottom orientation.

Bottom Row Orient

(*Bottom/Left Row Orient*, if vertical row support is enabled)

Specifies the orientation of the bottom/left row in the core area. The default is an `R0` orientation, or you can choose the `MX` orientation (mirrored through the x axis) for horizontal rows or MY orientation for vertical rows.

Note: Support for vertical rows is a beta feature. Usage and support of this beta feature are subject to prior agreement with Cadence. Contact your Cadence representative if you have any questions.

Row Spacing for Every # rows

Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pull-down menu, specify *1* for every row, or *2* for every other row.

Site Name

Specifies a core row site. The tech site names listed in the pull-down menu come from the *LEF Files* field of the Design Import form.

Row height

Specifies the standard cell row height, in micrometers. During design import, the standard cell row height is automatically determined.

Allow overlapping same site rows

If selected, specifies that same-site rows can overlap with one another. If deselected, specifies that same-site rows cannot overlap with one another.

Single height rows must not overlap. Only double- or multiple-height rows can overlap. The overlap must be in sections that are multiple of single height—any other overlap section size will result in the rows being ignored.

Bottom IO Pad Orientation	Specifies an orientation of *R0* (default), *R90*, *R180*, and *R270*. If the bottom I/O pad orientation is changed, the other three sides will also change. The west side is rotated 90 degrees counterclockwise from the bottom I/O pad orientation; the north side is rotated 180 degrees counterclockwise from the bottom I/O pad orientation; and the east side is rotated 270 degrees counterclockwise from the bottom I/O pad orientation. The default orientation of the bottom I/O pad instance is *R0*; however, during design import, the software approximates the I/O pad orientation.
X Routing Style	Specifies that the design has X routing. *Important* X Routing Style is obsolete and will be removed in the next major release of the software.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `floorPlan`
- `setBottomIoPadOrient`
- `setFlipping`
- `setFPlanRowSpacingAndType`

Related Topics

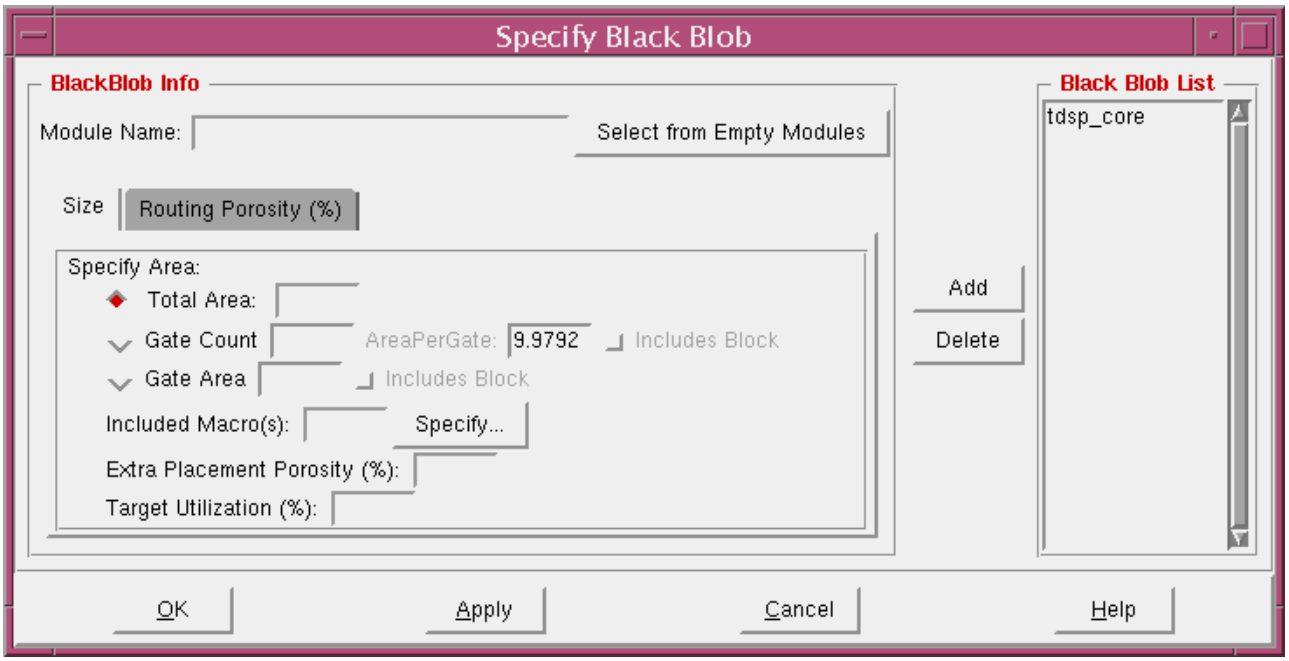
For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Viewing the Floorplan

Specify BlackBlob

Use the Specify BlackBlob form to create a new blackblob.

➤ Choose *Floorplan – Specify Floorplan*.



Specify BlackBlob – Fields and Options

Module Name

Specifies the name of the cell that should be specified as a blackblob.

You can specify empty Verilog modules by clicking the *Select from Empty Modules.*

Select from Empty Modules

Displays the *Select Empty Module* form, in which you can choose from the available empty Verilog modules.For more information, see Select Empty Module on page 544.

Size tab

Use the *Specify BlackBlob Size* form to specify the area, placement porosity, macros to include, and target utilization for the blackblob. For more information, see Specify BlackBlob Size on page 547.

Routing Porosity tab	Use the *Specify BlackBlob Routing Porosity* form to specify the routing resources, per layer, that will be reserved for the blob. For more information, see Specify BlackBlob Routing Porosity on page 552.
Add	Adds the name of the module specified in the *Module Name* field to the *BlackBlob List*
BlackBlob List	Displays a list of the modules that will be specified as blackblobs when you click *OK* or *Apply*. When you click *Add*, the module specified in the Module List is added to the *BlackBlob List*. You can thus specify multiple blackboxes as follows: **1.** Specify a name for the module in the *Module Name* field. **2.** Specify the fields and options in the *Size* tab. For more information, see Specify BlackBlob Size on page 547. **3.** Optionally, specify the fields and options in the *Routing Porosity* Tab. For more information, see Specify BlackBlob Routing Porosity on page 552. **4.** Click *Add*. The module is added to the *BlackBlob List* **5.** Repeat steps 1 to 3 for each blackblob you want to specify. **6.** Click OK or Apply. All the blackboxes in the Blackblob list are created. **Note:** Clicking the Apply button does not run the `elaborateBlackBlob` command, but clicking the OK button does. The `elaborateBlackBlob` command instantiates the hard macros in a blackblob and completes the virtual connections for these hard macros. The blackblobs are also filled with dummy instances as per the size/area specified.
Delete	To delete a macro from the *BlackBlob List*, select the macro in the *BlackBlob List,* and click *Delete*.

Select Empty Module

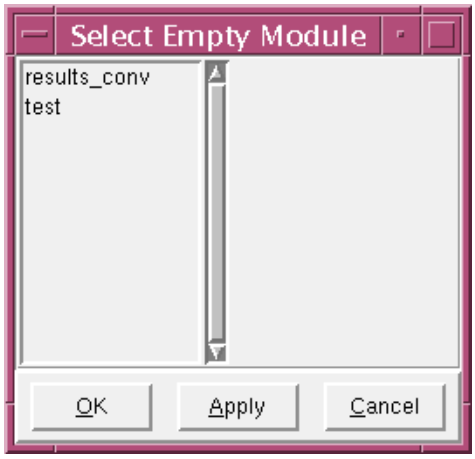
The Select Empty Module form displays the list of empty Verilog Modules that you can use as a blackblob module.

Important

To have the list of empty modules available in the GUI, add the following line to the configuration file:

```
set rda_Input(import_mode) {-treatUndefinedCellAsBbox 0 -keepEmptyModule 1
-useLefDef56 1}
```

➤ In the Specify BlackBlob form, click *Select Empty Module*.



A list of the available empty Verilog modules is displayed. Select the module that you want to use as a blackblob module, and then click *OK* or *Apply*.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `convertBlobInstToModule`
- `convertBlobModuleToInst`
- `elaborateBlackBlob`
- `loadBlackBlobNetlist`
- `specifyBlackBlob`
- `unspecifyBlackBlob`

Related Topics

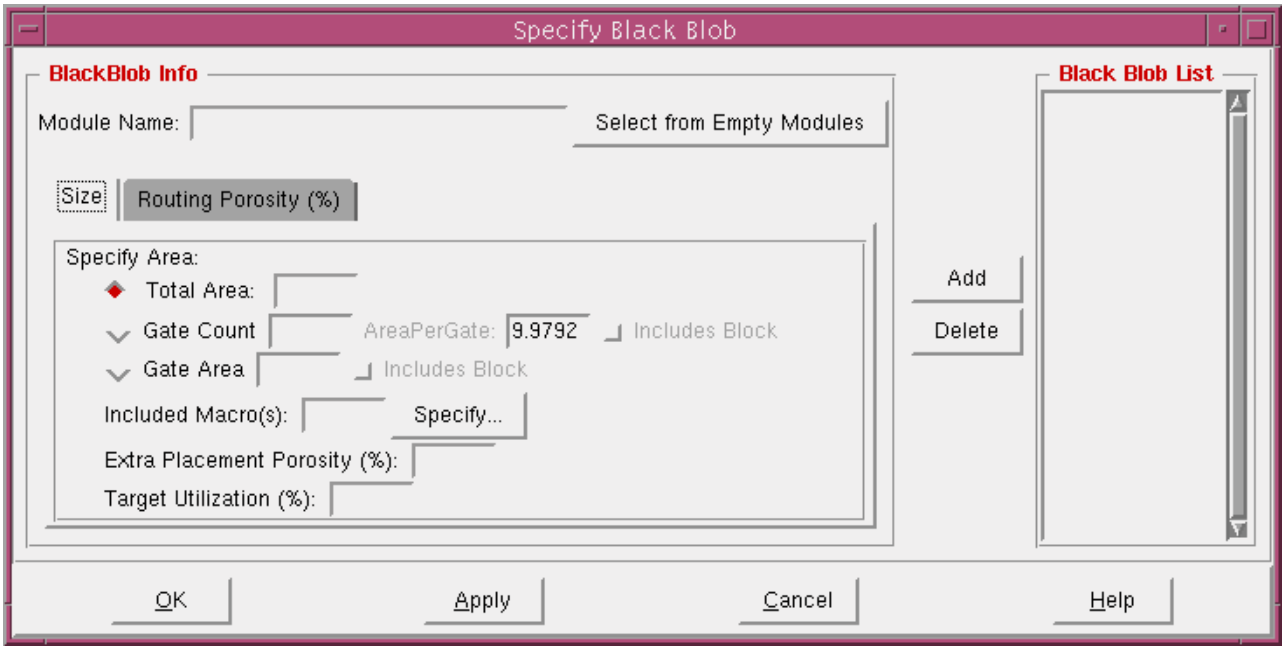
For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Using Blackblobs

Specify BlackBlob Size

Use the *Specify BlackBlob Size* form to specify the area, placement porosity, macros to include, and target utilization for the blackblob.

➤ Choose *Floorplan – Specify Black Blob*, and then click on the *Size* tab.



Specify BlackBlob Size – Fields and Options

Specify Area — Select one of the following options:

- *Total Area* — Specifies the area of the blackblob. Use this option when you want to specify the area of the blackblob, instead of gate area or gate count and area per gate.

- *Gate Count*
- *AreaPerGate*

  Specify, respectively, the gate count, area per gate, and whether the area of any hard macros present in the blackblob should be included in the total gate area.

- *Include Block*

  If you select the *Include Block* checkbox, the gate area will be calculated as follows:

  ```
  (gate count) * (area per gate)
  ```

  If you do not select the *Include Block* checkbox, the gate area will be calculated as follows:

  ```
  {(gate count) * (area per gate)} + area
  of specified macro(s)
  ```

- *Gate Area*

  Gate Area specifies the total area of the gate, which is equal to the gate count multiplied by the area per gate.

- *Include Block*

  Include Block specifies whether the gate area includes the gate areas of any hard macro(s) present in the design.

  If you do not select the *Include Block* checkbox, the final gate area for the blackblob is derived by adding the area of the hard macro(s) to the gate area specified in the *Gate Area* field.

  If you select the *Include Block* checkbox, the specified gate area also includes the area of the specified hard macro(s).

Include Macro(s)

Specifies the hard macro(s) to include in the blackblob. Enter the name of the macro followed by the number of times the macro will be instantiated in the blackblob. You can specify multiple blackblobs. For example, to specify the macro `ram_128x16A` two times and the macro `pllcl` one time, enter the following in the *Include Macros* field:

```
ram_128x16A 2 pllcl 1
```

You can also select the macros from a list of available macros. For this, click the *Specify...* button and enter the details in the Specify Blob Macros form that appears. For more information, see Specify Blob Macros on page 550.

Extra Placement Porosity (%)	Specifies the percentage of cell area that will be added to the blob area during placement. This area allows IPO cells to be placed over the blob area. A placement porosity of 0 implies that the blob area after placement is the same as the blob area before placement.
Target Utilization (%)	Specifies the target utilization for the blackblob. This option can be used to reduce congestion.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `convertBlobInstToModule`
- `convertBlobModuleToInst`
- `elaborateBlackBlob`
- `loadBlackBlobNetlist`
- `specifyBlackBlob`
- `unspecifyBlackBlob`

Related Topics

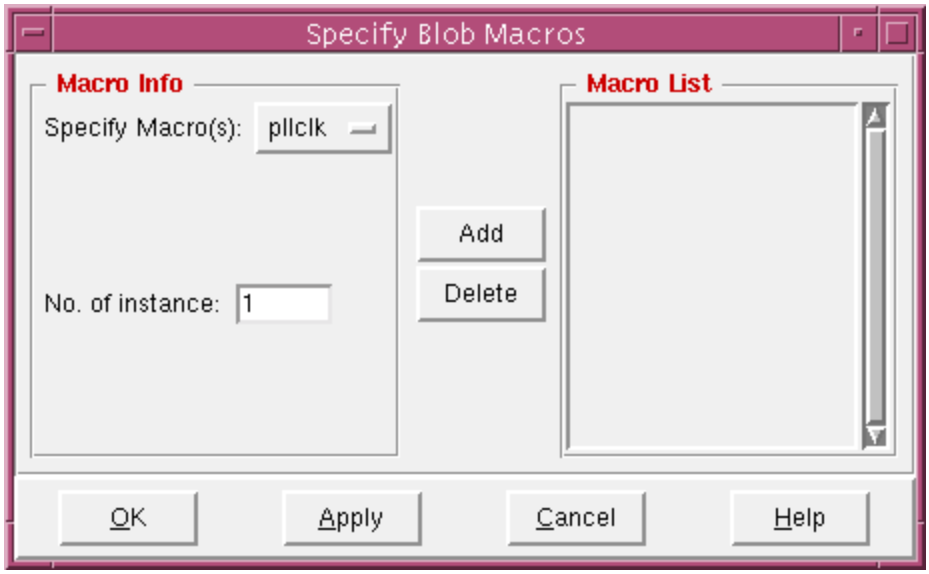
For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Using Blackblobs

Specify Blob Macros

Use the *Specify Blob Macros* form to select, from a list of available macros, the macros to include in the blackblob.

➤ Choose *Floorplan – Specify Black Blob*, and in the *Size* tab, click the *Specify...* button next to the *Include Macros* field.



Specify Blob Macro – Fields and Options

Specify Macro(s)	Specifies the name of the macro from a list of the available macros.
No. of instance	Specifies that number of times the macro is instantiated in the design.
Add	Adds the macro selected in the *Specify Macro* field to the list of macros to include in the blackblob.
Macro List	Displays the list of macros that will be added to the blackblob. When you select a macro from the Specify Macro list and click *Add*, the macro is added to the Macro List.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `convertBlobInstToModule`
- `convertBlobModuleToInst`
- `elaborateBlackBlob`
- `loadBlackBlobNetlist`
- `specifyBlackBlob`
- `unspecifyBlackBlob`

Related Topics

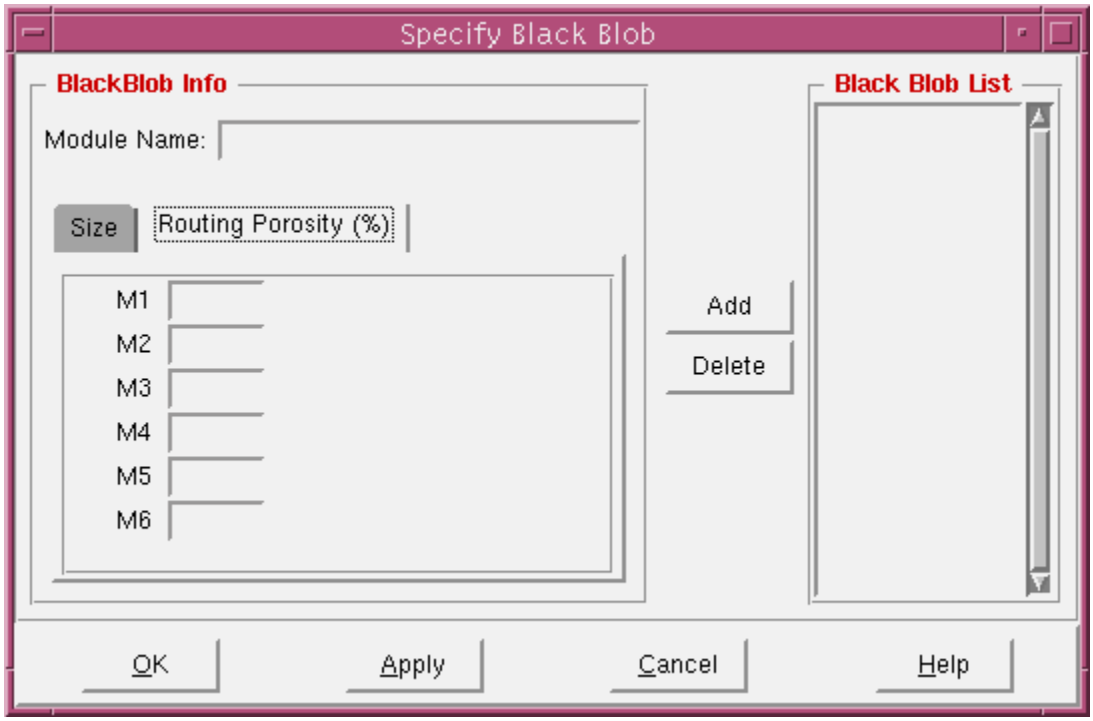
For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Using Blackblobs

Specify BlackBlob Routing Porosity

Use the *Specify BlackBlob Routing Porosity* form to specify the routing resources, per layer, that will be reserved for the blob.

➤ Choose *Floorplan – Specify BlackBlob*, and then click the *Routing Porosity (%)* tab.



Specify BlackBlob Routing Porosity Fields and Options

Module Name	Specifies the name of the blackblob module.
■ *M1* ■ *M2* ■ *M3* ■ *M4* ■ *M5* ■ *M6*	Specifies the routing resources, in percentage, that will be reserved for the blob on the M1, M2, M3, M4, M5, and M6 layers, respectively. Default: The default value is 0%.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `convertBlobInstToModule`
- `convertBlobModuleToInst`
- `elaborateBlackBlob`
- `loadBlackBlobNetlist`
- `specifyBlackBlob`
- `unspecifyBlackBlob`

Related Topics

For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Using Blackblobs

Automatic Floorplan

The Automatic Floorplan menu provides the following forms and menu commands for running the Masterplan automatic floorplanner features:

- Plan Design on page 555
- Refine Macro Placement on page 564
- Finish Floorplan on page 566
- Report Plan Design on page 568
- Multi Plan Design on page 569
- Module Colors on page 580

Plan Design

The Plan Design form enables you to set the Masterplan automatic floorplanner global parameters, and run Masterplan to generate quick, initial floorplans.

The Plan Design form includes the following pages:

- Plan Design – planDesign on page 556
- Plan Design – setPlanDesignMode on page 558

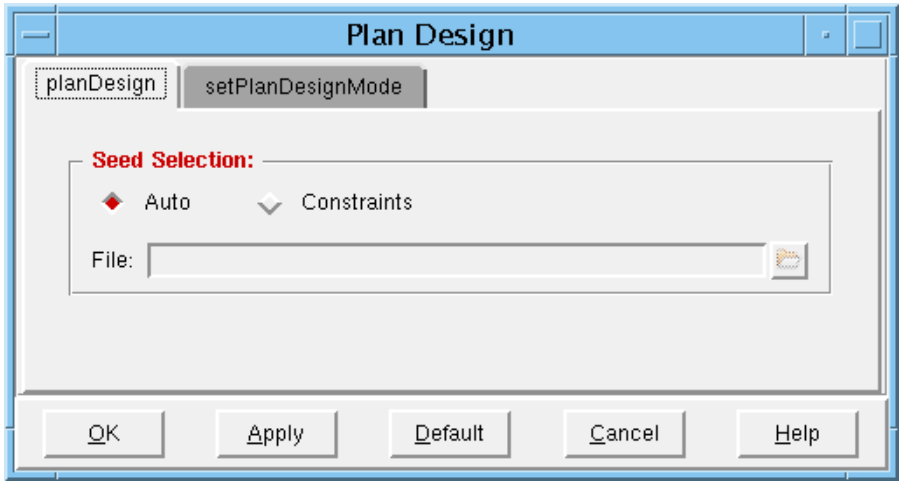
Plan Design – planDesign

Use the *planDesign* page to generate a quick, initial floorplan that can be used as a starting point for making the final floorplan. Use Masterplan to create multiple floorplans. You can then test the floorplans to find the one that gives you the best placement and routing results.

When you click *OK*, Masterplan performs the following internal functions in order:

- Selects the floorplan objects (called seeds) to be placed.
- Places the seeds.
- Refines the seeds.
- Places the macros.

➤ Choose *Floorplan – Automatic Floorplan – Plan Design*.



Fields and Options

Auto

Performs automatic seed selection. Masterplan selects seeds using the following methods in the specified order:

- Chooses modules that fit an internally calculated size range
- Chooses large hard macros as seeds
- Groups small modules or single standard cells to fit an internally calculated size range

Default: On

Constraints	Uses the constraints set in the specified Masterplan constraint file for fence creation, macro placement and module guide generation. A constraint file is a text file that can contain a list of seeds for Masterplan to use when generating fences and module guides, and basic relative, spacing and orientation constraints to follow during macro placement. For more information, see "Masterplan Constraint File Format." *Default:* Off
File	Specifies the name a constraint file.

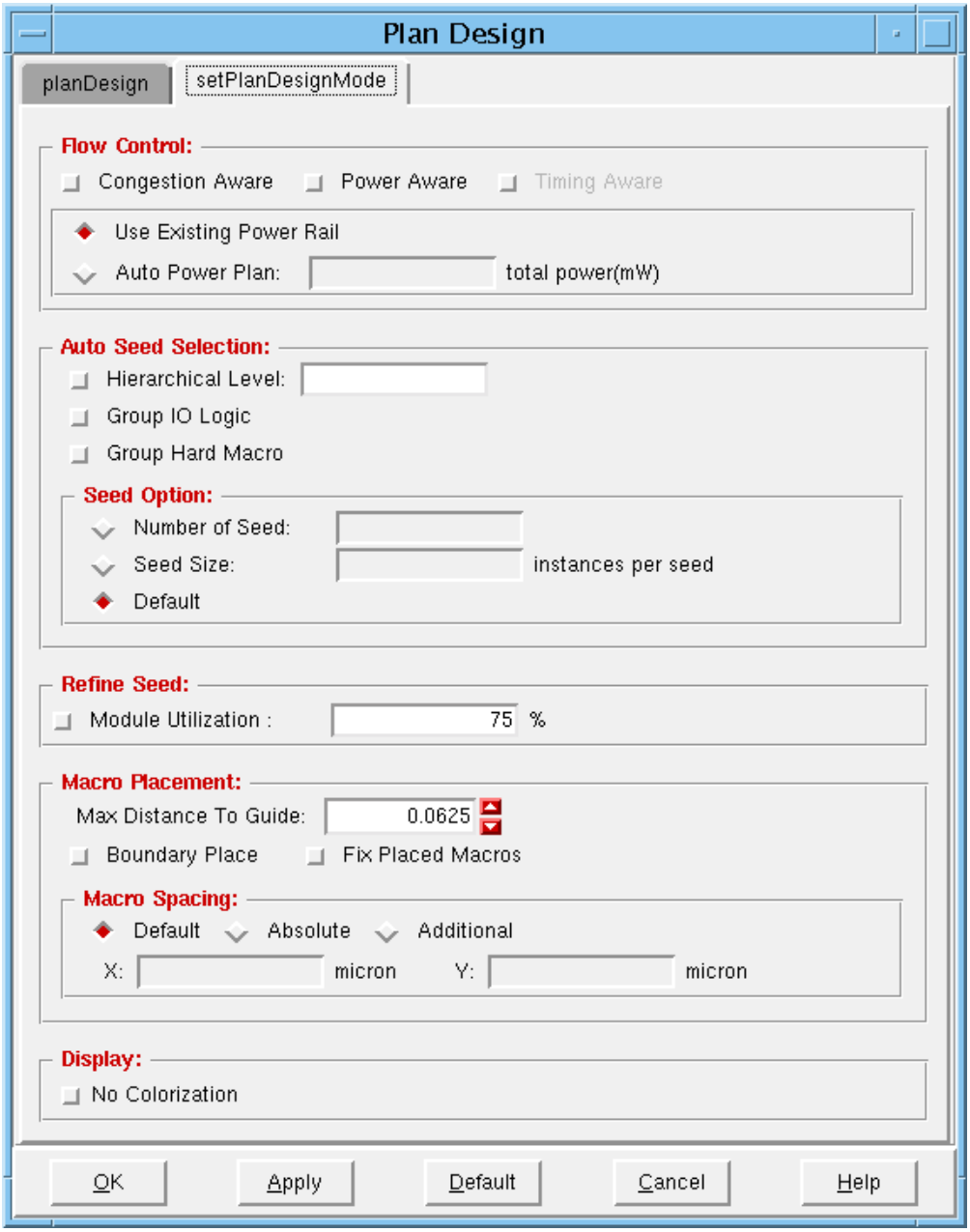
Related Text Commands

- `planDesign`
- `setPlanDesignMode`

Plan Design – setPlanDesignMode

Use the *setPlanDesignMode* page of the Plan Design form to set the Masterplan automatic floorplanner global parameters. Parameters specified with the *setPlanDesignMode* page are then used whenever you run Masterplan to create an initial floorplan.

➤ Choose *Floorplan – Automatic Floorplan – Plan Design*, and click the *setPlanDesignMode* tab.



Fields and Options

Congestion Aware

Estimates the congestion for the floorplan after macro placement.

If congestion (the Trial Route estimated Gcell overflow percentage) is greater than 0.5 percent in either the X or Y direction, Masterplan attempts to resolve it by refining the macro placement (such as changing the spacing, orientation, or grouping). Masterplan does not touch user-preplaced macros during this refinement. After re-estimating the congestion, if the congestion improved, Masterplan keeps the new floorplan. If congestion did not improve, Masterplan restores the previous floorplan.

If you select the *Auto Power Plan* option with *Congestion Aware*, the automatic power planner generates a power plan that Masterplan takes into consideration when estimating and resolving congestion.

If you select the *Use Existing Power Rail* option with *Congestion Aware*, Masterplan uses the existing power routing when estimating and resolving congestion.

Note: For better accuracy, it is recommended that you have power information available, to use this feature.

Default: Off

Power Aware

Performs IR drop analysis after macro placement, and displays an IR drop map.

If you select the *Auto Power Plan* option with *Power Aware*, the automatic power planner generates a power plan that Masterplan uses for IR drop analysis.

If you select the *Use Existing Power Rail* option with *Power Aware*, Masterplan uses the existing power routing for IR drop analysis.

The following conditions exist for this parameter:

- For better accuracy, it is recommended that you have power information available, to use this feature.
- Masterplan currently analyzes only one power net by default (the one with the most instance connections).
- The default threshold for the IR drop map is 5 percent of the main power supply voltage.

Default: Off

Use Existing Power Rail

Uses the existing power routing in the design for estimating congestion, or performing basic power analysis.

Default: On

Auto Power Plan

Calls the automatic power planner to generate a generic power plan after macro placement, based on the specified total average power value. You can use this power plan for estimating congestion, or performing basic power analysis.

The following conditions exist for this parameter:

- To use *Auto Power Plan* for a chip design, the power pads must already be placed in the design.
- The global power net connection must be defined.
- The *Auto Power Plan* feature uses the default template for power planning.

Default: Off

Hierarchical Level

Forces automatic seed selection to select all hierarchical instances at the specified logic level as seeds. The top design cell is at hierarchy level 0.

Select this option only when you want to bias the seed selection process to favor hierarchy when selecting seeds. To use this option, your hierarchy levels should be very well defined and organized.

Default: Off

Group IO Logic

Creates instance group seeds by traversing the logic from the I/O pads (or pins) to the first level of sequential elements. When you select this option, Masterplan creates a maximum of eight instance group seeds (two on each side), depending on the design size.

Note: You must have a timing library specified in order to use this option.

Default: Off

Group Hard Macro

Controls the selection of hierarchical instances as seeds, based on hard macro distribution. When you select this option, if hierarchical instances at a certain hierarchy level contain the same types of macros, Masterplan chooses their common parent hierarchical instance as a seed.

Default: Off

Seed Option

Forces automatic seed selection to favor certain constraints during the seed selection process.

Number of Seed

Forces automatic seed selection to select approximately the specified number of seeds. For most designs, the optimal number of seeds to select is between 20 to 50. You should not select fewer than 10 seeds, or more than 100.

The total number of seeds actually selected by the tool can be within a range of plus or minus 5 of the specified number.

Select this option only when you want to bias the seed selection process to favor seed number when selecting seeds.

Default: Off

Seed Size

Forces automatic seed selection to use the specified size (in terms of area) as the basic seed size when grouping instances.

Select this option only when you want to bias the seed selection process to favor seed size when selecting seeds.

Default: Off

Default

Uses the default automatic seed selection method for seed selection. By default, Masterplan selects seeds using the following methods in order:

- Chooses modules that fit an internally calculated size range
- Chooses large hard macros as seeds
- Groups small modules or single standard cells to fit an internally calculated size range

Default: On

Max Distance To Guide

Restricts macro placement to an area that is relative to the macro's associated guide boundary. Specify a value that is between `0` and `1`.

Default: `0.0625` (1/16)

Boundary Place

Places macros along the core boundary for chip and block designs. Macros are placed along the fence boundary for hierarchical floorplans. Preplaced hard macro boundaries are also used, if possible.

Note: Selecting this option can disable the *Max Distance To Guide* option. Seed locations might also be ignored.

Fix Placed Macros

Marks all placed macros as `FIXED` after running Masterplan. Marking the macros as `FIXED` prevents them from accidentally being moved when the design is placed.

Default: Off

Macro Spacing

Specifies the spacing between adjacent hard macros. Use one of these options to add space, in order to decrease congestion between hard macros.

Default: Default

Default

Uses the following default spacing:

$(25 + num_pin_on_edge/8) \times M2_pitch$

Absolute

Specifies the absolute spacing between adjacent hard macros.

Additional

Specifies extra spacing to add to the default spacing between adjacent hard macros.

X/Y:

Specifies the horizontal and vertical absolute or additional spacing, in microns.

Type: Float

No Colorization

Does not color the module guides and macros in the resulting floorplan.

Default: off

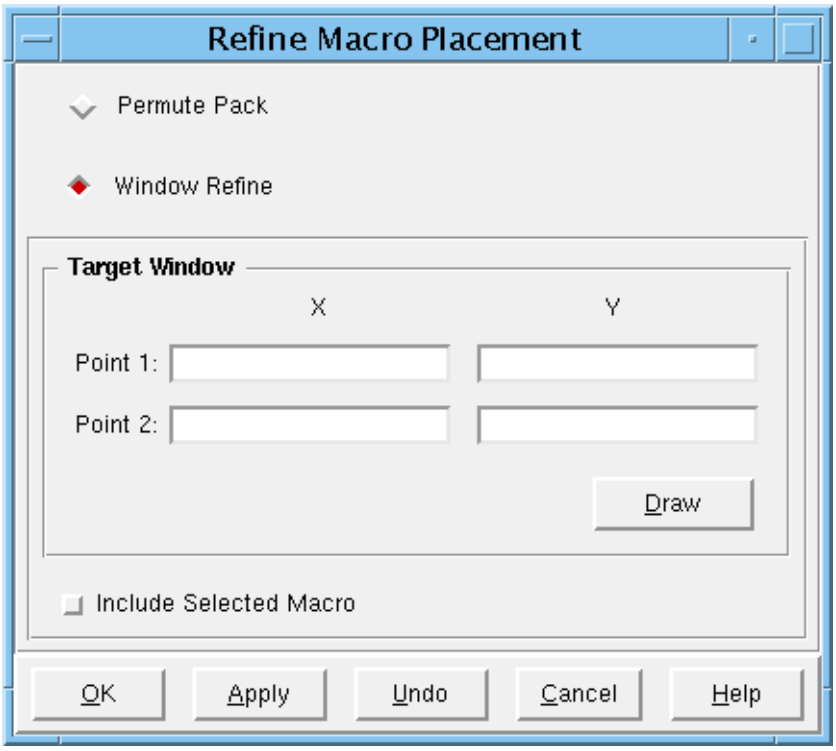
Related Text Commands

- `setPlanDesignMode`
- `planDesign`

Refine Macro Placement

Use the Refine Macro Placement form to adjust the placement of macros in the floorplan. You can adjust specific macro packs, or all of the macros in a specific area of the design.

➤ Choose *Floorplan – Automatic Floorplan – Refine Macro Placement*.



Fields and Options

Permute Pack	Adjusts the placement of a selected pack of macros to reduce empty area between them. A pack is a set of macros from the same seed that have similar sizes and aspect ratios and have been grouped together. **Note:** You must select the macro pack in the main window before using this option. You can select one macro to select the entire pack.
Window Refine	Adjusts the placement of any macros within a specified area (*Target Window*) to reduce empty area between them.

Target Window — Creates a box in the design window. Masterplan adjusts any macros within the specified area to reduce empty area between them.

- *Point 1 X/Y* — Specifies the coordinates of one corner of the box. This corner can be the lower-left, upper-left, lower-right, or upper-right corner of the box.
- *Point 2 X/Y* — Specifies the opposite corner of the box.
- *Draw* — Enables you to physically draw the box in the design window.

  The coordinates for where you start drawing the box populate the text fields for *Point 1*. The coordinates for where you finish drawing the box populate the text fields for *Point 2*.

Include Selected Macro — Moves the selected macros to the *Target Window* area, and adjusts their position along with any macros already within the area.

Note: You must select one or more macros in the main window before using this option.

Related Text Commands

- `refineMacro`

Related Topics

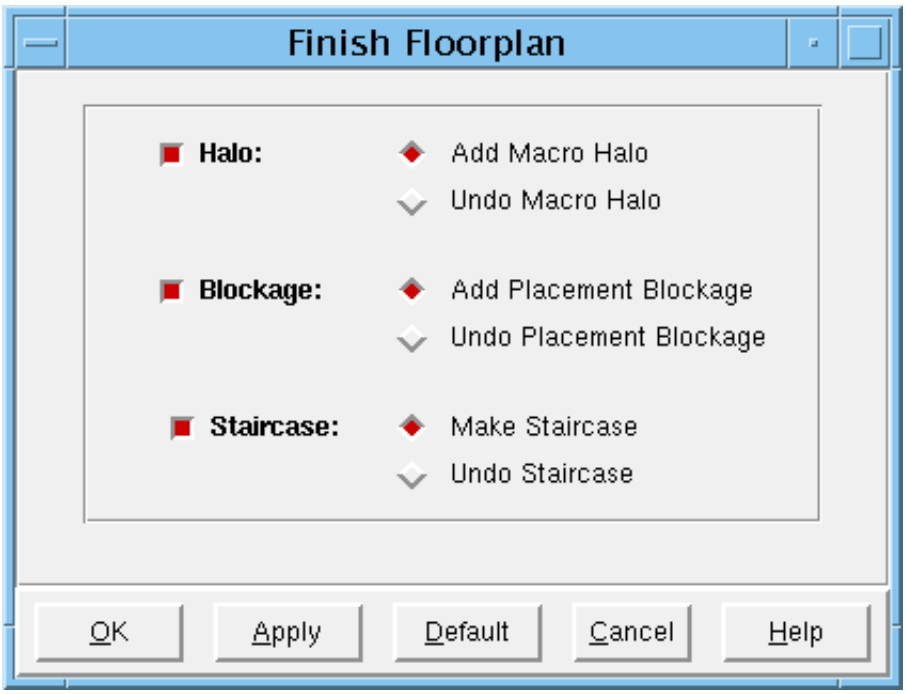
- Adjusting Macro Placement

Finish Floorplan

Use the Finish Floorplan form to perform advanced placement-related refinements to a floorplan, to produce a more polished floorplan.

The Finish Floorplan form (with the exception of the *Staircase* option), can be used on any floorplan, including third-party generated floorplans.

➤ Choose *Floorplan – Automatic Floorplan – Finish Floorplan*.



Fields and Options

Halo

Add Macro Halo

Adds placement halos to macro boundaries. For each macro edge, the halo thickness is proportional to pin density on that edge.

Undo Macro Halo

		Reverses the previous *Add Macro Halo* operation. When specified, the software restores the floorplan to the state it was in before the last *Add Macro Halo* was performed. Any other refinement operations that were performed remain the same.
Blockage	*Add Placement Blockage*	
		Adds partial (50 percent) placement blockages around macros to reduce potential congestion after placement.
	Undo Placement Blockage	
		Reverses the previous *Add Placement Blockage* operation. When specified, the software restores the floorplan to the state it was in before the last *Add Placement Blockage* was performed. Any other refinement operations that were performed remain the same.
Staircase	*Make Staircase*	Adjusts the macro sequence by size to smooth out the macro-to-core interface, creating a “staircase” pattern. You can specify this option only on floorplans that were created using Masterplan in the current session. Macros must be marked as `PLACED`, in order to use this option.
	Undo Staircase	Reverses the previous *Make Staircase* operation. When specified, the software restores the floorplan to the state it was in before the last *Make Staircase* was specified. Any other refinement operations that were performed remain the same.

Related Text Commands

- `finishFloorplan`

Report Plan Design

Use the Report Plan Design menu command to generate a quality of results report for the floorplan you created.

You can use this command to generate reports for each floorplan you create, then compare the reports to gauge which floorplan will give you the best placement and routing results.

The report includes statistics on the following items:

- Out-of-core macros and module guides
- Crossing nets between module guides, and guides to I/Os
- Wire crossings over macros and module guides
- Wire length between module guides, and guides to I/Os
- Macro placement empty area
- Module guide overlap area
- Macro-macro overlap area, and macro-blockage overlap area

Note: Items in the report have an absolute value and a percentage value, whenever possible. Because each floorplan you generate is different., not every statistic in the report will have a value for a specific floorplan.

Related Text Commands

- `reportPlanDesign`

Multi Plan Design

The Multi Plan Design form enables you to create multiple alternative floorplans by running different variations of the `setPlanDesignMode` and `planDesign` commands. Masterplan then analyzes the resulting floorplans, and ranks their usability using estimated wire length and congestion criteria.

You can run `planDesign` jobs sequentially on one machine, or in parallel on multiple host machines. To run `planDesign` in parallel, you must first use the `setDistributeHost` and `setMultiCpuUsage` commands to set up the configuration for the distributed processing. For example:

```
setDistributeHost {-local | -rsh -add {machine1 machine2}}
setMultiCpuUsage -numHosts 2
multiPlanDesign -autoTrials 2
```

Floorplan rankings are automatically displayed in the separate Floorplan Ranking Result form after all of the `planDesign` jobs are completed. Additionally, Masterplan saves a text report of the ranking results to a user-specified file.

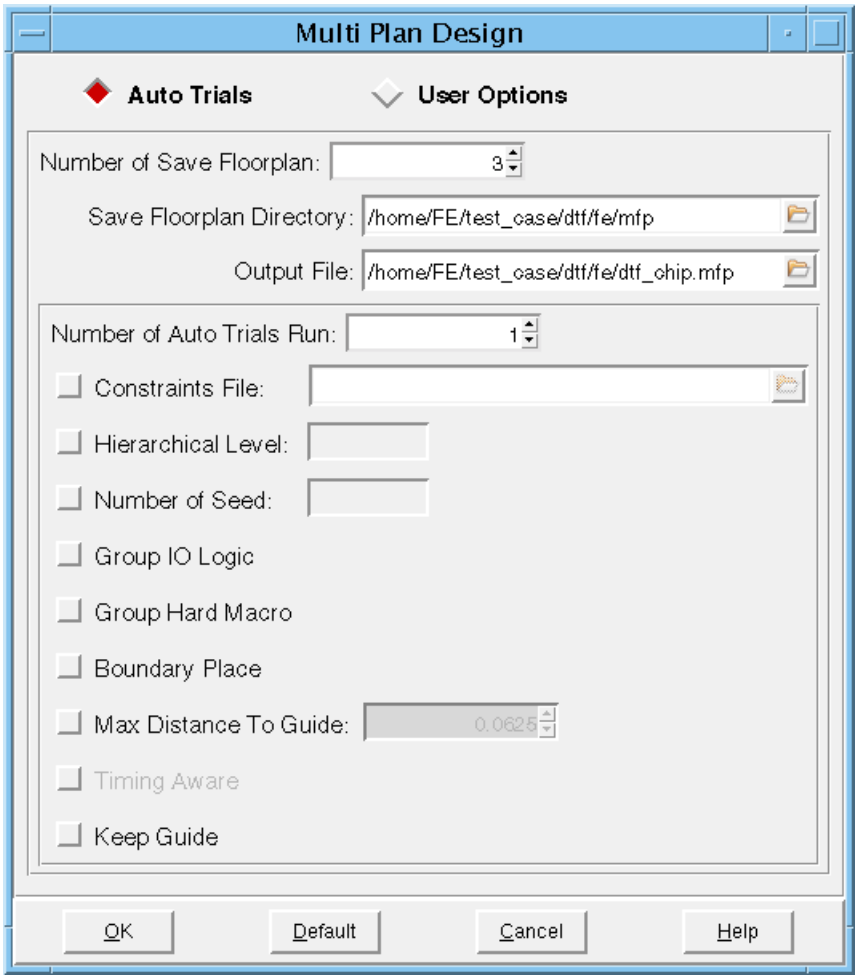
The Multi Plan Design form includes two pages:

- Multi Plan Design – Auto Trials on page 570
- Multi Plan Design – User Options on page 574

Multi Plan Design – Auto Trials

Use the *Auto Trials* page to specify a basic subset of Masterplan global parameters for Masterplan to use when creating floorplans. For each parameter in the subset, you can instruct Masterplan to always use it, or to never use it. Masterplan then creates floorplans using these settings, and chooses settings for the remaining global parameters that are not in the subset. Masterplan only creates the number of floorplans that you specify.

➤ Choose *FloorPlan – Automatic Floorplan – Multi Plan Design.*



Fields and Options

Number of Save Floorplan

Specifies the number of best floorplans to save out of the ones created.

Default: 3

Save Floorplan Directory

Specifies the directory in which to store the saved floorplans.

Default: `current_working_directory/mfp`

Output File

Saves the text report of the floorplan ranking results in a file with the specified name. The text report includes information such as the wire length and congestion values, and the commands that were run for each saved floorplan.

For example:

```
##################################################
###FLOORPLAN RANKED BY WIRE LENGTH ESTIMATION###
##################################################
##No.1 best result
##Wire Length: 2.467297e+07
##Congestion Overflow: 0.24%H + 0.11%V
##Floorplan file: /home/pfd/mptest/mp_fp0.fp
##Commands
    setPlanDesignMode -reset
    setPlanDesignMode -congAware true -setSeedHierLevel 1
    planDesign -constraints constraintfile
##No.2 result
...
```

Default: `topcell_name.mfp`

Number of Auto Trials Run

Specifies the number of `planDesign` jobs to run.

Default: 1

Constraints File	Uses the constraints set in the specified constraint file for macro placement and module guide generation. A constraint file is a text file that can contain a list of seeds for Masterplan to use when generating module guides, and spacing and orientation constraints to follow during macro placement. For more information, see "Masterplan Constraint File Format."
Hierarchical Level	Forces automatic seed selection to select all hierarchical instances at the specified logic level as seeds. *Default:* off
Number of Seed	Forces automatic seed selection to select approximately the specified number of seeds. *Default:* off
Group IO Logic	Creates I/O instance group seeds by traversing the logic from the I/O pads (or pins) to the first level of sequential elements. *Default:* off
Group Hard Macro	Controls the selection of hierarchical instances as seeds, based on hard macro distribution. *Default:* off
Boundary Place	Places macros along the core boundary for chip and block designs. *Default:* off
Max Distance To Guide	Restricts macro placement to a specified area that is relative to the macro's associated guide boundary. *Default:* off
Timing Aware	**Note:** This is a Beta feature.
Keep Guide	Retains the Masterplan-generated modules guides after the floorplan is created. *Default:* Off

Related Text Commands

- `multiPlanDesign`

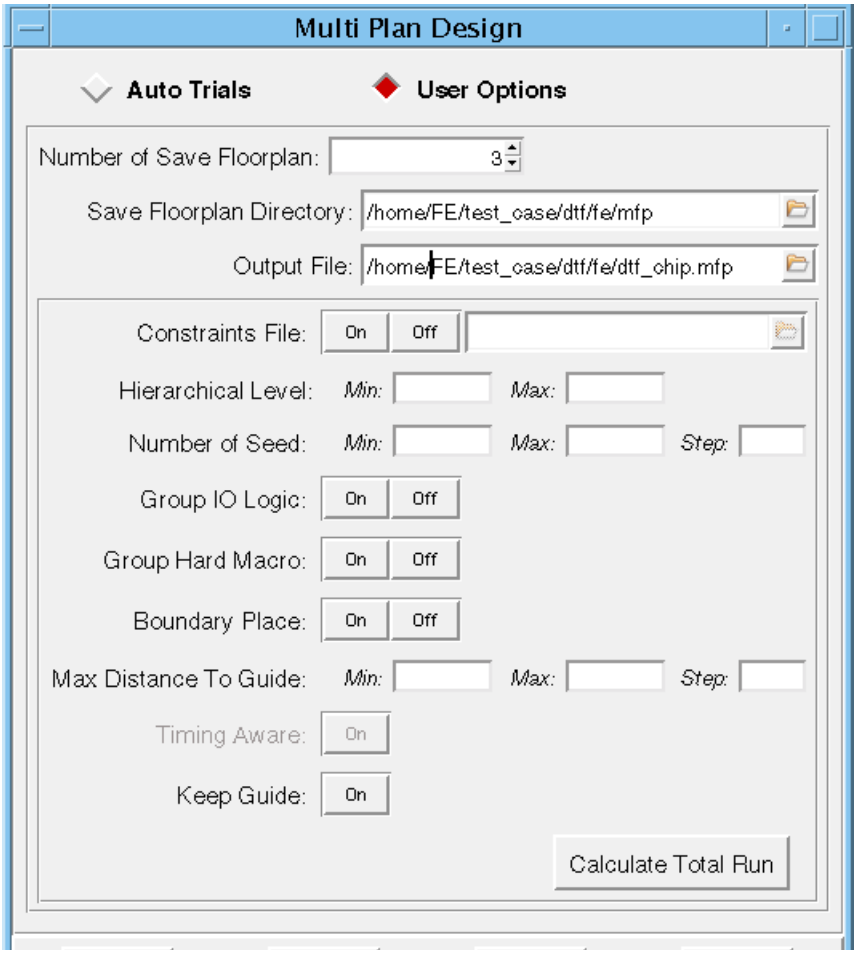
- planDesign
- setPlanDesignMode

Multi Plan Design – User Options

Use the *User Options* page to specify more variation in the global parameter settings that Masterplan uses when creating floorplans.

For some parameters, you can instruct Masterplan to always use the parameter, to never use the parameter, or to use and not use the parameter in a predefined order, when creating the floorplans. For other parameters, you can instruct Masterplan to use different values for each floorplan, within a specified range, and at specified intervals. Masterplan then creates as many floorplans as is necessary to meet all of the user-specified settings.

➤ Choose *FloorPlan – Automatic Floorplan – Multi Plan Design,* and click the *User Options* button.



Fields and Options

Number of Save Floorplan

Specifies the number of best floorplans to save out of the ones created.

Default: 3

Save Floorplan Directory

Specifies the directory in which to store the saved floorplans.

Default: `current_working_directory/mfp`

Output File

Saves the text report of the floorplan ranking results in a file with the specified name. The text report includes information such as the wire length and congestion values, and the commands that were run for each saved floorplan.

For example:

```
##################################################
###FLOORPLAN RANKED BY WIRE LENGTH ESTIMATION###
##################################################
##No.1 best result
##Wire Length: 2.467297e+07
##Congestion Overflow: 0.24%H + 0.11%V
##Floorplan file: /home/pfd/mptest/mp_fp0.fp
##Commands
    setPlanDesignMode -reset
    setPlanDesignMode -congAware true -setSeedHierLevel 1
    planDesign -constraints constraintfile
##No.2 result
...
```

Default: `topcell_name.mfp`

Constraints File

Determines whether to use the constraints set in the specified constraint file for macro placement and module guide generation.

A constraint file is a text file that can contain a list of seeds for Masterplan to use when generating module guides, and spacing and orientation constraints to follow during macro placement. For more information, see "Constraint File Format."

If you select *On*, Masterplan uses the constraints in the file for *all* floorplans generated.

If you select *Off*, Masterplan does not use the constraints in the file for any floorplan generated.

If you select *On* and *Off*, Masterplan only uses the constraints in the file for some of the floorplans generated.

Hierarchical Level

Forces automatic seed selection to choose all hierarchical instances at a specific logic level as seeds.

When you specify this parameter, Masterplan will select all hierarchical instances at the specified `minLevel` logic level as seeds for the first floorplan, as long as the instances also meet the other seed criteria. For each consecutive floorplan generated, Masterplan selects all hierarchical instances at the next logic level (current logic level + one level) as seeds, until it reaches the maximum logic level specified (`maxLevel`). The top design cell has a logic level of `0`.

For example, if you specify the following values:

Min: `1` *Max:* `3`

Masterplan selects hierarchical instances at logic level 1 as seeds for the first floorplan, hierarchical instances at logic level 2 as seeds for the second floorplan, and hierarchical instances at logic level 3 as seeds for the third floorplan.

You should not specify a `Max` value that is lower than the deepest logic level in your netlist.

Number of Seed

Forces automatic seed selection to select approximately a specified number of seeds.

If you specify values for this parameter, Masterplan will select approximately the minimum number of seeds specified (`Min`) for a floorplan. For each additional floorplan generated, it selects a seed number that is `Step` more than the previous seed number selected. Masterplan will continue to create floorplans until it selects the maximum seed number specified (`Max`).

For example, if you specify the following values:

Min: `20` *Max:* `50` *Step:* `10`

Masterplan selects approximately 20 seeds for one floorplan, 30 seeds for another floorplan, 40 seeds for another floorplan, and 50 seeds for the final floorplan.

Group IO Logic

Determines whether to I/O create instance group seeds by traversing the logic from the I/O pads (or pins) to the first level of sequential elements.

If you select *On*, Masterplan creates I/O instance group seeds by traversing the logic for *all* floorplans generated.

If you select *Off*, Masterplan does not create I/O instance group seeds by traversing the logic for any floorplan generated.

If you select *On* and *Off*, Masterplan only creates I/O instance group seeds by traversing the logic for some of the floorplans generated.

Group Hard Macro

Determines whether to control the selection of hierarchical instances as seeds, based on hard macro distribution.

If you select *On*, Masterplan bases the selection of hierarchical instances as seeds on hard macro distribution for *all* floorplans generated.

If you select *Off*, Masterplan does not base the selection of hierarchical instances as seeds on hard macro distribution for any floorplan generated.

If you select *On* and *Off*, Masterplan only bases the seed selection on hard macro distribution for some of the floorplans generated.

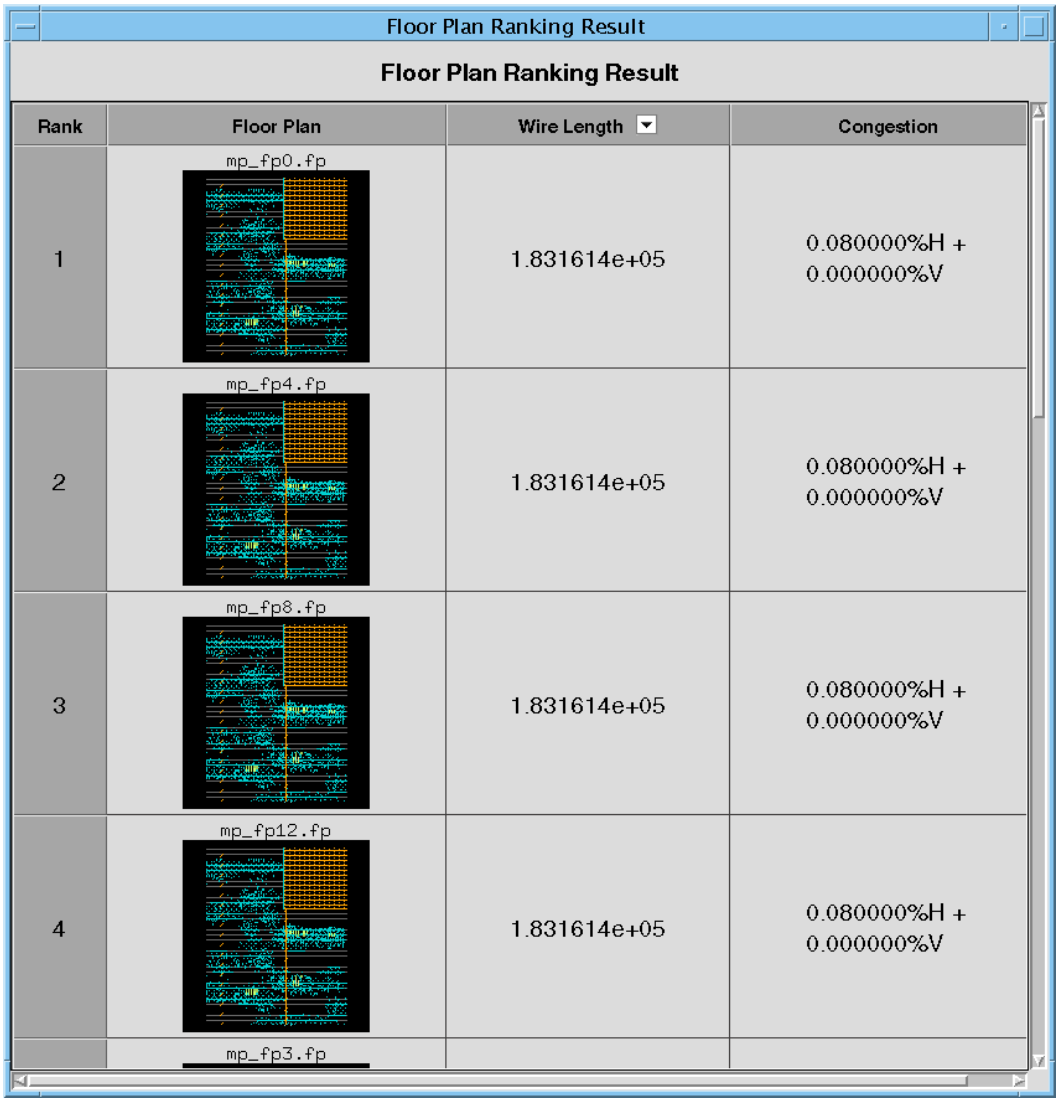
Boundary Place	Determines whether to place macros along the core boundary for chip and block designs. If you select *On*, Masterplan places macros along the core boundary for *all* floorplans generated. If you select *Off*, Masterplan does not place macros along the core boundary for any floorplan generated. If you select *On* and *Off*, Masterplan only places macros along the core boundary for some of the floorplans generated.
Max Distance To Guide	Restricts macro placement to an area that is relative to the macro's associated guide boundary. If you specify a value for this parameter, Masterplan will restrict placement for a floorplan to the minimum area value specified (`Min`). For each additional floorplan generated, it restricts placement to an area value that is `Step` more than the previous area value. Masterplan will continue to create floorplans until it restricts a floorplan to the maximum area value specified (`Max`).
Timing Aware	**Note:** This is a Beta feature.
Keep Guide	Retains the Masterplan-generated module guides after the floorplan is created.
Calculate Total Run	Calculates and displays the total number of `planDesign` jobs Masterplan will run in order to meet all of the user-specified settings.

Related Text Commands

- `multiPlanDesign`
- `planDesign`
- `setPlanDesignMode`

Floor Plan Ranking Result

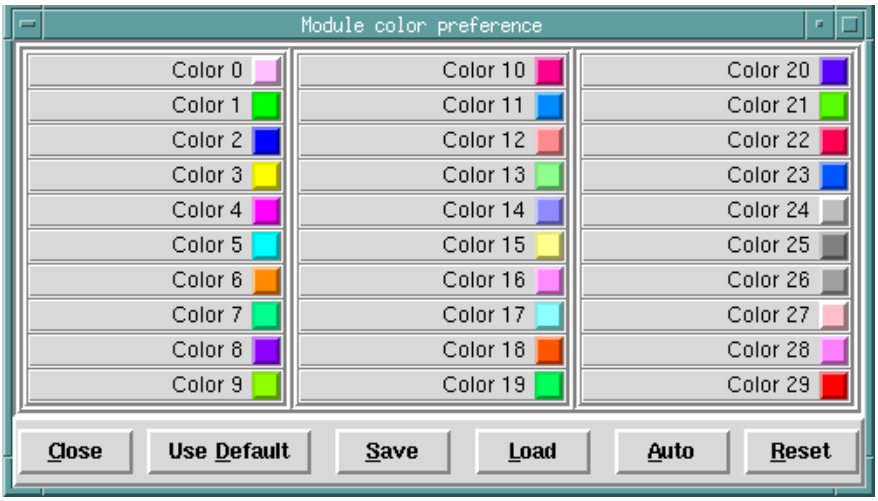
The Floor Plan Ranking Result form displays a list of the floorplans generated by the Multi Plan Design form. The floorplans are listed in order of their usability, using estimated wire length and congestion criteria. Click on *Wire Length* or *Congestion*, to sort the floorplans based on that criterion. You can click on the corresponding floorplan picture to load the floorplan into the current Encounter session.



Module Colors

Use the Module color preference form to create a color table to use for coloring modules.

➤ Choose *FloorPlan – Automatic Floorplan – Module Colors*.



Fields and Options

Close	Closes the Module color preference form.
Use Default	Loads the software's default color table into the form.
Save	Saves the color table.
Load	Loads a previously saved color table.
Auto	Applies colors from the color table to modules (starting from the lowest index color to the highest index color, depending on the number of modules in the design).
Reset	Resets the module colors to the software's default color values.

FlipChip

See Chapter 7, “FlipChip Menu” for more information.

Resize Floorplan

Use the Resize Floorplan form to resize the floorplan while maintaining the relative locations of the existing floorplan. You can resize the space among floorplan objects proportionally or you can shift floorplan objects at appropriate location(s) without changing the proportional spacing (shift-based resize). The resize values can be snapped to the multiple integer of the metal layer pitch.

You can adjust the space between the I/Os proportionally, by selecting *Adjust I/Os Proportionally* in the Resize Floorplan form. Resize floorplan treats the overlapping I/O pads as single entities that can be moved together when resizing the floorplan.

Resize floorplan preserves any offset that exists between the I/O pads and the design boundary.

➤ Choose *Floorplan – Resize Floorplan*. By default, the Proportional Mode is selected.

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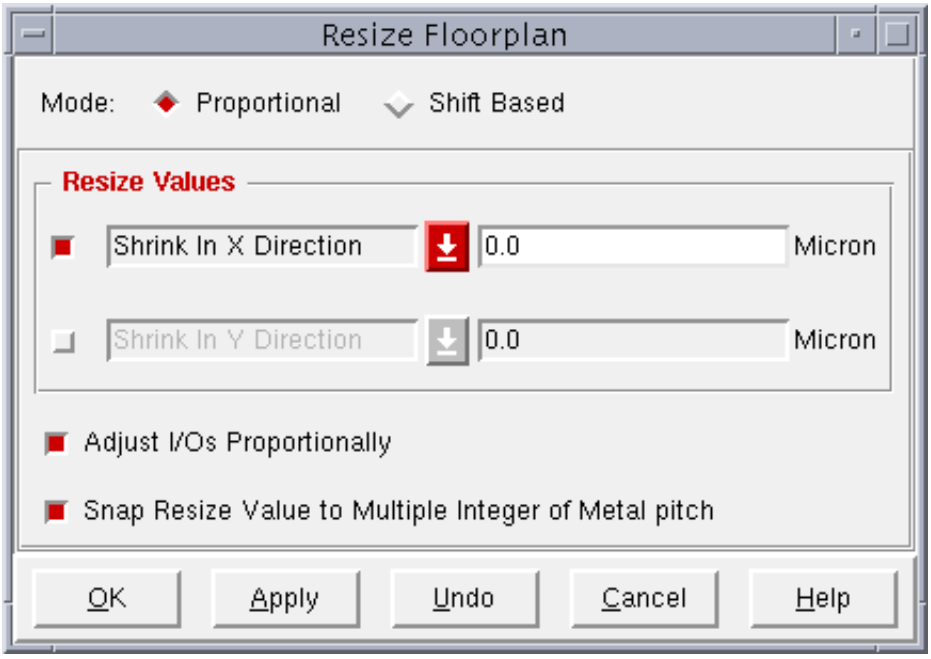
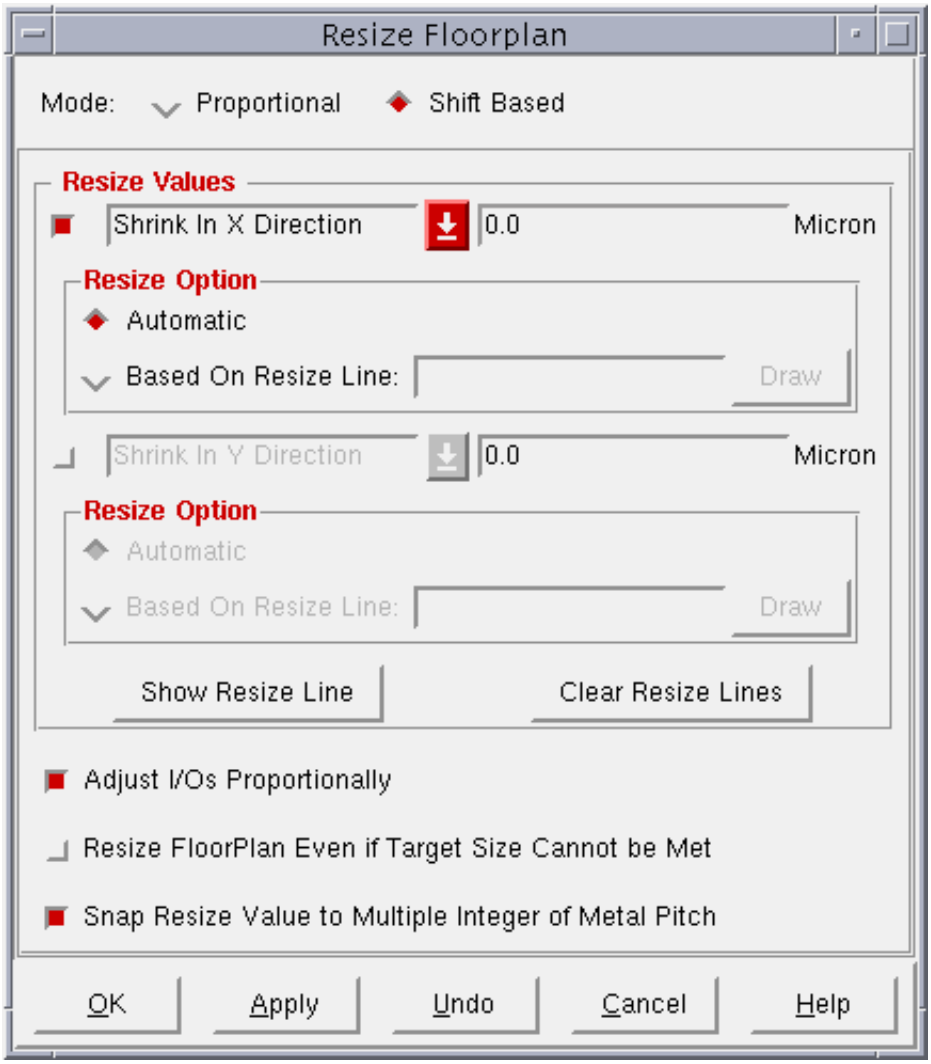


To select the Shift-based mode, select the Shift Based option.



Resize Floorplan – Fields and Options

Mode	Select one of the following options:	
	Proportional	Resizes the space among floorplan objects proportionally
	Shift Based	Shifts floorplan objects at appropriate location(s) without changing the proportional spacing.

Resize Values

Specifies the resize direction and the resize value. In the dropdown box on the top, you can select one of the four resize directions:

- *Shrink in X Direction*
- *Expand in X Direction*
- *Shrink in Y Direction*
- *Expand in Y Direction*

If you select resize in one direction from the dropdown menu on the top, the other direction is available in the dropdown menu on the bottom. For example, if you select *Shrink in X Direction* or *Expand in X Direction* in the dropdown box on the top, the following options are available in the dropdown menu on the bottom:

- *Shrink in Y Direction*
- *Expand in Y Direction*

The floorplan will be resized first in the direction specified in the top dropdown menu, and then in the direction specified in the bottom dropdown menu.

The resize value specifies how much the floorplan will be resized in the x and/or y directions. The value is in microns.

Resize Option

Specifies whether the floorplan will be resized automatically or based on the specified resize lines.

Automatic

Specifies that the floorplan will be resized automatically.

If you select this option, the resize lines are derived automatically based on the current floorplan and the specified resize values.

	Based On Resize Line	Specifies that the floorplan will be resized based on resize lines. Resize lines control the areas of floorplan that will be expanded or shrunk.You can specify coordinates for resize lines, or you can use the *Draw* button to draw resize lines in the floorplan area. You can specify resize lines using (x1 y1) (x2 y2)...(xn yn) coordinates. Each resize line can have multiple segments (for example, horizontal, vertical, and again horizontal) but it can only be applied to one direction. If you want to shrink or expand the floorplan in both directions, specify resize lines for each direction.
	Draw	Click the Draw button to draw resize lines in the floorplan area. To resize the floorplan in the x direction, draw vertical lines. To resize the floorplan in the y direction, draw horizontal lines. To complete a line, press the ESC key. You can draw multiple lines by dragging and clicking the left mouse button.
Show Resize Line	Displays the current resize line. If you update the values of the coordinates in the *Based on Resize Lines* field, you can click the *Show Resize Lines* button to update the display of the resize lines in the GUI.	
Clear Resize Line	Clears the current resize line. **Note:** The resize lines are automatically cleared when the floorplan is resized.	
Adjust I/Os Proportionally		

Resizes the space among I/Os proportionally.

`Default`: If you do not select this option, the I/Os are distributed evenly in both, Proportional and Shift Based modes.

Note: The overlapping I/Os are also spaced proportionally when you choose this option. By default, the overlapping I/Os are spaced evenly.

However, the relative placement order of the I/Os and the side constraints remain unchanged.

Resize Floorplan Even if Target Size Cannot be Met

Resizes the floorplan even if the target size can not be met. However, the floorplan is resized as near as possible to the specified size.

Snap Resize Value to Multiple Integer of Metal Pitch

Snaps resize values (shrink/expand) of the floorplan to a multiple integer of the metal layer pitch.

For example, if the horizontal metal pitch is 1.5 microns and you want to shrink the floorplan by 8 microns in y direction, the actual shrink value is 7.84 microns, the nearest multiple integer of the metal pitch.

For HHVV layer routing technology (M1M2M3M4), this option snaps the y direction resize value to the second horizontal layer pitch (M2) and the x direction resize value to the first vertical layer pitch (M3).

For VVHH layer routing technology (M1M2M3M4), this option snaps the y direction resize value to the first horizontal layer pitch (M3) and the x direction resize value to the second vertical layer pitch (M2).

For HVHV and VHVH layer routing technology, this option snaps the y direction resize value to the first horizontal layer pitch and the x direction resize value to the first vertical layer pitch.

`Default`: Off

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `resizeFP`
- `setResizeLine`

Relative Floorplan

You can capture and define the placement relationship of floorplan objects independently from the actual coordinates in a floorplan. You can also resize a module or blackbox based on other floorplan objects.You can also:

- Automatically generate constraints.
- Edit, save and Clear the constraints for floorplan objects.
- Place macros in an array

The Relative Floorplan menu contains the following submenus:

- Edit Constraints on page 589
- Generate Constraints on page 601
- Define Array Constraints on page 605
- Save Constraints on page 612
- Clear Constraints on page 613

Edit Constraints

The Edit Constraints form contains the following pages:

- Relative Floorplan – Place on page 590
- Relative Floorplan – Reshape on page 593
- Relative Floorplan – Resize on page 596
- Relative Floorplan – Pre-Route on page 599

Relative Floorplan – Place

Use the *Place* page of the Relative Floorplan form to place specific instances relative to other floorplan objects.

➤ Choose *Floorplan – Relative Floorplan – Edit Constraints*, and click *Place* from the *Floorplan Action* option.

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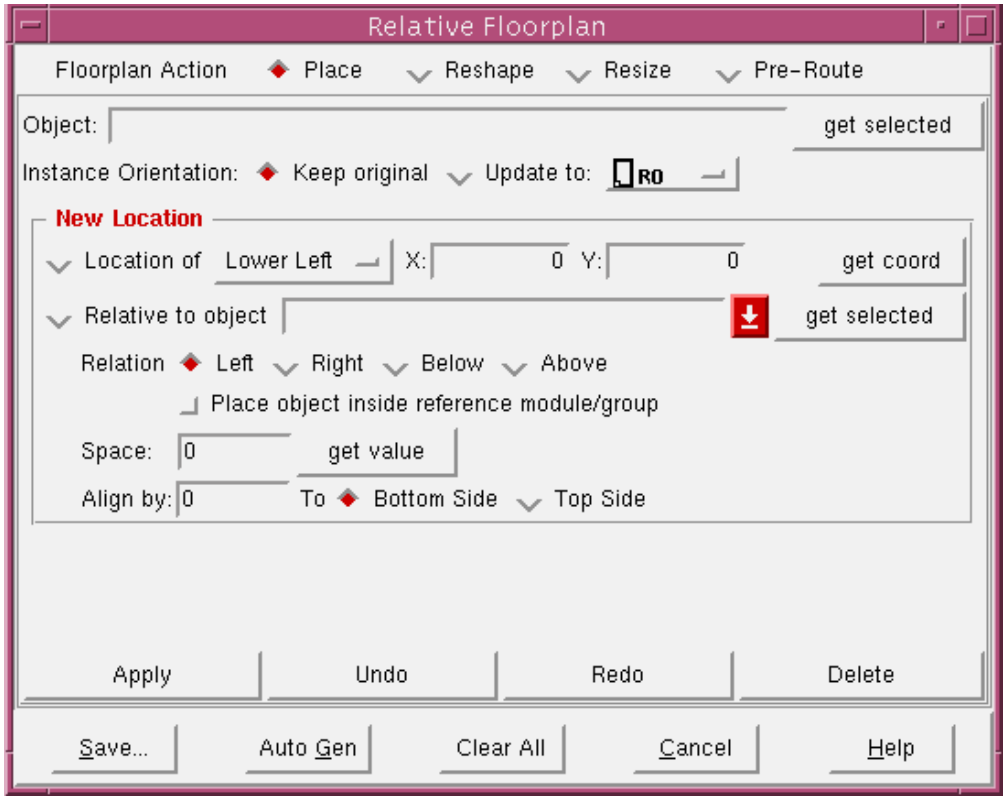


Relative Floorplan – Place Fields and Options

Object	Specifies the name of the placed instance. You can retrieve the name of the instance currently selected in the design display area by clicking *get selected*.

Instance Orientation	*Keep original* (the default) keeps the current object orientation. *Update to* with the pull-down menu specifies a new orientation. For a definition of the orientation symbols, see the Orientation Key table in the “Floorplanning the Design” chapter of the *Encounter User Guide*.
Location of	Places an instance by specifying the actual coordinates. You can specify the X and Y coordinates of the *Lower Left*, *Lower Right*, *Upper Left*, or *Upper Right* corner of the specified object. Use *get coord* to populate the X and Y fields with the current location of the specified object.
Relative to object	Places a specific object relative to a reference object. The reference object can be an instance or a core boundary. Use the pull-down menu to select a *left*, *right*, *bottom*, or *top* core boundary.
Relation	Places a specific object to the left, right, below, or above of the reference object. If the reference object is an edge of the core boundary, then you can only select a specific relation option. For example, if the reference object is *Left_Core_Boundary*, *Right_Core_Boundary*, *Bottom_Core_Boundary*, or *Top_Core_Boundary*, then you can only select the *Right*, *Left*, *Above*, or *Below* option, respectively.
Place object inside reference module/group	
	Places a specific object inside the reference object. The object is placed relative to the *Left*, *Right*, *Below*, or *Above* the edge of the reference object.
Space	Specifies the spacing between the placed and the reference objects, in micrometers.
Align by	Specifies the placed object will be aligned to a specific side of the reference object by an offset value, in micrometers. This offset value can be a positive or negative number.

get value	Populates the *Space* and *Align by* fields with the current spacing and offset values of the specified objects relative to the specified reference object in the design display area.
To	Specifies the side of the reference object to which the placed object will be aligned. This is automatically updated based on the *Relation* value. If *Relation* is *Left* or *Right*, then the radio buttons are *Bottom Side* and *Top Side*. If *Relation* is *Above* or *Below*, the radio buttons are *Left Side* and *Right Side*.
Auto Gen	Generates an initial pre-routed relative floorplan.

Tip

To save all the Relative Floorplan commands that were executed during a session, click *Save*. This saves a script that can be used later for updating or adjusting an existing floorplan based on the new blocks' size and position.

Related Text Commands

For information on the following commands, see "Floorplan Commands" in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`
- `relativeFPlan`
- `saveRelativeFPlan`

Related Topics

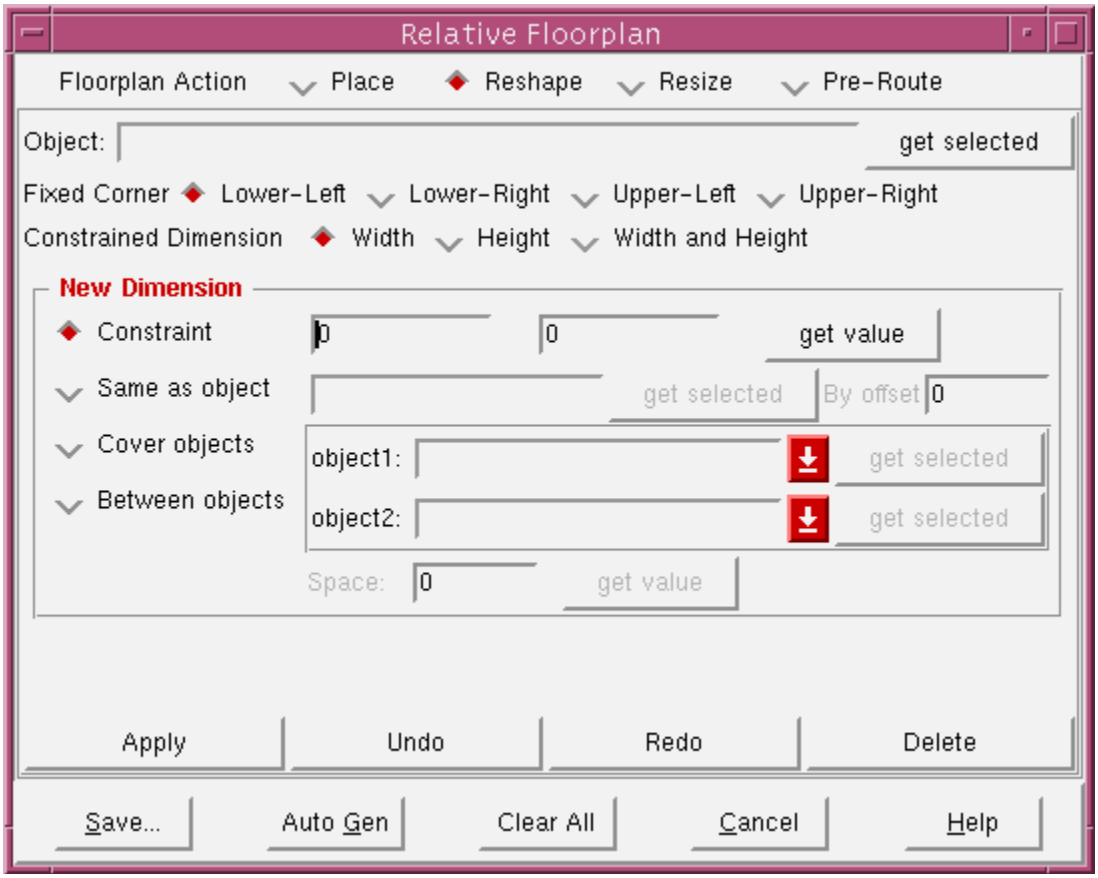
For information on the following topics, see "Floorplanning the Design" in the *Encounter User Guide*.

- Running Relative Floorplanning

Relative Floorplan – Reshape

Use the *Reshape* page of the Relative Floorplan form to reshape specific instances.

➤ Choose *Floorplan – Relative Floorplan – Edit Constraints*, and click *Reshape* from the *Floorplan Action* option.



Relative Floorplan – Reshape Fields and Options

Object	Specifies the name of the placed instance. You can retrieve the name of the instance currently selected in the design display area by clicking *get selected*.
Fixed Corner	Specifies which corner of the instance remains fixed during reshape. You can specify *Lower-Left*, *Lower-Right*, *Upper-Left*, or *Upper-Right* corner of the specified object.

Constrained Dimension	Specifies *Width*, or *Height*, or a paired *Width and Height* dimension.
Constraint	Specifies a new dimension value, or values, that a specific object is stretched in the specified dimension from a given fixed corner. Use both value fields when specifying a *Width and Height* dimension values. Use *get value* to populate the width and height fields with the current width and height of the specified object in the design display area.
Same as object	Specifies the reference object. This reshapes a given object to be the same as the reference object in the specified dimension, but offset by the value specified in *By offset*. The offset value can be a positive or negative number.
Cover objects	Specifies two reference objects. This reshapes a given object such that its new dimension value in the constrained dimension is the same as the sum of the first object dimension, second object dimension, and the spacing between these two reference objects.
Between objects	Reshapes a given object such that its new dimension value in the constrained dimension will be equal to the spacing from the fixed reference corner to the reference object. This command does not re-position the reshaped object unless the object boundary after reshaping is extended outside of the core boundary.
Space	Reserves channel spacing between the reshaped object and the reference object.
Auto Gen	Generates an initial pre-routed relative floorplan.

Tip

To save all the Relative Floorplan commands that were executed during a session, click *Save*. This saves a script that can be used later for updating or adjusting an existing floorplan based on the new blocks' size and position.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`
- `relativeFPlan`
- `saveRelativeFPlan`

Related Topics

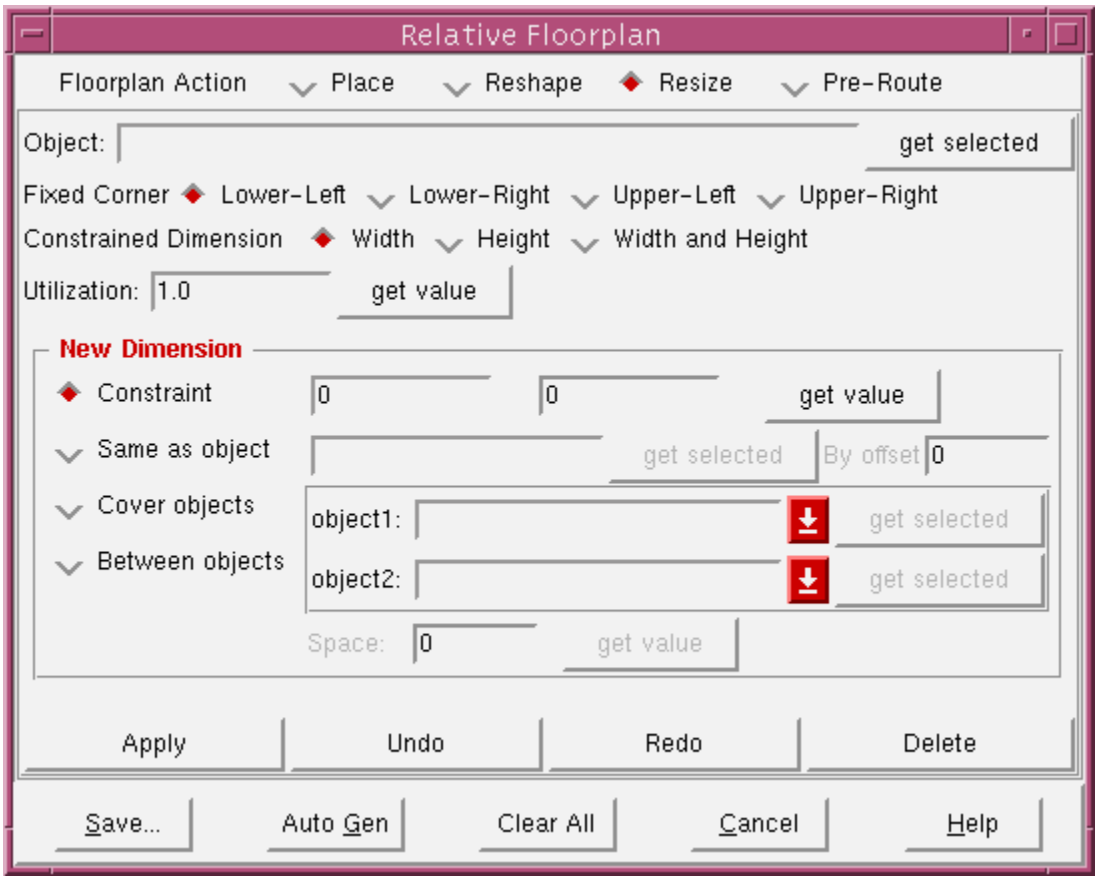
For information on the following topics, see “Floorplanning the Design” in the *Encounter User Guide*.

- Running Relative Floorplanning

Relative Floorplan – Resize

Use the *Resize* page of the Relative Floorplan form to an object while maintaining its current area based on a specified width and height, a given dimension (width or height), and a target utilization value.

➤ Choose *Floorplan – Relative Floorplan – Edit Constraints*, and click *Resize* from the *Floorplan Action* option.



Relative Floorplan – Resize Fields and Options

Object

Specifies the name of the placed instance. You can retrieve the name of the instance currently selected in the design display area by clicking *get selected*.

Fixed Corner	Specifies which corner of the instance remains fixed during reshape. You can specify *Lower-Left*, *Lower-Right*, *Upper-Left*, or *Upper-Right* corner of the specified object.
Constrained Dimension	Specifies *Width*, or *Height*, or a paired *Width and Height* dimension.
Utilization	Specifies the utilization. You can retrieve the utilization of the instance currently selected in the design display area by clicking *get value*.
Constraint	Specifies a new dimension value, or values, that a specific object is stretched in the specified dimension from a given fixed corner. Use both value fields when specifying a *Width and Height* dimension values. Use *get value* to populate the width and height fields with the current width and height of the specified object in the design display area.
Same as object	Specifies the reference object. This reshapes a given object to be the same as the reference object in the specified dimension, but offset by the value specified in *By offset*. The offset value can be a positive or negative number.
Cover objects	Specifies two reference objects. This reshapes a given object such that its new dimension value in the constrained dimension is the same as the sum of the first object dimension, second object dimension, and the spacing between these two reference objects.
Between objects	Reshapes a given object such that its new dimension value in the constrained dimension will be equal to the spacing from the fixed reference corner to the reference object. This command does not re-position the reshaped object unless the object boundary after reshaping is extended outside of the core boundary.
Space	Reserves channel spacing between the reshaped object and the reference object.
Auto Gen	Generates an initial pre-routed relative floorplan.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`
- `relativeFPlan`
- `saveRelativeFPlan`

Related Topics

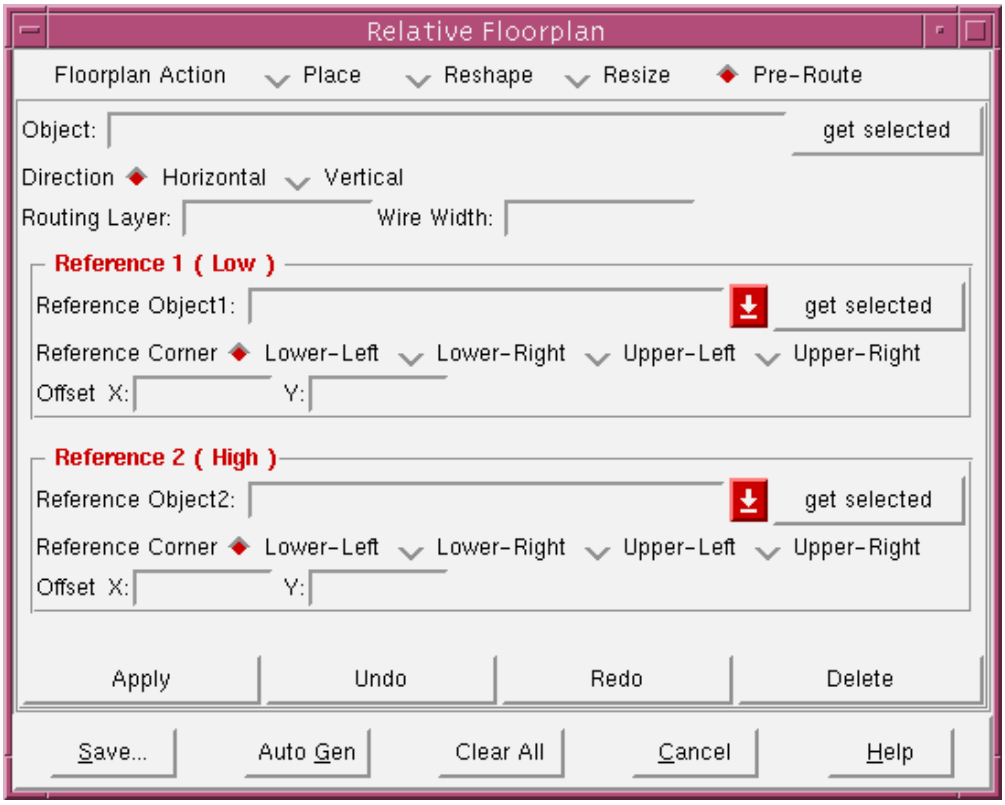
For information on the following topics, see “Floorplanning the Design” in the *Encounter User Guide*.

- Running Relative Floorplanning

Relative Floorplan – Pre-Route

Use the *Pre-Route* page of the Relative Floorplan form to specify a wire's start or end point relative to the reference object's reference corner, or specify a wire's start or end point directly.

➤ Choose *Floorplan – Relative Floorplan – Edit Constraints*. If *Pre-Route* is not already selected in the Floorplan Action option, select it.



Relative Floorplan – Pre-Route Fields and Options

Object	Specifies the name of the wire. You can retrieve the name of the wire currently selected in the design display area by clicking *get selected*.
Direction	Specifies a *Horizontal* or *Vertical* wire direction.
Routing Layer	Specifies the horizontal layer of the wire segment or strip box.
Wire Width	Specifies the wire width.

Reference Object 1	Specifies the first reference object, which can be the core, design, or other floorplan objects.
Reference Corner	Specifies the reference corner of reference object 1. You can specify *Lower-Left*, *Lower-Right*, *Upper-Left*, or *Upper-Right* corner of the specified object.
Offset	Specifies the X and Y offsets.
Reference Object 2	Specifies the second reference object, which can be the core, design, or other floorplan objects.
Reference Corner	Specifies the reference corner of reference object 2. You can specify *Lower-Left*, *Lower-Right*, *Upper-Left*, or *Upper-Right* corner of the specified object.
Offset	Specifies the X and Y offsets.
Auto Gen	Generates an initial pre-routed relative floorplan.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`
- `relativeFPlan`
- `saveRelativeFPlan`

Related Topics

For information on the following topics, see “Floorplanning the Design” in the *Encounter User Guide*.

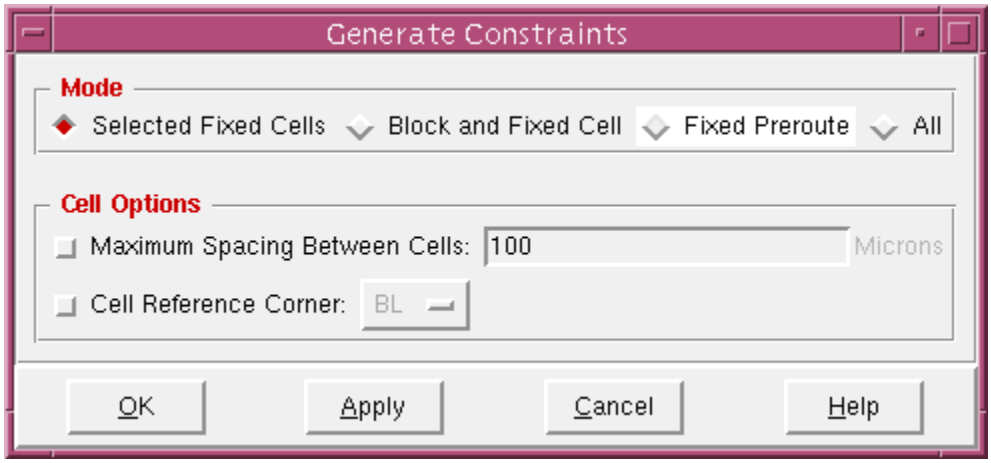
- Running Relative Floorplanning

Generate Constraints

Use the generate Constraints form to automatically create constraints for the following objects through the GUI:

- Fixed standard cells that are currently selected in the display area
- Blocks and all fixed standard cells
- Fixed wire editing routes, that is, routes created by wire editing

➤ Choose *Floorplan – Relative Floorplan* and click *Generate Constraints.*



Generate Constraints Fields and Options

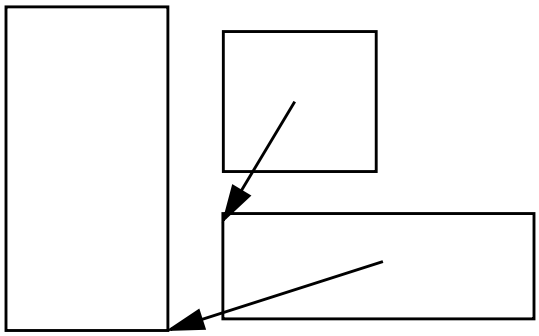
Selected Fixed Cells	Specifies that constraints will be generated automatically for those fixed standard cells that are currently selected in the display area.
Block and Fixed Cell	Specifies that constraints will be generated automatically for blocks and all fixed standard cells.
Fixed Preroute	Specifies that constraints will be generated automatically for fixed wire editing routes, that is, the routes created by wire editing.

All	Specifies that constraints will be generated automatically for: ■ blocks and all fixed standard cells ■ fixed wire editing routes, that is, the routes created by wire editing
Maximum Spacing Between Cells	Specifies the maximum space, in microns, between fixed cells and/or blocks for deriving constraints. The default value is 100.
Cell Reference Corner	Specifies the reference corner for the cells. Specify one of the following: *BL* (bottom left). The position calculation relative to the cell will be first toward the bottom and then toward the left side.

LB (left bottom). The position calculation relative to the cell will be first toward the left side and then toward the bottom.

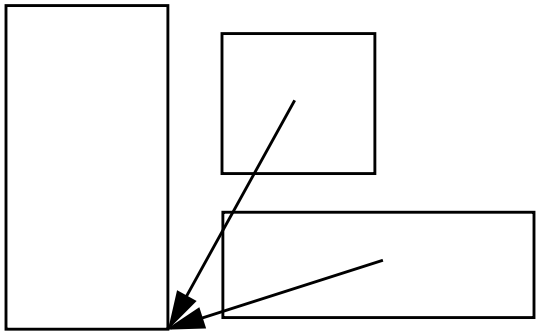
The difference between BL and LB is illustrated as follows:

Reference Corner BL



If you specify BL as the reference corner, the movement is first to bottom and then to the left.

Reference Corner LB



If you specify LB as the reference corner, the movement is first to left and then to the bottom.

There is a similar difference between BR and RB and between TL and LT.

BR (bottom right). The position calculation relative to the cell will be first toward the bottom and then toward the right side.

RB (right bottom). The position calculation relative to the cell will be first toward the bottom and then toward the right side.

TL (top left). The position calculation relative to the cell will be first toward the top and then toward the left side.

LT (left top). The position calculation relative to the cell will be first toward the left side and then toward the top.

TR (top right). The position calculation relative to the cell will be first toward the top and then toward the right side.

RT (right top). The position calculation relative to the cell will be first toward the right side and then toward the top.

Related Text Commands

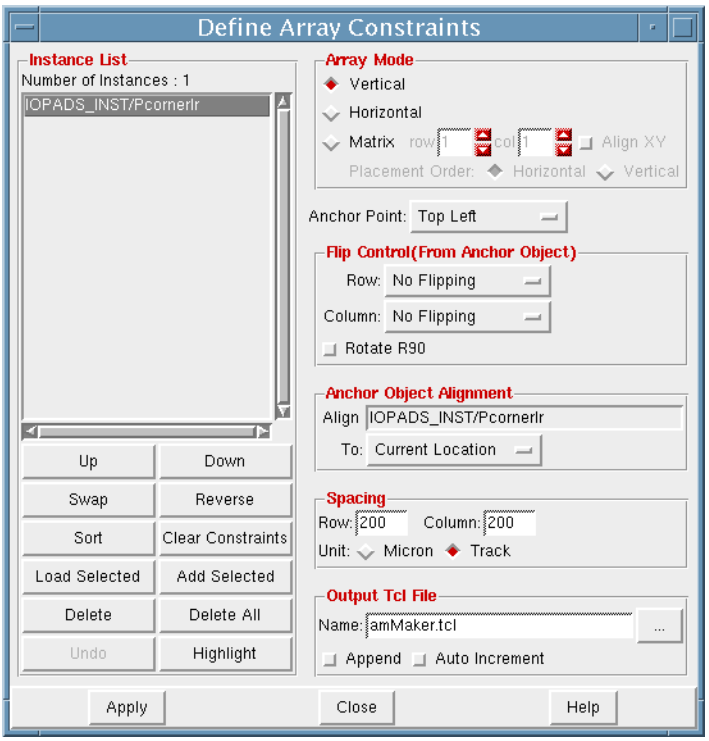
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`
- `relativeFPlan`
- `saveRelativeFPlan`

Define Array Constraints

Use the Array Maker form to easily place macros in a matrix. You can use the Array Maker form to place macros in a matrix aligned to a region, guide, or boundary.

➤ Select the macros that you want to display in an array. Choose *Floorplan – Relative Floorplan* and click *Define Array Constraints.*



Define Array Constraints Fields and Options

Instance List	Displays the macros that will be placed in the array. The topmost macro in the list is considered as the reference object.
Up	Moves the selected macro up in the Instance List.
Down	Moves the selected macro down in the Instance List.
Swap	Swaps two selected macros.
Reverse	Reverses the order of the macros in the Instance List.
Sort	Sorts the macros, by name, in the Instance List

Clear Constraints	Clears the array constraints, specified for macros, from the Instance List.
Load Selected	If any macros are selected in the main GUI window, includes them in the Instance List **Note:** Any macros that are not selected in the main GUI window are removed from the Instance List.
Include Selected	If any macros are selected in the main GUI window, adds them to the Instance List. Other macros in the Instance List are also retained.
Delete	Removes the selected macros from the Instance List. **Note:** Removes those macros that are selected in the Instance List. This does not remove the macros selected in the main GUI window.
DeleteAll	Removes all macros from the Instance List
Undo	Undo the last operation performed on the Instance List.
Highlight	Specifies that the macros selected in the Instance List should be highlighted in the main GUI window.
Array Mode	Select one of the modes for the array:

Vertical: Specifies that the macros should be placed in a column.

Horizontal: Specifies that the macros should be placed in a row.

Matrix: Specifies that the macros should be placed in a matrix.

row: For the *Matrix* option, specifies the number of rows in the matrix

col: For the *Matrix* option, specifies the number of columns in the matrix

Align XY: For the *Matrix* option, specifies that the objects should be aligned to the maximum height and width.

Horizontal: For the *Matrix* option, specifies that the macros should be placed in a horizontal direction first and then in the vertical directions. That is, the macros will be placed row-wise.

Vertical: For the *Matrix* option, specifies that the macros should be placed in a vertical direction first and then in the horizontal direction. That is, the macros will be placed column-wise.

Anchor Point

Choose one of the following as the anchor point. This is the corner in which the anchor object (the first macro in the Instance List) will be placed, relative to the other macros.

- *Top Left:* The anchor object is placed at the top left corner relative to the other macros.
- *Top Right:* The anchor object is placed at the top right corner relative to the other macros.
- *Bottom Left:* The anchor object is placed at the bottom left corner relative to the other macros.
- *Bottom Right:* The anchor object is placed at the bottom right corner relative to the other macros.

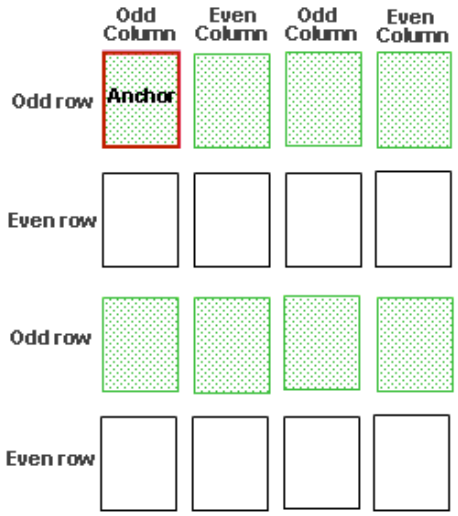
Flip Control (From Anchor Object)

Specify the flip options for the rows as follows:

- *Row*: Specify one of the following for the horizontal rows:
  - *No Flipping*: Specifies that the rows should not be flipped
  - *Flip Even Ones*: Specifies that even numbered rows should be flipped.
  - *Flip Odd Ones*: Specifies that odd numbered rows should be flipped.
  - *Flip All*: Specifies that all rows should be flipped.
- *Column*: Specify one of the following for the vertical rows:
  - *No Flipping*: Specifies that the rows should not be flipped
  - *Flip Even Ones*: Specifies that even numbered rows should be flipped.
  - *Flip Odd Ones*: Specifies that odd numbered rows should be flipped.
  - *Flip All*: Specifies that all rows should be flipped.

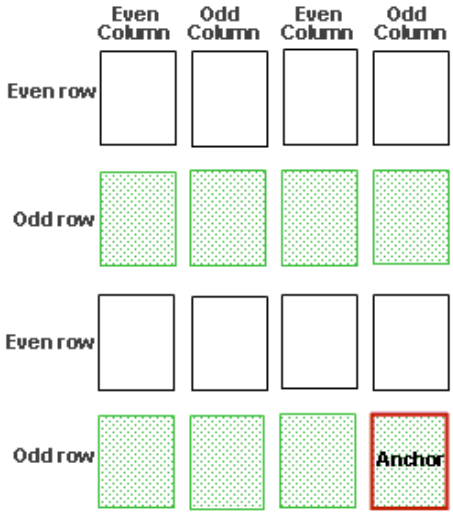
The way even/odd columns are flipped depends on the location of the anchor object. This is illustrated as follows:

Here is the scenario with the anchor object at the top left



Anchor Point: Top Left

Here is the scenario with the anchor object at the bottom right.



Anchor Point: Bottom Right

Rotate R90 — If selected, the macros are rotated right by 90 degrees.

Anchor Object Alignment — Has the following fields

- *Align*: The name of the anchor object is displayed in this field.
- *To*: Specify one of the following:
  - *Current Location*: Specifies that the anchor object stays at the current location.
  - *Guide*: Specifies that the anchor object is aligned to the parent module of the macro.
  - *Core*: Specifies that the anchor object is aligned to the core boundary.
  - *Boundary*: Specifies that the anchor object is aligned to the design boundary.

Spacing

Provide the details of the spacing as follows:

- *Row*: Provide the spacing between rows.
- *Column*: Provide the spacing between columns.
- *Unit*: Select whether the unit for spacing is microns or tracks.

Output TCL file

Provide options for the file in which the details of array constraints are stored. Specify the following:

- *Name*: Name of the file.
- *Append*: Specifies that the corresponding relative constraints will be appended to the specified output file.
- *Auto Increment:* Specifies that the file name is incremented automatically, starting from 0, every time the changes are applied.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `autoGenRelativeFPlan`
- `clearRelativeFPlan`
- `deleteRelativeFPlan`

- `relativeFPlan`
- `saveRelativeFPlan`

Save Constraints

Use the Save Constraints form to save the floorplan constraints.

➤ Choose *Floorplan - Relative Floorplan - Save Constraints* and specify a file in which to save floorplan constraints.

Clear Constraints

Use the *Clear Constraints* form to clear the floorplan constraints.

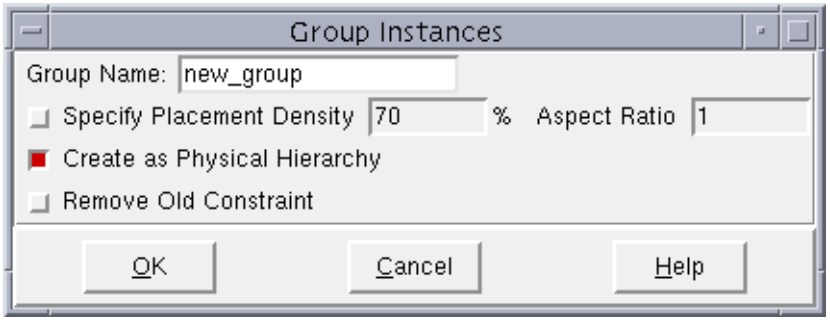
➤ Choose *Floorplan - Relative Floorplan - Clear Constraints*

Create Physical Hierarchy

Use the Group Instances form to improve your design hierarchy, apply and test different hierarchical schemes prior to regrouping the netlist, and determine the initial size and shape of the floorplan object.

By default, all instance groups are output to the netlist as logic modules when saving the regrouped netlist. The new group can be viewed or displayed by using the pull-down menu from *Floorplan – Create Physical Hierarchy*, or by using the Design Browser and selecting *Group*.

➤ Click on and highlight the module or submodule guides that you want in the group and choose *Floorplan – Create Physical Hierarchy– New Hierarchy*.



Group Instances Fields and Options

Group Name	Specifies the name of the new group.
Specify Placement Density %	Specifies a placement density value. The default is 70%.
Aspect Ratio	Specifies an aspect ratio value. This is the ratio of the floorplan object's width divided by the height.
Create as Physical Hierarchy	Specifies that the created group is a physical hierarchy. If you deselect this option, the created group is not saved back to the netlist. To change this option after creating the instance group, use the Object Attribute form.
Remove Old Constraint	Specifies that the existing constraints are removed when creating the instance group.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `addInstToInstGroup`
- `createInstGroup`
- `deleteAllInstGroups`
- `deleteInstFromInstGroup`
- `deleteInstGroup`

Related Topics

For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

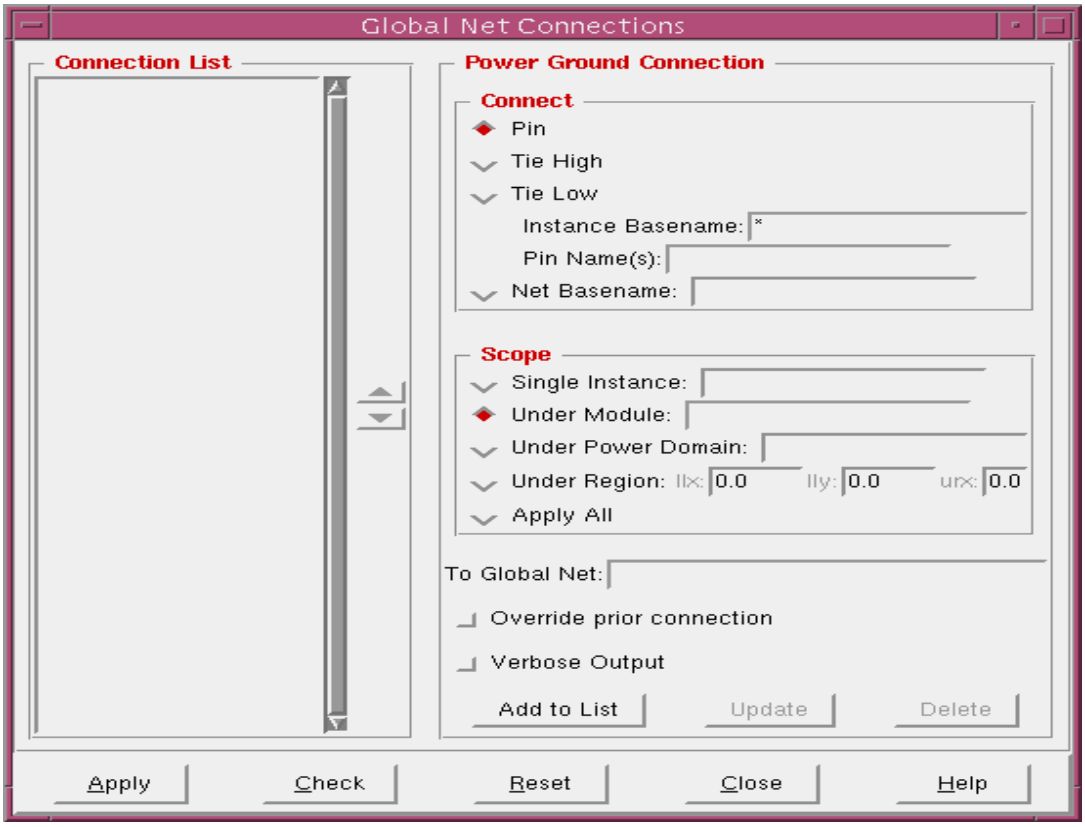
- Grouping Instances

Connect Global Nets

The Global Net Connections form assigns pins or nets to a global net such as a power or ground. In addition, tie-high and tie-low pins are assigned to global nets.

Note: This form can be used for incremental updating.

➤ Choose *Floorplan – Connect Global Net*.



Global Net Connections Fields and Options

Connection List	The list of connection information. When you select an item on the list, the *Power Ground Connection* panel of the form is populated with the corresponding information.
Connect	Controls which objects are connected to the global net. Select one of the following options:

	Pins	Select this option, then use the text entry field to specify the pin name to be connected. These are the power and ground port names in the standard cells, block cells, and I/O pad cells.
	Tie High	Connects the tie-high pins to a global power and ground net.
	Tie Low	Connects the tie-low pins to a global power and ground net.
	Instance Basename	Specifies the leaf instance basenames whose pins are to be connected to the global net. You can use a wildcard (*) as an entry. By default, all pins are connected.
	Pin Name(s)	Specifies the pins to connect to the global net.
	Net Basename	Select this option, then use the text entry field to specify the local net names. This connects local power and ground nets to the global power and ground nets. These net names must be initially specified during design import.
Scope	Provides a greater degree of control for specifying objects to connect to the global net. Select one of the following:	
	Single Instance	Makes a connection only to the specified instance.
	Under Module	Select this option, then use the text entry field to specify the module (or hierarchical instance) name from which the pins or local nets connect. Only the pins or local nets of the instances under the specified module are connected.
	Under Power Domain	Applies the global net connection to the instances within the specified power domain.

Under Region Select this option, then specify the coordinates for a region within the design display area that encompasses the pins or local nets to be connected.

Tip

Clicking on the mouse icon and moving the cursor to the design display area enables you to use the mouse to specify the region coordinates.

Apply All Specifies that the pins or local nets connect from the top module in the hierarchy.

To Global Net The power and ground net to which to connect a group of standard cells. Standard cells are connected to the net that you specify in the text entry field.

Override prior connection

If selected, disconnects pins and local nets that are already connected to a global net before reconnecting them to the global net specified in this form. If deselected, only new pins and local nets are connected to the specified global net. This is the default.

Verbose Output If selected, connection statistics and warning messages are displayed in the console. If deselected, some warning messages are suppressed. This is the default.

Add to List Adds the new connection information to the *Connection List* at the left side of the form

Update Applies new values to the selected connection in the *Connection List*.

Delete Removes the selected connection from the *Connection List*.

Apply The pins and instances or local nets specified in the *Connection List* are connected to the specified global net.

Check Displays a list of instances for which power and ground pins are not connected to special nets.

Reset Removes power and ground connectivity from the global net.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `globalNetConnect`

Related Topics

For information on the following topic, see “Power Planning and Routing” in the *Encounter User Guide*.

- Global Net Connections

Edit Floorplan

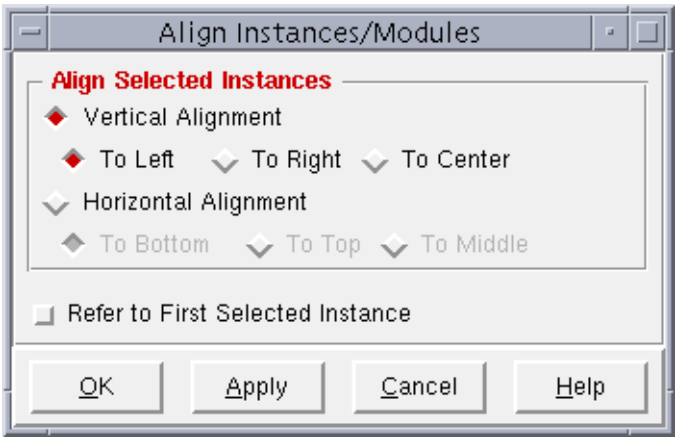
The *Edit Floorplan* submenu provides access to the following features:

- Align Instances on page 621
- Shift Instances on page 623
- Space Instances on page 625
- Flip/Rotate Instances on page 626
- Snap Floorplan on page 628
- Legalize Floorplan on page 630
- Set Block Placement Status on page 632
- Edit Halos on page 633
- Edit IO Row on page 636
- Core Row on page 637
- Clear Floorplan on page 643

Align Instances

Use the Align Instances/Modules form to align instances vertically or horizontally.

➤ Highlight instance(s) in the design display area and choose *Floorplan – Edit Floorplan – Align Instances*.



Alliteratively, you can click the middle mouse button to bring up a context sensitive pop-up menu to select the *Align* commands.

Note: To undo the previous action, use the *Undo* widget or U bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or R bindkey.

Align Instances/Modules Fields and Options

Vertical Alignment
Specifies the selected vertical instance alignment. Choose either *To Left*, *To Right*, or *To Center*.

Horizontal Alignment
Specifies the selected horizontal instance alignment. Choose either *To Bottom*, *To Top*, or *To Middle*.

Refer to First Selected Instance
Specifies a reference instance highlighted in the design display area. If you specify this option, the first selected instance is the reference object.

Related Text Commands

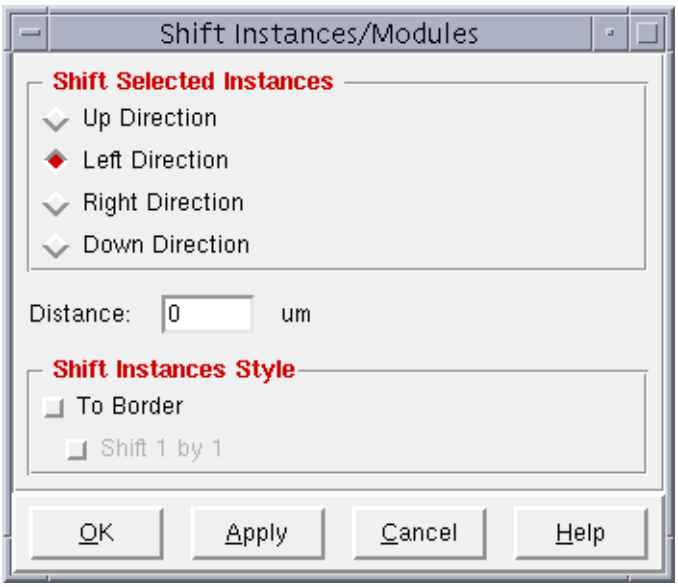
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `alignInst`

Shift Instances

Use the Shift Instances/Modules form to shift instances vertically or horizontally by a specified distance value.

➤ Highlight instance(s) in the design display area and choose *Floorplan – Edit Floorplan – Shift Instances*.



Note: To undo the previous action, use the *Undo* widget or U bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or R bindkey.

Shift Instances/Modules Fields and Options

Up Direction	Shifts the selected instance(s) upward.
Left Direction	Shifts the selected instance(s) to the left.
Right Direction	Shifts the selected instance(s) to the right.
Down Direction	Shifts the selected instance(s) downward.
Distance	Specifies the distance value, in micrometers.

Related Text Commands

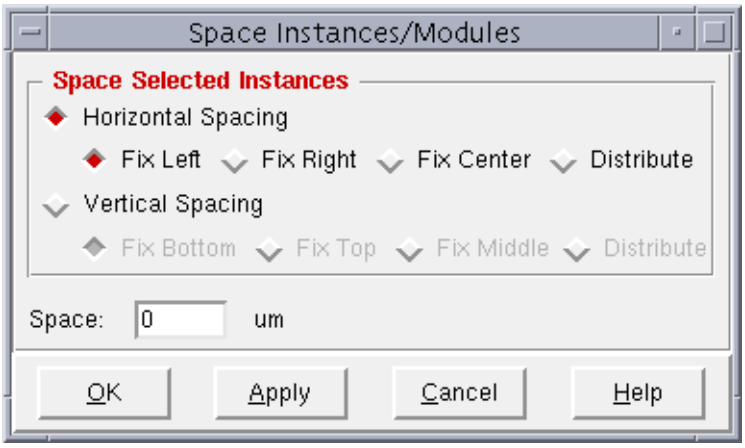
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `shiftInst`

Space Instances

Use the Space Instances/Modules form to space instances horizontally or vertically by a specified distance value. You can also evenly distribute the spacing horizontally or vertically between three or more instances.

➤ Highlight instance(s) in the design display area and choose *Floorplan – Edit Floorplan – Space Instances*.



Note: To undo the previous action, use the *Undo* widget or U bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or R bindkey.

Space Instances/Modules Fields and Options

Horizontal Spacing	Specifies the selected horizontal instance spacing. Choose either *Fix Left*, *Fix Right*, *Fix Center*, or *Distribute*.
Vertical Spacing	Specifies the selected vertical instance spacing. Choose either *Fix Bottom*, *Fix Top*, *Fix Middle*, or *Distribute*.
Space	Specifies the spacing value, in micrometers.

Related Text Commands

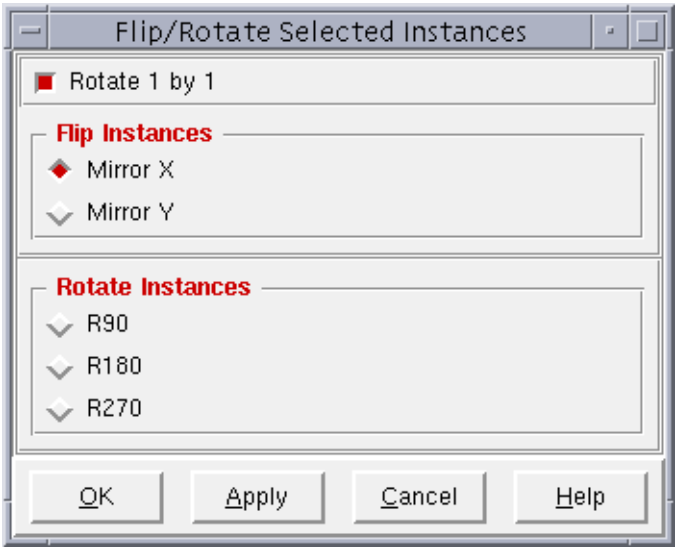
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

■ `spaceInst`

Flip/Rotate Instances

Use the Flip/Rotate Selected Instances form to flip or rotate instances.

➤ Highlight instance(s) in the design display area and choose *Floorplan – Edit Floorplan – Flip/Rotate Instances*.



Alternatively, you can click the middle mouse button to bring up a context sensitive pop-up menu to select the *Flip* and *Rotate* commands. Another alternative is to open the Block Attribute form by double-clicking on the block, and selecting the new orientation (default orientation is R0).

Note: To undo the previous action, use the *Undo* widget or U bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or R bindkey.

Flip/Rotate Selected Instances Fields and Options

Mirror X	Flips the selected instance(s) through the x axis.
Mirror Y	Flips the selected instance(s) through the y axis.
R90	Rotates the selected instance(s) 90 degrees.
R180	Rotates the selected instance(s) 180 degrees.
R270	Rotates the selected instance(s) 270 degrees.

Related Text Commands

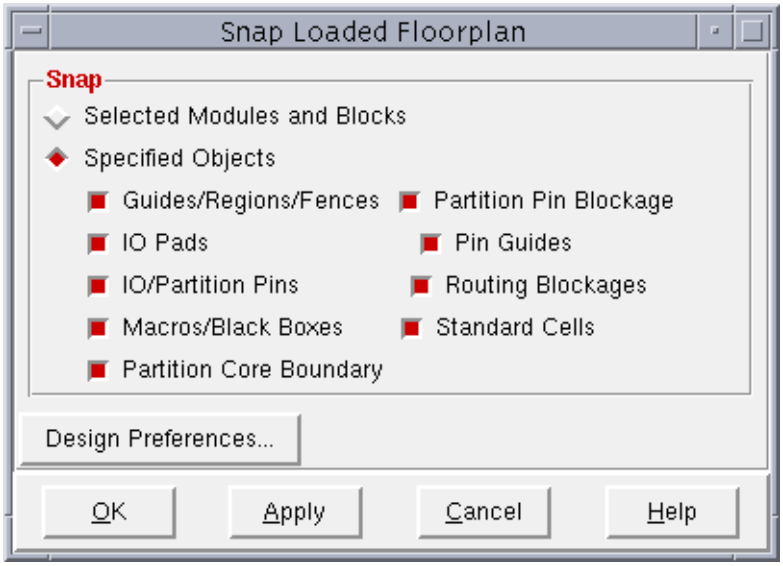
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `flipInst`
- `rotateInst`

Snap Floorplan

Use the Snap Loaded Floorplan form to snap objects to the grid. You can define the snap grid in the Preferences form (see Preferences – Floorplan on page 277).

➤ Choose *Floorplan – Snap Floorplan*.



Alternatively, you can click the middle mouse button to bring up a context sensitive pop-up menu to select the *Snap* command.

Note: To undo the previous action, use the *Undo* widget or U bindkey. To restore the design to the same state as before the undo, use the *Redo* widget or R bindkey.

Snap Loaded Floorplan Fields and Options

Selected Modules and Blocks	Specifies snapping floorplan modules and blocks that are selected in the design display area.
Specified Objects	Specifies snapping one or more of the following floorplan objects
Guides/Regions/Fences	Specifies snapping floorplan guides, regions, and fences.
IO Pads	Specifies snapping floorplan I/O pads.
IO Pins/Partition Pins	Specifies snapping floorplan I/O pins and partition pins.

Macros/Blackboxes	Specifies snapping floorplan macros (hard blocks).
Partition Core Boundary	Specifies snapping floorplan partition core boundary. **Note:** This will snap to core-grid. However, if the partition is a power-domain, this will snap to placement grid.
Partition Pin Blockage	Specifies snapping floorplan partition pin blockage.
Pin Guides	Specifies snapping floorplan pin guides. **Note:** This will snap to mfg. grid and not to tracks.
Routing Blockages	Specifies snapping floorplan routing blockages.
Standard Cells	Specifies snapping floorplan standard cells.
Design Preferences...	Brings up the Design Preferences GUI.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `snapFPlan`
- `snapFPlanIO`

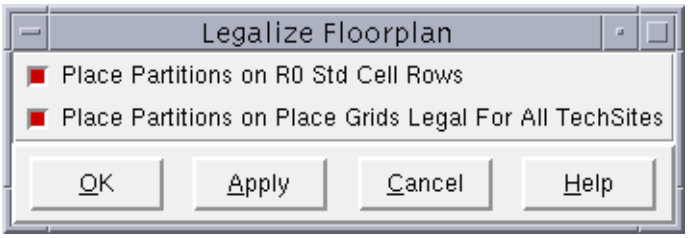
Legalize Floorplan

Use the Legalize Floorplan form for cases where you might have to legalize partition locations according to standard cell row orientations or specific constraints of your design. For each partition, the software checks if it overlaps with any row cutting areas. If it does, the software finds the closest location where the partition has no overlap with any row cutting area.

If the horizontal distance between the new location and old location is less than or equal to the width of the partition, and the vertical distance between the new location and old location is less than or equal to the height of the partition, the software moves the partition to a new location.

Note: If no legalization rules are specified, the Encounter software does not check any legal rules.

➤ Choose *Floorplan – Edit Floorplan – Legalize Floorplan*.



Legalize Floorplan Fields and Options

Place Partitions on R0 Std Cell Rows

Specifies that all partitions snap to the closest `R0` row on the grid. For this rule, the Encounter software assumes that standard cell rows start with an `R0` orientation and continue in an `R0`-to-`MX` pattern.

Place Partitions on Place Grids Legal For All TechSites

Specifies that partitions be placed on grids so that they are legal for all design constraints.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

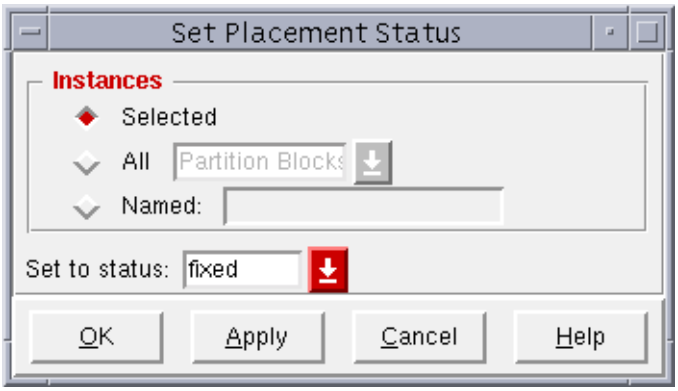
- `legalizeFPlan`

Set Block Placement Status

Use the Set Placement Status form to change placement status for all instances or selected instances.

Note: This cannot be used to change the placement status of standard cells.

➤ Choose *Floorplan – Edit Floorplan – Set Block Placement Status*.



Set Placement Status Fields and Options

Selected	Specifies all instances selected (highlighted) in the design display area.
All	Specifies the type of instance to enclose macros. Use the pull-down menu to choose *Hard Macros*, *Partition Blocks*, or *Black Boxes*.
Named	Specifies a particular instance. You can use a wildcard character (*) in this field.
Set to status	Use the pull-down menu to specify a *cover*, *fixed*, *placed*, or *unplaced* placement status for the specified instances.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

■ `setBlockPlacementStatus`

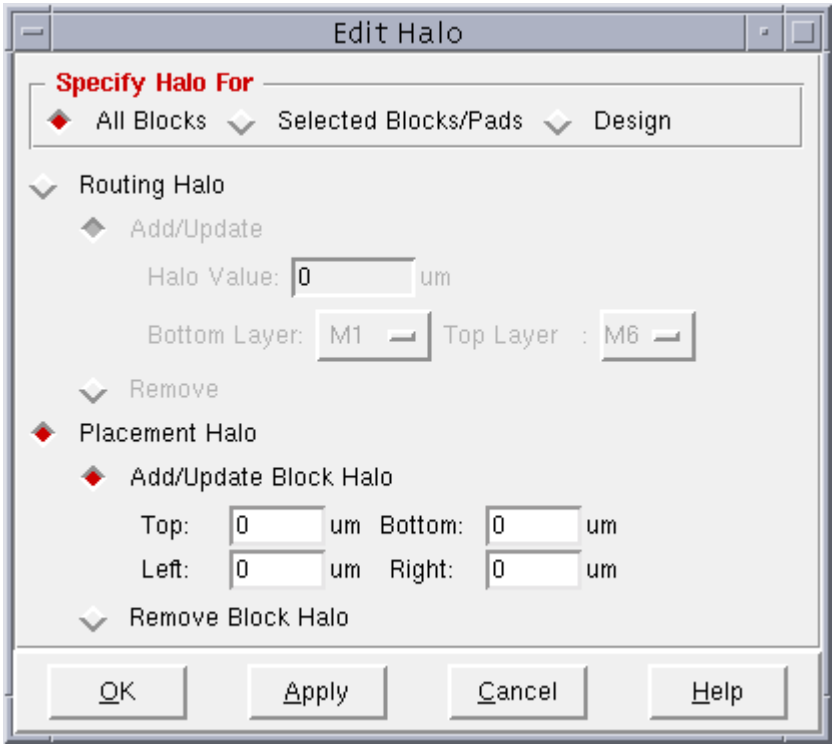
Edit Halos

Use the Edit Block Halo form to add a routing halo or a placement halo to prevent the routing and/or placement of blocks and standard cells in order to reduce congestion around a block. These halos can be specified for hard macros, blackboxes, or committed partitions. When you add a halo to a block, it becomes part of the block's properties. If you move the block, the halo moves with it.

For the bottom-up hierarchical flow, use this form to specify routing halo for a block at the top-level design or at the block-level design.

Note: For top-down hierarchical flow, specify routing halo for a partition through the Specify Partition form.

➤ Highlight block(s) in the design display area and choose *Floorplan – Edit Floorplan* – Edit *Halos*.



Edit Halos Fields and Options

All Blocks	Specifies that the halo will be created for all blocks.

Selected Blocks	Specifies that the halo will be created for the selected blocks.	
Design	Specifies that the halo will be created at the design level.	
Add/Update	Adds or overrides the routing halo. Define the halo using the following fields.	
	Halo Value	Specifies the value for the routing halo.
	Bottom Layer	Specifies the bottom layer for the routing halo.
	Top layer	Specifies the top layer for the routing halo.
Remove	Removes the routing halo.	
Add/Update Block Halo	(Default) Adds or overwrites a placement halo. Define the halo using the following fields:	
	Top	Specifies the distance, in micrometers, from the top edge of the block to the end of the halo area.
	Bottom	Specifies the distance, in micrometers, from the bottom edge of the block to the end of the halo area.
	Left	Specifies the distance, in micrometers, from the left edge of the block to the end of the halo area.
	Right	Specifies the distance, in micrometers, from the right edge of the block to the end of the halo area.
Remove Block Halo	Removes the placement halo.	

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

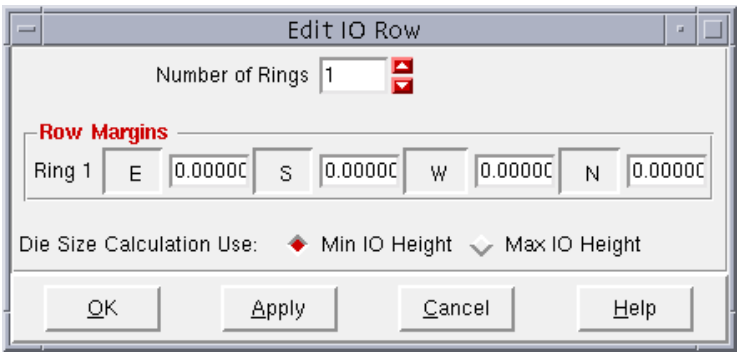
- `addHaloToBlock`
- `addRoutingHalo`
- `deleteHaloFromBlock`

- deleteRoutingHalo

Edit IO Row

Use the Edit IO Row form to specify I/O pad rings and row margins. You can use this form to create symmetric or asymmetric I/O rows.

➤ Choose *Floorplan – Edit Floorplan – Edit IO Row*.



Edit IO Row Fields and Options

Number of Rings	Specifies the number of I/O rings needed for the placement.
Row Margins	Specifies the distance between the die boundary edge to the I/O row edge, in microns, where `E` is the East side, `S` is the South side, `W` is the West side, and `N` is the North side.
Die Size Calculation Use	Select either the minimum or maximum height that will be used to calculate the design size.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `placePadIO`
- `saveIoFile`
- `setIoRowMargin`

Core Row

You can create, edit, delete and stretch core rows for a site.

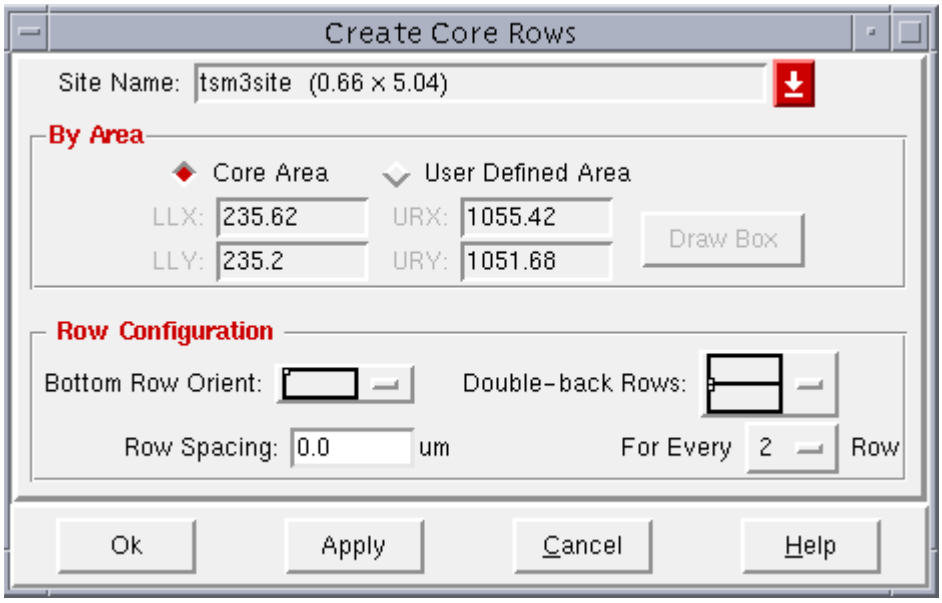
The Core Row Menu contains the following forms:

- Create Core Rows on page 638
- Cut Core Rows on page 640
- Stretch Selected Rows on page 642

Create Core Rows

Use the *Create Row* form to create rows for the specified site, both inside and outside the core area, but within the die.

➤ Choose *Floorplan – Edit Floorplan – Core Row – Create*.



Create Core Rows Fields and Options

Site Name	Specifies the name of the site for which rows will be created.
Core Area	Specifies the lower-left and upper-right x and y coordinates within the core area of site for which rows will be created. The coordinates of the core area core area are selected by default.
User Defined Area	If selected, you can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the area in which rows will be created.
Bottom Row Orient	Specifies whether the first row is not flipped (default) or flipped.
Double-back Rows	Specifies whether rows are created back-to-back or not.

Row Spacing For Every # rows

Specifies the standard row spacing, in micrometers. This must be a positive value. By default, this value is zero. In the *For Every Row* pull-down menu, specify *1* for every row, or *2* for every other row.

Related Text Commands

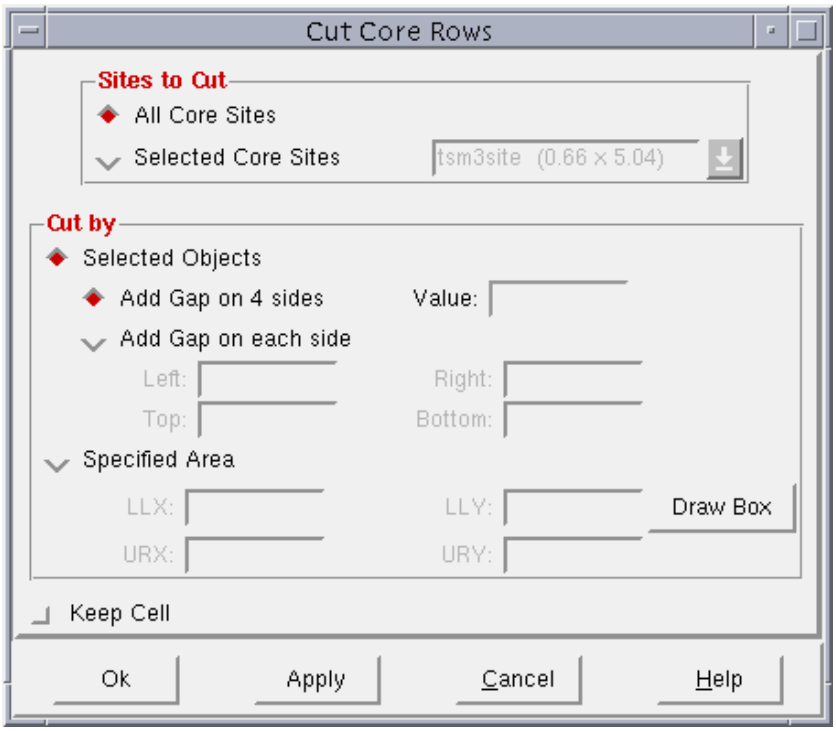
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `createRow`
- `cutRow`
- `deleteRow`
- `stretchRows`

Cut Core Rows

Use the *Cut Core Rows* form to cut site rows that intersect with the specified area or selected object(s).

➤ Choose *Floorplan – Edit Floorplan – Core Row – Cut*.



Cut Core Rows Fields and Options

All Core Sites	Specifies that rows will be cut for all core sites.
Selected Core Sites	Specifies the core site for which rows will be cut.
Selected Objects	Specifies that rows that intersect with the selected objects will be cut.
Add Gap on 4 Sides	Specifies the additional space to be provided on the left, right, top, and bottom sides of the selected objects. The same value will be used for all sides.
Add Gap on each side	Specifies the additional space to be provided on the top, bottom, left, and right sides respectively of the selected objects.

Specified Area	Specifies the lower-left and upper-right x and y coordinates within the core area of site for which rows will be created. The coordinates of the core area core area are selected by default.
Draw Box	You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the area for which rows will be cut.
Keep Cell	Specifies that all cells that are placed inside the cut row area will not be unplaced. *Default*: By default, all cells inside the target area will be unplaced.

Related Text Commands

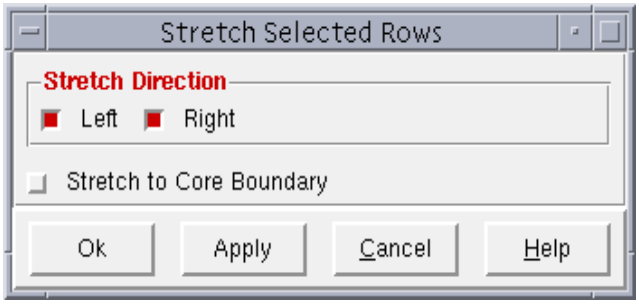
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `createRow`
- `cutRow`
- `deleteRow`
- `stretchRows`

Stretch Selected Rows

Use the *Stretch Selected Rows* form to stretch selected rows.

➤ Choose *Floorplan – Edit Floorplan – Core Row – Stretch*.



Stretch Selected Rows Fields and Options

Left	Specifies that the left edge of all selected rows should be aligned to the left-most edge among all selected tows
Right	Specifies that the right edge of all selected rows should be aligned to the right-most edge among all selected rows
Stretch to Edge of Core Boundary	Specifies that row edges should be aligned to the core boundary.

Related Text Commands

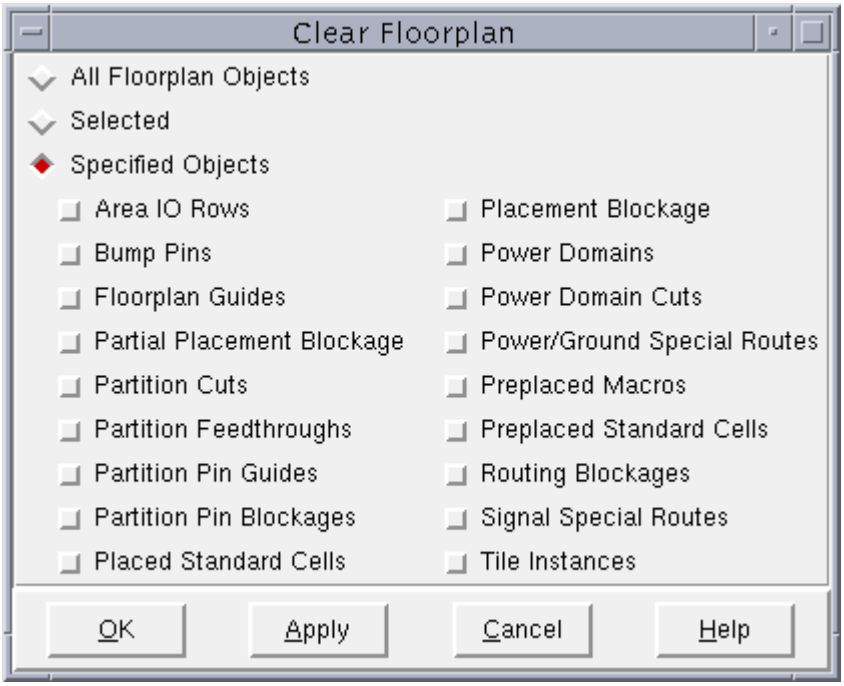
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `createRow`
- `cutRow`
- `deleteRow`
- `stretchRows`

Clear Floorplan

Use the Clear Floorplan form to remove the design's floorplan constraints. You can clear these constraints at any time. If any floorplan constraints are changed, you must run, or rerun, the placement program.

➤ Choose *Floorplan – Clear Floorplan*.



Clear Floorplan Fields and Options

All Floorplan Objects	Clears all floorplan objects, including instance groups.
Selected	Clears all floorplan objects currently selected in the design window.
Specify Objects	Clears all the specified objects. You can specify one or more of the following objects.
	Area IO Rows — Removes all area I/O rows
	Bump Pins — Removes all bump pins.
	Floorplan Guides — Removes all module constraints. The modules will be unplaced outside the core area.

Partial Placement Blockages

Removes all partial placement blockages (area density screens)

Partition Cuts Removes all partition cuts for partition modules.

Partition Feedthroughs

Removes all partition feedthrough guides for the partition modules.

Partition Pin Guides

Removes all partition pin guides for partition modules.

Partition Pin Blockages

Removes all partition pin blockages for partition modules.

Placed Standard Cells

Unplaces all standard cells that have a fixed placement status.

Placement Blockage

Removes all placement blockages.

Power Domains Removes all power domain objects.

Power Domain Cuts

Removes all power domain cuts.

Power/Ground Special Routes

Removes all power and ground special wires.

Preplaced Macros

Unplaces all preplaced macros.

Preplaced Standard Cells

Unplaces all preplaced standard cells.

Routing Blockages

Removes all routing blockages.

Signal Special Routes

Removes all signal special routes.

Tile Instances

Removes all tile instances.

Related Text Commands

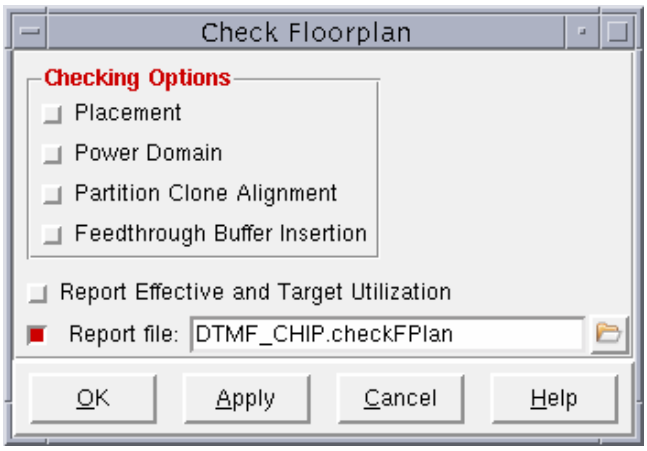
For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `deleteAllDensityAreas`
- `deleteAllFPObjects`
- `deleteAllObstruction`
- `deleteAllPowerPreroutes`
- `deleteAllRouteBlks`
- `deleteAllSignalPreroutes`

Check Floorplan

Use the Check Floorplan form to identify problems before a design is passed to downstream tools. You can check the routing grid, placement, pins, power domains, partition clone alignment, and feedthrough buffer insertion.

➤ Choose *Floorplan – Check Floorplan*.



Check Floorplan Fields and Options

Placement	Checks the placement.
Power Domains	Checks the power domains.
Partition Clone Alignment	Checks that partition clones are aligned with their master on the power mesh. This checks that the master and clones partitions are inside a core boundary, and ensures that the partition fence instances sizes match the master instance.
Feedthrough Buffer Insertion	Checks feedthrough buffer insertion.
Report Effective and Target Utilization	Reports effective utilization (EU) and target utilization (TU) for the entire design, fences, and regions (partitions, power domains, and regular fences).
checkFPlan Report File	Outputs detailed information for the specified checks. The default filename is `hdr_top.checkFPlan`.

Related Text Commands

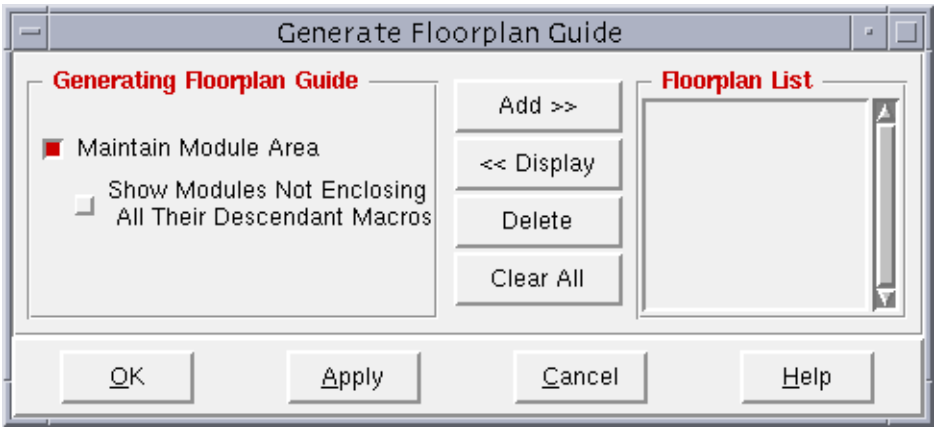
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `checkFPlan`

Generate FP Guide

Use the Generate FP Guide form to generate the module guides and update the display.

➤ Run the placement program, or load or import a placement file, and choose *Floorplan – Generate FP Guide*.



Generate FP Guide Fields and Options

Maintain Module Area	Keeps the module's physical size roughly equivalent to the module's placement size when generating the floorplan guide. Use this when working with a top-level partition floorplan.
Show Modules Not Enclosing All Their Descendant Macros	Highlights the blocks in the design display area and resizes the module to enclose all of the blocks.
Add >>	Temporarily saves the floorplan version to a name in the *Floorplan List*.
<< Display	Redisplays the floorplan version from the *Floorplan List*.
Delete	Deletes the floorplan version from the *Floorplan List*.
Clear All	Deletes all floorplan versions from the *Floorplan List*.

Related Text Commands

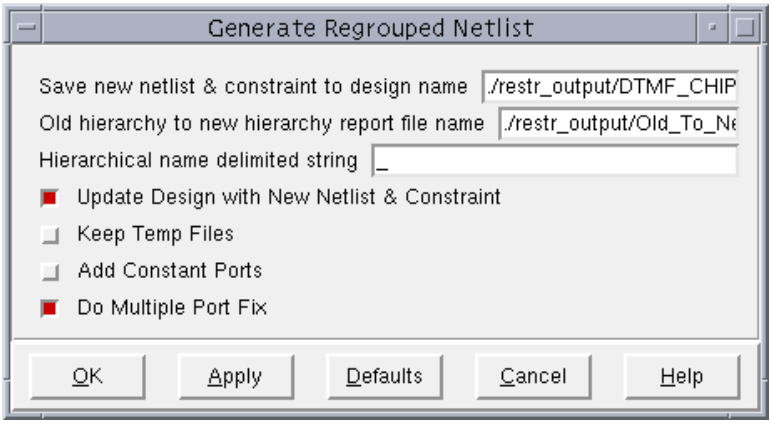
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `generateGuide`

Generate Regrouped Netlist

Use the Generate Regrouped Netlist form to save instance groups back to the netlist.

➤ Choose *Floorplan – Generate Regrouped Netlist*.



Generate Regrouped Netlist Fields and Options

Save new netlist & constraint to design name

Specifies the new directory prefix where the data will be stored. The default name is `top_module_restruct.enc`.

Old hierarchy to new hierarchy report file name

Specifies a report file that provides the mapping between the old and new logical hierarchy. This enables you to provide the report file directory and file name.

Hierarchical name delimited string

Generates the hierarchical name for moved instances after restructuring. For example, if you have an original hierarchy of `/a/b/c` and want to place module `c` into a new module called `r`, using the following delimiters will enable you to retain the original hierarchy name after restructuring:

delimiter: _ (underscore)
original hierarchy: `/a/b/c`
new hierarchy: `/r/a_b_c`

delimiter: `/` (slash)
original hierarchy: `/a/b/c`
new hierarchy: `/r/a\/b\/c`

delimiter: `""` (no name delimiter)
original hierarchy: `/a/b/c`
new hierarchy: `/r/c`

Update Design with New Netlist & Constraint

Updates the design netlist and constraints.

Keep Temp Files

Keeps temporary files.

Add Constant Ports

Adds constant ports and avoids additional assign nets for restructured instances. The software creates a constant port to propagate the tie-high and tie-low ports through the new hierarchy. A new netlist is assigned to the port with an assignment of 1.

Do Multiple Port Fix

Specifies that no nets will be split.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `runRcNetlistRestruct`

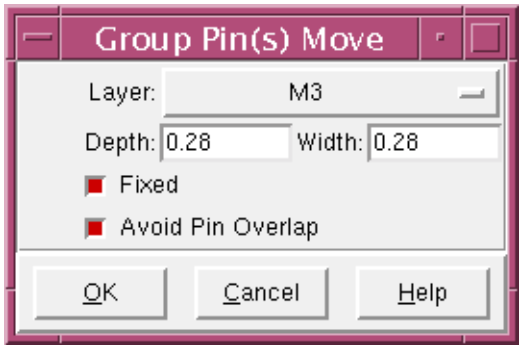
Group Pin(s) Move

Use the Group Pin(s) Move form to change the pin layer, the pin size, pin status, and resolve pin overlap.

Complete the following steps in the design display area:

1. Click the *Move/Resize/Reshape* widget.
2. Left click on the pin.

   For a group of pins, press the `Shift` key to highlight each pin.
3. Click the *F3* key.



Group Pin(s) Move Fields and Options

Layer	Specifies the layer for the pin or pin group move.
Depth	Specifies the depth of the pin or pin group, in micrometers.
Width	Specifies the width of the pin or pin group, in micrometers.
Fixed	Specifies that the moved pin or group of pins are set to a *fixed* status.
Avoid Pin Overlap	Specifies that pin(s) will be moved to avoid overlaps, if overlaps are present.

Related Text Commands

For information on the following commands, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `moveGroupPins`
- `swapPins`

Related Topics

For information on the following topic, see “Floorplanning the Design” in the *Encounter User Guide*.

- Moving Pins

Swap Two Selected I/O Cells

You can swap the locations of two selected I/O cells.

➤ Select the two I/O cells whose locations you want to swap and click the middle mouse button. From the context menu that appears, select *Swap Instances*.

View Relative Floorplan Through Context Menu

You can access the *Relative Floorplan* form from a context menu (that appears when you click the middle mouse button) of any object that has relative floorplan constraints.

➤ Select the object and click the middle mouse button. From the context menu that appears, select *Relative Floorplan.*

Flip Hierarchical Instances on X-axis or Y-axis

You can flip a hierarchical instance on the x-axis or the y-axis, as follows

➤ Select the hierarchical instance and click the middle mouse button. From the context menu that appears, select *Flip X* or *Flip Y* to flip the hierarchical instance on the x-axis or the y-axis respectively.

All the placed or fixed instances inside the hierarchical instance are also flipped.

7

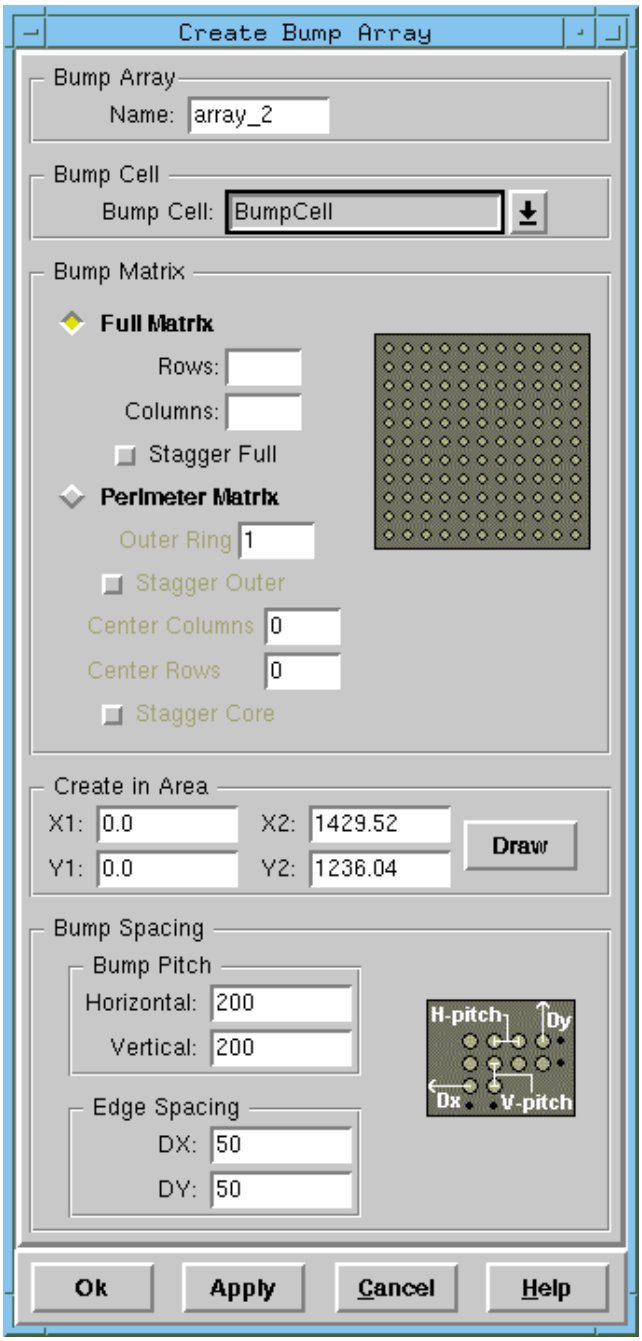
FlipChip Menu

- Create Bump Array on page 658
- Edit Bump Array on page 662
- Add Bump To Array on page 666
- Create Area IO Rows on page 668
- Assign Signals on page 672
- Assign Power/Ground Bumps on page 674
- Unassign Bump on page 676
- Swap Signals on page 677
- Show Pin Status on page 678
- Display Options on page 680

Create Bump Array

Use the Create Bump Array form to specify bump array parameters.

➤ To open the Create Bump Array form, choose *Floorplan – FlipChip – Create Bump Array*.



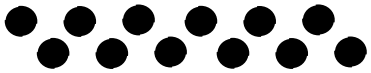
Create Bump Array Fields and Options

Array Name — Specifies the name of the bump array. A drop-down list is available to let you select a specific bump array to edit.

Bump Cell — Specifies the name of the bump cell. A drop-down list is available to enable you to select a specific bump cell.

Full Matrix — Uses the full chip area to create the bump matrix.

- Rows — Specifies the number of rows for the matrix.
- Columns — Specifies the number of rows for the matrix
- *Stagger Full* — Staggers (offsets each column/row) of the full matrix. The following figure shows a stagger pattern.



Perimeter Matrix — Uses the chip perimeter to create an outer bump matrix.

Note: You can use this option with the core columns and rows to create a specific bump pattern.

- *Outer Ring* — Specifies the number of outer rings.
- *Stagger Outer* — Staggers the bumps in the outer ring.

Center Columns — Number of columns of the bump array when creating bumps in the die center.

Center Rows — Number of rows of the bump array when creating bumps in the die center

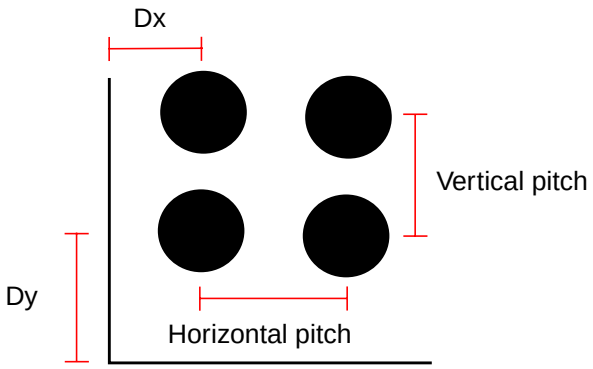
- *Stagger Core* — Staggers (offsets each column/row) of the core bump matrix.

Create in Area — Specifies the area coordinates of the bump array and outlines the legal area where bumps can be placed. For example, a bump would not be placed on the coordinates for the edge of the box, the bumps would be placed at the first legal location within the area.

Draw Button — Gets the area coordinates (above) when you create a box with the mouse.

Bump Pitch	Determines the vertical and horizontal spacing between bumps.
Horizontal	Specifies the horizontal distance, in microns, between bump centers.
Vertical	Specifies the vertical distance, in microns, between bump centers.
Edge Spacing	Sets up the point where the tile grid starts. Legal placement for bumps will be based on the bump pitch from this point.
DX	Specifies the horizontal offset, in microns, to be reserved from the left and right edges to the center of the outermost bumps.
DY	Specifies the vertical offset, in microns, to be reserved from the top and bottom edges to the center of the outermost bumps.

Pitch and Edge Spacing Parameters



Related Text Commands

For information on the following text command, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `ciopCreateBump`

Related Topics

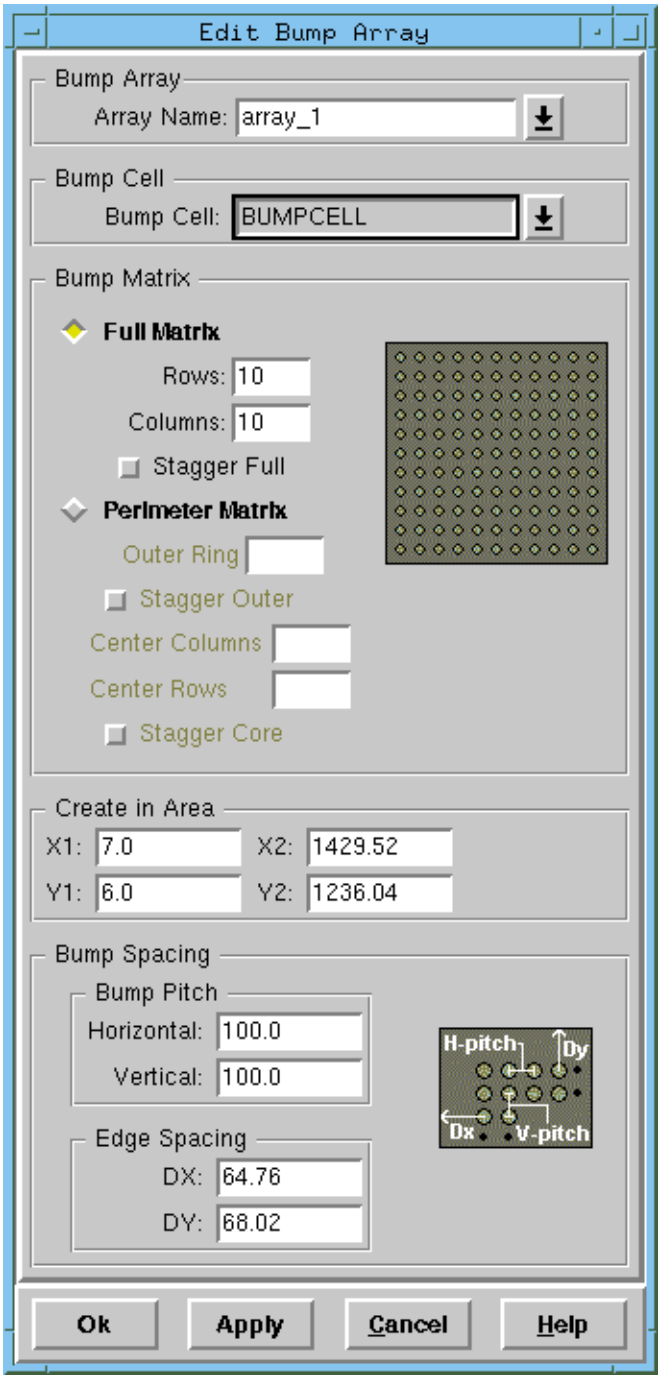
For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Bump Flow
- Flip Chip Flow in Encounter

Edit Bump Array

Use the Edit Bump Array form to edit the bump array parameters.

➤ To open the Edit Bump Array form, choose *Floorplan – FlipChip – Edit Bump Array*.



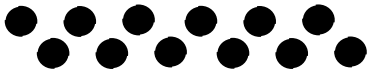
Edit Bump Array Fields and Options

Array Name — Specifies the name of the bump array. A drop-down list is available to let you select a specific bump array to edit.

Bump Cell — Specifies the name of the bump cell. A drop-down list is available to enable you to select a specific bump cell.

Full Matrix — Uses the full chip area to create the bump matrix.

- Rows — Specifies the number of rows for the matrix.
- Columns — Specifies the number of columns for the matrix.
- *Stagger Full* — Staggers (offsets each column/row) of the full matrix. The following figure shows a stagger pattern.



Perimeter Matrix — Uses the chip perimeter to create an outer bump matrix.

Note: You can use this option with the core columns and rows to create a specific bump pattern.

- *Outer Ring* — Specifies the number of outer rings.
- *Stagger Outer* — Staggers the bumps in the outer ring.

Center Columns — Number of columns of the bump array when creating bumps in the die center.

Center Rows — Number of rows of the bump array when creating bumps in the die center

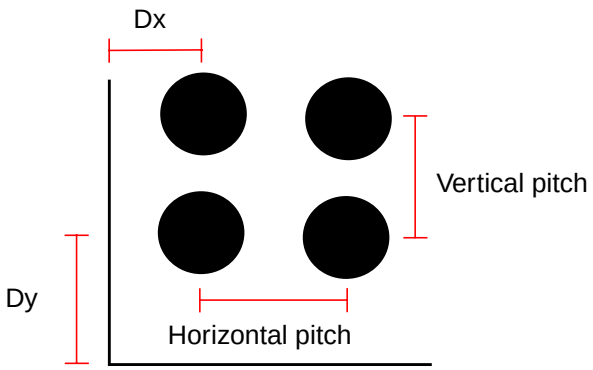
- *Stagger Core* — Staggers (offsets each column/row) of the core bump matrix.

Create in Area — Specifies the area coordinates of the bump array and outlines the legal area where bumps can be placed. For example, a bump would not be placed on the coordinates for the edge of the box, the bumps would be placed at the first legal location within the area.

Bump Pitch — Determines the vertical and horizontal spacing between bumps.

Horizontal	Specifies the horizontal distance, in microns, between bump centers.
Vertical	Specifies the vertical distance, in microns, between bump centers.
Edge Spacing	Sets up the point where the tile grid starts. Legal placement for bumps will be based on the bump pitch from this point.
DX	Specifies the horizontal offset, in microns, to be reserved from the left and right edges to the center of the outermost bumps.
DY	Specifies the vertical offset, in microns, to be reserved from the top and bottom edges to the center of the outermost bumps.

Pitch and Edge Spacing Parameters



Related Text Commands

For information on the following text commands, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `addBumpToArrayGrid`
- `ciopCreateBump`
- `deleteBumpArray`
- `editBumpArray`
- `selectBumpArray`

Related Topics

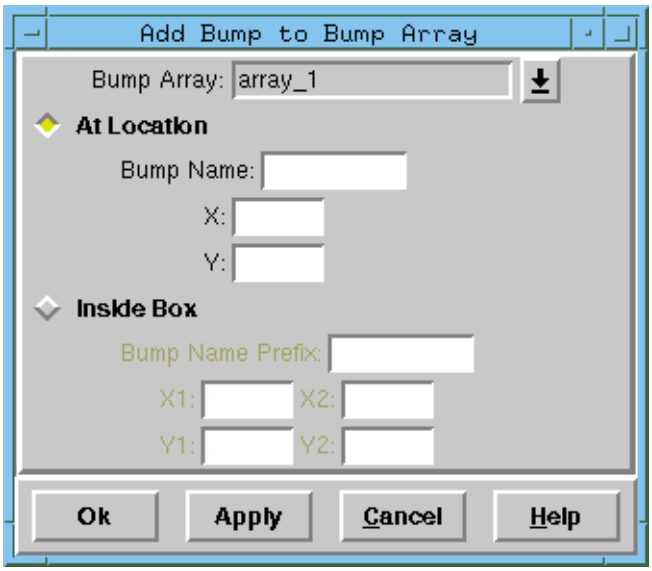
For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Bump Flow
- Flip Chip Flow in Encounter

Add Bump To Array

Use the Add Bump to Bump Array form to add bumps to a bump array.

➤ To open the Add Bump to Bump Array form, choose *Floorplan – FlipChip – Add Bump To Array*.



Add Bump To Bump Array Fields and Options

Bump Array	Specifies the name of the bump array grid.	
At Location	Specifies the location of where to add the bump.	
	Bump Name	Specifies the name of the bump.
	X	Specifies the lower left *X* coordinate of the first bump. Units in microns.
	Y	Specifies the lower left *Y* coordinate of the first bump. Units in microns.

Related Text Commands

For information on the following text commands, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `addBumpToArrayGrid`
- `ciopCreateBump`
- `deleteBumpArray`
- `editBumpArray`
- `selectBumpArray`

Related Topics

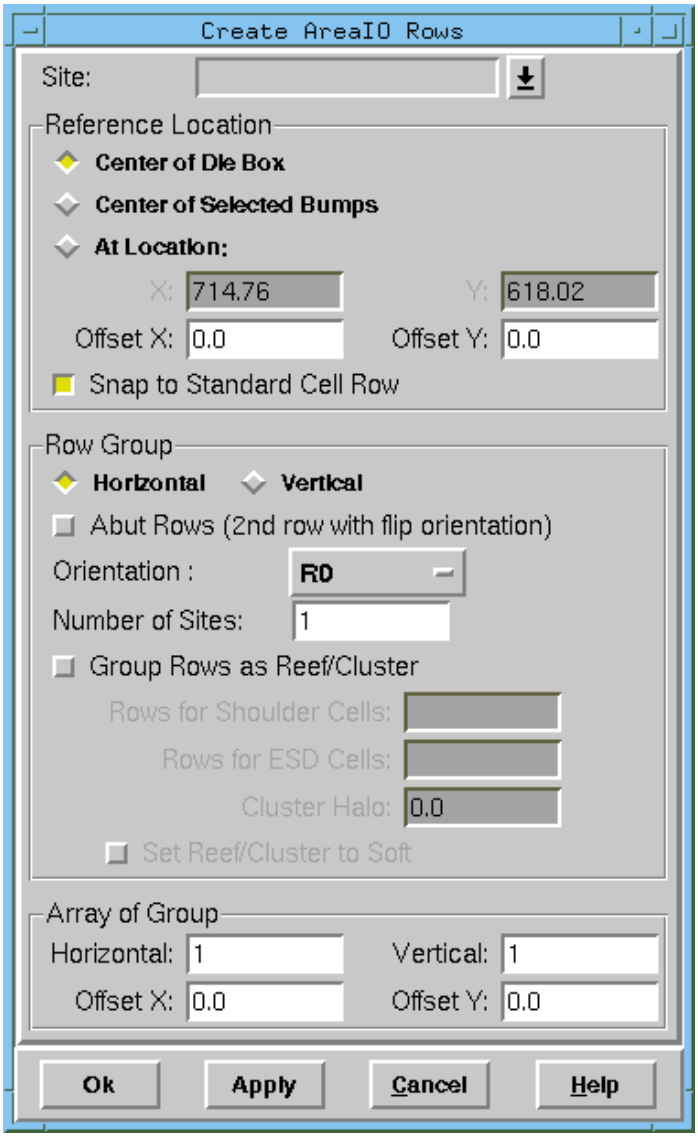
For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Bump Flow
- Flip Chip Flow in Encounter

Create Area IO Rows

Use the *Create AreaIO Rows* form to specify I/O driver row parameters.

➤ To open the Setup Chip IO – IO Driver Row form, choose *Floorplan – FlipChip – Create Area IO Row*.



Setup Chip IO – IO Driver Row Fields and Options

Center of Die Box	Specifies that the row location is at the center of the chip area.
Center of Selected Bumps	Specifies that the row location is at the center of the selected bump.
At Location	Specifies the exact coordinates of the row, in microns, using the following parameters:
X	Specifies the lower-left `X` coordinate of the row.
Y	Specifies the lower-left `Y` coordinate of the row.
Offset X	Specifies the lower-left offset from the `X` coordinate of the row.
Offset Y	Specifies the lower-left offset from the `Y` coordinate of the row.
Horizontal or Vertical	Specifies the selected row as either horizontal or vertical.
Abut Rows	Creates two rows that abut each other in a flip orientation.
Orientation	Specifies the orientation of the row. For more information, see Orientation Key on page 670.
Number of Sites	Specifies the site multiplier number. The base unit for *Number of Sites* is determined by the `SITE` statement in the LEF file and shows up as the value of *Total* in the *Site to be Created* panel. For an example, see step 3 of the Bump Flow in the *Encounter User Guide*.
Group Rows as Reef/Cluster	Specifies selected row as a grouped object. Use this option if you want to group I/O drivers in a cluster in the core.
Rows for Shoulder Cells	Specifies the row number where shoulder cells are to be placed. Shoulder cells are typically used on outer rows as special cell clusters.
Rows for ESD Cells	Specifies the row number where electrostatic discharge cell (ESD) rows are to be placed.

Cluster Halo	Specifies the distance, in microns, surrounding the cluster box to prevent other cells from being placed near it.
Set Reef/Cluster to Soft	Specifies that the reef or cluster can be collapsed if no I/O cells are placed in the available spaces within the reef or cluster. Use this option if the cluster site is not fully placed so that standard cells can be placed in these spaces if I/O cells are not placed there.
Array of Group	Specifies the number of sites that are abutted to create the cluster.
Horizontal	Specifies the number of elements on the `X` axis in the array.
Vertical	Specifies the number of elements on the `y` axis in the array.
Offset X	Specifies the offset, in microns, from element to element on the `x` axis of the array.
Offset Y	Specifies the offset, in microns, from element to element on the `y` axis of the array.

Orientation Key

Use the following table as a key to row orientation.

Value	Definition
`R0`	No rotation
`MX`	Mirror through the `x` axis
`MY`	Mirror through the `y` axis
`R180`	Rotate counter-clockwise `180` degrees
`MX90`	Mirror through the `x` axis and rotate counter-clockwise `90` degrees
`R90`	Rotate counter-clockwise `90` degrees
`R270`	Rotate counter-clockwise `270` degrees
`MY90`	Mirror through the `y` axis and rotate counter-clockwise `90` degrees

Related Text Commands

The following text command provides equivalent or additional functionality:

- `addAIORow`

Related Topics

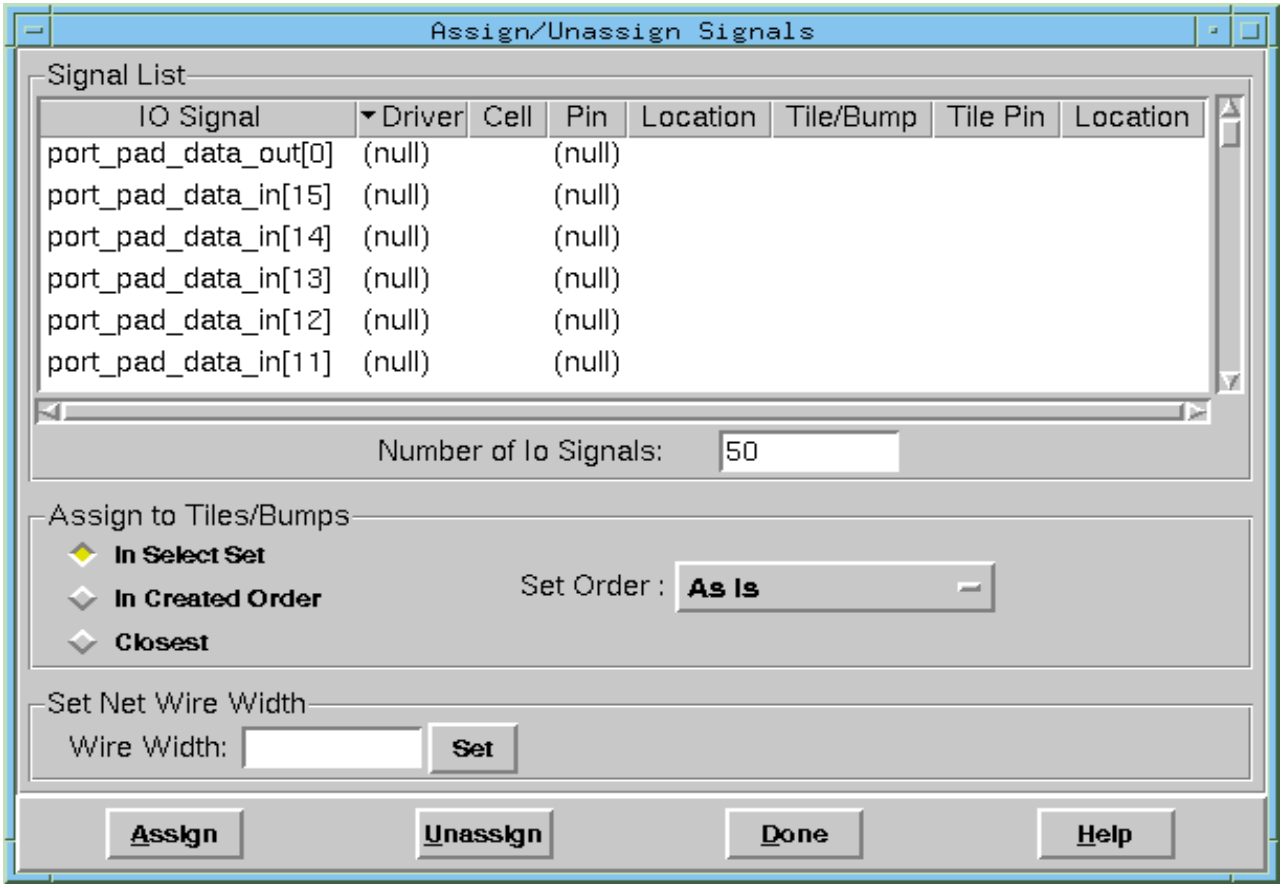
For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- IO_FILE Example
- Flip Chip Flow in Encounter

Assign Signals

Use the Assign/Unassign Signals form to assign and unassign signals to tile pins or bumps.

➤ To open the Assign/Unassign Signals form, choose *Floorplan – FlipChip – Assign Signals*.

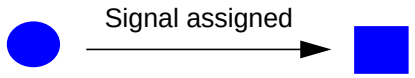


Assign/Unassign Signals Fields and Options

In Select Set	(Default) Specifies the assignment of the signal to a tile pin or a bump according to the selections you make in the design window.
In Created Order	Specifies the assignment of the signal to a tile pin in the order the tiles were created in the database.

Closest	Specifies that the assignment will be done automatically for all signals by assigning them to the closest bumps. **Note:** This option is only available after I/O cells are placed.
As Is	Specifies to use the current order the bumps were selected in the design window.
X, Y Ascend	Assign using ascending `x, y` coordinates of bumps.
X, Y Descend	Assign using descending `x, y` coordinates of bumps.
Y, X Ascend	Assign using ascending `y, x` coordinates of bumps.
Y,X Descend	Assign using descending `y, x` coordinates of bumps.
Wire Width	The width of the wire.

Note: The columns of the *Signal List* table will populate with the bump and tile pin information. When a signal is assigned, the bump changes from a blue-filled circle to a blue-filled square. For example:



Related Text Commands

For information on the following text commands, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `assignBump`
- `assignPGBumps`
- `assignSigToBump`
- `unassignBump`

Related Topics

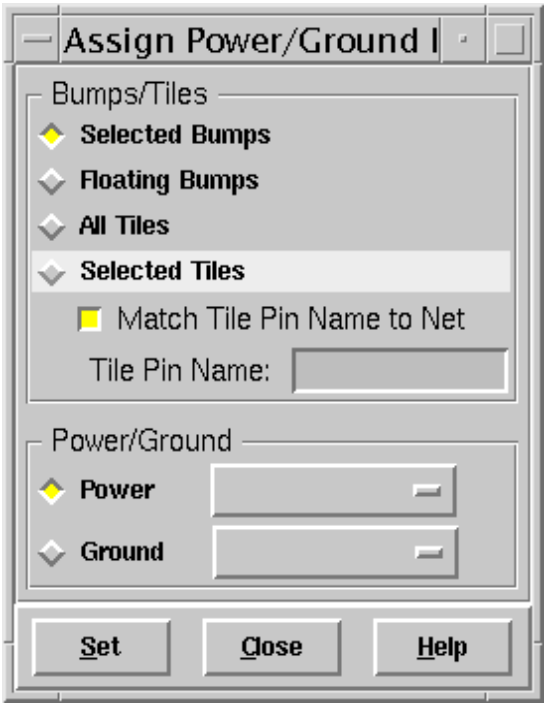
For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Signal Swapping

Assign Power/Ground Bumps

Use the Assign Power/Ground Bumps form to assign power and ground nets to bumps and tiles.

➤ To open the Assign Power/Ground Bumps form, choose *Floorplan – FlipChip – Assign Power/Ground Bumps*.



Assign Power/Ground Bumps Fields and Options

Selected	Specifies that the bumps you have selected will be assigned to the power/ground net selected in the *Power/Ground* panel.
Floating	Specifies that all floating bumps will be assigned to the power/ground net selected in the *Power/Ground* panel.
All Tiles	Specifies that all tiles will be assigned to the power/ground net selected in the *Power/Ground* panel.
Selected Tiles	Specifies that only the tiles you have selected will be assigned to the power/ground net selected in the *Power/Ground* panel.

Match Tile Pin Name to Net	Automatically assigns the appropriate net to the tile pin, matching the power or ground pin to the net of the same name.
Tile Pin Name	When using *Selected Tiles*, you have the option of entering the specific tile pin name to be assigned to the power/ground net selected in the *Power/Ground* panel.
Power	Designates the bump/tile in the *Bumps/Tiles* panel as a power net. Use the pull-down menus to select the power and ground nets (for example, *VDD*).
Ground	Designates the bump/tile in the *Bumps/Tiles* panel as a ground net. Use the pull-down menus to select the power and ground nets (for example, *VSS)*.

Related Text Commands

For information on the following text commands, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `assignPGBumps`

Related Topics

For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Signal Swapping

Unassign Bump

Use the Unassign Bump command to unassign bumps.

➤ To use the Unassign Bump command, select the bump to be unassigned and then choose *Floorplan – FlipChip – Unassign Bump*. There is no form for this menu item.

Related Text Commands

For information on the following text commands, see “Flip Chip Commands” in the *Encounter Text Command Reference*:

- `unassignBump`

Related Topics

For information on the following topics, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

- Signal Swapping

Swap Signals

Use the Swap Signals menu item to swap signals between two bumps. Either one or both of these bumps must be assigned.

➤ To use the Swap Signals command, select the signals to be swapped and then choose *Floorplan – FlipChip – Swap Signals*. There is no form for this menu item.

Related Text Commands

There is no text command for this menu item.

Related Topics

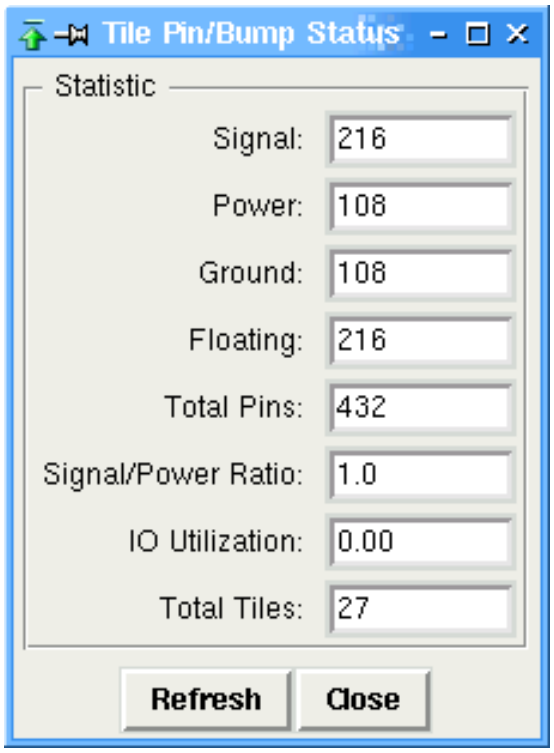
For information on the following topic, see “Flip Chip and Area I/O” in the *Encounter User Guide*:

■ Signal Swapping

Show Pin Status

Use the Tile Pin/Bump Status form to view statistical information about signals, tiles, and bumps.

➤ To open the Tile Pin/Bump Status form, choose *Floorplan – FlipChip – Show Status*



Tile Pin/Bump Status Fields and Options

Signal	Shows the total number of signals.
Power	Shows the total number of power signals.
Ground	Shows the total number of ground signals.
Floating	Shows the total number of floating signals.
Total Pins	Shows the total number of pins.
Signal/Power Ratio	Shows the total number of signals divided by the total number of power and ground signals.

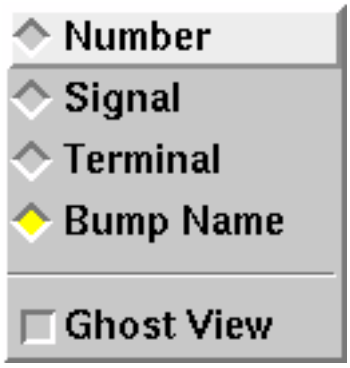
IO Utilization	Shows the utilization number (I/O driver area divided by the I/O row area).
Total Tiles	Shows the total number of tiles.

Display Options

Use the Display Options command to view bump information contained in a tile.

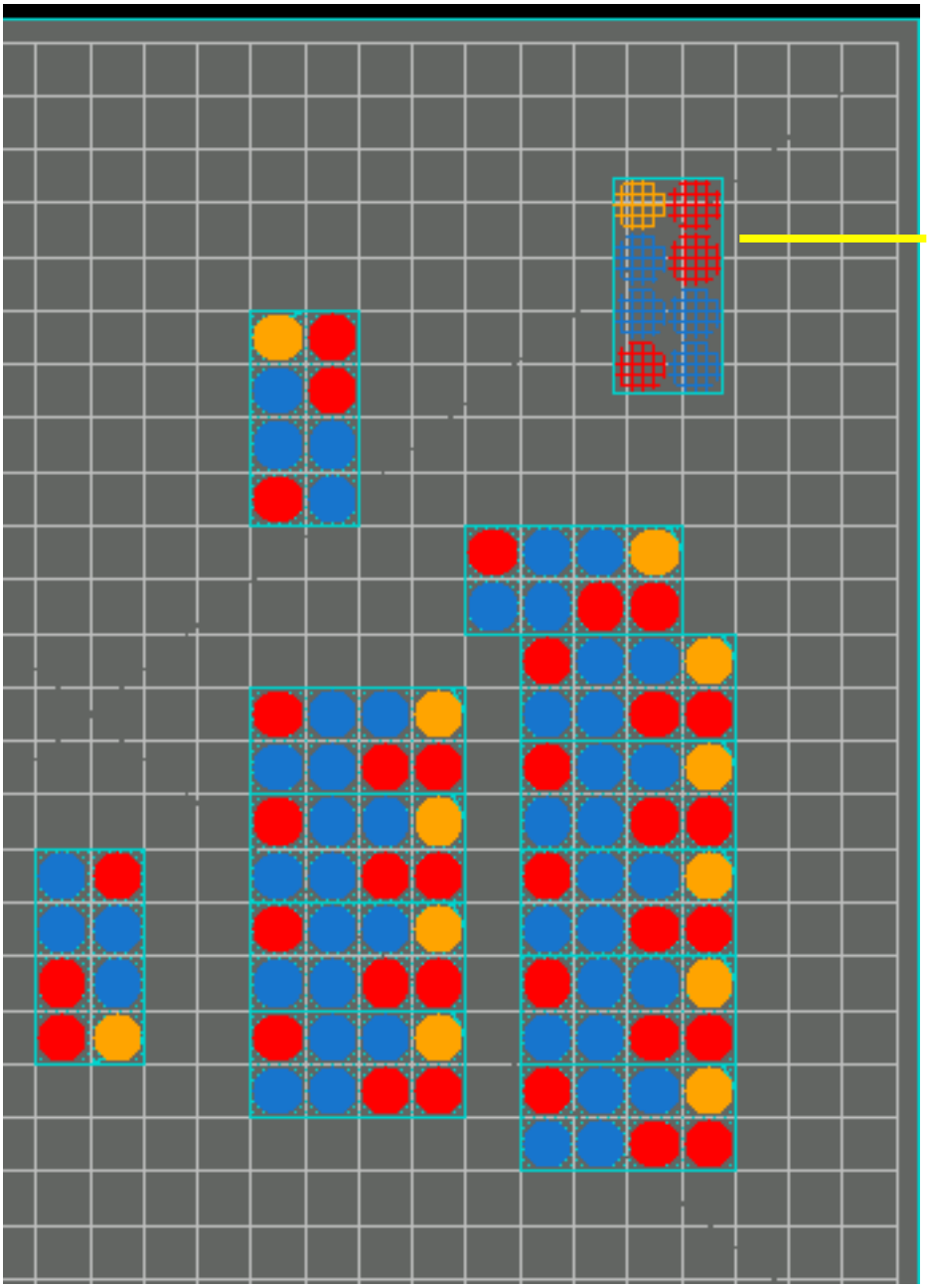
Note: This command is used for tiles only.

➤ To see the Display Options selection, choose *Floorplan – FlipChip – Display Options*.



Display Options Fields and Options

Number	Displays bumps' numbers in the order they occur in the LEF file. You may find this useful when making signal assignments for tiles since signal pairs will have the same number (see Assign Signals on page 672).
Signal	Displays bumps' signal names.
Terminal	Displays bumps' terminal names.
Bump Name	Displays bumps' names.
Ghost View	View the selected tile image master cell to be used to create the instance. The following figure shows a tile in ghost view as it is being placed. If *Ghost View* is not selected, you will not be able to see the tile master cell image as it is being placed.



Related Text Commands

There are no related text commands.

8

Power Menu

- Multiple Supply Voltage on page 684
- Power Planning on page 766
- Power Analysis on page 907
- Rail Analysis on page 936

Multiple Supply Voltage

The Multiple Supply Voltage submenu contains the following items:

- Load/Commit CPF

  Opens the Load/Commit CPF Fields and Options on page 685

- Create/Modify Power Domain

  Opens the Create/Modify Power Domain form.

  Applies only to backward compatibility mode.

- Cut Power Domain by Overlaps

  Opens the Cut Power Domain by Overlaps form.

- Create Shifter Rows

  Opens the Create Shifter Rows form.

- Align Shifter Rows

  Opens the Adjust Power Domain to Align Rows form.

- Shifter/Isolation Cells

  Shows the Shifter/Isolation Cells submenu.

- Add Power Switch

  Opens the Power Switch Insertion forms.

- Delete Power Switch

  Opens the Delete Power Switches form.

- Highlight Power Domains.

  Opens the Highlight Power Domains forms.

- Report Power Domain

  Opens the Report Power Domain form.

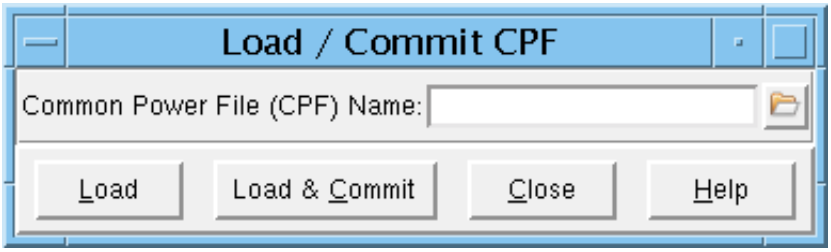
- Verify Power Domain

  Opens the Verify Power Domain form.

Load/Commit CPF

Use the Load/Commit CPF form to load a Common Power Format (CPF) form into the design, or commit a CPF file that you have already loaded.

➤ To open the Load/Commit CPF form, choose *Power – Multiple Supply Voltage – Load/Commit CPF.*



Load/Commit CPF Fields and Options

Commit

Executes the commands provided in the loaded CPF file, such as `create_power_domain`, `create_power_ground_connection`, and `create_*_logic`. As a result, running this command does the following:

- Creates power domains
- Creates logical power/ground net connections
- Specifies timing libraries for power domains
- Inserts shifter cells and isolation cells
- Replaces regular registers with state-retention (SRPG) registers

After running this command, you can then place and floorplan the power domains.

Common Power File (CPF) Name

Specifies the name of the CPF file to load or commit.

Load

Reads the CPF file and performs lint, parsing, and semantics checking. The `loadCPF` command does not execute any of the commands within the CPF file.

If the power/ground connections are incomplete, then the command automatically generates a power net specification template in CPF. You can then examine the template and update it to fully specify the power/ground connections. This command is equivalent to `globalNetConnect` in Encounter, but with limited power domain-oriented functionality.

Load & Commit

Reads the CPF file, as in *Load*, and runs the commands provided in the CPF file. Among many operations, this option does the following:

- Creates power domains
- Creates logical power/ground net connections
- Specifies timing libraries for power domains
- Inserts shifter cells and isolation cells
- Replaces registers with state-retention (SRPG) registers

Related Text Commands

For information about the following text commands, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `loadCPF`
- `commitCPF`

Create/Modify Power Domain

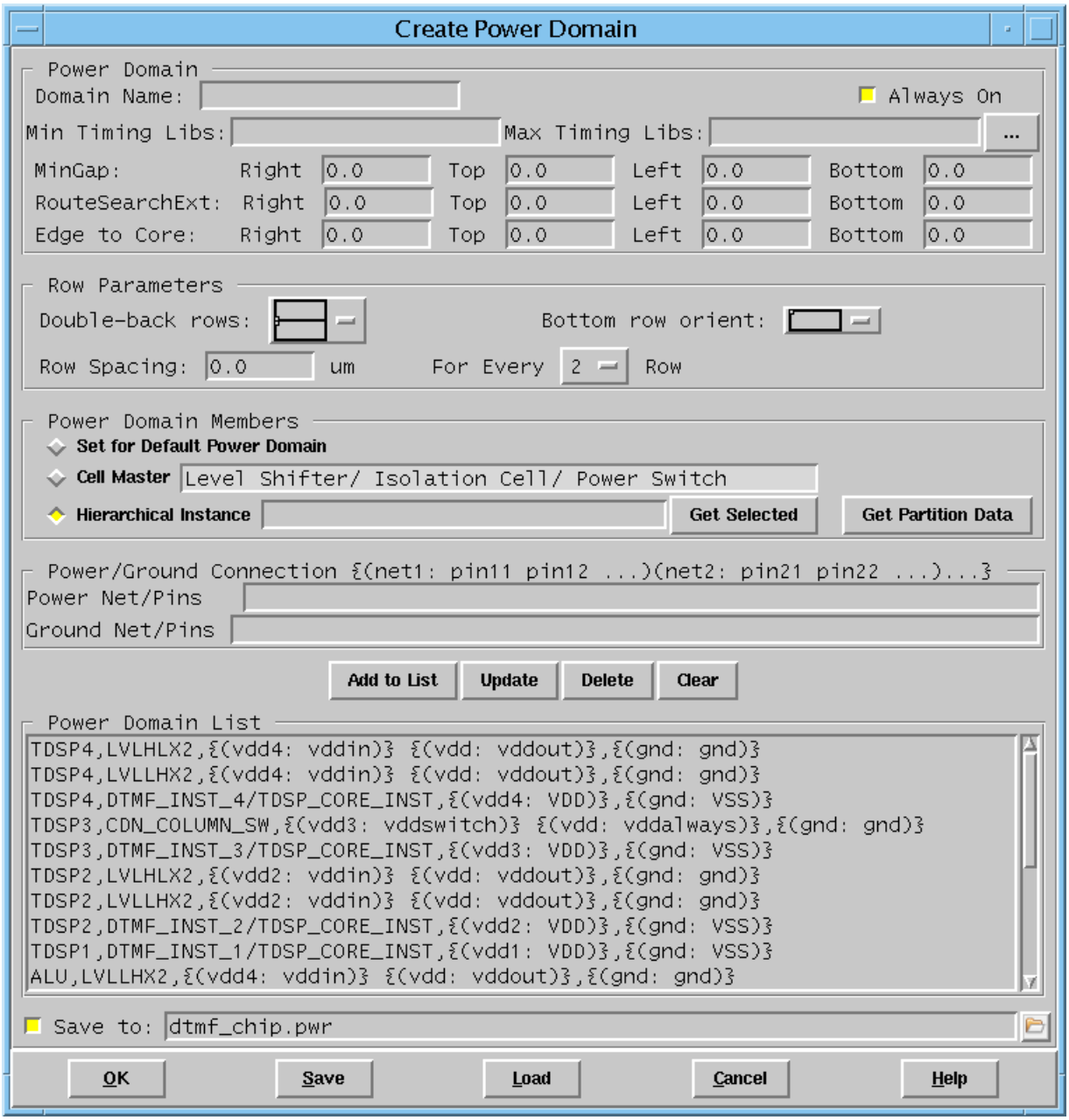
Use the Create Power Domain form to create separate power domains for areas of the design that use different voltage levels.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Create Power Domain form, choose *Power – Multiple Supply Voltage – Create/Modify Power Domain.*



Create Power Domain Fields and Options

Domain Name	The name of the power domain to be created.
Min Timing Libs	Specifies the minimum timing library to associate with the power domain. To choose a timing library, use the Specify Timing Libraries form. For information about using this form, see "Specify Timing Libraries – min" on page 693. If the software is in multi-mode multi-corner mode, the browse (…) button displays the MMMC Browser form instead of the Specify Timing Libraries form. For more information, see MMMC in the "Design Menu" chapter of the *Encounter Menu Reference*. When you click on a delay corner and double click on *Power Domain*, the Add Power Domain form opens. You must specify the power domain for that delay corner, then specify the appropriate libraries in the *Library Set*, *OpCond Lib* and *OpCond* (depending on the *Type* you select). For more information, see Add Power Domain.
Max Timing Libs	Specifies the max timing libraries to associate with the power domain. To choose a timing library, use the Specify Timing Libraries form. For information about using this form, see Specify Timing Libraries – max on page 695. If the software is in multi-mode multi-corner mode, the browse (…) button displays the MMMC Browser form instead of the Specify Timing Libraries form. For more information, see MMMC in the "Design Menu" chapter of the *Encounter Menu Reference*. When you click on a delay corner and double click on *Power Domain*, the Add Power Domain form opens. You must specify the power domain for that delay corner, then specify the appropriate libraries in the *Library Set*, *OpCond Lib* and *OpCond* (depending on the *Type* you select). For more information, see Add Power Domain.
Always On	Specifies whether a power domain is always on.
MinGap	(Optional) The distance, in microns, to be reserved outside the power domain boundary edges for power routing. You cannot enter a negative value. For more information, see Get Partition Data.

RouteSearchExt	(Optional) A distance, in microns, that limits the search for legal targets by the power planning and routing software beyond the power domain boundary. This prevents unwanted connections to targets of the same net that are not associated with the power domain. You cannot enter a negative value. For more information, see Get Partition Data.
Edge to Core	Specifies the distance between the power domain boundary and the core rows. You cannot enter a negative value. For more information, see Get Partition Data.
Double-back rows	Lets you select double-back to populate the power domain. *Default:* Double-back rows
Bottom row orient	Specifies the orientation (north or south) of the bottom row, if you have selected double-back rows. This option is deselected if you selected non-double back rows. *Default:* North
Row spacing	Specifies the distance between rows.
For Every Row	Add info Applies the row spacing to every row, or every pair of rows

Set for Default Power Domain

Disables the *Hierarchical Instance* field, and populates it with the following description:

```
<DEFAULT_PD: includes all modules/instances not in other
Power Domains>
```

Cell Master	Specifies the level shifter, isolation cell, and power switch master names.
Hierarchical Instance	Specifies the hierarchical instance (module) or PAD instance name. The hierarchical instance can be a partition.
Get Selected	Adds the HInsts you have selected in the artwork window to the *Hierarchical Instances* list.
Get Partition Data	If the hierarchical instance you specify is also a partition, this option populates the *MinGap*, *RouteSearchExt*, and *Edge to Core* values you specified when you created the partition. To apply these settings, click *Update*. The partition definition allows only one *MinGap* value, so in this form, all the *MinGap* values are identical.

Power Net/Pins	A list of power net and power pin connections to be included in the power domain. These must be specified in the following format: (*power_net1*: *power_pin1 power_pin2* ...) (*power_net2*: *power_pin3 power_pin4* ....) ...
Ground Net/Pins	A list of ground nets and ground pin connections to be included in the power domain. These must be specified in the following format: (*ground_net1*: *ground_pin1 ground_pin2* ...) (*ground_net2*: *ground_pin3 ground_pin4* ...) ...
Add to List	Adds a new item to the *Power Domain List*.
Update	Modifies the values for the selected item on the *Power Domain List*.
Delete	Removes the selected item from the *Power Domain List*.
Clear	Removes all items from the *Power Domain List*.
Power Domain List	The list of all power domains and their associated modules and power/ground connections. A new item is added to the list whenever you click the *Add to List* button.
Save to	If selected, you can specify a filename, or click the file folder icon and choose a file, to which to save the power domain information. **Note:** To load a saved power domain file, click *Load*. This reads the information in the saved power domain file specified in the *Save to* field.

Related Text Commands

For information about the following text commands, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `createPowerDomain`
- `modifyPowerDomainAttr`
- `modifyPowerDomainMember`

Related Topics

For information on the following topics, see “Low Power Design” in the *Encounter User Guide*.

- Multiple Supply Voltage Flat Flow

Specify Timing Libraries – min

Use the Specify Timing Libraries – min form to select min timing libraries to associate with the power domain. All the cells and macros in the power domain receive their timing and power information from these libraries.

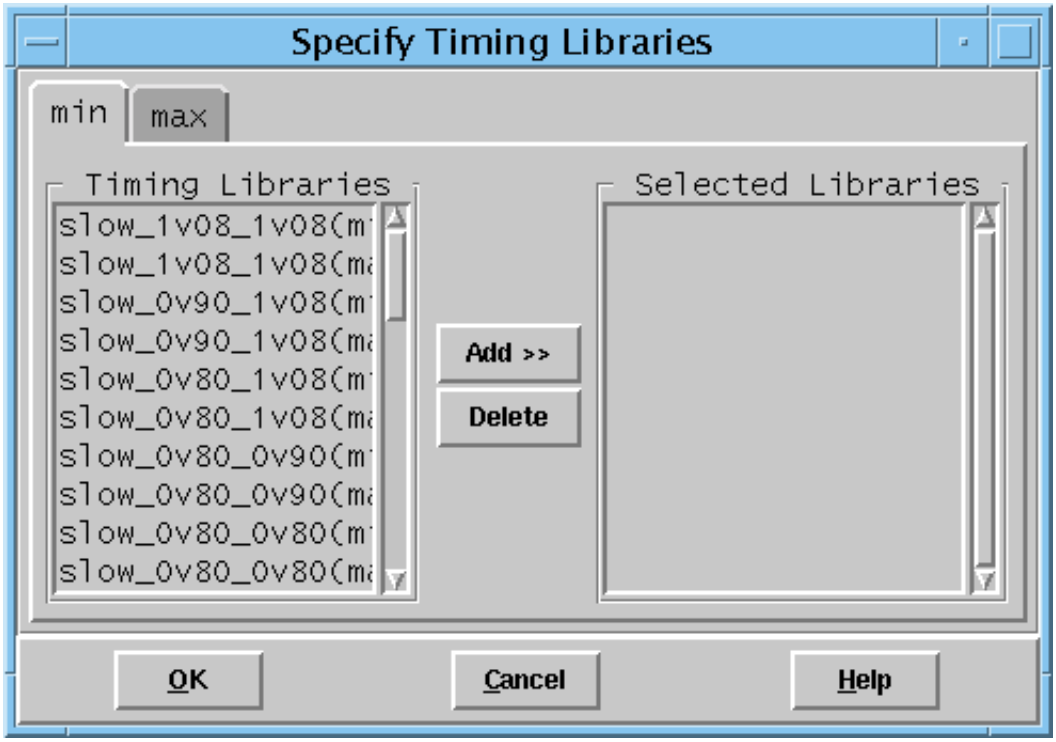
Note: This form opens when the software is not in multi-mode multi-corner mode.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Specify Timing Libraries – min form, choose *Power – Multiple Supply Voltage – Create/Modify Power Domain*, then click the button (...) next to the *Max Timing Libs* field of the Create Power Domain form.



Specify Timing Libraries Fields and Options

Timing Libraries Lists the available timing libraries (`.lib` and TLF).

Add	Adds the selected timing library to the *Selected Libraries* list.
Delete	Removes the selected timing library from the *Selected Libraries* list.
Selected Libraries	Lists the timing libraries (`.lib` and TLF) that will be added to the *Timing Libs* field of the Create Power Domain form. You can include any or all of the available timing libraries.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `createPowerDomain`

Related Topics

For information on the following topic, see “Low Power Design” in the *Encounter User Guide*.

- Multiple Supply Voltage Flat Flow

Specify Timing Libraries – max

Use the Specify Timing Libraries – min form to select max timing libraries to associate with the power domain. All the cells and macros in the power domain receive their timing and power information from these libraries.

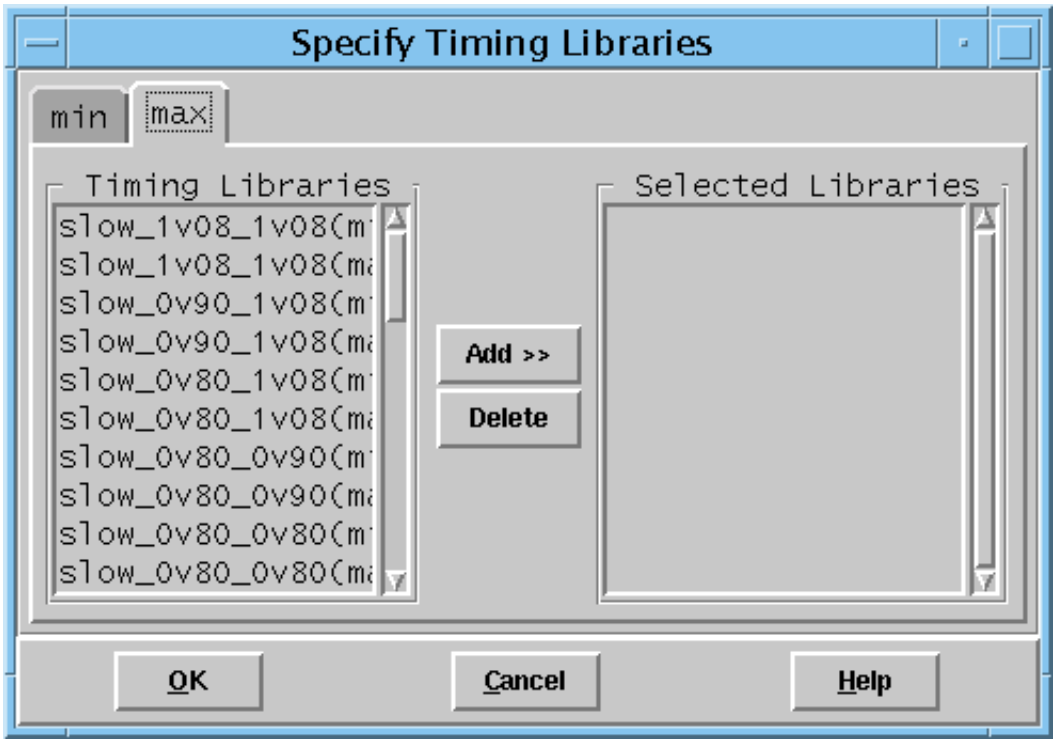
Note: This form opens when the software is not in multi-mode multi-corner mode.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Specify Timing Libraries – max form, choose *Power – Multiple Supply Voltage – Create/Modify Power Domain*, then click the button (...) next to the *Max Timing Libs* field of the Create Power Domain form.



Specify Timing Libraries Fields and Options

Timing Libraries	Lists the available timing libraries (`.lib` and TLF).
Add	Adds the selected timing library to the *Selected Libraries* list.
Delete	Removes the selected timing library from the *Selected Libraries* list.
Selected Libraries	Lists the timing libraries (`.lib` and TLF) that will be added to the *Timing Libs* field of the Create Power Domain form. You can include any or all of the available timing libraries.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `createPowerDomain`

Related Topics

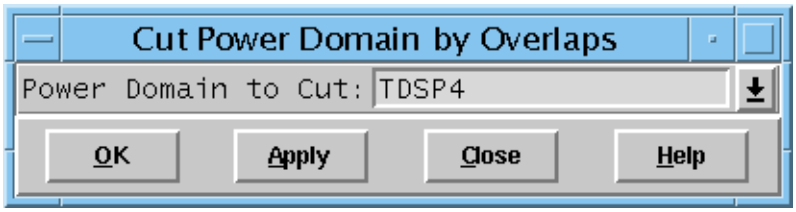
For information on the following topic, see “Low Power Design” in the *Encounter User Guide*.

- Multiple Supply Voltage Flat Flow

Cut Power Domain by Overlaps

Use the Cut Power Domain by Overlaps form to specify the power domain you want to cut to include another power domain you have created.

➤ To open the Cut Power Domain by Overlaps form, choose *Power – Multiple Supply Voltage – Cut Power Domain by Overlaps*.



Cut Power Domain by Overlaps Fields and Options

Power Domain to Cut	Specifies the power domain to cut to include the nested power domain you have created.

Related Text Commands

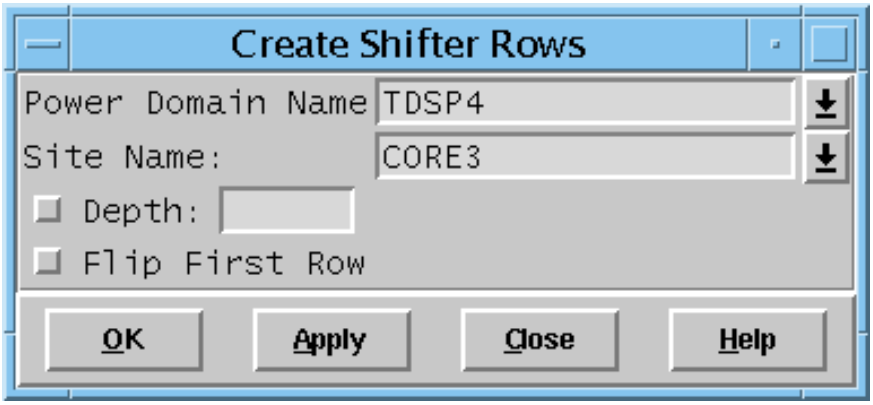
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

■ `cutPowerDomainByOverlaps`

Create Shifter Rows

Use the Create Shifter Rows form to create rows specifically for shifter in a power domain.

➤ To open the Create Shifter Rows form, choose *Power – Multiple Supply Voltage – Create Shifter Rows*.



Create Shifter Rows Fields and Options

Power Domain Name	Specifies the power domain in which you want to create the shifter rows.
Site Name	Specifies the site for the rows.
Depth	Specifies the multiplying factor for each composite row.
Flip First Row	Flips the orientation of the first shifter row. The default orientation is `R0`.
No Flip	Does not flip alternate rows: All the rows have the same orientation.
Left Edge	Creates rows on the left side of the power domain only.
Right Edge	Creates rows on the right side of the power domain only.

Related Text Commands

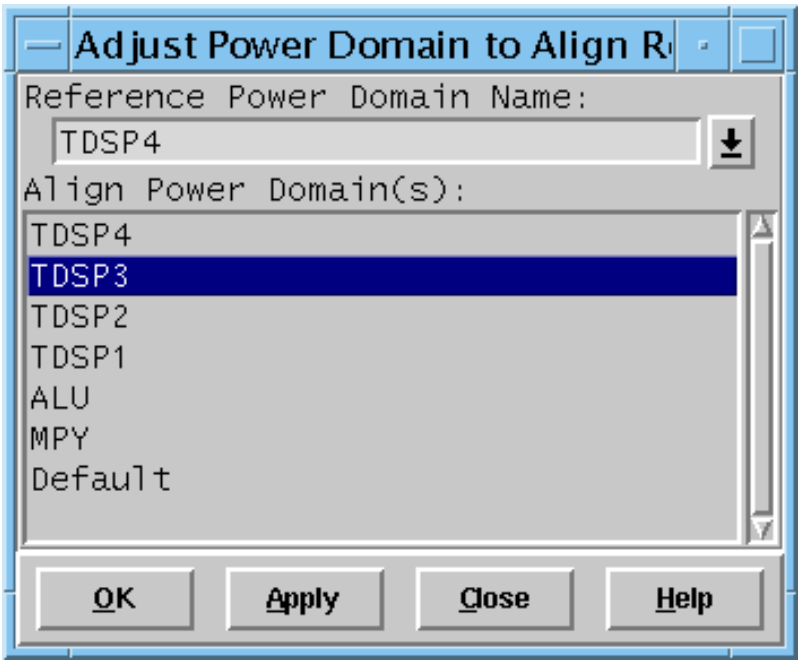
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `createShifterRows`

Adjust Power Domain to Align Rows

Use the Adjust Power Domain to Align Rows form to adjust power domains to align shifter rows in relation to a reference power domain.

➤ To open the Align Shifter Rows form, choose *Power – Multiple Supply Voltage – Align Shifter Rows*.



Adjust Power Domain to Align Rows Fields and Options

Reference Power Domain

Specifies a reference power domain. The selected power domains adjust to align their shifter rows with the rows in this power domain.

Align Power Domain(s)

Lets you select a power domain from a list of power domains created in your design.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `adjustPowerDomainToAlignRows`

Shifter/Isolation Cells

The Shifter/Isolation Cells submenu contains the following items:

- Load Shifter/Isolation Cells File on page 702
- Generate Shifter/Isolation Cells Template on page 703
- Add Shifter/Isolation Cells on page 705
- Report Shifter/Isolation Cells on page 707
- Remove Redundant Shifter/Isolation Cells on page 708

Load Shifter/Isolation Cells File

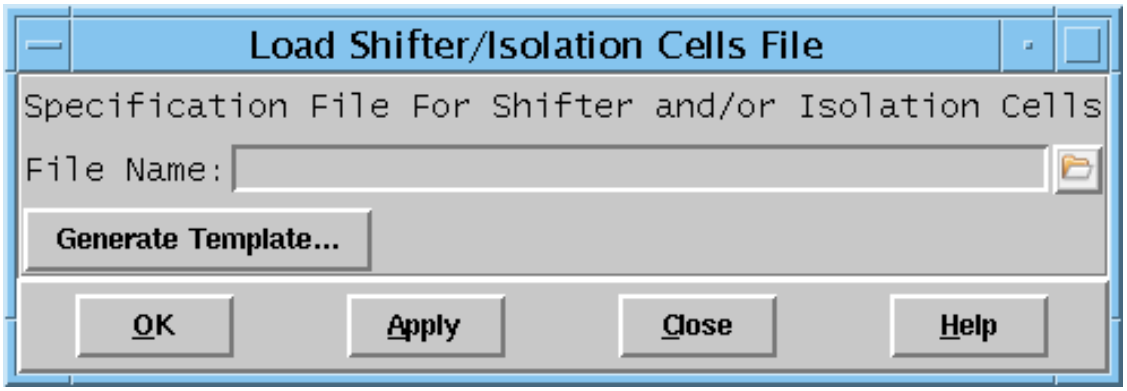
Use the Load Shifter/Isolation Cells File form to load the shifter table. If you do not have a file, you can generate a template.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Shifter/Isolation Cells form, choose *Power – Multiple Supply Voltage – Shifter/Isolation Cells – Load*.



Shifter/Isolation Cells File Fields and Options

File Name	Specifies the file (shifter table) for shifter and/or isolation cells.
Generate Template	Opens the Generate Shifter/Isolation Cells Template form.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `loadShifter`

Generate Shifter/Isolation Cells Template

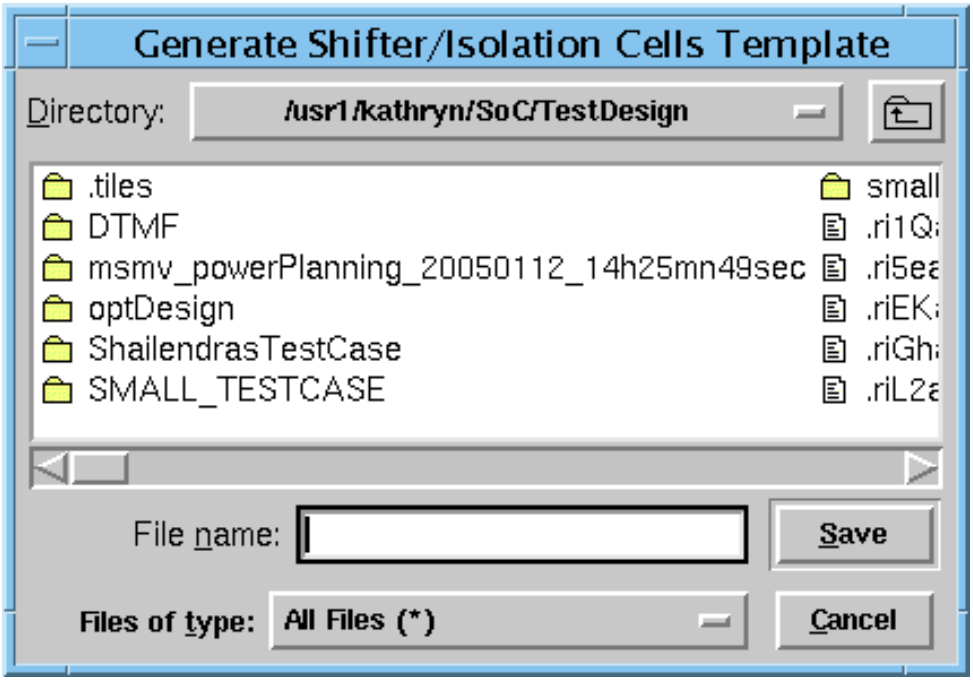
Use the Generate Shifter/Isolation Cells Template form to specify the location where you would like to save the generated shifter table template. This template is blank except for the headings you need to create your own table.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Generate Shifter/Isolation Cells form, choose *Power – Multiple Supply Voltage – Shifter/Isolation Cells – Load*, then click on the *Generate* button.



Generate Shifter/Isolation Cells Template Fields and Options

Directory	Selects the directory where you want to save the template file.
File name	Specifies the name of the template file.
Files of type	Specifies the file type.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `loadShifter`

Add Shifter/Isolation Cells

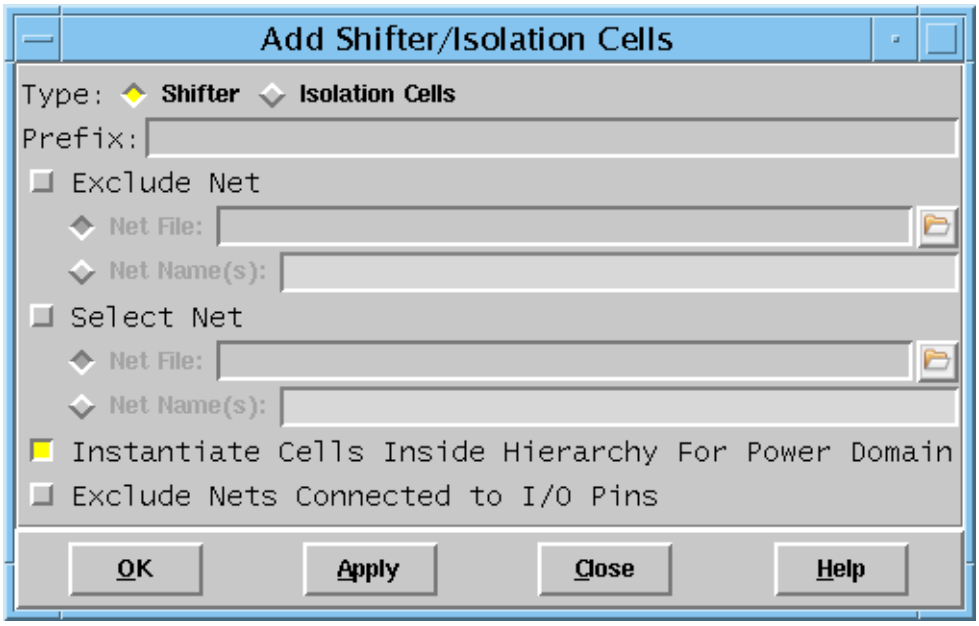
Use the Shifter/Isolation Cells form to add level shifters or isolation cells.

Important

This form is only available on the Multiple Supply Voltage menu in backward compatibility mode, when you set the following variable:

```
setVar dbgSaveOldMsvDbOnly 1
```

➤ To open the Shifter/Isolation Cells form, choose *Power – Multiple Supply Voltage – Shifter/Isolation Cells – Add*.



Add Shifter/Isolation Cells Fields and Options

Shifter	Adds level shifters.
Isolation Cells	Adds isolation cells.
Prefix	Adds the specified prefix to the added instance names. This prefix overrides the default prefix. *Default:* `msvBuf_` for shifters, and `isoBuf` for isolation cells.
Exclude Net	Determines whether a net is excluded.

Net File	Specifies the name of the file containing a list of nets for the software to exclude when adding isolation cells or shifters. You must list each net on a separate line in the file.
Net Names	Adds isolation cells or shifters to all nets except the specified net(s).
Selected Net	Specifies the nets to which shifters or isolation cells are added.
Net File	Specifies the name of the file containing a list of nets for the software to include when adding isolation cells or shifters. You must list each net on a separate line in the file.
Net Name(s)	Adds isolation cells or shifters to the specified nets.

Insert Cells Inside Hierarchy for Power Domain

Forces the software to add isolation cells to the HInsts in a location power domain as specified in the shifter table.

Default: The software inserts the minimum number of isolation cells inside the receiving power domain, without inserting isolation cells inside the HInsts.

Exclude Nets Connected to I/O Pins

Excludes all nets connected to I/O pins.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addIsolationCell`
- `addShifter`

Related Topics

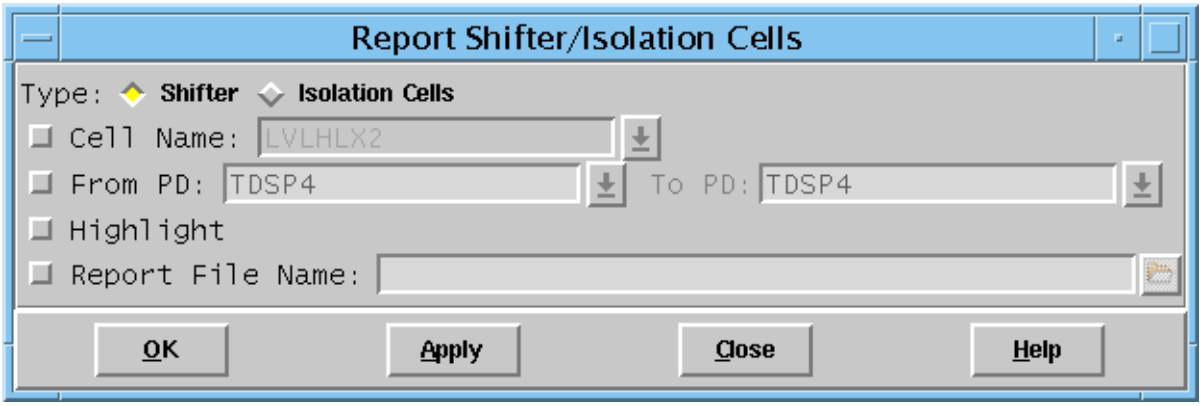
For information on the following topic, see “Low Power Design” in the *Encounter User Guide*.

- Multiple Supply Voltage Flat Flow

Report Shifter/Isolation Cells

Use the Report Shifter/Isolation Cells form to report or show isolation cells and instances, or level shifters.

➤ To open the Report Shifter/Isolation Cells form, choose *Power – Multiple Supply Voltage – Shifter/Isolation Cells – Report/Highlight*.



Report Shifter/Isolation Cells Fields and Options

Shifter	Reports shifters.
Isolation Cells	Reports isolation cells.
Cell Name	Reports shifters or isolation cells with the specified cell name.
From PD	Reports shifters or isolation cells between power domain pairs.
To PD	Reports shifters or isolation cells in the receiving power domain.
Highlight	Highlights placed level shifters or isolation cells.
Report File Name	Specifies the name of the report file you want to generate.

Related Text Commands

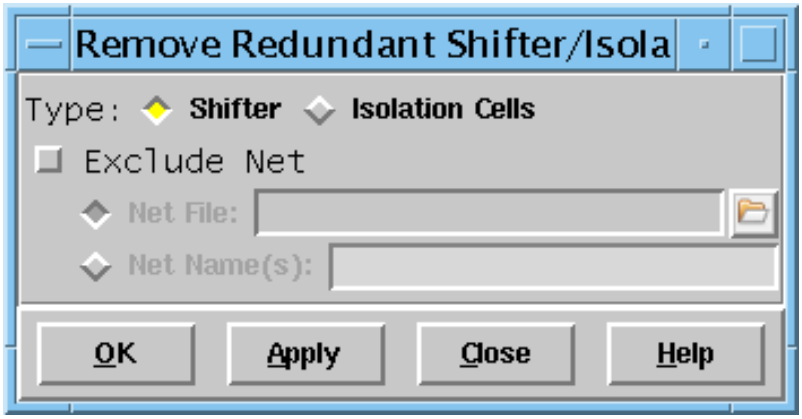
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `reportIsolation`
- `reportShifter`

Remove Redundant Shifter/Isolation Cells

Use the Remove Redundant Shifter/Isolation Cells form to delete redundant back-to-back shifters and isolation cells.

➤ To open the Remove Shifter/Isolation Cells form, choose *Power – Multiple Supply Voltage – Shifter/Isolation Cells – Remove Redundant*.



Remove Shifter/Isolation Cells Fields and Options

Shifter	Removes redundant shifters.
Isolation Cells	Removes redundant isolation cells.
Exclude Net	Specifies the nets to exclude.
Net File	Retains back-to-back level shifters or isolation cells on the nets named in the specified file.
Net Name(s)	Retains back-to-back level shifters or isolation cells on the specified excluded nets.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

■ `cleanRedundantShifter`

Power Switch Insertion

The Power Switch Insertion form has the following pages:

- Power Switch Insertion – Ring on page 710
- Power Switch Insertion – Column on page 742

Power Switch Insertion – Ring

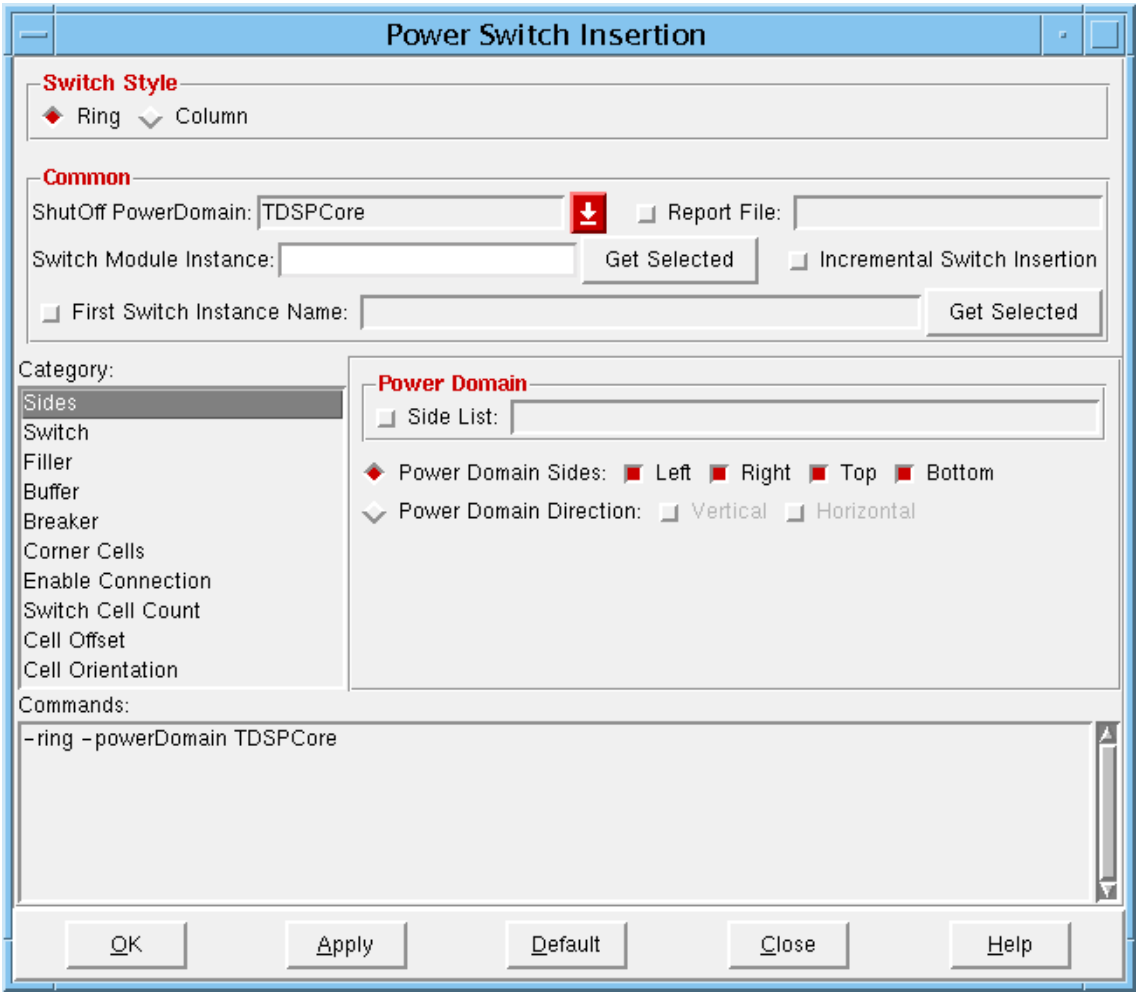
The *Ring* button controls the following pages:

- Power Switch Insertion – Ring – Sides on page 711
- Power Switch Insertion – Ring – Switch on page 714
- Power Switch Insertion – Ring – Filler on page 717
- Power Switch Insertion – Ring – Buffer on page 720
- Power Switch Insertion – Ring – Breaker on page 723
- Power Switch Insertion – Ring – Corner Cells on page 726
- Power Switch Insertion – Ring – Enable Connection on page 728
- Power Switch Insertion – Ring – Switch Cell Count on page 731
- Power Switch Insertion – Ring – Cell Offset on page 735
- Power Switch Insertion – Ring – Cell Orientation on page 739

Power Switch Insertion – Ring – Sides

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Sides* option specifies the sides of the power domain on which the switches are placed.

➤ To open the Power Switch Insertion – Ring – Sides form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click on the *Ring* button, and select the *Sides* option from the *Category* panel.



Power Switch Insertion – Ring – Sides Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Side List	Specifies the sides of a power domain where switches can and cannot be placed. In the list, 1 indicates that the side can contain ring switches, and 0 indicates that the side cannot contain ring switches. The list must contain either 0 or 1 for each side of the shape. The first member of the list indicates the first side relative to Corner 0, which is the lower left corner of the ring. If *Start Placing Cells in Counter-Clockwise Direction* is specified on the *Switch Cell Count* form, the first side is counterclockwise from Corner 0.
Power Domain Sides	Specifies the sides on which switches are placed.
Left	Inserts switches on the left side of the power domain.
Right	Inserts switches on the right side of the power domain.
Top	Inserts switches on the top side of the power domain.
Bottom	Inserts switches on the bottom side of the power domain.
Power Domain Direction	Inserts switches on multiple sides of the same direction. These options are useful for rectilinear power domains.
Vertical	Inserts switches on all vertical sides of the power domain.

Horizontal	Inserts switches on all horizontal sides of the power domain.

Related Text Commands

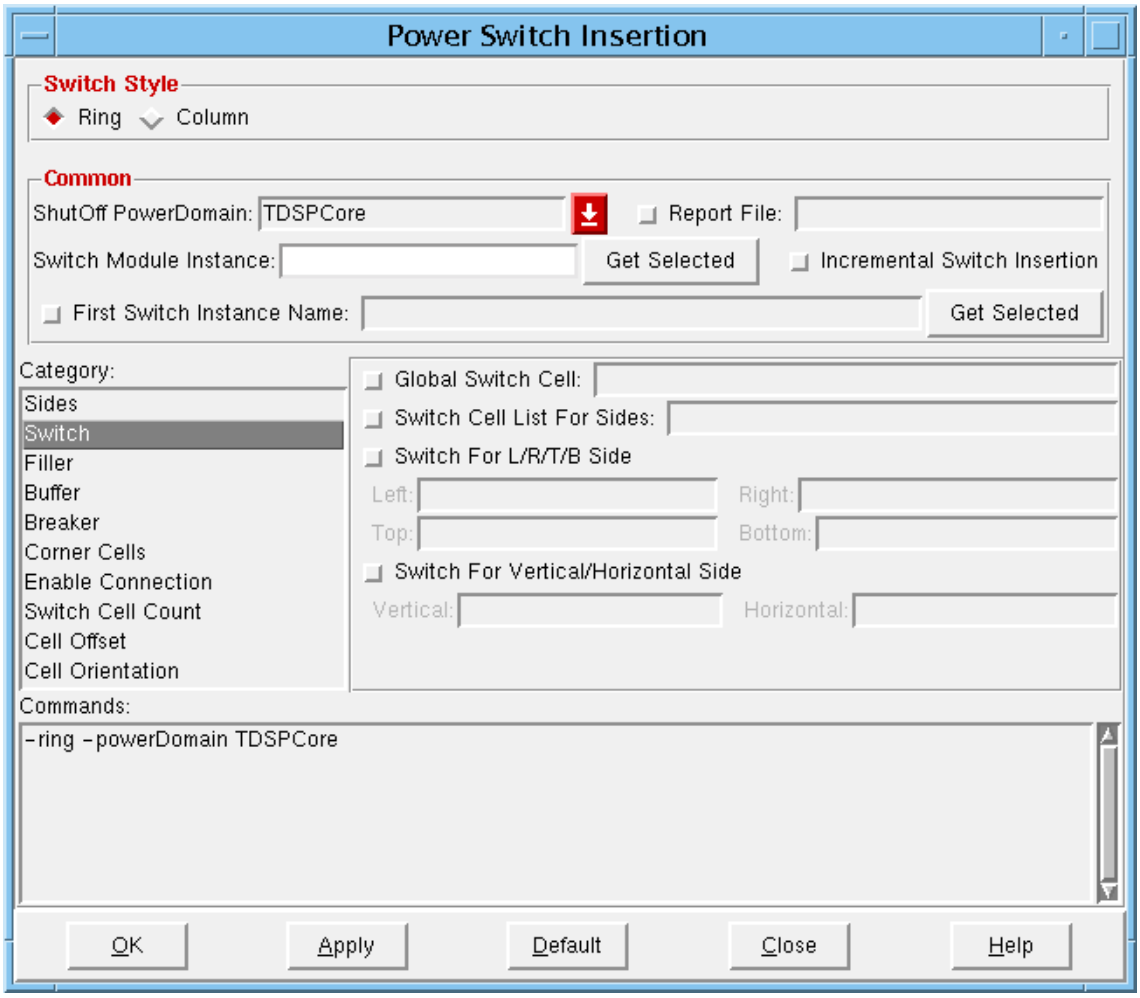
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Switch

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Switch* option specifies switch placement.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Switch* in the *Category* pane.



Power Switch Insertion – Ring – Switch Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Switch Cell	Specifies the cell name of the switch cell to insert in the power switch ring surrounding the specified power domain.
Switch Cell List for Sides	The number of cells must match the number of sides in the power domain. The software checks that the number of cells you specify is the number you specified with `optPowerSwitch -specifySideList`, and issues an error message if it finds a discrepancy.
Switch Cell List for L/R/T/B Side	
	Lists switch cells for specific sides. You can choose different cells for each side.
Left	Specifies a switch cell for the left side of the power switch ring.
Right	Specifies a switch cell for the right side of the power switch ring.
Top	Specifies a switch cell for the top side of the power switch ring.
Bottom	Specifies a switch cell for the bottom side of the power switch ring.

Switch for Vertical/Horizontal Side

	Lists switch cells for all horizontal or all vertical sides. You can choose different cells for each side.
Vertical	Specifies a switch cell for the vertical sides of the power switch ring.
Horizontal	Specifies a switch cell for the horizontal sides of the power switch ring.

Related Text Commands

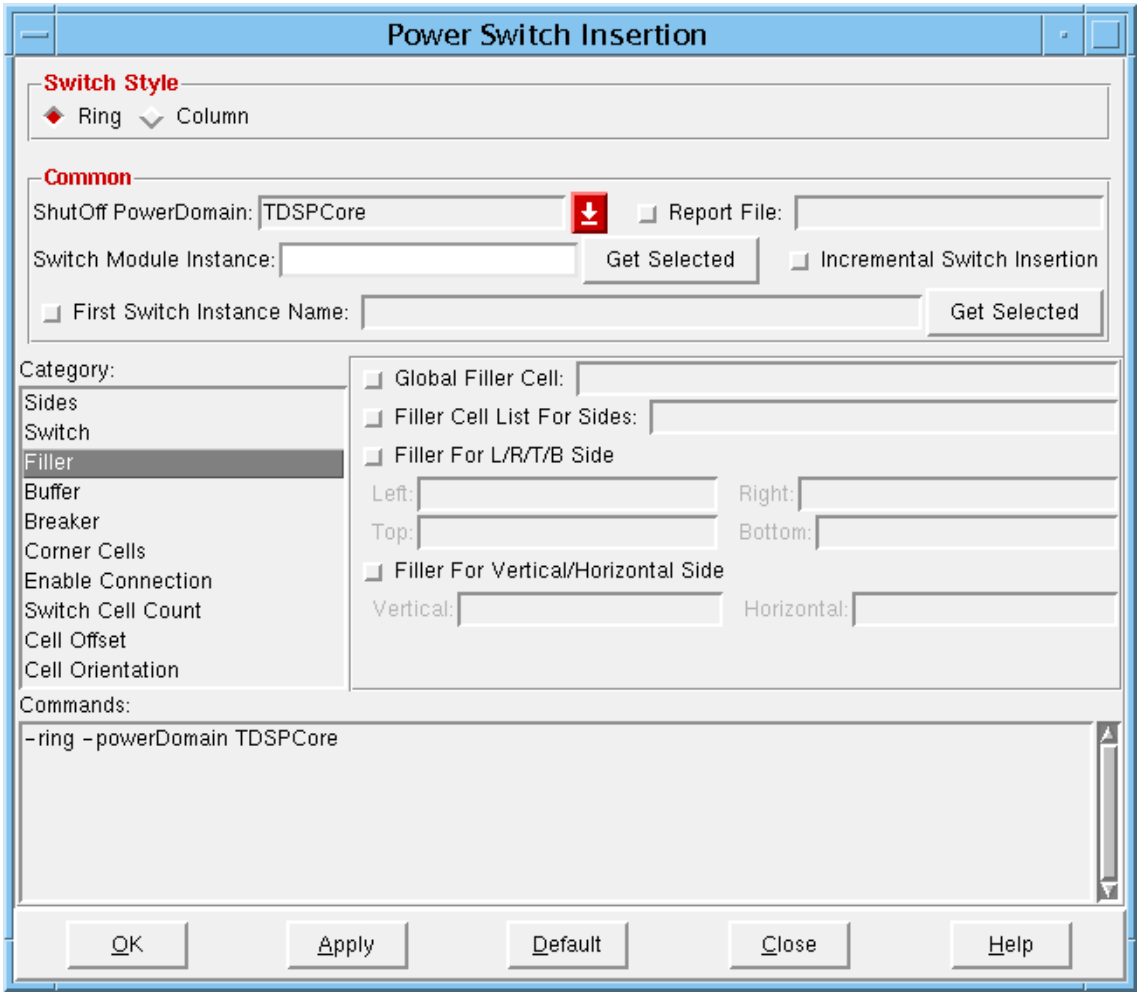
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Filler

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Filler* option specifies filler cell placement.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Filler* in the *Category* pane.



Power Switch Insertion – Ring – Filler Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Filler Cell	Specifies the cell name of the filler cell to insert in the power switch ring surrounding the specified power domain.
Filler Cell List for Sides	Specifies the filler cell to use for all sides.
Filler Cell List for L/R/T/B Side	
	Lists filler cells for specific sides. You can choose different cells for each side.
Left	Specifies a filler cell for the left side of the power switch ring.
Right	Specifies a filler cell for the right side of the power switch ring.
Top	Specifies a filler cell for the top side of the power switch ring.
Bottom	Specifies a filler cell for the bottom side of the power switch ring.
Filler for Vertical/Horizontal Side	
	Lists filler cells for all horizontal or all vertical sides. You can choose different cells for each side.
Vertical	Specifies a filler cell for the vertical sides of the power switch ring.

Horizontal	Specifies a filler cell for the horizontal sides of the power switch ring.

Related Text Commands

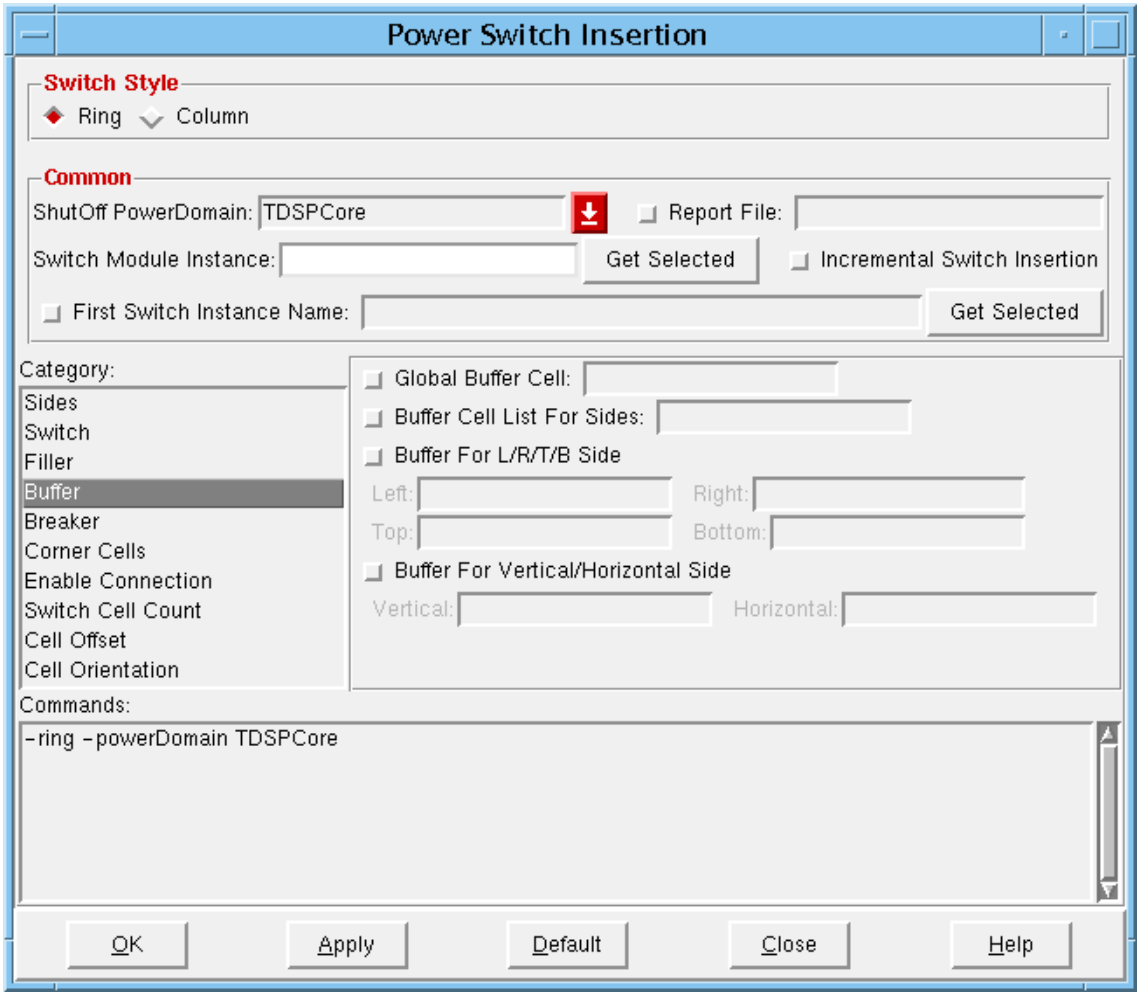
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Buffer

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Buffer* option specifies buffer cell placement.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Buffer* in the *Category* pane.



Power Switch Insertion – Ring – Buffer Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Buffer Cell	Specifies the cell name of the buffer cell to insert in the power switch ring surrounding the specified power domain.
Buffer Cell List for Sides	Specifies the buffer switch cell to use for all sides.
Buffer Cell List for L/R/T/B Side	
	Lists buffer cells for specific sides. You can choose different cells for each side.
Left	Specifies a buffer cell for the left side of the power switch ring.
Right	Specifies a buffer cell for the right side of the power switch ring.
Top	Specifies a buffer cell for the top side of the power switch ring.
Bottom	Specifies a buffer cell for the bottom side of the power switch ring.
Buffer for Vertical/Horizontal Side	
	Lists buffer cells for all horizontal or all vertical sides. You can choose different cells for each side.

Vertical	Specifies a buffer cell for the vertical sides of the power switch ring.
Horizontal	Specifies a buffer cell for the horizontal sides of the power switch ring.

Related Text Commands

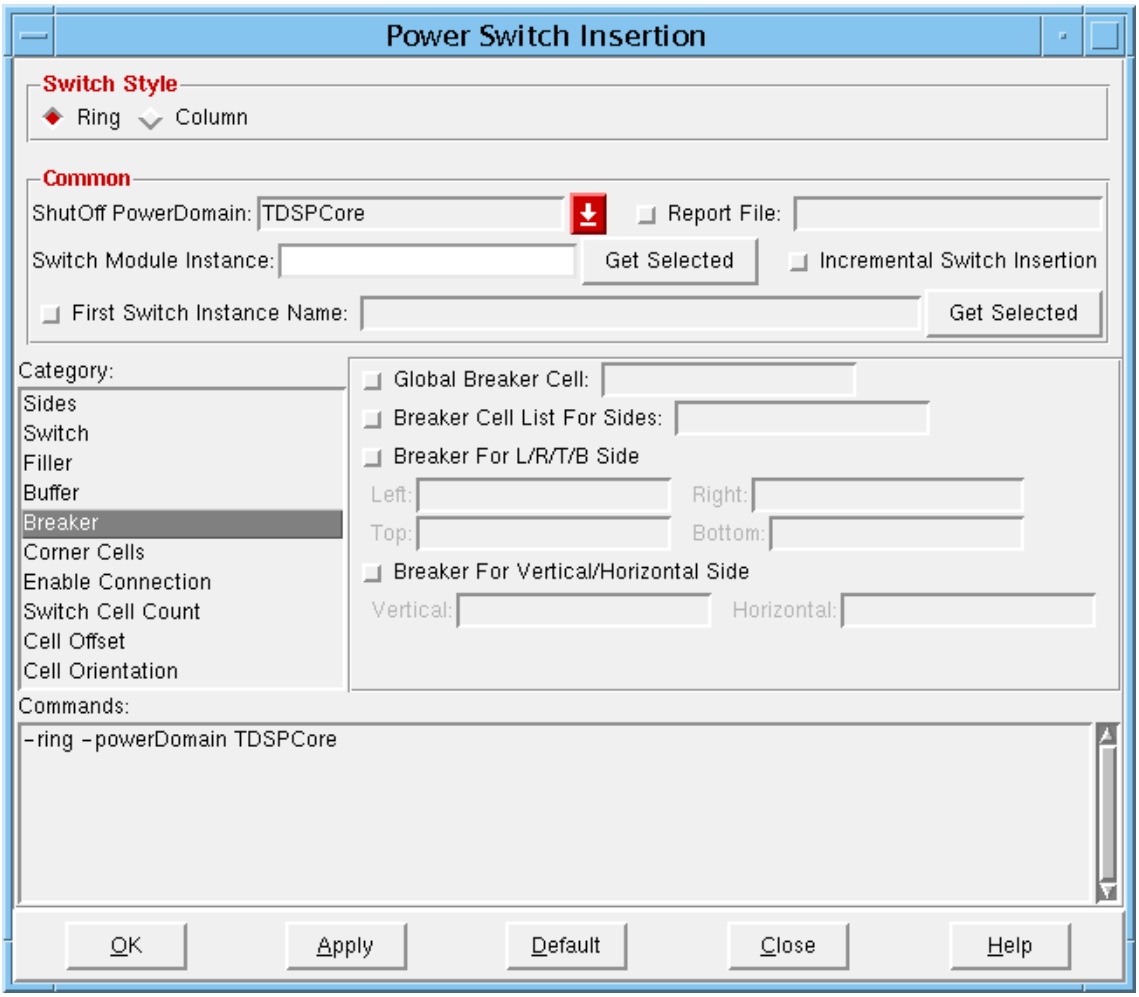
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Breaker

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Breaker* option specifies breaker cell placement.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Breaker* in the *Category* pane.



Power Switch Insertion – Ring – Breaker Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Global Breaker Cell	Specifies the cell name of the breaker cell to insert in the power switch ring surrounding the specified power domain.
Breaker Cell List for Sides	Specifies the breaker cell to use for all sides.
Breaker Cell List for L/R/T/B Side	
	Lists cells for specific sides. You can choose different cells for each side.
Left	Specifies a breaker cell for the left side of the power switch ring.
Right	Specifies a breaker cell for the right side of the power switch ring.
Top	Specifies a breaker cell for the top side of the power switch ring.
Bottom	Specifies a breaker cell for the bottom side of the power switch ring.
Breaker for Vertical/Horizontal Side	
	Lists breaker cells for all horizontal or all vertical sides. You can choose different cells for each side.

Vertical	Specifies a breaker cell for the vertical sides of the power switch ring.
Horizontal	Specifies a breaker cell for the horizontal sides of the power switch ring.

Related Text Commands

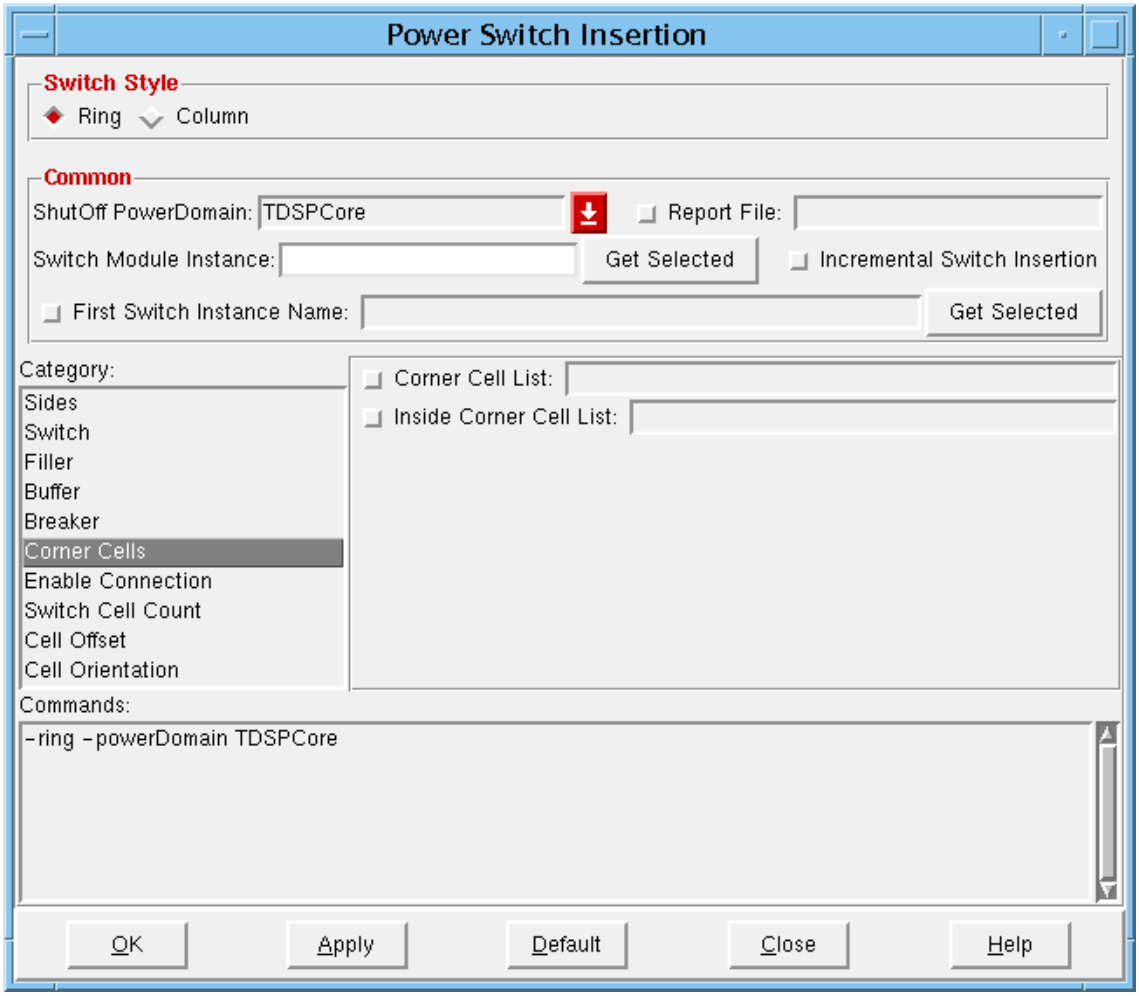
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Corner Cells

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Corner Cells* option specifies which corner cells to use.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Corner Cells* in the *Category* pane.



Power Switch Insertion – Ring – Corner Cells Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
Corner Cell List	Specifies the list of available corner cells that can be used by the tool to fill the corners of the ring. If you specify only one corner cell, that same cell is used on all four corners with the appropriate orientation.
Inside Corner Cell List	Specifies a list of cells for the tool to choose for the inside corners of the ring. You do not need to list a specific cell for a specific corner. The tool selects from the list you provide.

Related Text Commands

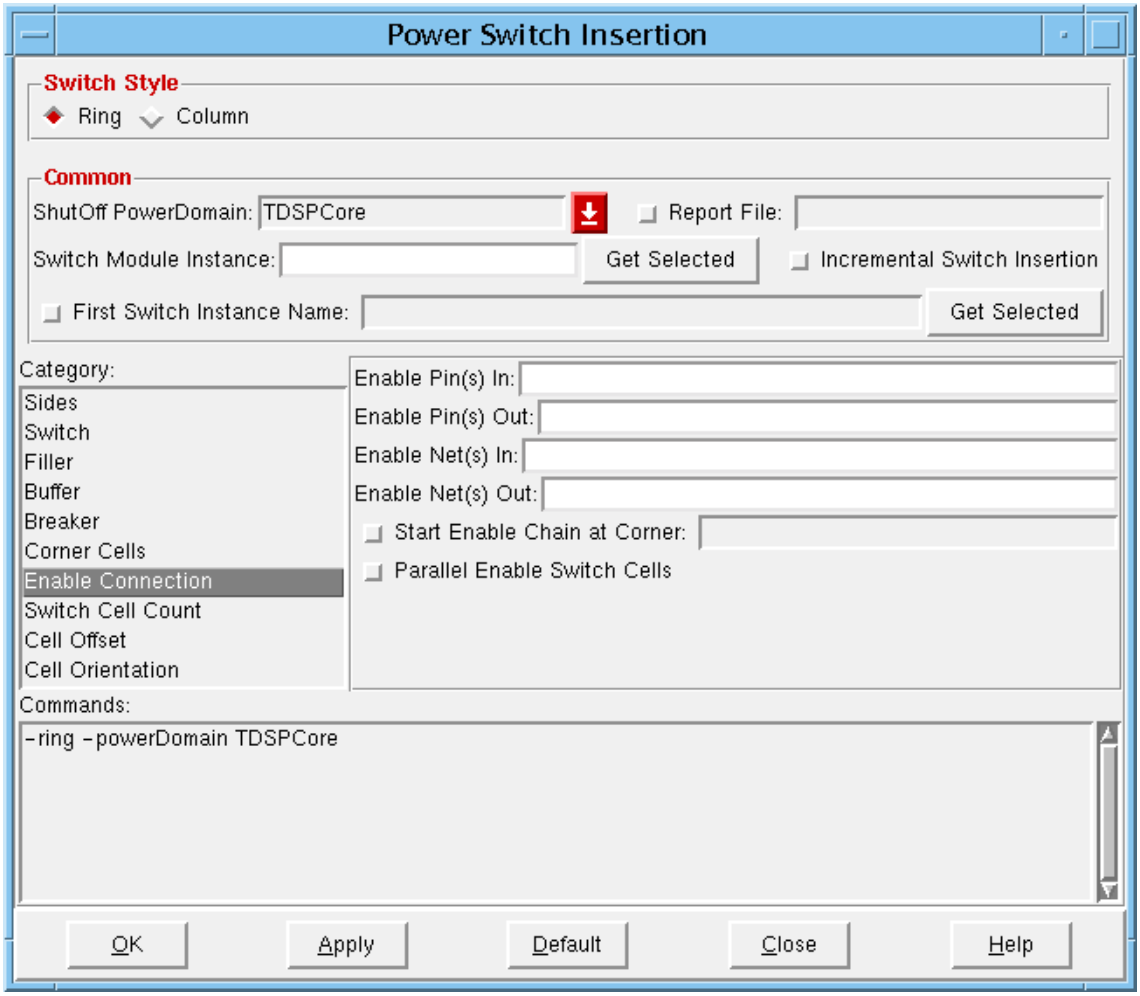
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Enable Connection

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Enable Connection* option specifies the enable pins and nets to use, and the enable connection style.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Enable Connection* in the *Category* pane.



Power Switch Insertion – Ring – Enable Connection Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Enable Pin(s) In	Specifies the list of enable input pins of the buffers inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same ring: All the enable pin of the switch cells in the same column are daisy-chained together. For the first switch of the ring, the Enable Pin In is tied to Enable Net In.
Enable Pin(s) Out	Specifies the list of enable output pin(s) of the buffer(s) inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: all the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.
Enable Net(s) In	Specifies the list of input nets that the software attaches to the enable input pins. The order in which you specify these nets is important because nets are assigned to pins sequentially.

Enable Net(s) Out

Specifies the enable output nets that the software attaches to the enable output pins. The order in which you specify these nets is important because nets are assigned to pins sequentially. For the last switch of the ring, the Enable Pin Out is tied to the Enable Pin Out.

Start Enable Chain at Corner

Specifies the corner where the switch ring insertion begins. The software inserts switches starting from the specified corner and continuing in a clockwise direction (unless *Start Placing Cells in the Counter-Clockwise Direction* is specified on the *Switch Cell Count* form) until it completes the full ring.

Parallel Enable Switch Cells

Connects a power switch's input pin in parallel style rather than daisy-chaining. You do not have to specify *Enable Pin(s) Out* or *Enable Net(s) Out*.

Related Text Commands

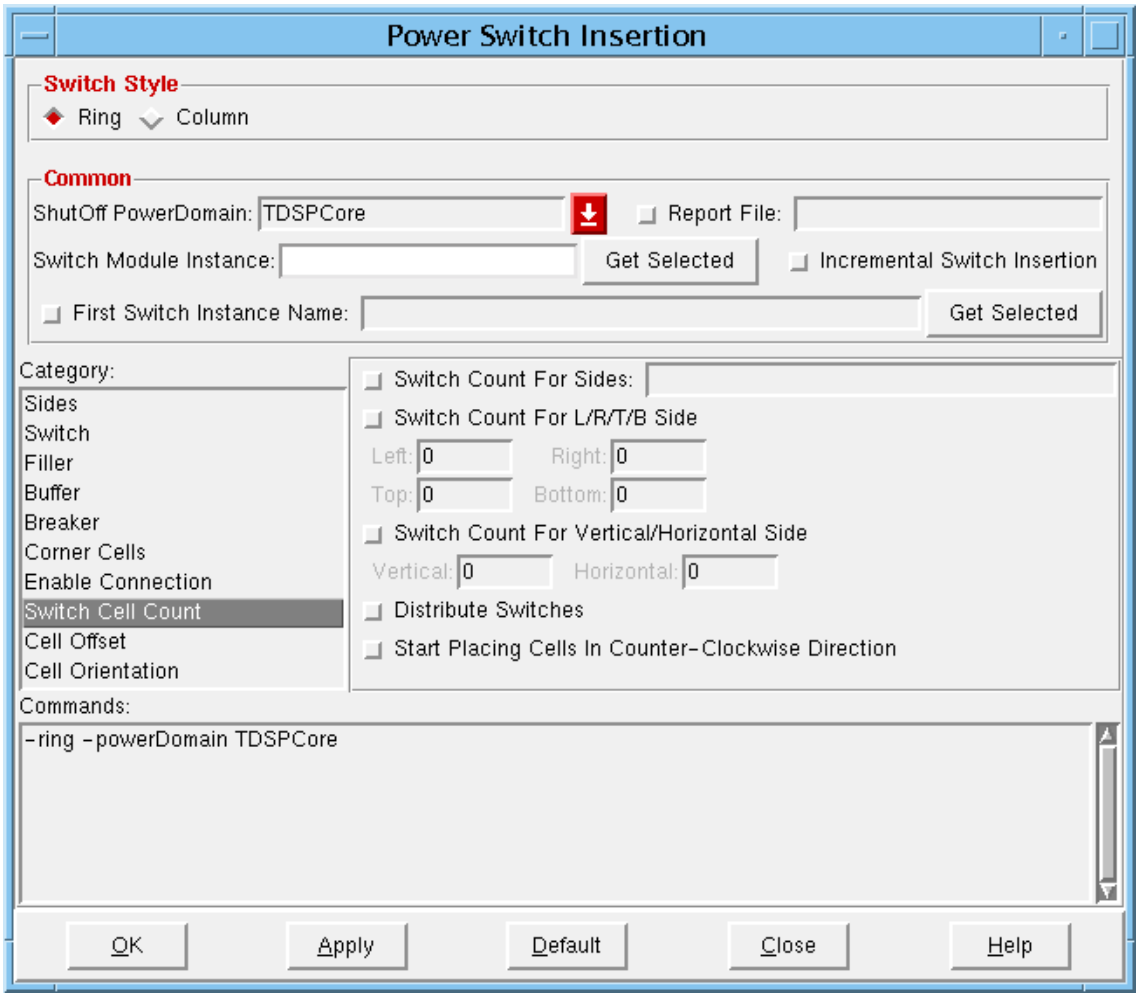
For information on the following command, see "Low Power Commands" in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Switch Cell Count

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Switch Cell Count* option specifies the number of switches to use.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Switch Cell Count* in the *Category* pane.



Power Switch Insertion – Ring – Switch Cell Count Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.

Switch Cell Count for Sides

Lists the number of switches to insert on each side. Each value in the list corresponds to a side specified with *Side List* in on the *Sides* form.

Switch Cell Count for L/R/T/B Side

Specifies the cell count for each side.

Note: This parameter applies to power switch ring creation only.

Three scenarios can occur:

- If the spaces available match the number specified, the software fills these spaces with switches.
- If the number exceeds the spaces available, the software issues an error message.

If the number is less than the spaces available, the tool inserts the switches, then inserts filler cells to fill the space.

Left
Specifies the number of switches to insert on the left side of the power domain.

Right
Specifies the number of switches to insert on the right side of the power domain.

Top
Specifies the number of switches to insert on the Top side of the power domain.

Bottom
Specifies the number of switches to insert on the bottom side of the power domain.

Switch Count for Vertical/Horizontal Side

Specifies the cell count for each horizontal and/or vertical side.

Note: This parameter applies to power switch ring creation only.

Three scenarios can occur:

- If the spaces available match the number specified, the software fills these spaces with switches.
- If the number exceeds the spaces available, the software issues an error message.

If the number is less than the spaces available, the tool inserts the switches, then inserts filler cells to fill the space.

Vertical
Specifies the number of switches to insert on all vertical side(s) of the power domain.

Horizontal
Specifies the number of switches to insert on all horizontal side(s) of the power domain.

Distribute Switches
Distributes switches of different types as evenly as possible on a ring side. For example, if there are 40 available slots, and there are 20 switches and 20 fillers, the software will alternate switches and fillers in the available slots.

Start Placing Switches in the Counter-Clockwise Direction

Places the cell pattern in a counter-clockwise direction in a switch ring. Switch placement begins at the lower left corner of the ring.

Related Text Commands

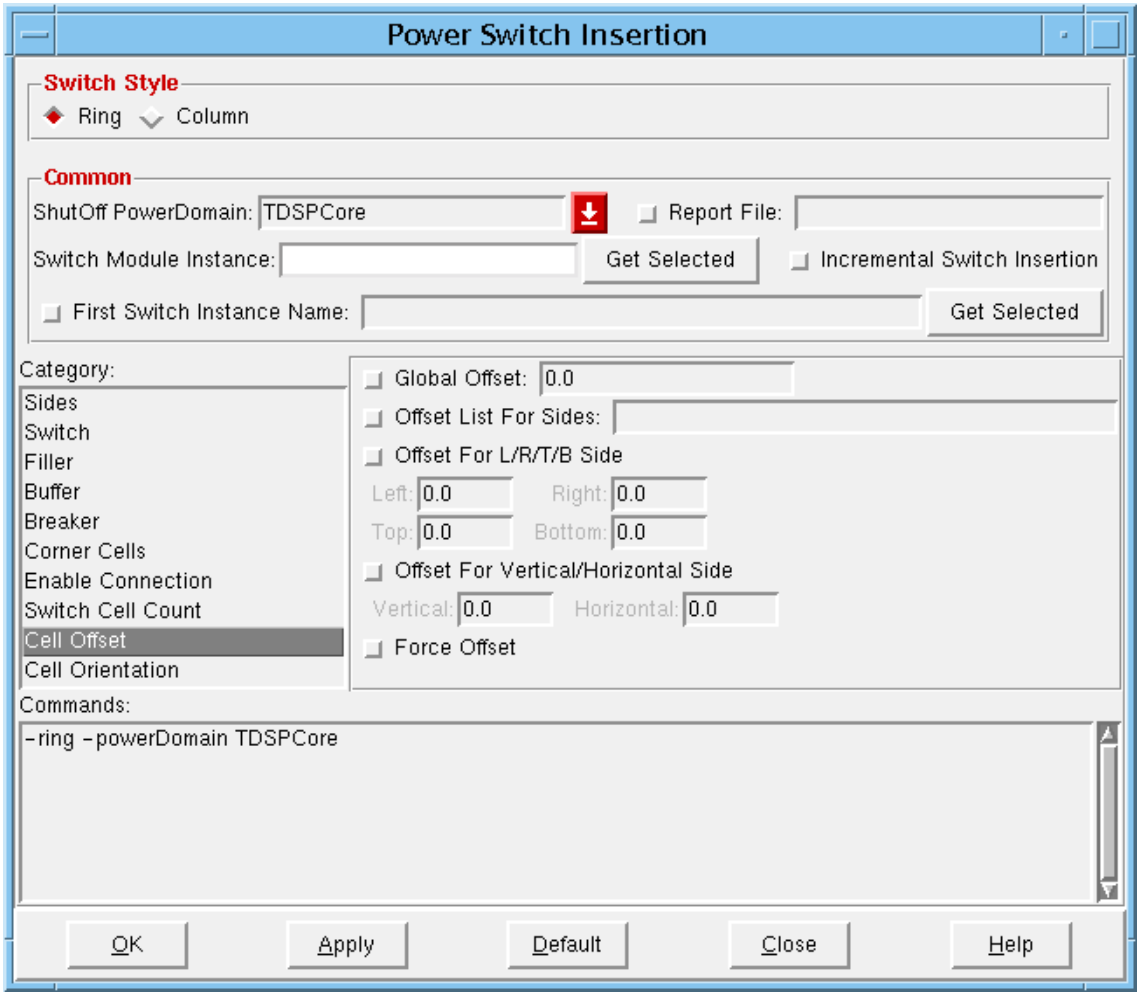
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Cell Offset

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Cell Offset* option specifies the offsets to use.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Cell Offset* in the *Category* pane.



Power Switch Insertion – Ring – Cell Offset Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.

First Switch Instance Name

Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.

Global Offset

Offsets all sides of the power switch ring the specified distance from the power domain. Specify the offset in µm.

Note: If you do not specify a global offset, or offset for any sides, the tool places switches with `0` offset.

Offset List For Sides

Lists the offset values representing the distance between the power domain fence boundary and each side of the power switch ring. Each value in the list corresponds to a side specified with the *Side List* on the *Sides* form.

Note: When you create a power domain, a `minGap` exists for this power domain, and the switches are inserted within this `minGap`. However, if the specified `minGap` is less than the switch dimension, then the tool automatically adds filler cells and assigns a new `minGap` for this power domain.

Important

You *must* specify a valid cell name for each side, even if no cells can be specified for a side.

The tools checks that the number of cells you specify is the same number you specified with the *Side List* on the *Sides* form, and issues an error message if it finds a discrepancy.

Offset For L/R/T/B Sides

Specifies the distance between the power domain boundary and the nearest switch cell on the specified side(s).

Left

Specifies the distance between the left power domain boundary and the nearest switch cell.

Right

Specifies the distance between the right power domain boundary and the nearest switch cell. T

Top

Specifies the distance between the top power domain boundary and the nearest switch cell.

Bottom

Specifies the distance between the bottom power domain boundary and the nearest switch cell.

Offset For Vertical/Horizontal Side

Specifies the distance between the power domain boundary and the nearest switch cell on the specified horizontal and vertical sides.

Vertical — Offsets the switch ring from the vertical edges of the power domain. Specify the offset in µm.

Horizontal — Offsets the switch ring from the horizontal edges of the power domain. Specify the offset in µm.

Force Offset — Forces the software to place ring switches at the exact offset you specify for all sides. Sides with unspecified offsets are forces to 0.0 µ.

When you specify any other offset without specifying *Force Offset*, the tool places switches at the smallest distance that is greater than or equal to the specified offset for each side, in order to maintain a contiguous ring.

Related Text Commands

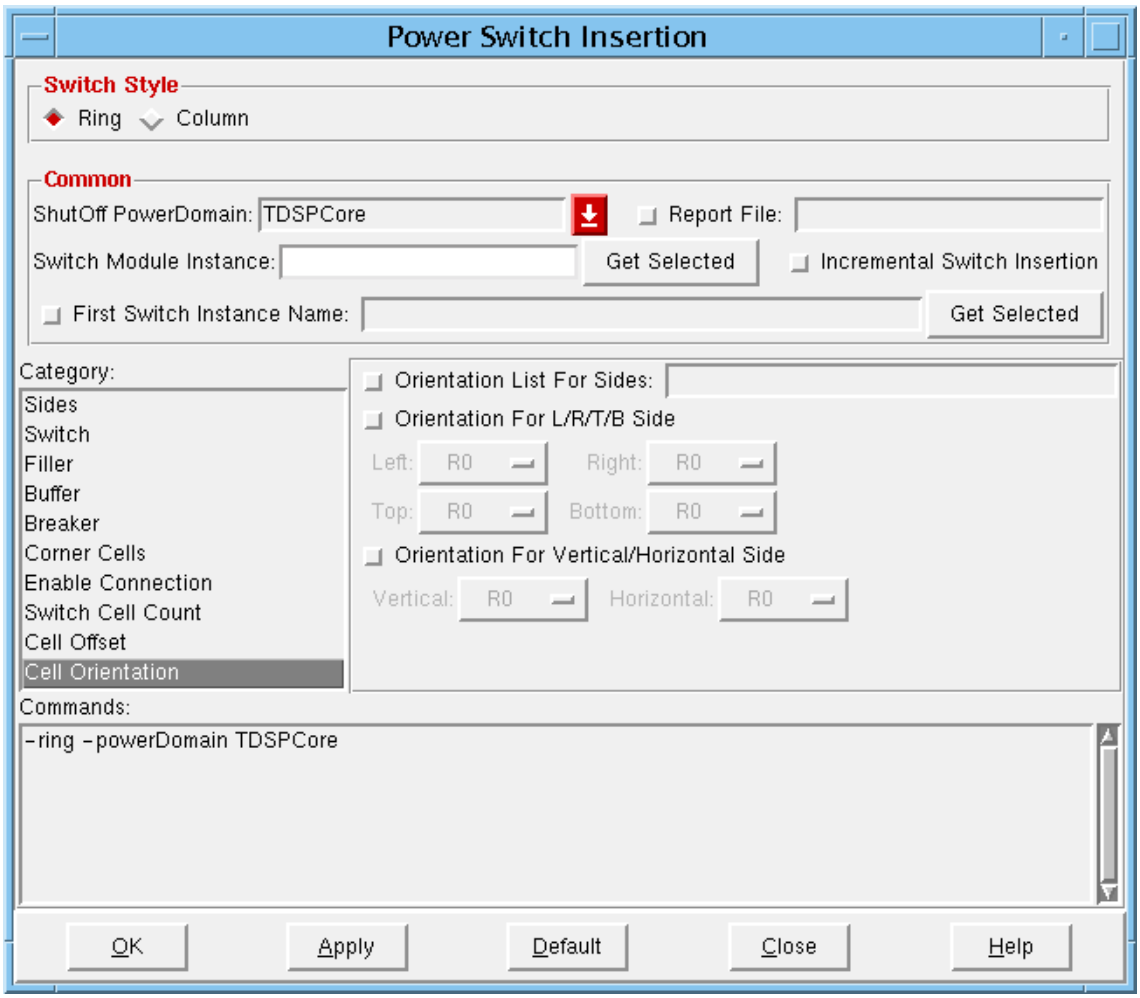
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Ring – Cell Orientation

Use the Power Switch Insertion – Ring form to add a ring of switches around a power domain. The *Cell Orientation* option specifies the orientation for ring sides.

➤ To open the Power Switch Insertion – Ring form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Ring* button, then click on *Cell Orientation* in the *Category* pane.



Power Switch Insertion – Ring – Cell Orientation Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Orientation List For Sides	
	Lists the orientations for cells for each side of the power switch ring. Each orientation in the list corresponds to a side specified, so you must have already specified sides. Use the following notation for orientation: `R0|R90|R180|R270|MX|MY|MX90|MY90`
Orientation for L/R/T/B Side	
	Specifies the orientation for specific sides.
Left	Specifies the cell orientation for the left side of the power switch ring.
Right	Specifies the cell orientation for the right side of the power switch ring.
Top	Specifies the cell orientation for the top side of the power switch ring.
Bottom	Specifies the cell orientation for the bottom side of the power switch ring.

Orientation for Vertical/Horizontal Side

	Specifies the cell orientation for vertical and horizontal sides.
Vertical	Specifies the cell orientation for vertical sides.
Horizontal	Specifies the cell orientation for horizontal sides.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Column

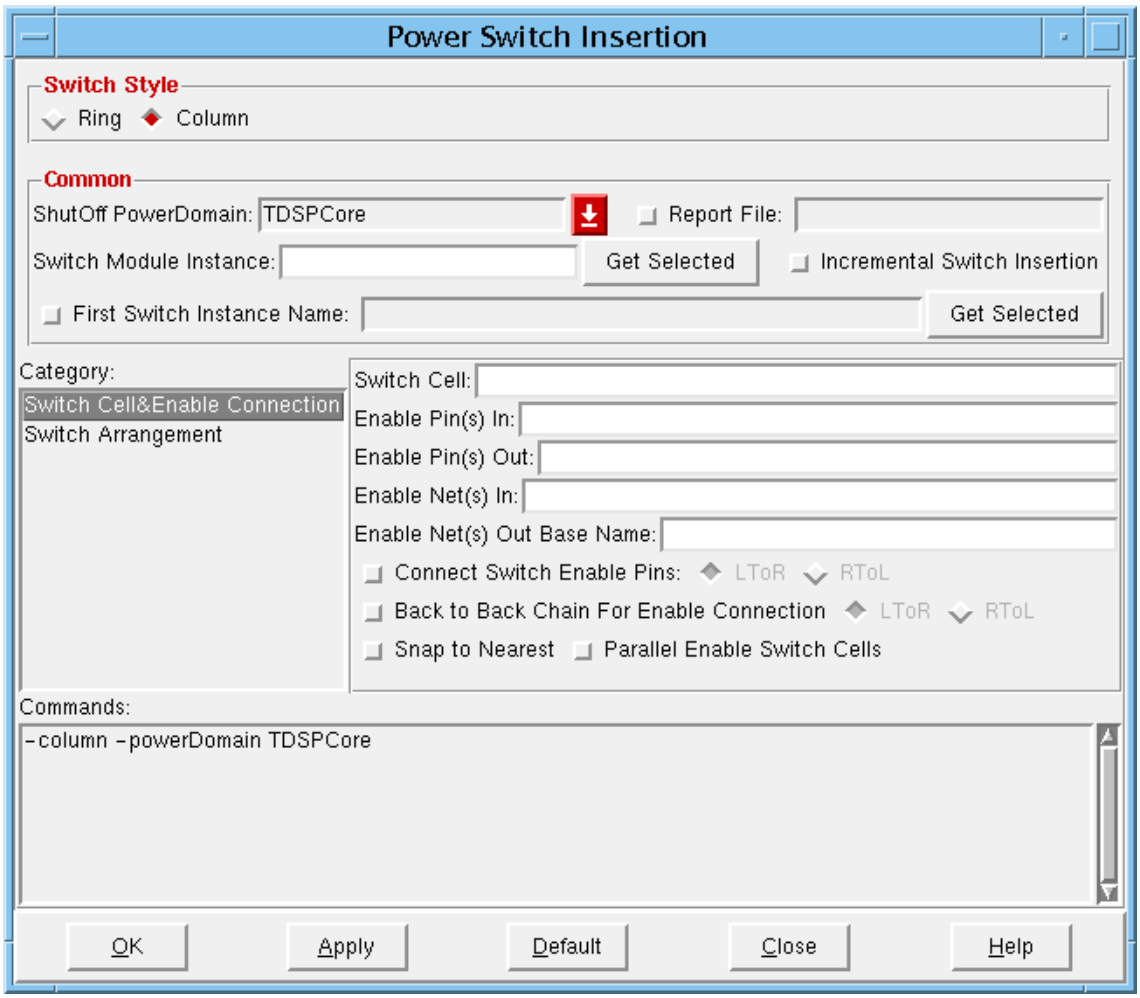
The *Column* button controls the following pages:

- Power Switch Insertion – Column – Switch Cell and Enable Connection on page 743
- Power Switch Insertion – Column – Switch Arrangement on page 747

Power Switch Insertion – Column – Switch Cell and Enable Connection

Use the Power Switch Insertion – Column form to add a ring of switches around a power domain. The *Switch Cell and Enable Connection* option specifies which switch an enable usage.

➤ To open the Power Switch Insertion – Column form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Column* button, then click on *Switch Cell and Enable Connection* in the *Category* pane.



Power Switch Insertion – Column – Switch Cell and Enable Connections Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Switch Cell	Specifies the cell name of the switch to insert in the specified power domain.
Enable Pin(s) In	Specifies the list of enable input pins of the buffers inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: All the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.
Enable Pin(s) Out	Specifies the list of enable output pin(s) of the buffer(s) inside the switch cell. The order in which you specify these pins is important because nets are assigned to pins sequentially. The software ties the Enable Pin Out of the first switch cell to the Enable Pin In of the next switch cell in the same column: all the enable pin of the switch cells in the same column are daisy-chained together. For the last switch of the column, the Enable Pin Out is tied to Enable Net Out.

Enable Net(s) In: Specifies the list of input nets that the software attaches to the enable input pins. The order in which you specify these pins is important because nets are assigned to pins sequentially.

Enable Net Out Base Name

Specifies the base name for the Enable Out Nets.

Connect Switch Enable Pins

Connects the first switch of the first column to the enable net specified. The software connects the first switch in the remaining columns to the output enable net of the first switch in the previous column.

For more information, see the `-connectBottomSwitchEnablePins` option to the `addPowerSwitch` command in the “Low Power Commands” in the *Encounter Text Command Reference*.

L To R Connects switches left-to-right.

R To L Connects switches right-to-left.

Back to Back Chain for Enable Connection

Connect the Enable Net Out at the top of a column to the Enable Net In at the top of the next column, and connects the Enable Net In at the bottom of a column to the Enable Net In at the bottom of the next column. By default, the Enable Net In is connected to the bottom of each column, and the Enable Net Out exits from the top of each column, in parallel.

Snap to Nearest Snaps the cell placement to the nearest legal location. This parameter can be used when a hard macro blocks part of a column. The switches that would overlap the hard macro blockage are placed at legal locations nearest to the expected original location.

Parallel Enable Switch Cells

Connects a power switch’s input pin in parallel style rather than daisy-chaining. You do not have to specify *Enable Pin(s) Out* or *Enable Net(s) Out*.

Related Text Commands

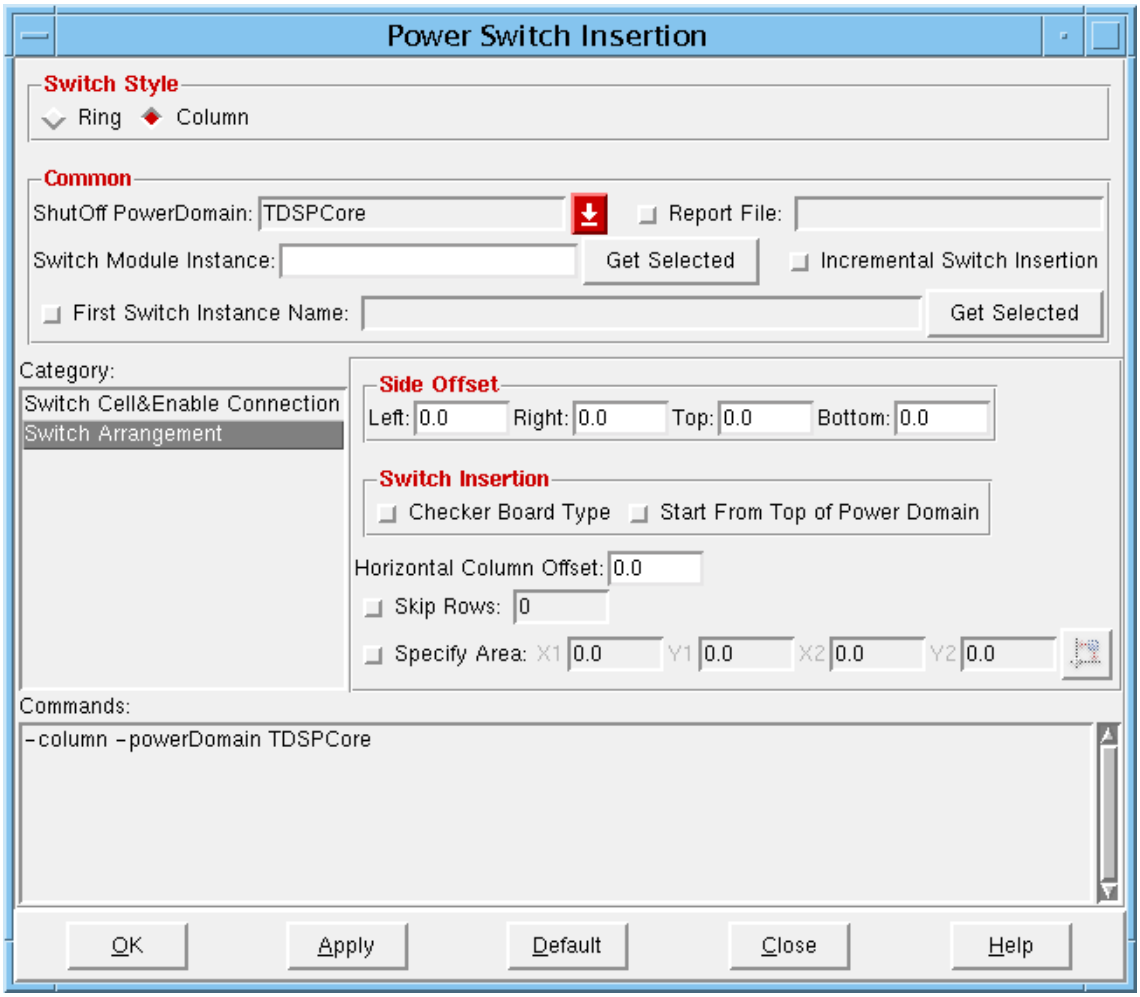
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Power Switch Insertion – Column – Switch Arrangement

Use the Power Switch Insertion – Column form to add a switch columns for a power domain. The *Switch Arrangement* option specifies how switches are arranged.

➤ To open the Power Switch Insertion – Column form, choose *Power – Multiple Supply Voltage – Add Power Switch*, click the *Column* button, then click on *Switch Arrangement* in the *Category* pane.



Power Switch Insertion – Column – Switch Arrangement Fields and Options

Switch Style	Specifies how the switches are arranged.
Ring	Specifies ring style power switch insertion. Power switches are placed outside the power domain.
Column	Specifies the column style of power switch insertion.
Common	Specifies the options common to all *Power Switch Insertion* forms.
Shut Off Power Domain	Specifies the power domain that shuts off.
Switch Module Instance	Specifies module instance where all the switches will be instantiated. This parameter is required.
Report File	Writes switch instances and their corresponding input/output enable signal pin/net connections to the specified file name.
Incremental Switch Insertion	Inserts switches to the power domain without removing the existing switches.
First Switch Instance Name	Specifies the instance name of an existing switch cell in the netlist (specified by *Switch Module Instance*) to use as the first cell in the column or ring.
Side Offset	Specifies the distance between the power domain boundaries and the nearest switch cell.
Left	Specifies the distance between the left power domain boundary and the nearest switch cell.
Right	Specifies the distance between the right power domain boundary and the nearest switch cell.
Top	Specifies the distance between the top power domain boundary and the nearest switch cell.
Bottom	Specifies the distance between the bottom power domain boundary and the nearest switch cell.
Checker Board Type	Arranges switch cells in a checkerboard pattern within a power domain.
Start From Top of Power Domain	Adds switches from the top down rather than from the bottom up.

Horizontal Column Offset	Specifies the distance between switch columns in µm. This parameter is required.
Skip Rows	Specifies the number of rows to skip when placing a switch in a column. For example, 2 skips two rows before placing the next switch in a column.
Specify Area	Defines an area within a power domain where the tool can insert power switches. *x1 y1* is the lower left coordinate of the area. *x2 y2* is the upper right corner of the area. You can specify left, right, top, and/or bottom offsets to offset the switches from the boundaries of the area.

Related Text Commands

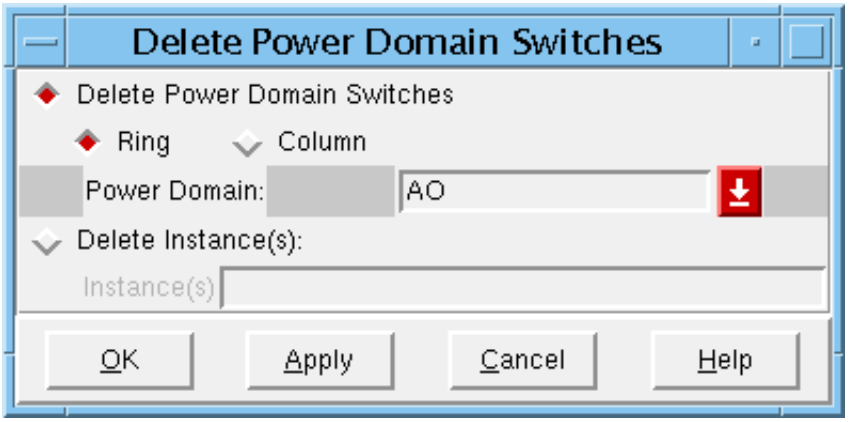
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `addPowerSwitch`

Delete Power Switches

Use the Delete Power Switches form to remove power switches from multiple power domain designs.

➤ To open the Delete Power Switches form, choose *Power – Multiple Supply Voltage – Delete Power Switches*.



Delete Power Switches Fields and Options

Delete Power Domain Switches	
	Removes switches from rings or columns.
Ring	Removes all switches and filler cells that were inserted by the *Power Switch Insertion* (`addPowerSwitch`) command, from the switch ring for the specified power domain.
Column	Removes all switches and filler cells that were inserted by the *Power Switch Insertion* (`addPowerSwitch`) command, from the switch columns for the specified power domain.
Power Domain	Specifies the power domain.
Delete Instances	Specifies the power switch cell instances to delete.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `deletePowerDomain`

Highlight Power Domains

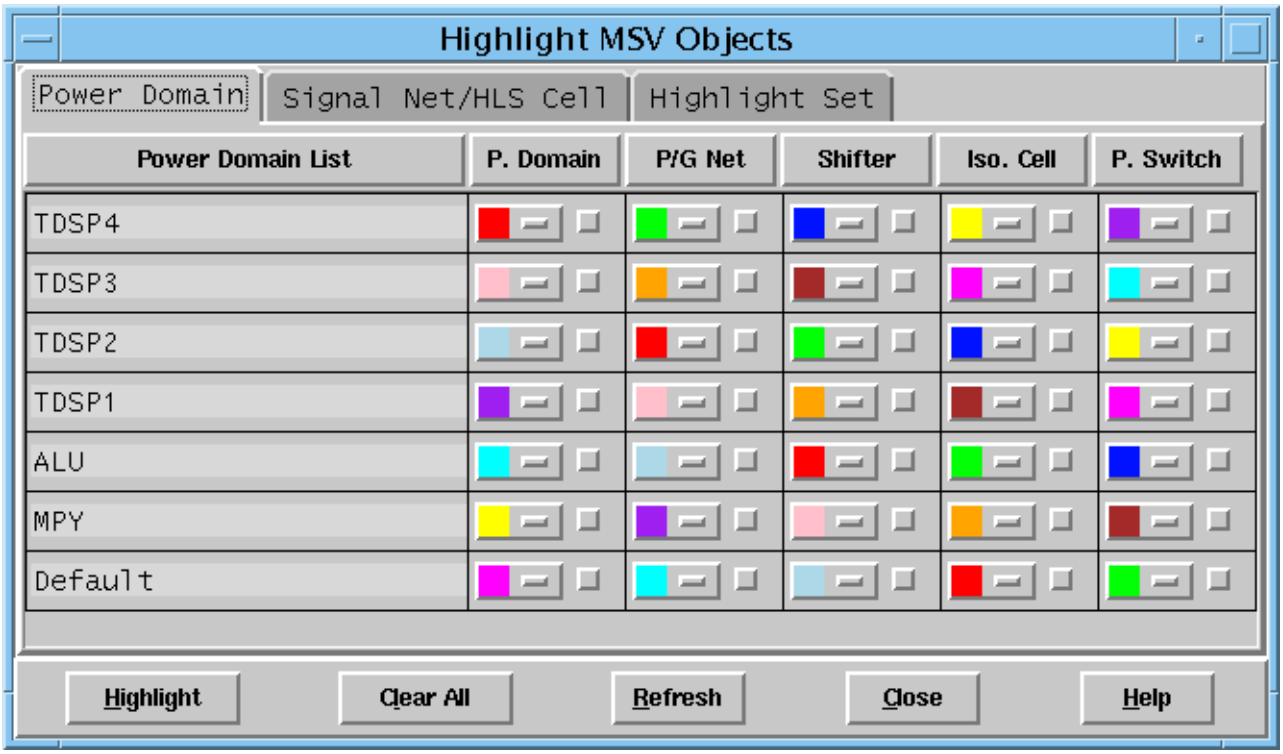
The Highlight Power Domains submenu opens the Highlight MSV objects form. The Highlight MSV Objects form contains the following three pages:

- Highlight MSV Objects – Power Domain on page 753
- Highlight MSV Objects – Signal Net/HLS Cell on page 755
- Highlight MSV Objects – Highlight Set on page 758
- Color on page 760

Highlight MSV Objects – Power Domain

Use the Highlight MSV Objects – Power Domain form to highlight power domains, and power/ground nets, level shifters, isolation cells, and power switches in power domains.

➤ To open the Highlight MSV Objects –Power Domain form, choose *Power – Multiple Supply Voltage –Highlight Power Domain* and click on the Power Domain tab.



Highlight MSV Objects – Power Domain Fields and Options

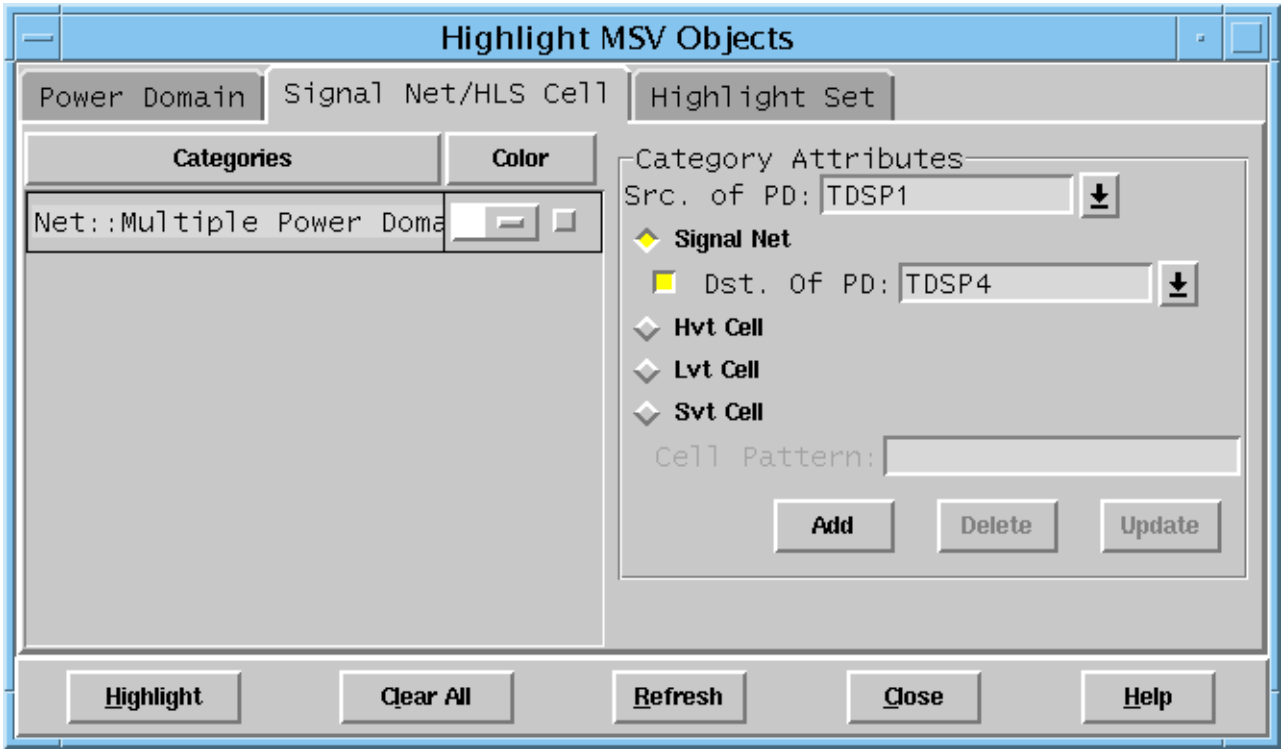
Power Domain List	Lists the power domains in your design. The software populates this list automatically.
P. Domain	Lets you select the color (highlight set) to use when highlighting a power domain. Click the checkbox and *Highlight* to highlight a power domain. For more information about highlight sets, see "Highlight MSV Objects – Highlight Set" on page 758.

P/G Net	Lets you select the color (highlight set) to use when highlighting power/ground nets in a power domain. Click the checkbox and *Highlight* to highlight the power/ground nets. For more information about highlight sets, see "Highlight MSV Objects – Highlight Set" on page 758.
Shifter	Lets you select the color (highlight set) to use when highlighting level shifters in a power domain. Click the checkbox and *Highlight* to highlight the level shifters. For more information about highlight sets, see "Highlight MSV Objects – Highlight Set" on page 758.
Iso. Cell	Lets you select the color (highlight set) to use when highlighting isolation cells in a power domain. Click the check box and *Highlight* to highlight the isolation cells. For more information about highlight sets, see "Highlight MSV Objects – Highlight Set" on page 758.
P. Switch	Lets you select the color (highlight set) to use when highlighting power switches in a power domain. Click the checkbox and *Highlight* to highlight the power switches. For more information about highlight sets, see "Highlight MSV Objects – Highlight Set" on page 758.
Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects – Power Domain page and categories from the Highlight MSV Objects – Signal Net/HLS Cell page. Settings on the Highlight MSV Objects – Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects – Power Domain and Highlight MSV Objects – Signal Net/HLS Cell pages.
Refresh	Adds or deletes power domains from the Highlight MSV Objects – Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects – Signal Net/HLS Cell page if you have deleted power domains.

Highlight MSV Objects – Signal Net/HLS Cell

Use the Highlight MSV Objects – Signal/HLS form to specify the signal nets or cells you want to highlight.

➤ To open the Highlight MSV Objects – Signal Net/HLS Cell form, choose *Power – Multiple Supply Voltage –Highlight Power Domain* and click on the Signal Net/HLS tab.



Highlight MSV Objects – Highlight Set Fields and Options

Categories	Specifies the categories created when you make selections from *Category Attributes* and click *Add*.
Color	Specifies the color for the category. The colors available are determined by the highlight sets. For more information, see "Highlight MSV Objects – Highlight Set" on page 758.
Src. of PD.	Specifies the power domain containing the Hvt, Lvt, or Svt cells, or the power domain from where the signal nets originate.

Signal Net	Creates a signal net category. You must specify the *Src. of PD* to indicate where the signal nets originate. Optionally, you can specify the *Dst. Of PD* to specify the signal nets that originate in *Src. of PD* and are connected to the *Dst. Of PD*.
Dst. of PD	Specifies the destination power domain for the signal nets.
Hvt Cell	Creates a category for high voltage threshold (Hvt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Hvt cells and a *Cell Pattern* to specify the cell names.
Lvt Cell	Creates a category for low voltage threshold (Lvt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Lvt cells and a *Cell Pattern* to specify the cell names.
Svt Cell	Creates a category for standard voltage threshold (Svt) cells. You must specify a *Src. of PD* to indicate the power domain that contains the Svt cells, and a *Cell Pattern* to specify the cell names.
Cell Pattern	Specifies the cell names. You can use a prefix or suffix, plus a wildcard, for example `MyCells*` indicates all cells with prefix `MyCells`. You must specify a *Cell Pattern* if you select *Hvt Cell*, *Lvt Cell*, or *Svt Cell*.
Add	Adds a category to the *Categories* list based on the selections you have made in *Category Attributes*.
Highlight	Highlights the selected objects (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects – Power Domain settings and categories from the Highlight MSV Objects – Signal Net/HLS Cell page. Settings on the Highlight MSV Objects – Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects – Power Domain and Highlight MSV Objects – Signal Net/HLS Cell pages.
Refresh	Adds or deletes power domains from the Highlight MSV Objects – Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects – Signal Net/HLS Cell page if you have deleted power domains.

Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects – Power Domain page and categories from the Highlight MSV Objects – Signal Net/HLS Cell page. Settings on the Highlight MSV Objects – Highlight Set page determine the highlight colors.
Update	Enables you to changes the source or destination power domains for a selected category.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

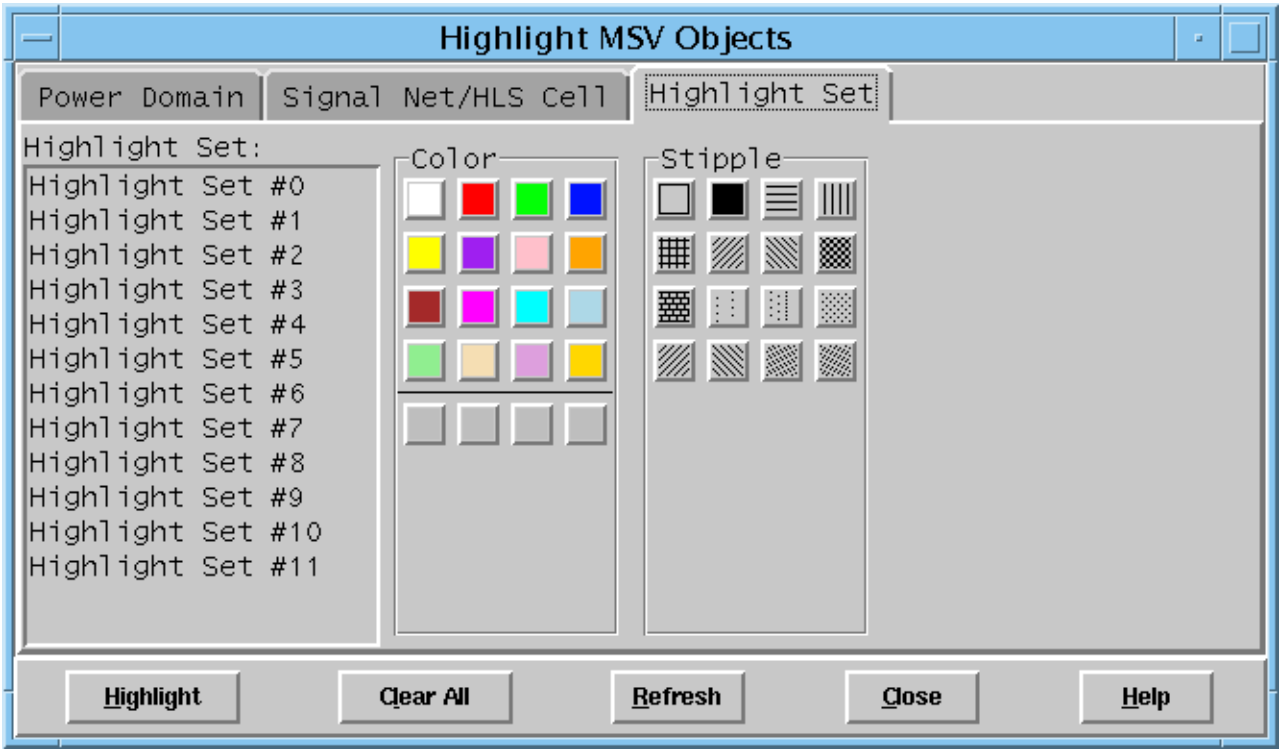
- `hilitePowerDomain`

Highlight MSV Objects – Highlight Set

Use the Highlight MSV Objects – Highlight Set form to specify the highlight colors for highlight sets.

➤ To open the Highlight MSV Objects – Highlight Set form, choose *Power – Multiple Supply Voltage –Highlight Power Domain* and click on the Highlight Set tab.

.



Highlight MSV Objects – Highlight Set Fields and Options

Highlight Set

Lists the 12 highlight sets. A highlight set is the combination of a color and stipple pattern. The highlight sets you define appear as choices for highlight colors for the various MSV objects on the Power Domain and Signal Net/HLS Cell forms. If you click on a highlight set, the current Color and Stipple settings are shown.

Color	Displays the colors you can select for the highlight set. The four gray boxes at the bottom of the color palette enable you to define custom colors. If you double-click on one of the gray boxes, the Color form opens. For more information, see "Color" on page 760.
Stipple	Displays the stipple patterns you can select for the highlight set.
Highlight	Highlights the selected object settings (power domains, power/ground nets, level shifters, isolation cells, and/or power switches) from the Highlight MSV Objects – Power Domain page and categories from the Highlight MSV Objects – Signal Net/HLS Cell page. Settings on the Highlight MSV Objects – Highlight Set page determine the highlight colors.
Clear All	Clears all highlights as determined from the current settings on the Highlight MSV Objects – Power Domain and Highlight MSV Objects – Signal Net/HLS Cell pages.
Refresh	Adds or deletes power domains from the Highlight MSV Objects – Power Domain if you have added or deleted power domains since the last time you highlighted objects. This option also removes categories on the Highlight MSV Objects – Signal Net/HLS Cell page if you have deleted power domains.

Related Text Commands

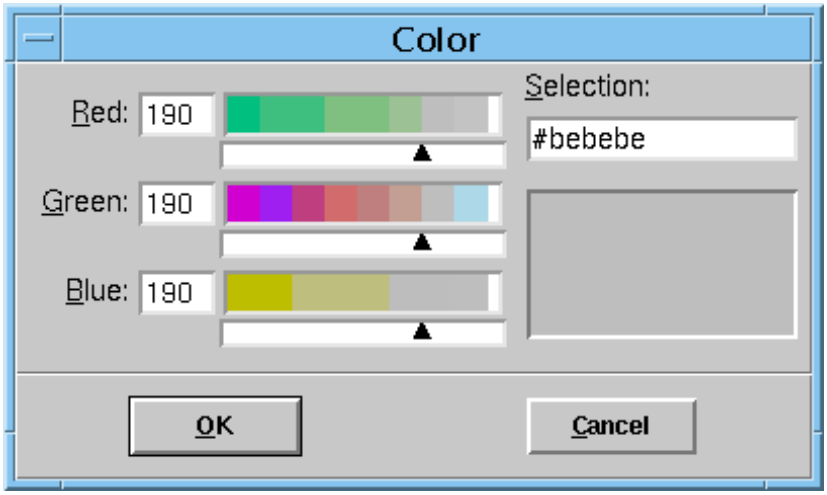
For information on the following command, see "Low Power Commands" in the *Encounter Text Command Reference*.

- `hilitePowerDomain`

Color

Use the Color form to create a custom color for the *Color* palette on the Highlight MSV Objects – Highlight Set form.

➤ To open the Color form, choose *Power – Multiple Supply Voltage –Highlight Power Domain*, click on the Highlight Set tab, then click on one of the gray boxes in the *Color* palette.



Color Fields and Options

Red	Lets you use a slider to select the red color value. The read-only box next to the slider displays the red color value.
Green	Lets you use a slider to select the green color value. The read-only box next to the slider displays the green color value.
Blue	Lets you use a slider to select the green color value. The read-only box next to the slider displays the blue color value.
Selection	Displays the RGB color determined by the *Red*, *Green*, and *Blue* settings. This is a read-only field. The color is displayed in the area below.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `hilitePowerDomain`

Report Power Domain

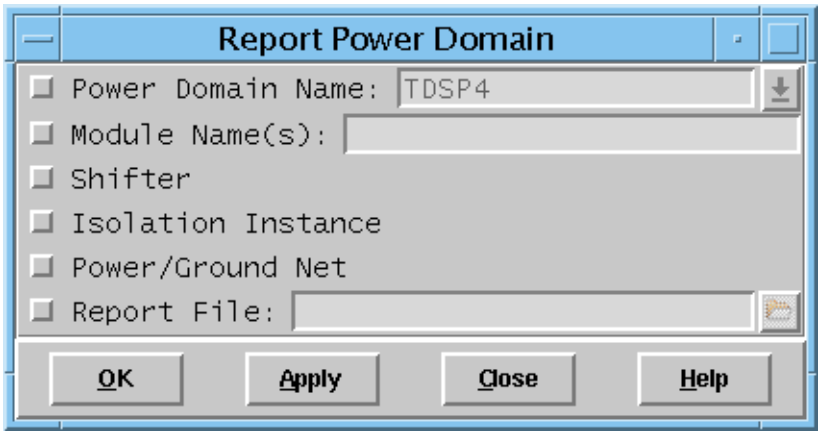
Use the Report Power Domain form to reports information about power domains.

➤ To open the Report Power Domain form, choose *Power – Multiple Supply Voltage – Report Power Domain*.

The report includes the following attributes:

- Power domain name
- Power domain bounding box
- Timing library
- Mingap
- RS extension
- Row type
- Row spacing

The command also reports whether the power domain is always on.



Report Power Domain Fields and Options

Power Domain Name	Specifies the power domain whose attributes you want to report. *Default:* If you do not specify the power domain, this command report data about all power domains.

Module Name(s)	Checks whether the specified instances or hierarchical instances are in the power domain.
Shifter	Reports all shifters in the power domain.
Isolation Instance	Reports all isolation cells in the power domain.
Power/Ground Net	Reports all the power/ground nets in the power domain.
Report File	Specifies the file in which you want to write the data.

Related Text Commands

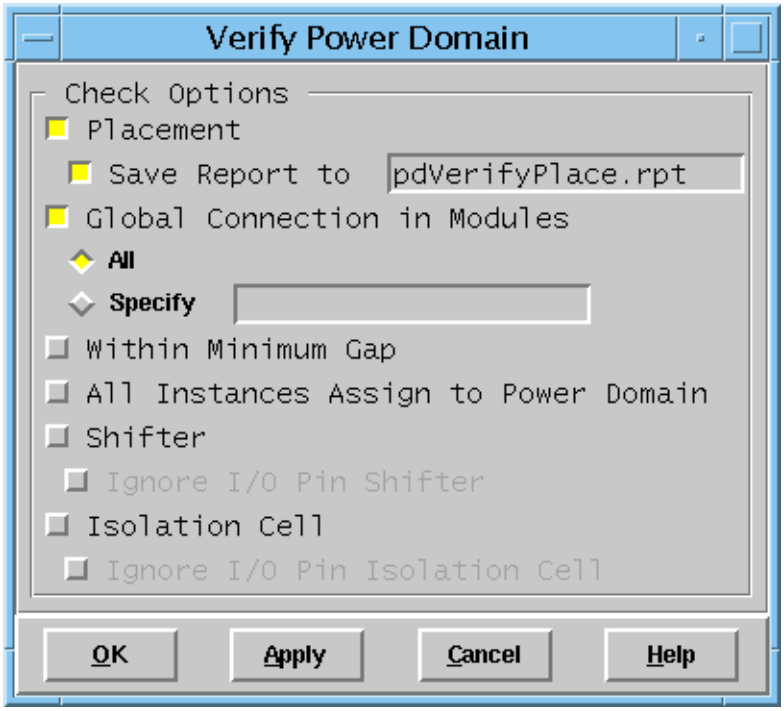
For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `reportPowerDomain`

Verify Power Domain

Use the Verify Power Domain form to verify that members of a power domain are placed correctly and that their power and ground pins are connected to the power domain's power and ground nets.

➤ To open the Verify Power Domain form, choose *Power - Multiple Supply Voltage - Verify Power Domain*.



Verify Power Domain Fields and Options

Placement	Verifies that only those cells assigned to a power domain are placed within the boundary of the power domain and reports any placement violations.
Save Report to	Specifies a name and location for the report generated when you select *Placement*.

Global Connection in Modules

Verifies that power and ground pins of instances within the power domain are connected to the power and ground nets of that power domain. In addition, this verifies that the tie-high and tie-low connections of a cell are connected to the same power and ground nets of the power domain to which the cell belongs.

All	All modules are verified.
Specify	Specified modules are verified.

Within Minimum Gap Verifies that the power domain ring is within the distance specified by the minimum gap specified when creating power domains.

Timing Library Binding Verifies that all cells are bound to correct timing library cells.

Note: This feature issues erroneous results in this release. Do not use it.

All Instances Assigned to Power Domain

Verifies that all instances are in the power domain.

Shifter Verifies that shifters are added to all nets crossing power domains.

Ignore I/O Pin Shifter Ignores I/O pin nets when verifying shifters.

Isolation Cell Verifies that isolation cells are added for all nets that need isolation cells.

Ignore I/O Pin Isolation Cell

Ignores I/O pin nets when verifying isolation cells.

Related Text Commands

For information on the following command, see “Low Power Commands” in the *Encounter Text Command Reference*.

- `verifyPowerDomain`

Power Planning

The Power Planning submenu contains the following items:

- Specify Electromigration

  Opens the Specify Electromigration Limits form.

- Edit Power Planning Option

  Opens the Edit Power Planning Option form.

- Synthesize Power Plan

  Opens the Synthesize Power Plan form.

- Add Rings

  Opens the Add Rings form.

- Add Stripes

  Opens the Add Stripes form.

- Add XStripes

  Opens the Add XStripes form.

- Create P/G Pin

  Opens the Create P/G Pin form.

- Edit Power Via

  Opens the Edit Power Vias form.

- Repair Power Stripes

  Opens the Repair Power Stripes form.

- Optimize Power Plan

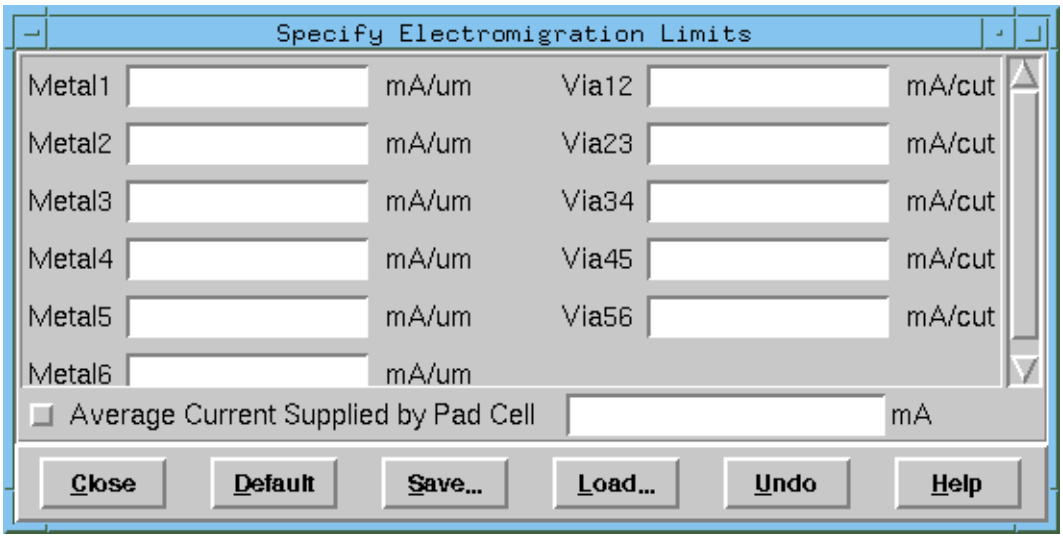
  Opens the Optimize Power Plan form.

Specify Electromigration Limits

Use the Specify Electromigration Limits form to define electromigration limits for metal layers (in milliamperes per micrometer) and vias (in milliamperes per cut).

The power planning software obtains the electromigration values from the LEF file if `DCCURRENTDENSITY` is specified in the LEF file.

➤ To open the Specify Electromigration Limits form, choose *Power – Power Planning – Specify Electromigration*.



Specify Electromigration Limits Fields and Options

METAL N	Specifies the electromigration limit for a metal layer (in milliamperes per micrometer).
VIA NN	Specifies the electromigration limit for a via cut (in milliamperes per cut).

Average Current Supplied by Pad Cell

Specifies the average current supplied by pad cell (in milliamperes).

The power planning software calculates the value for this field based on the EM limits and the pin shape of the pad cells. You can overwrite this calculated value by typing a new value in the text entry field. If EM limits are not specified in the LEF file, the power planning software cannot calculate this value. You will need to specify EM limits for each layer, along with a value in *Average Current Supplied by Pad Cell*.

Save

Saves your changes to an internal display setting file (`.dsf`) for use in a future session.

Important

You should not modify the `.dsf` file manually as this may cause data integrity issues within Encounter.

Load

Loads a `.dsf` file containing the electromigration limits from a previously saved session. To confirm the loading of the electromigration limits, you must click the *Close* button.

Important

You should not modify the `.dsf` file manually as this may cause data integrity issues within Encounter.

Edit Power Planning Option

Use the Edit Power Planning Option form to define sets of frequently used options. You can then load these options into the Add Rings, Add Stripes, and Edit Power Plan Template forms.

➤ To open the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*.

➤ You can also open the Edit Power Planning Option form by clicking *create/edit option set* icon on the *Basic* tabs of the Add Rings, Add Stripes, and Edit Power Plan Template forms.

Tip

The Edit Power Planning Option form initially contains default values for all vias, rings, and stripes in the currently loaded design. When you change any values on this form, the option set contains *only* the newly modified values. The changed values appear in the window at the top of the Edit Power Planning Option form.

To retrieve the default values, click the *Default* button.

Important

The descriptions of the following Edit Power Planning Option form pages omit the usual field descriptions, because each page of the form contains a self-explanatory diagram illustrating the usage of that page's options.

■ Eleven pages controlled by the *RING* object button:

- ❑ Edit Power Planning Option – RING – Ring Style on page 772
- ❑ Edit Power Planning Option – RING – Ring Offset on page 773
- ❑ Edit Power Planning Option – RING – Merge on page 774
- ❑ Edit Power Planning Option – RING – Jog on page 775
- ❑ Edit Power Planning Option – RING – Wire Group on page 776
- ❑ Edit Power Planning Option – RING – Wire Snap on page 777
- ❑ Edit Power Planning Option – RING – Connection Layer Range on page 778
- ❑ Edit Power Planning Option – RING – Partial Intersection Connection on page 779
- ❑ Edit Power Planning Option – RING – Orthogonal Connection on page 780
- ❑ Edit Power Planning Option – RING – Split Long Via on page 781

- ❑ Edit Power Planning Option – RING – Make Via Connect to on page 782

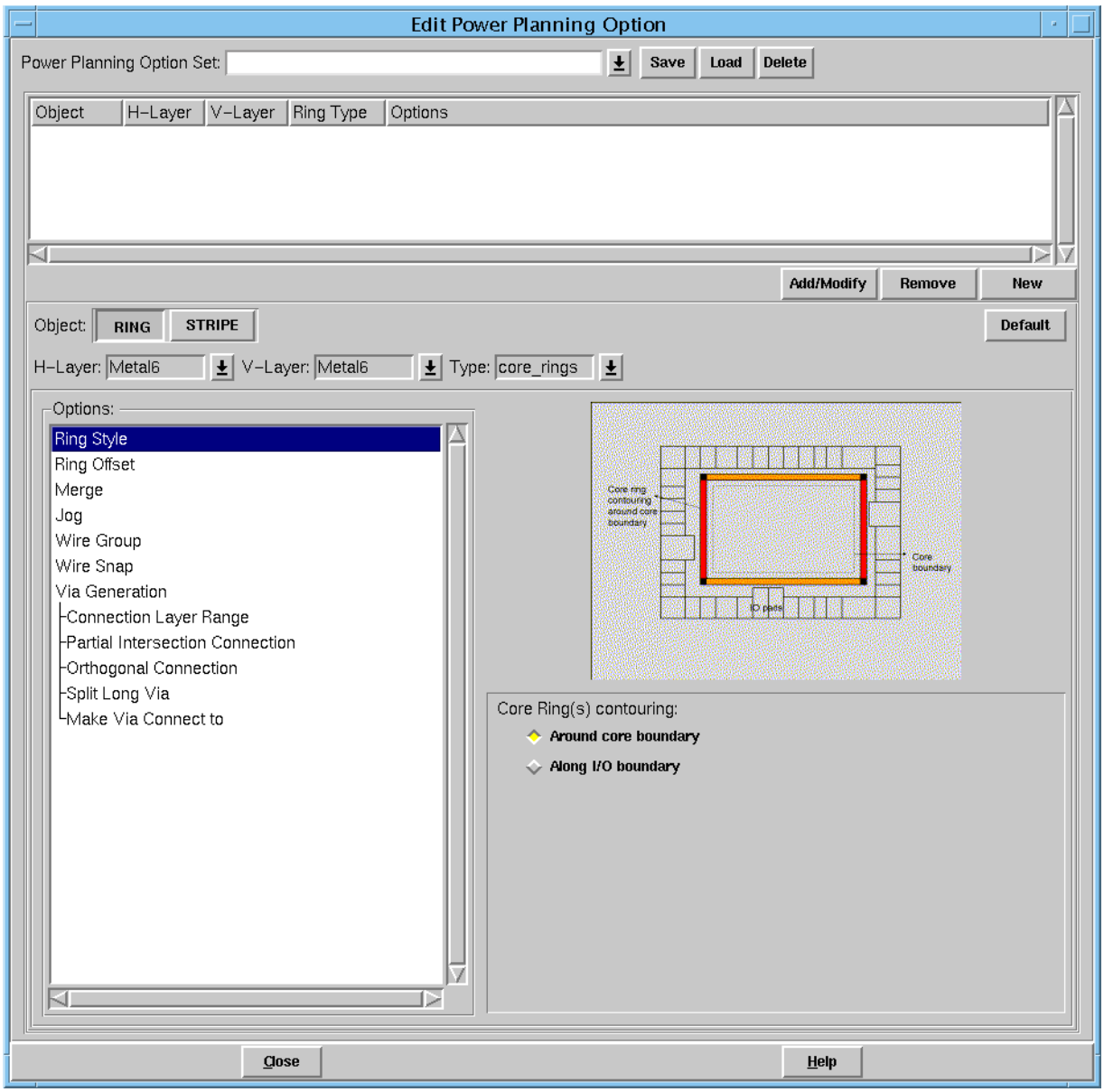
■ Twenty-four pages controlled by the *STRIPE* object button:

- ❑ Edit Power Planning Option – STRIPE – Stripe Boundary on page 783
- ❑ Edit Power Planning Option – STRIPE – First / Last Stripe on page 784
- ❑ Edit Power Planning Option – STRIPE – Stripe Breaking on page 785
- ❑ Edit Power Planning Option – STRIPE – Pad / Core Ring Connection – Jog on page 786
- ❑ Edit Power Planning Option – STRIPE – Block Ring Connection – Jog on page 787
- ❑ Edit Power Planning Option – STRIPE – Block Ring Connection – Merge on page 788
- ❑ Edit Power Planning Option – STRIPE – Jog Length on page 789
- ❑ Edit Power Planning Option – STRIPE – Pad / Core Ring Connection on page 790
- ❑ Edit Power Planning Option – STRIPE – Block Ring Connection on page 791
- ❑ Edit Power Planning Option – STRIPE – Wire Group on page 792
- ❑ Edit Power Planning Option – STRIPE – Wire Snap on page 793
- ❑ Edit Power Planning Option – STRIPE – Connection Layer Range on page 794
- ❑ Edit Power Planning Option – STRIPE – Partial Intersection Connection on page 795
- ❑ Edit Power Planning Option – STRIPE – Orthogonal Connection on page 796
- ❑ Edit Power Planning Option – STRIPE – Split Long Via on page 797
- ❑ Edit Power Planning Option – STRIPE – Make Via Connect to on page 798
- ❑ Edit Power Planning Option – STRIPE – Split Vias on page 799
- ❑ Edit Power Planning Option – STRIPE – Same Size Stack Vias on page 800
- ❑ Edit Power Planning Option – STRIPE – Same Layer Target Connection on page 801
- ❑ Edit Power Planning Option – STRIPE – Stripe Over Row on page 802
- ❑ Edit Power Planning Option – STRIPE – Closest Target on page 803
- ❑ Edit Power Planning Option – STRIPE – Switch Cell Pin Target on page 804

- Edit Power Planning Option – STRIPE – Split Wire on page 805
- Edit Power Planning Option – STRIPE – Spacing From Block on page 806
- Edit Power Planning Option – STRIPE – Minimum Length on page 807

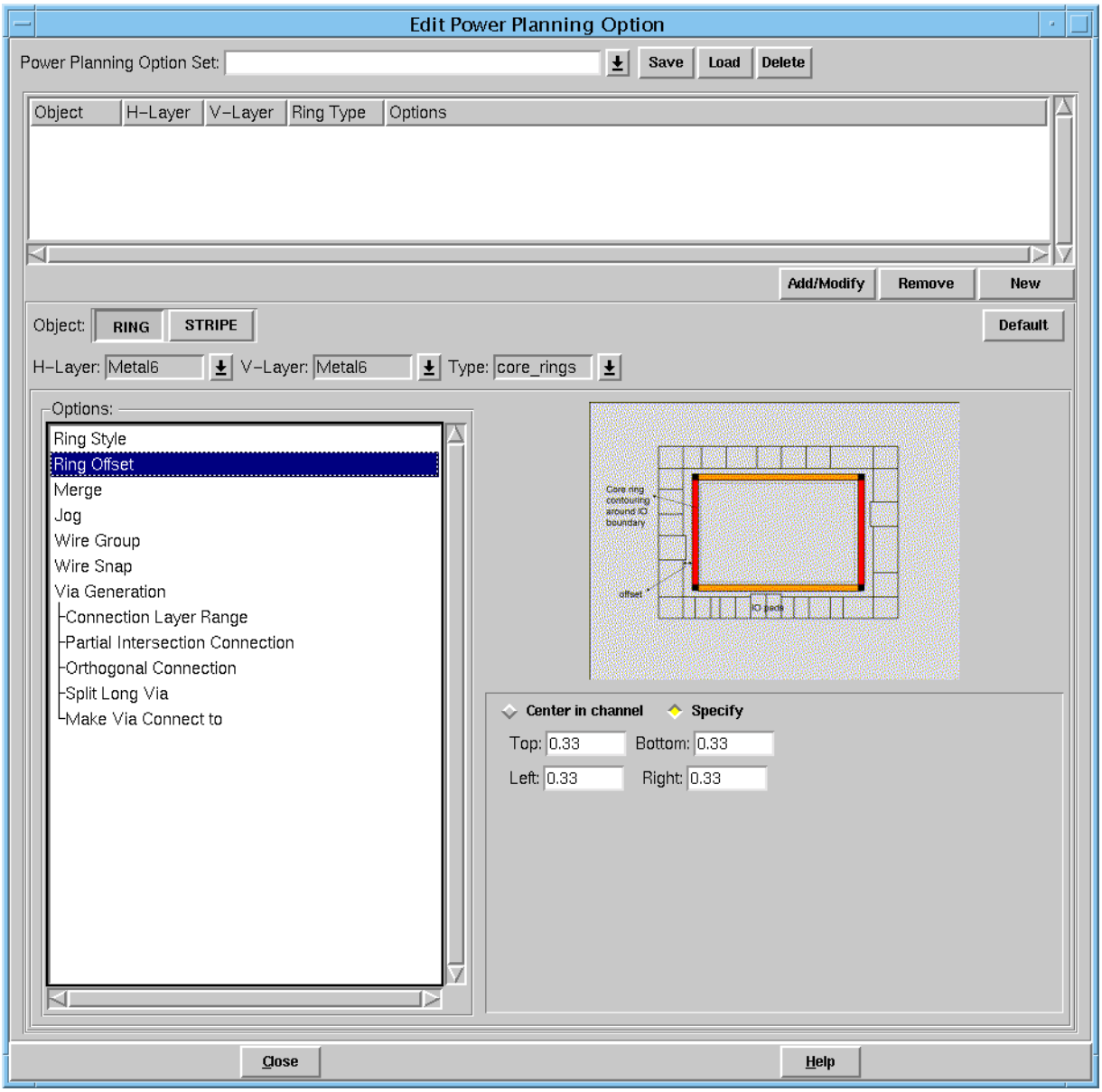
Edit Power Planning Option – RING – Ring Style

➤ To open the Ring Style page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Ring Style* from the display list.



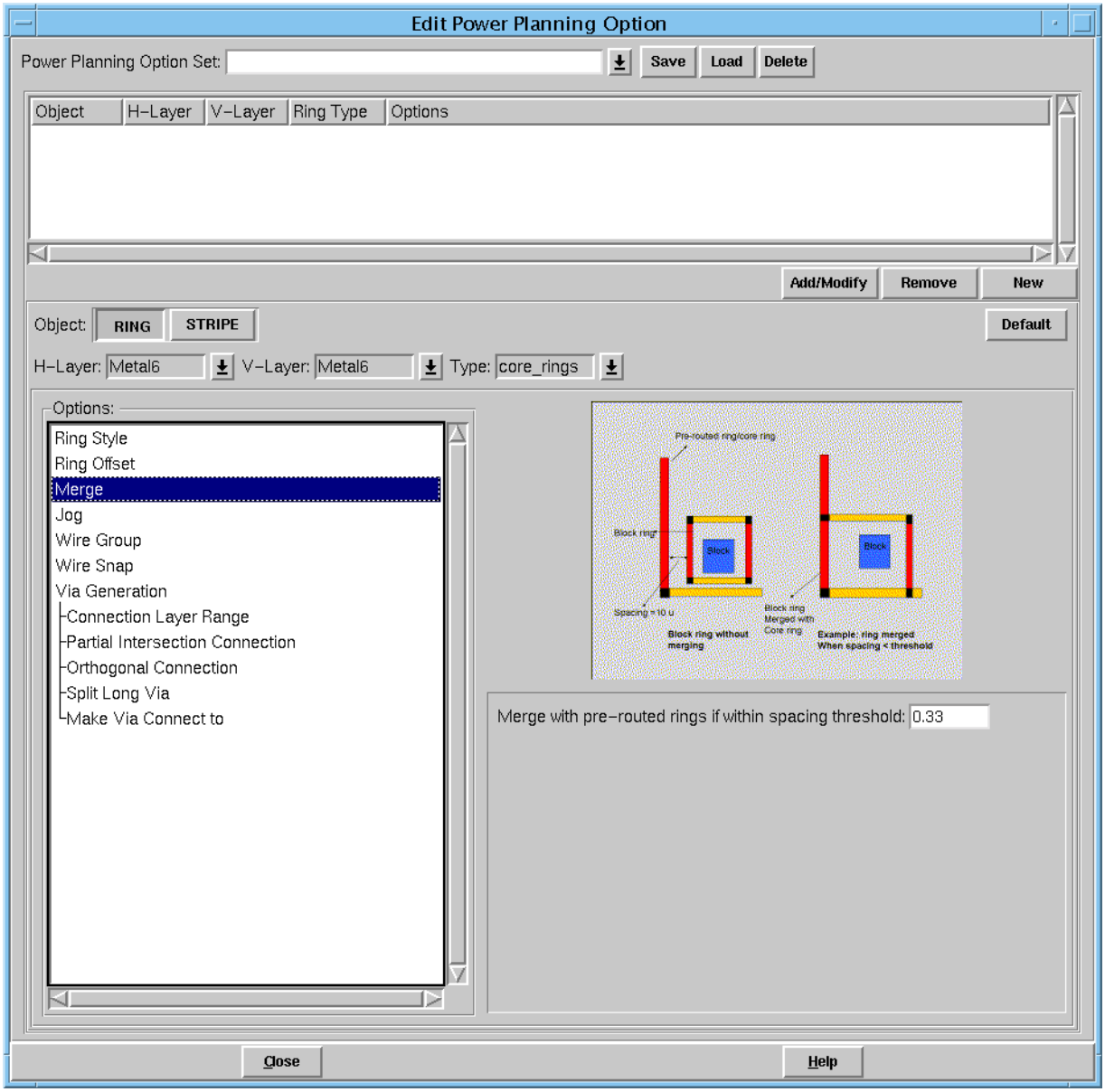
Edit Power Planning Option – RING – Ring Offset

➤ To open the Ring Offset page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Ring Offset* from the display list.



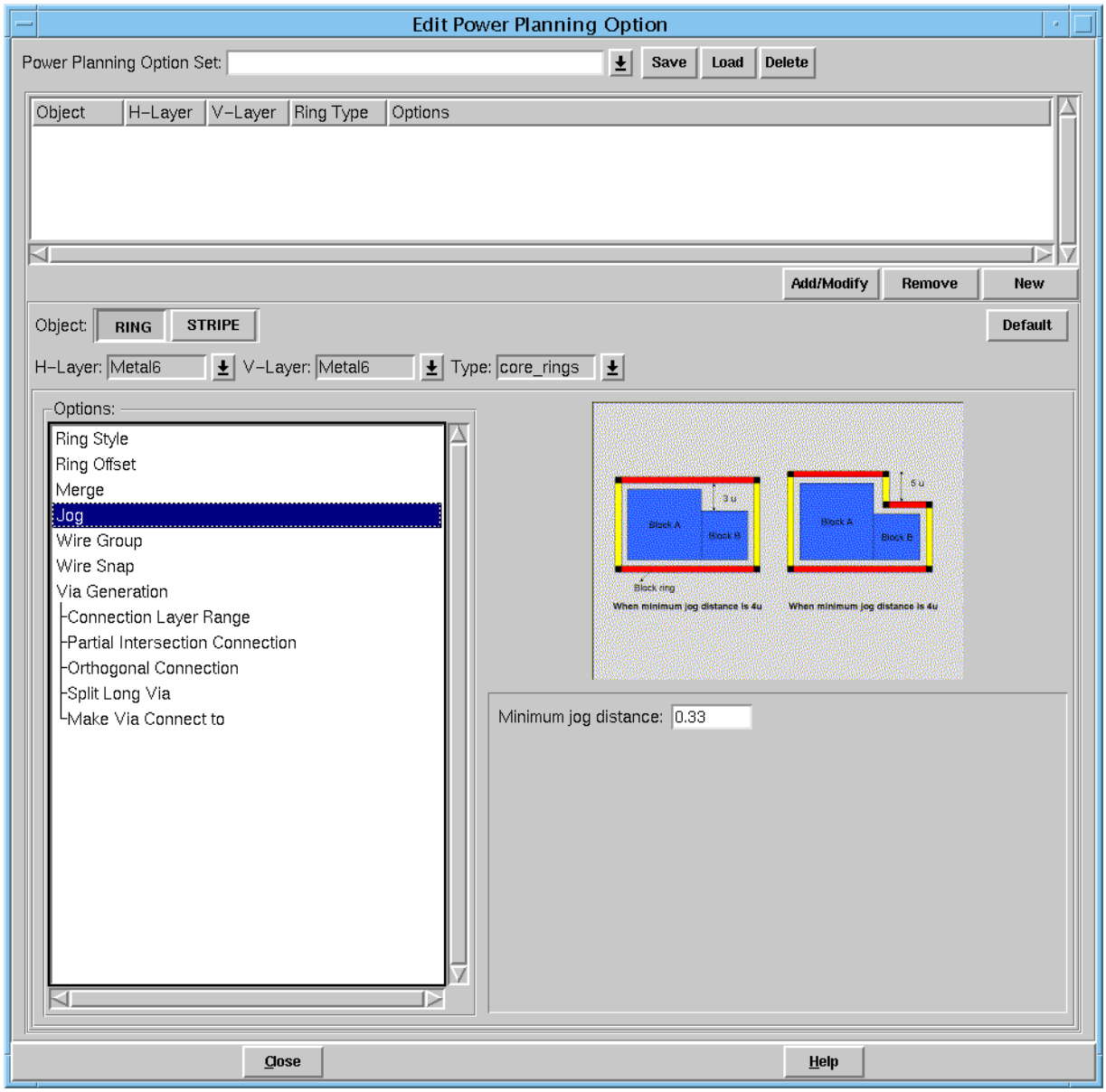
Edit Power Planning Option – RING – Merge

➤ To open the Merge page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Merge* from the display list.



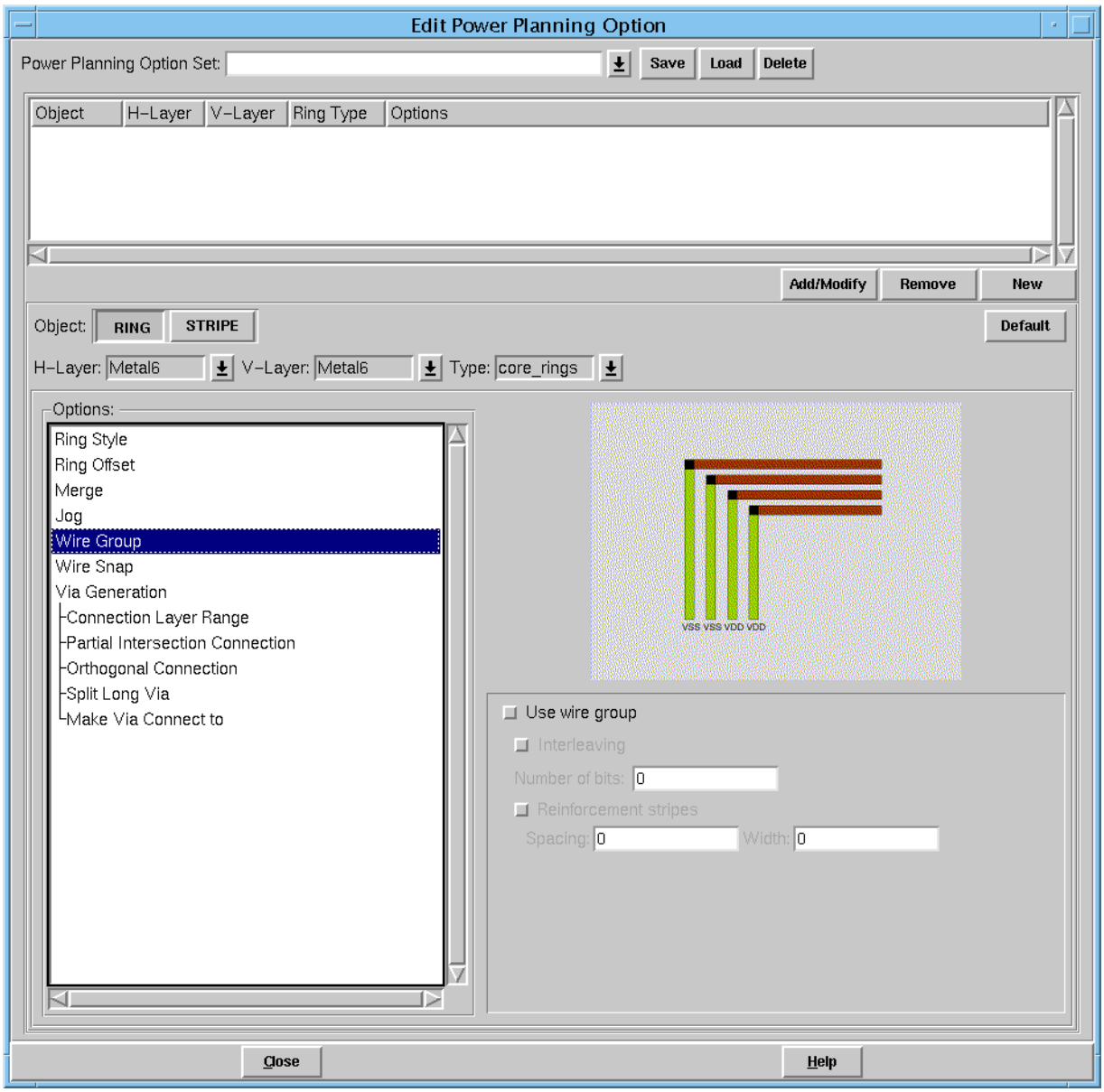
Edit Power Planning Option – RING – Jog

➤ To open the Jog page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Jog* from the display list.



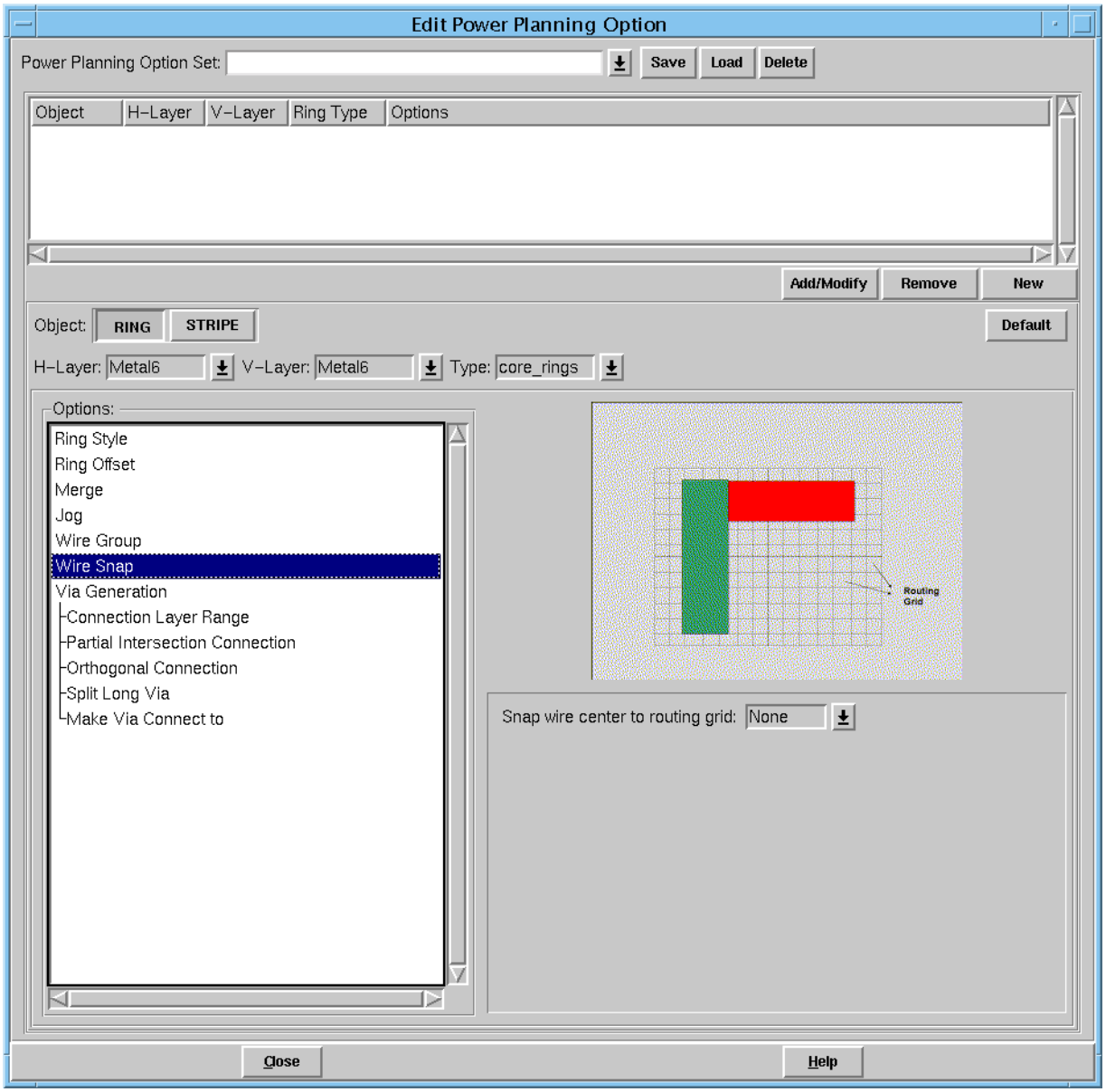
Edit Power Planning Option – RING – Wire Group

➤ To open the Wire Group page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Wire Group* from the display list.



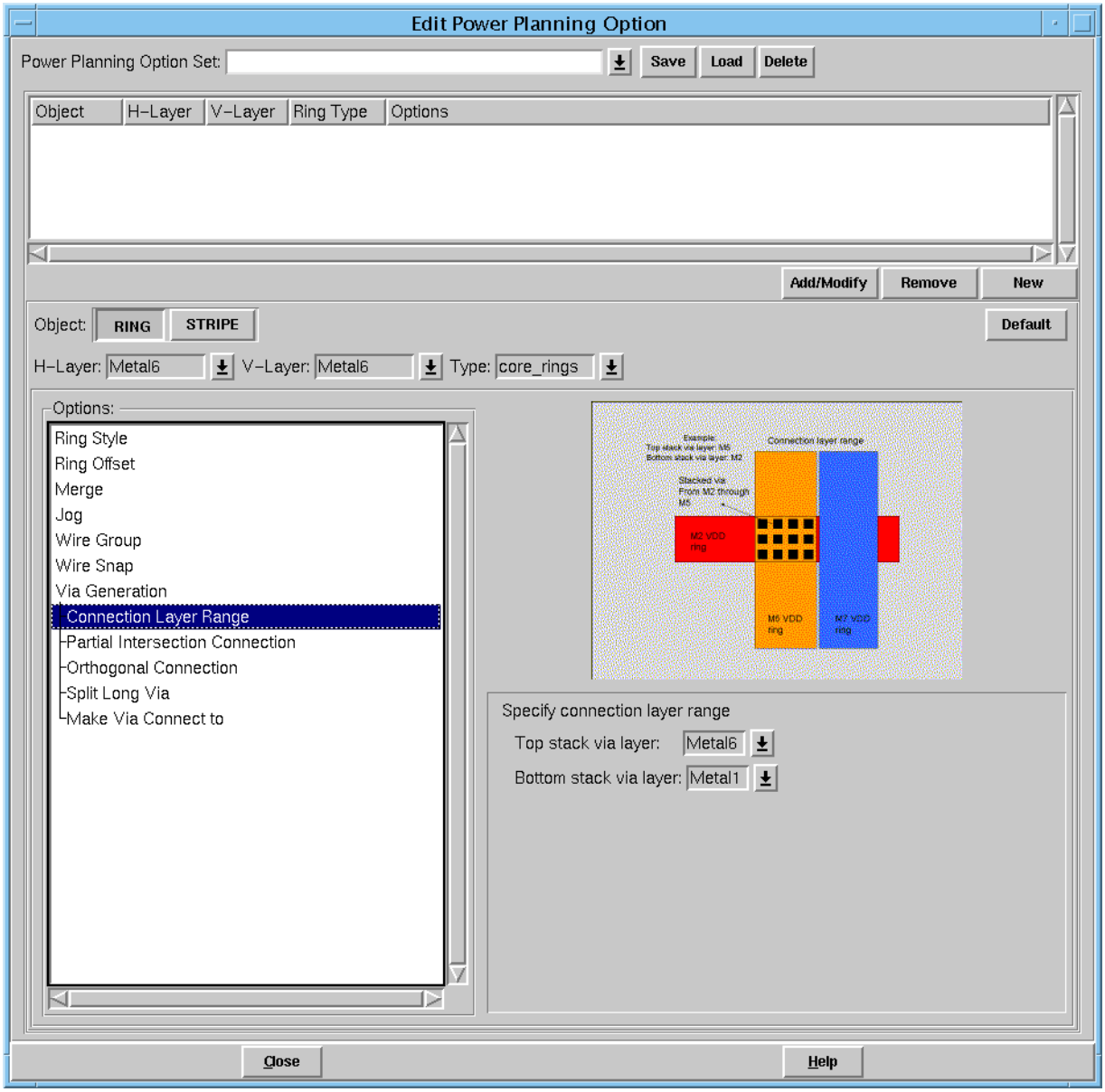
Edit Power Planning Option – RING – Wire Snap

➤ To open the Wire Snap page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Wire Snap* from the display list.



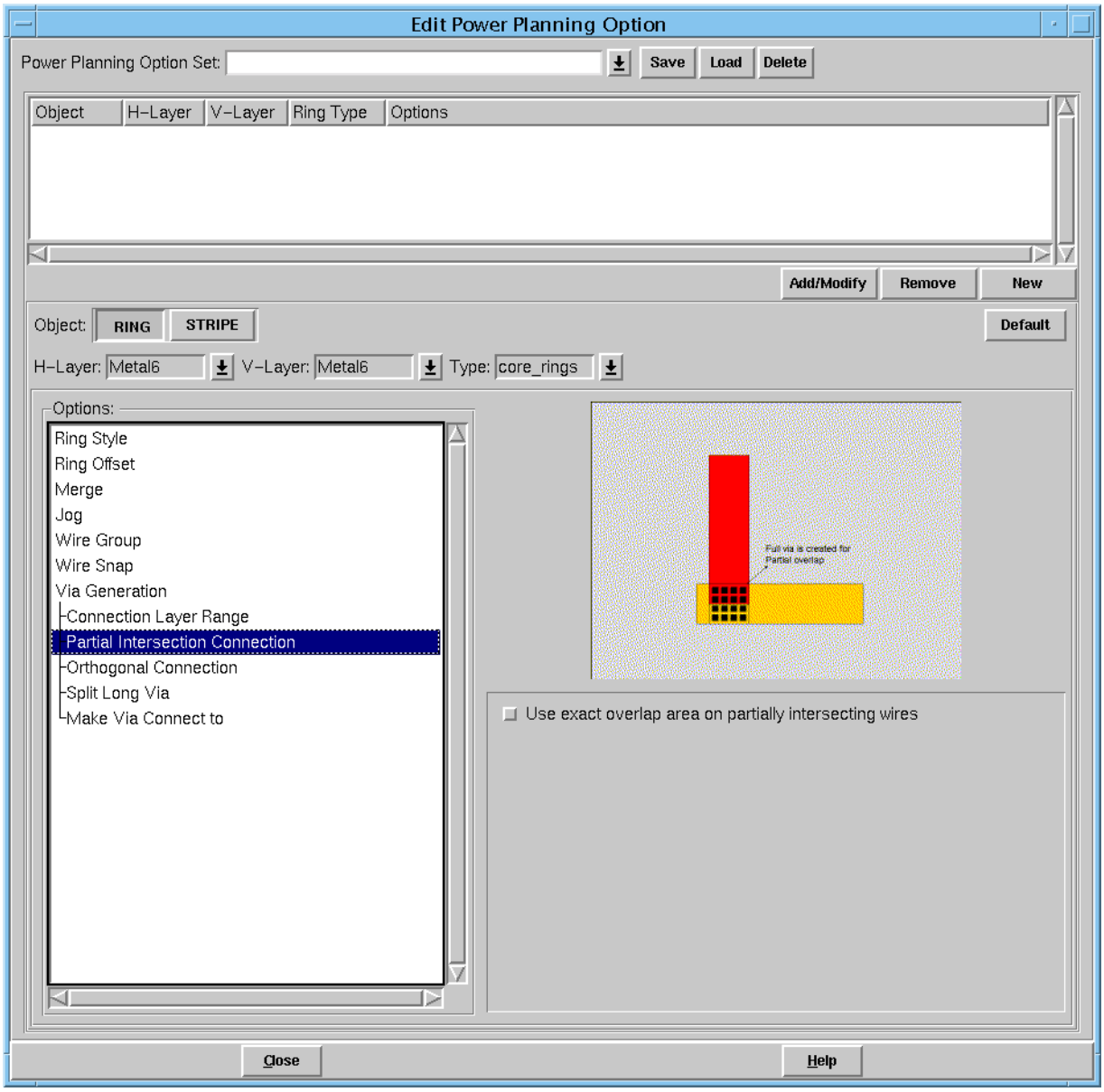
Edit Power Planning Option – RING – Connection Layer Range

➤ To open the Connect Layer Range page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Connection Layer Range* from the display list.



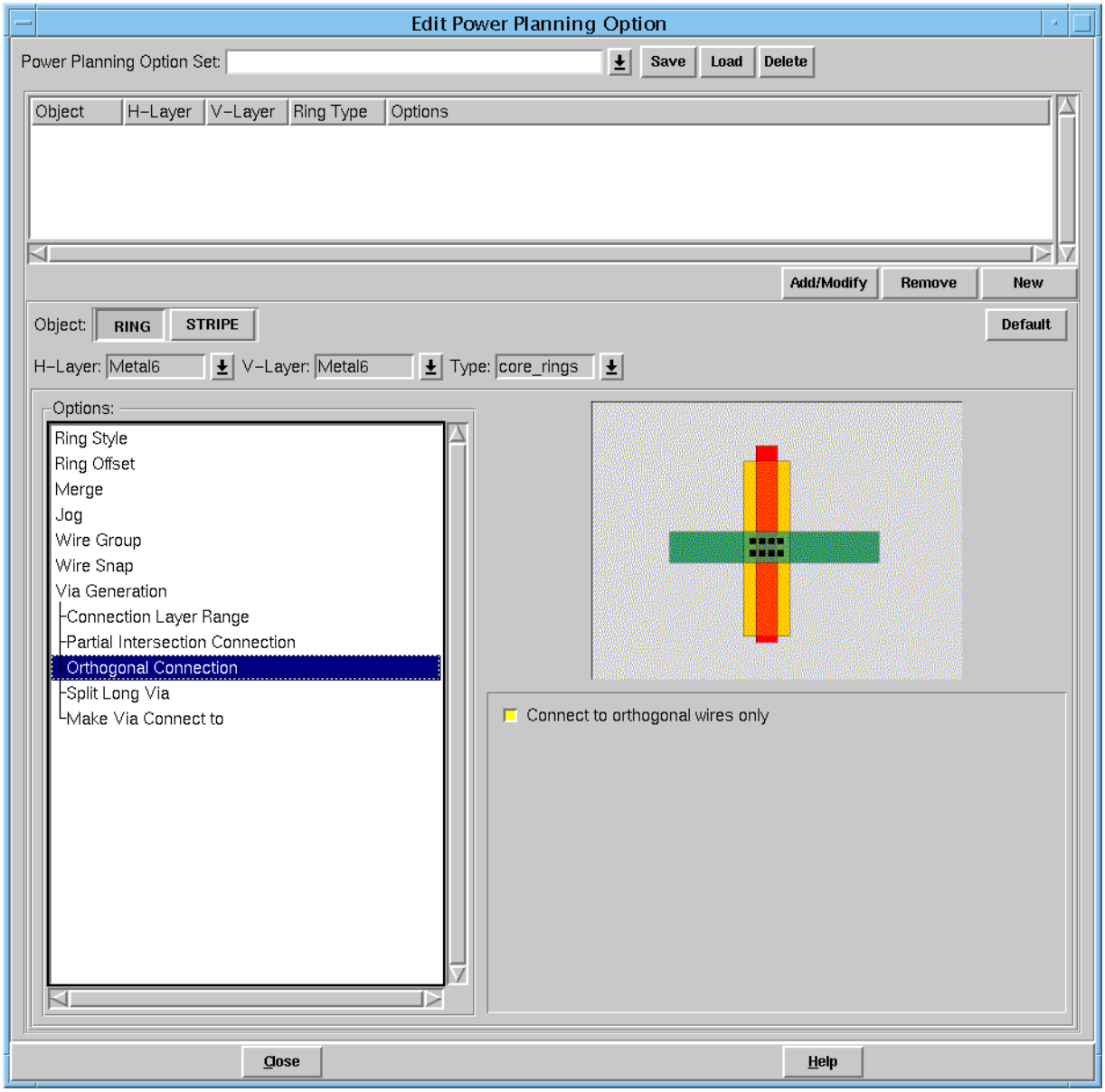
Edit Power Planning Option – RING – Partial Intersection Connection

➤ To open the Partial Intersection Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Partial Intersection Connection* from the display list.



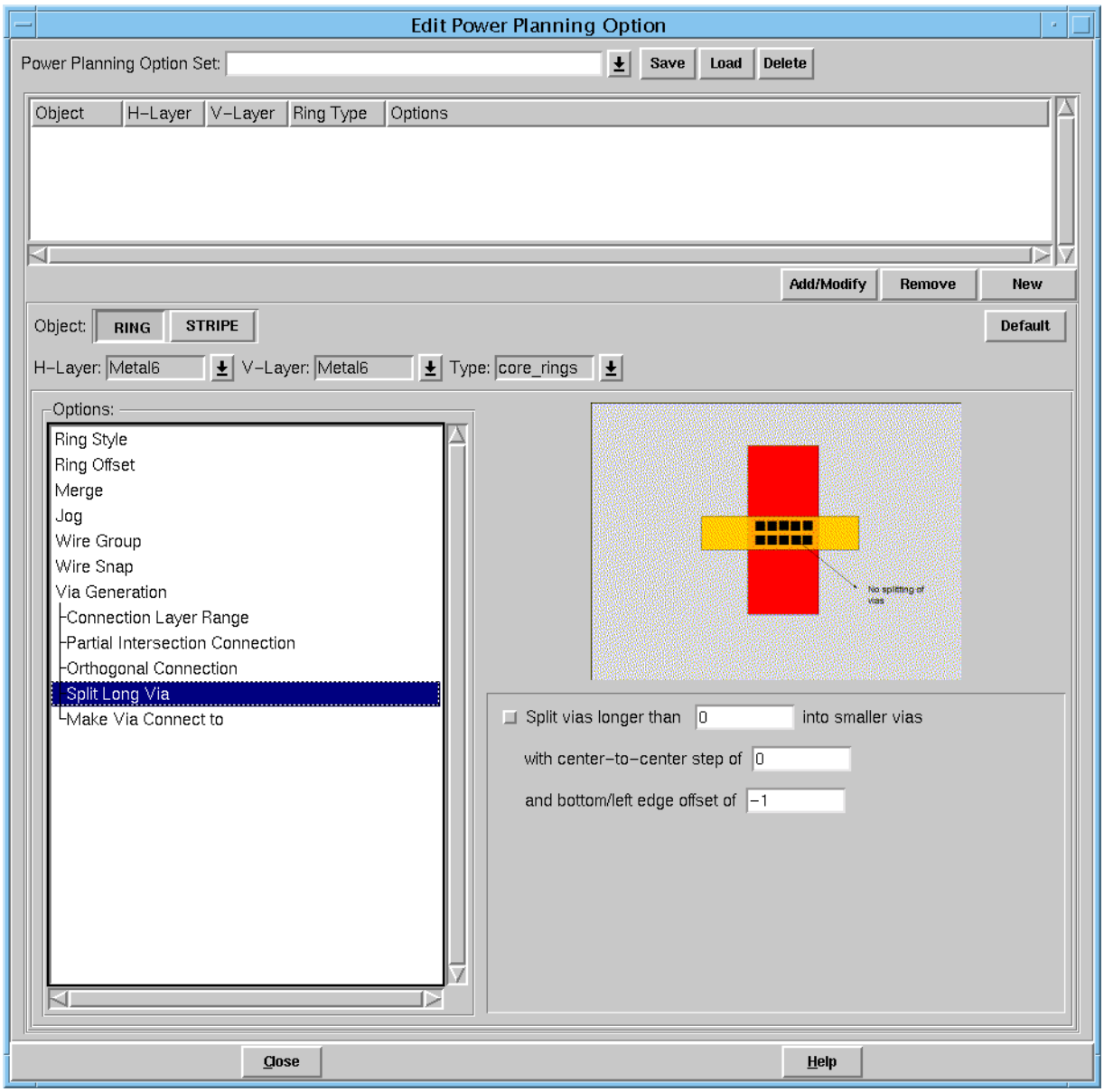
Edit Power Planning Option – RING – Orthogonal Connection

➤ To open the Orthogonal Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Orthogonal Connection* from the display list.



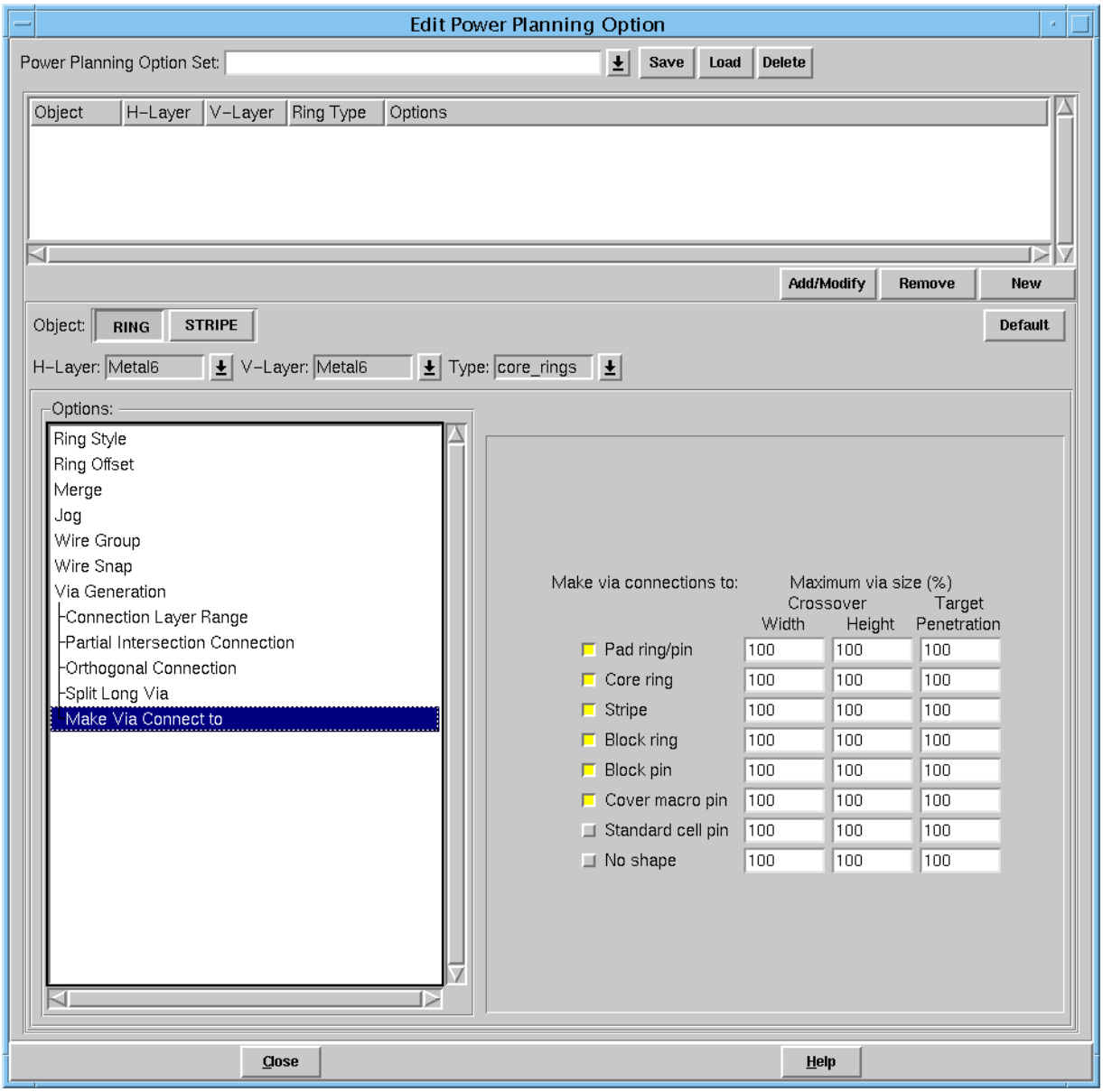
Edit Power Planning Option – RING – Split Long Via

➤ To open the Split Long Via page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Split Long Via* from the display list.



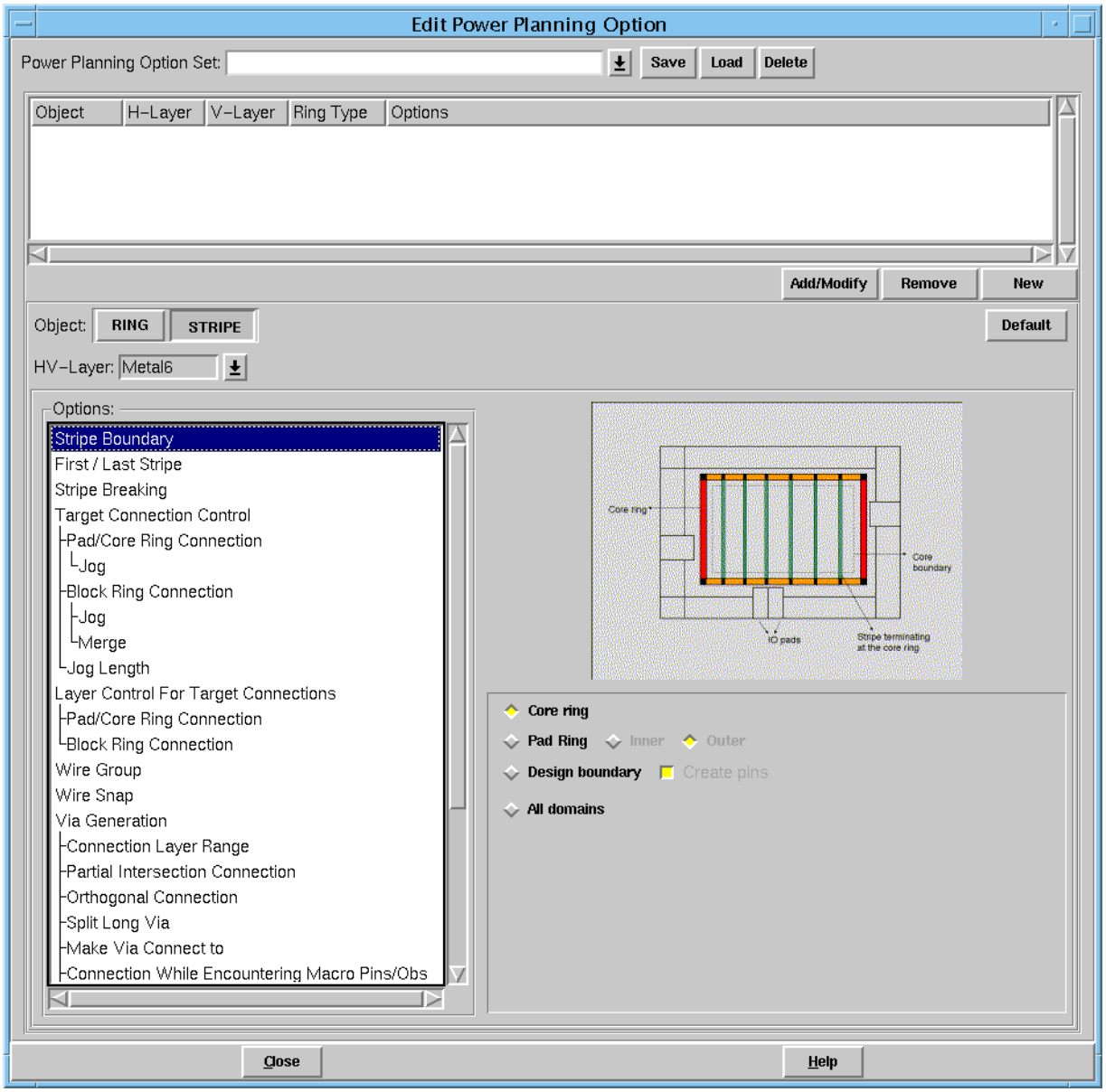
Edit Power Planning Option – RING – Make Via Connect to

➤ To open the Make Via Connect to page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *RING*, then choose *Make Via Connect to* from the display list.



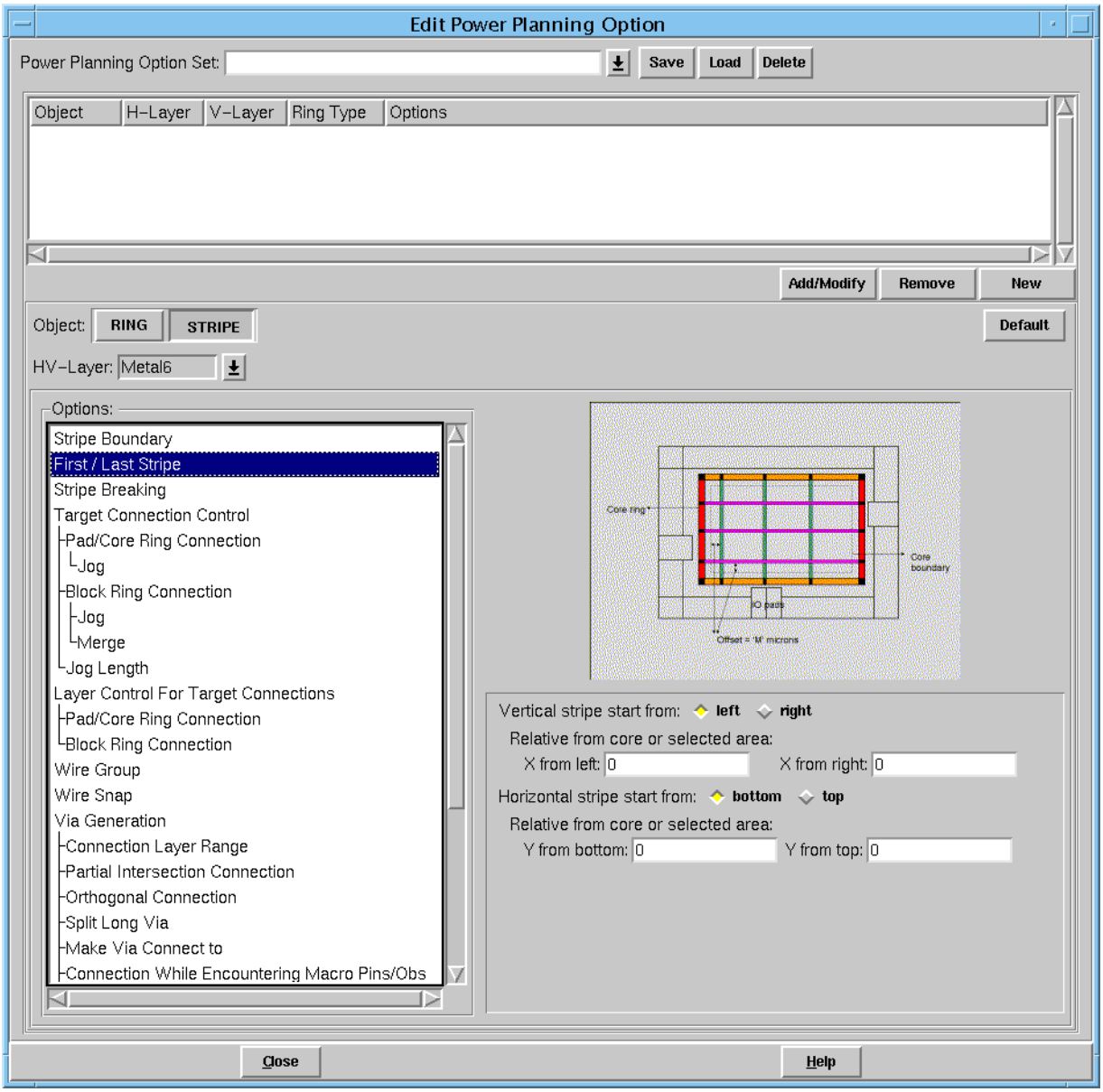
Edit Power Planning Option – STRIPE – Stripe Boundary

➤ To open the Stripe Boundary page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Stripe Boundary* from the display list.



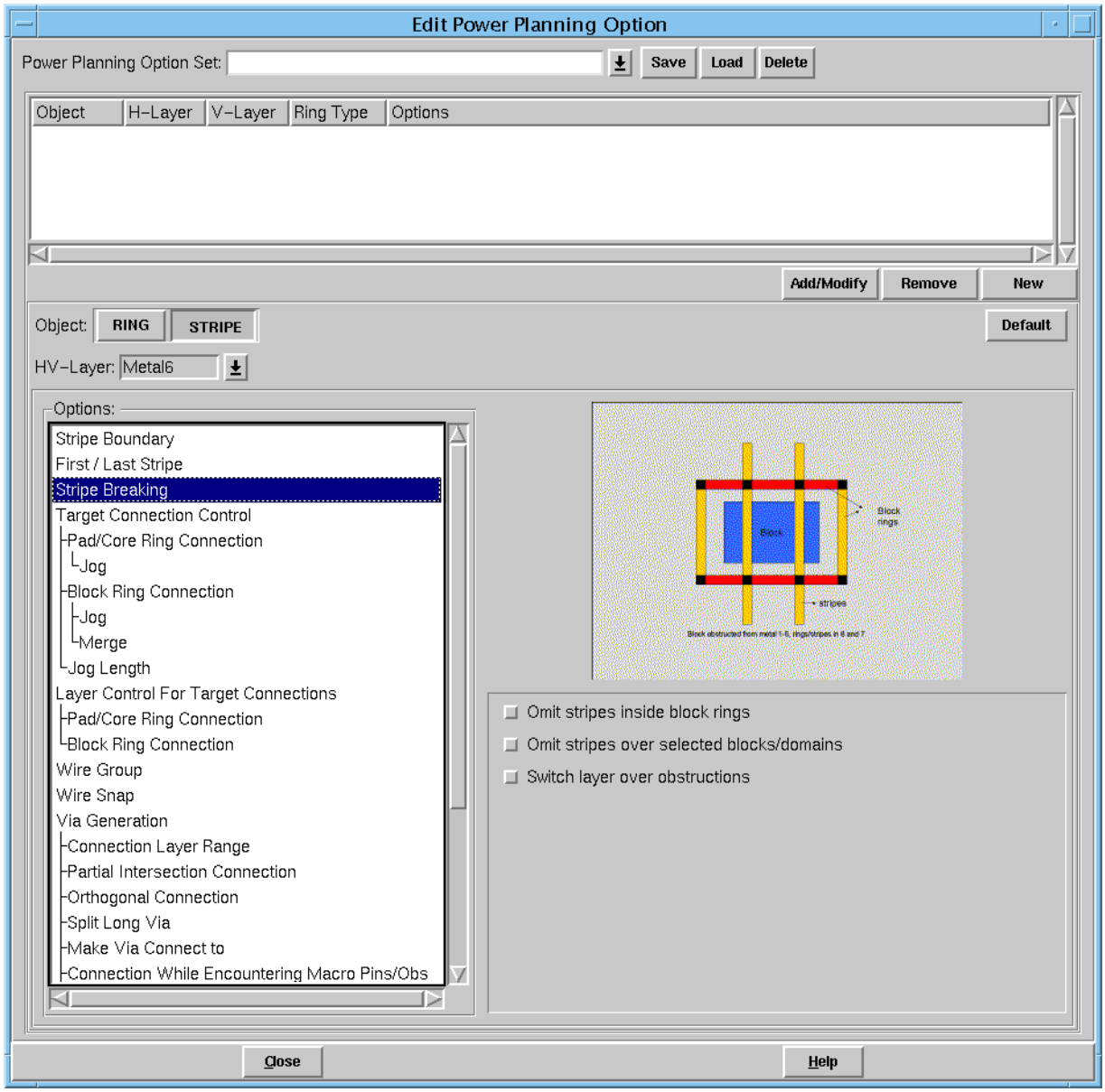
Edit Power Planning Option – STRIPE – First / Last Stripe

➤ To open the First / Last Stripe page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *First / Last Stripe* from the display list.



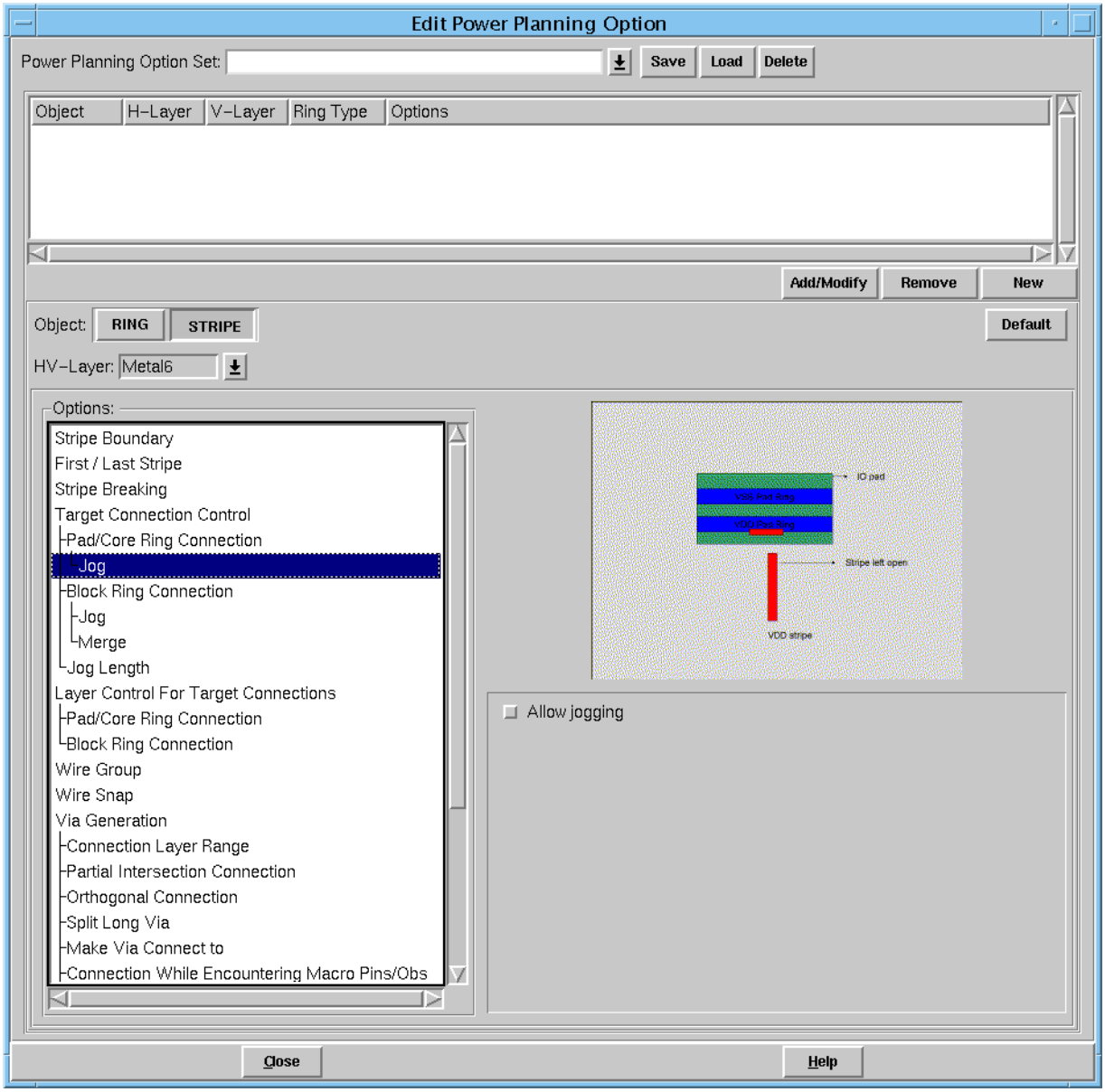
Edit Power Planning Option – STRIPE – Stripe Breaking

➤ To open the Stripe Breaking page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Stripe Breaking* from the display list.



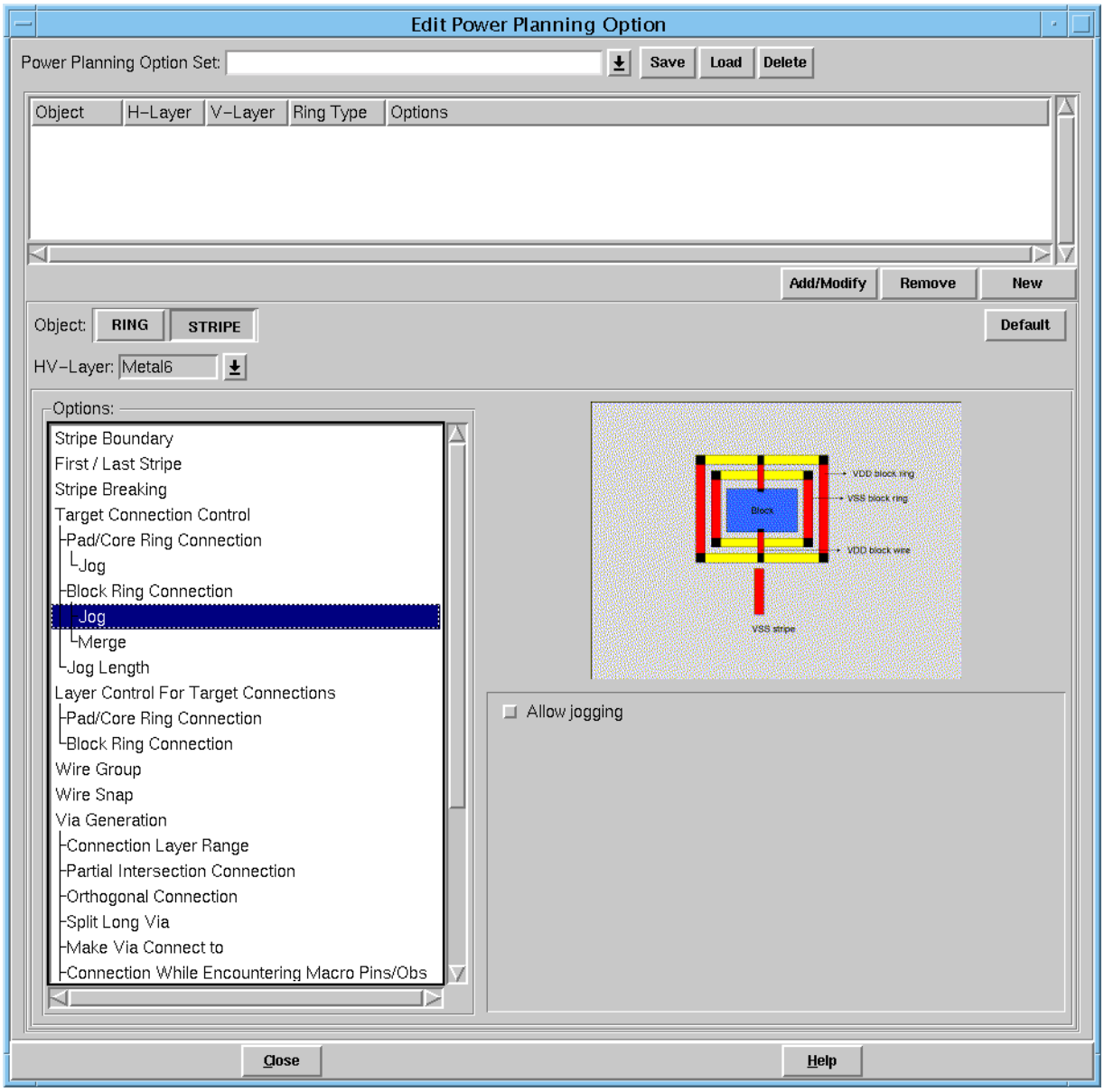
Edit Power Planning Option – STRIPE – Pad / Core Ring Connection – Jog

➤ To open the Pad / Core Ring Connection – Jog page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Pad / Core Ring Connection – Jog* from the display list.



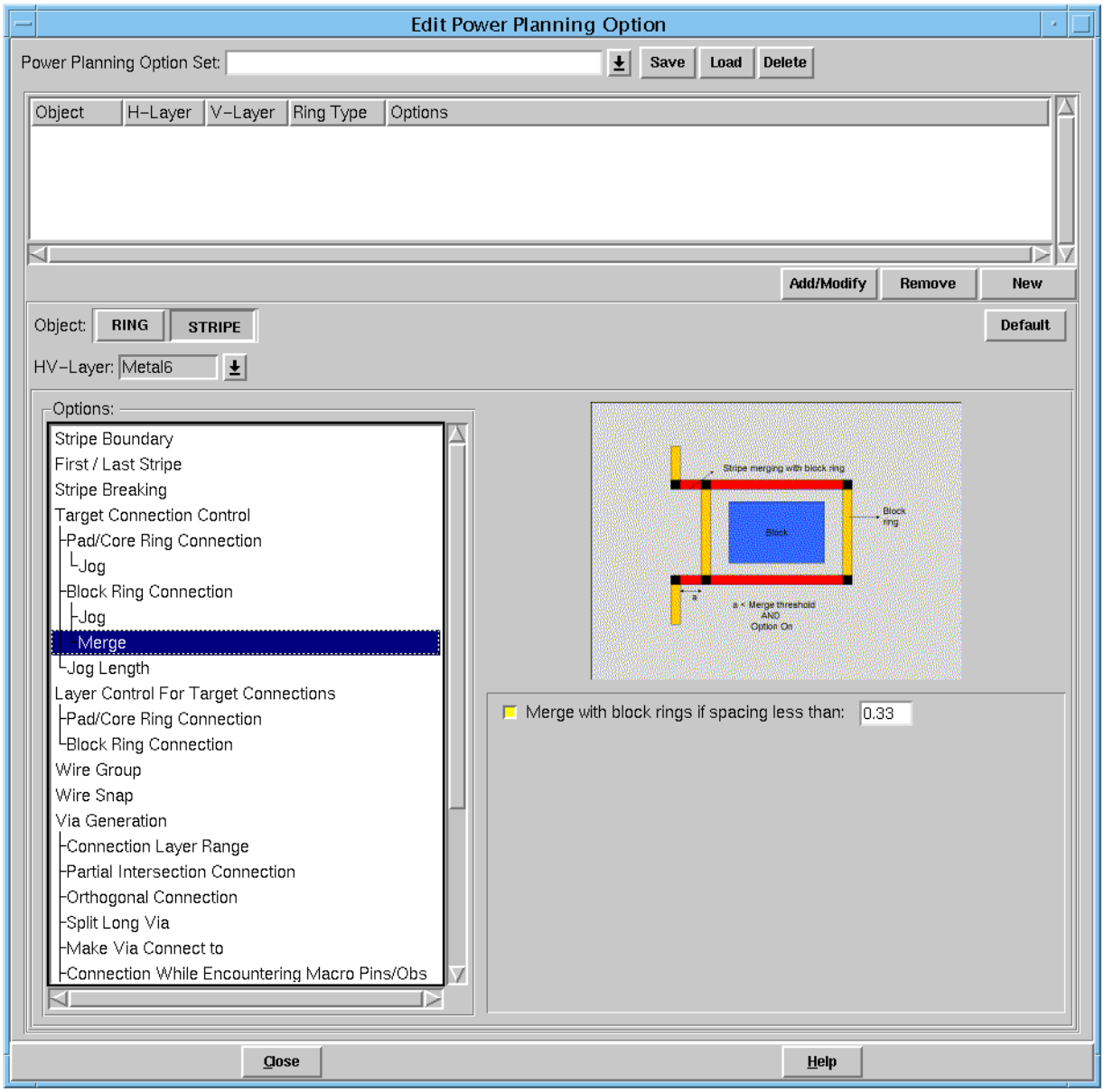
Edit Power Planning Option – STRIPE – Block Ring Connection – Jog

➤ To open the Block Ring Connection – Jog page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Block Ring Connection – Jog* from the display list.



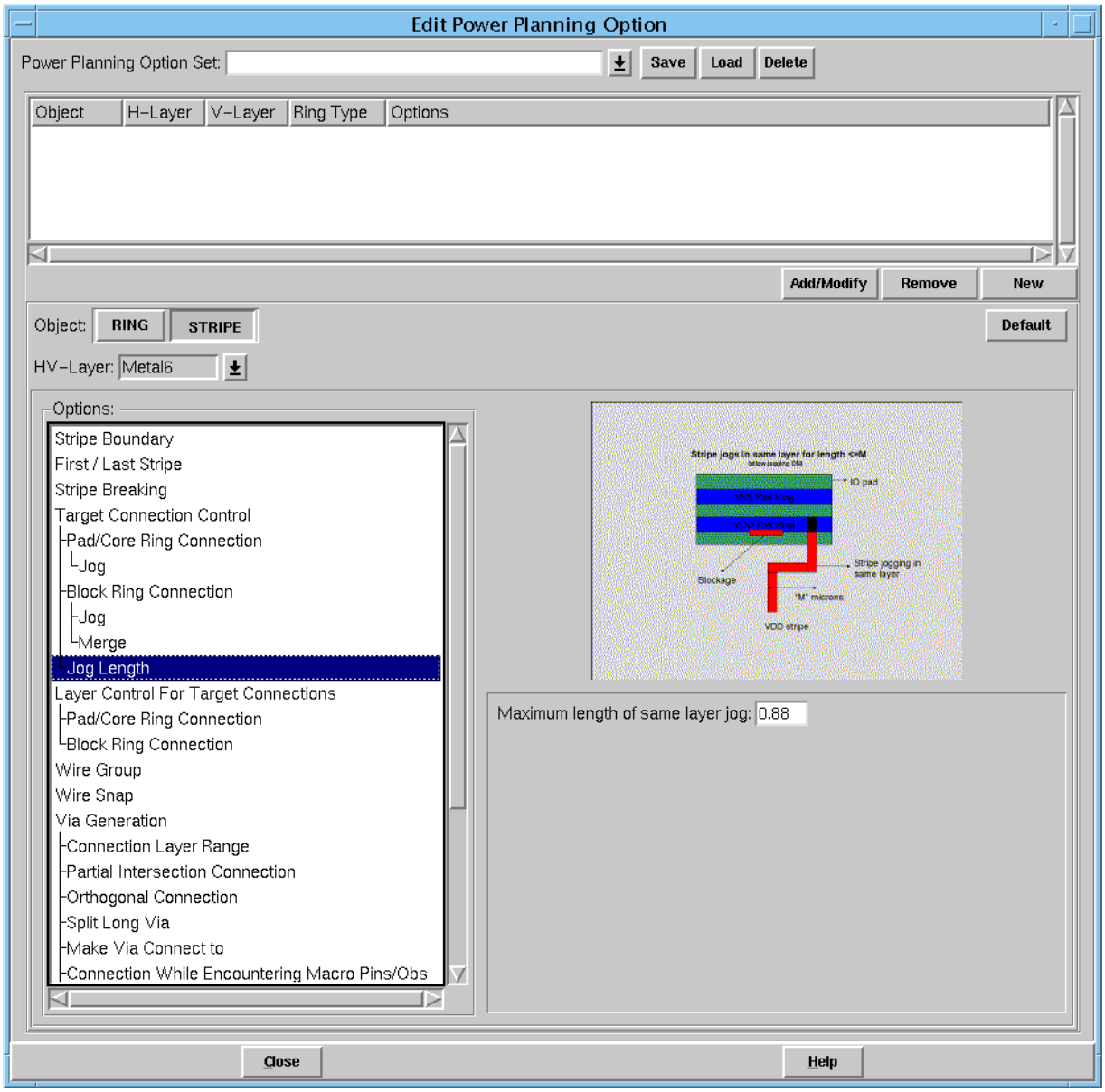
Edit Power Planning Option – STRIPE – Block Ring Connection – Merge

➤ To open the Block Ring Connection – Merge page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Block Ring Connection – Merge* from the display list.



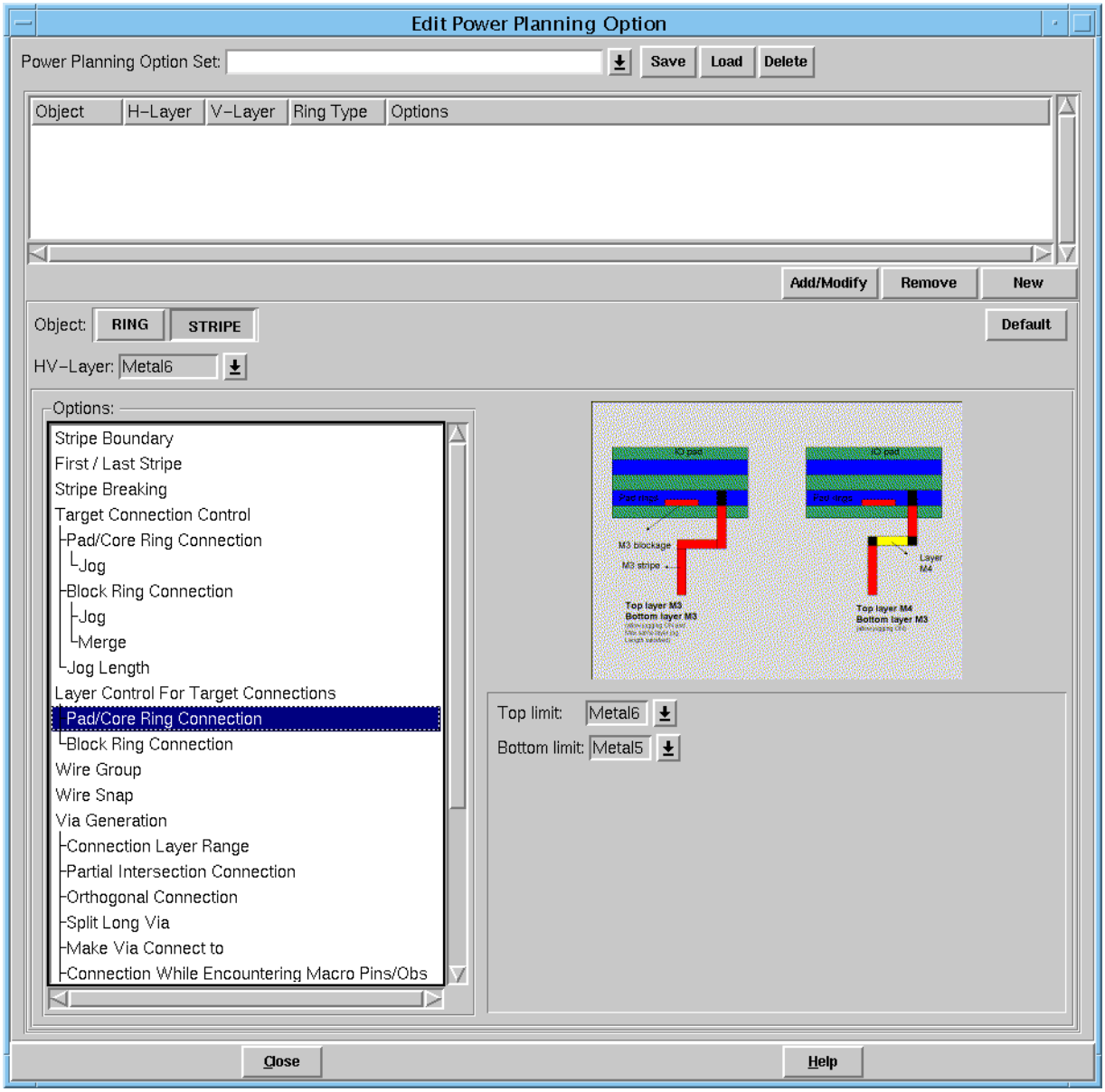
Edit Power Planning Option – STRIPE – Jog Length

➤ To open the Jog Length page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Jog Length* from the display list.



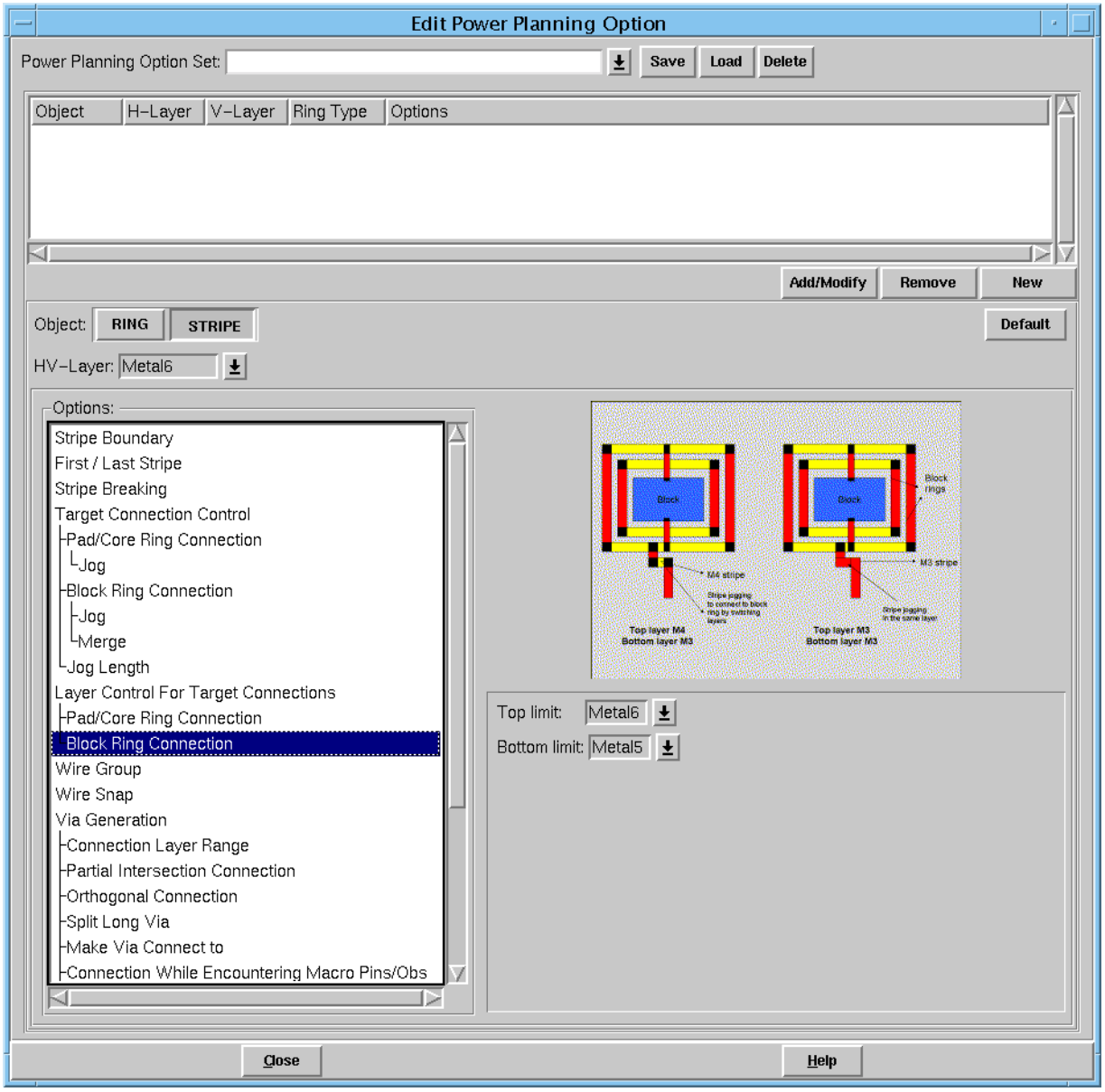
Edit Power Planning Option – STRIPE – Pad / Core Ring Connection

➤ To open the Pad / Core Ring Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Pad / Core Ring Connection* from the display list.



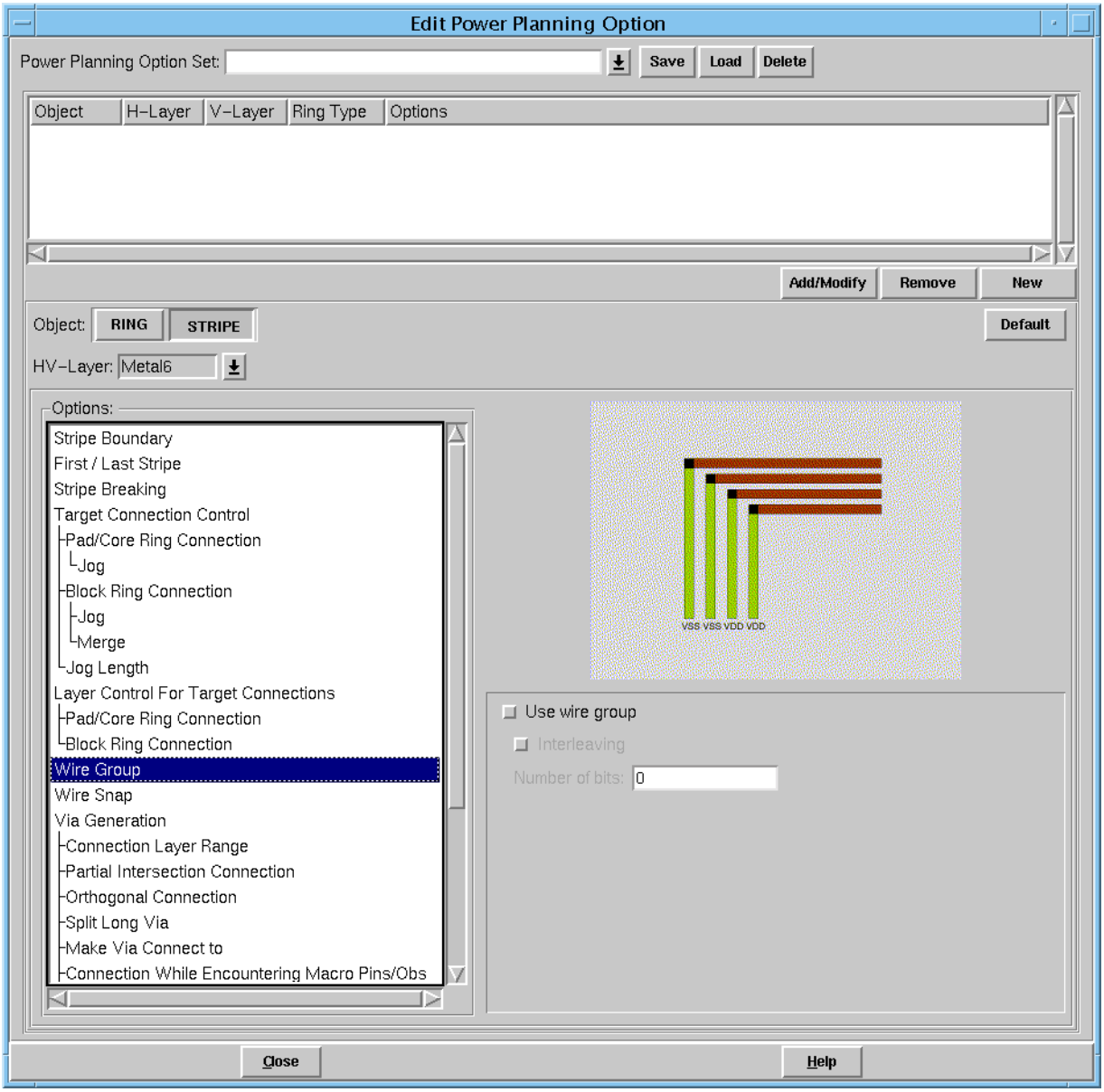
Edit Power Planning Option – STRIPE – Block Ring Connection

➤ To open the Block Ring Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Block Ring Connection* from the display list.



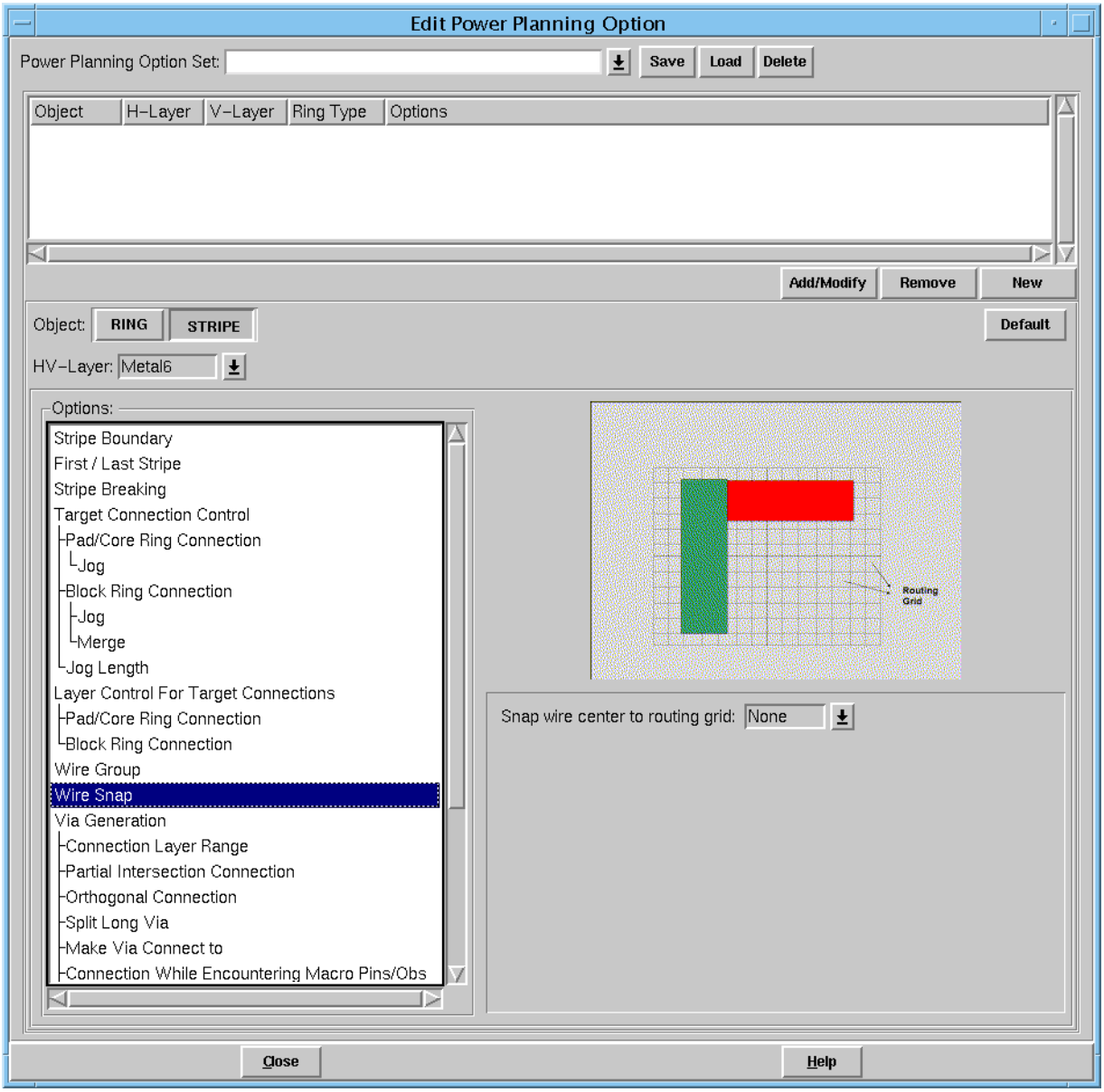
Edit Power Planning Option – STRIPE – Wire Group

➤ To open the Wire Group page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Wire Group* from the display list.



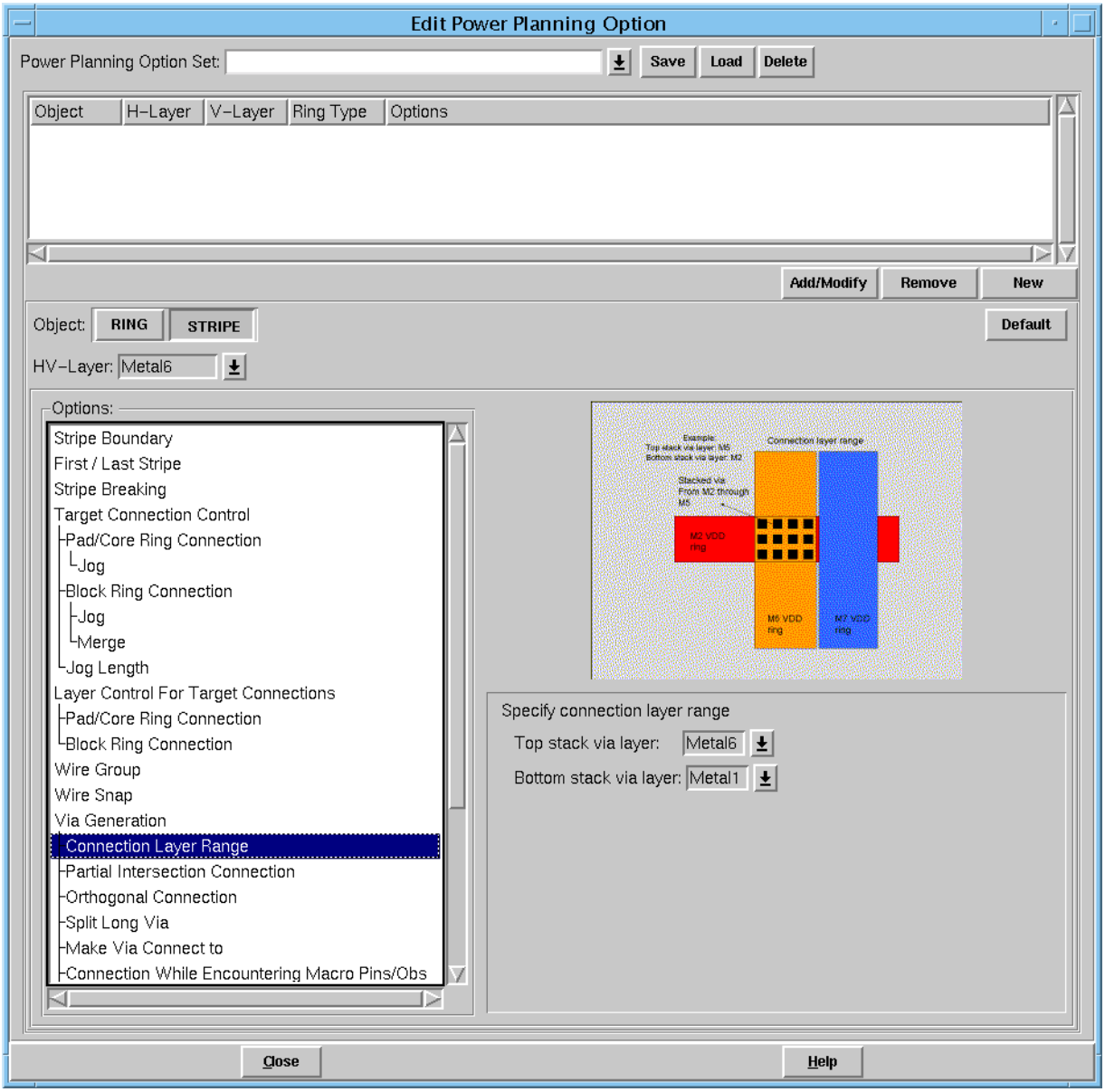
Edit Power Planning Option – STRIPE – Wire Snap

➤ To open the Wire Snap page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Wire Snap* from the display list.



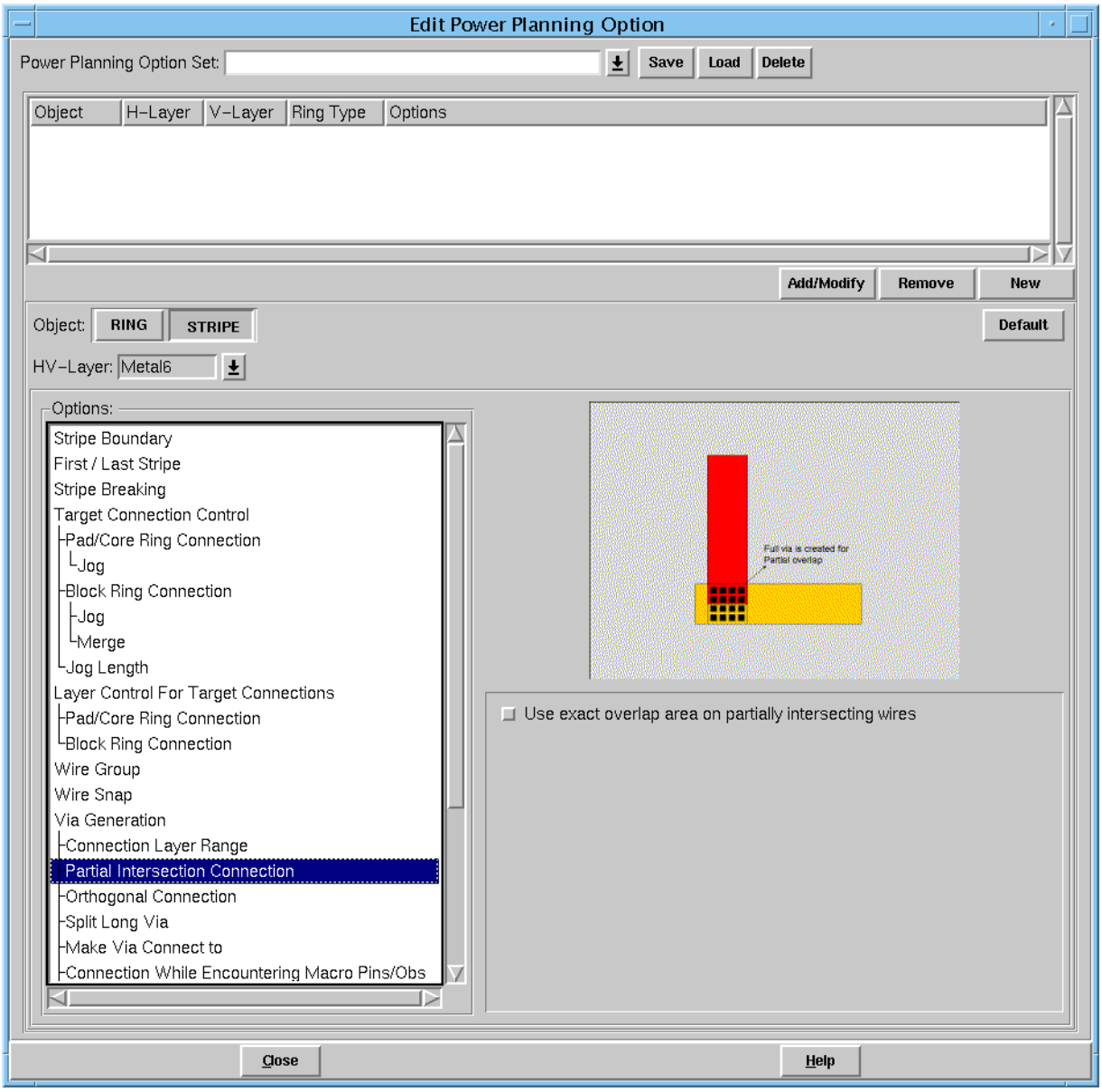
Edit Power Planning Option – STRIPE – Connection Layer Range

➤ To open the Connection Layer Range page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Connection Layer Range* from the display list.



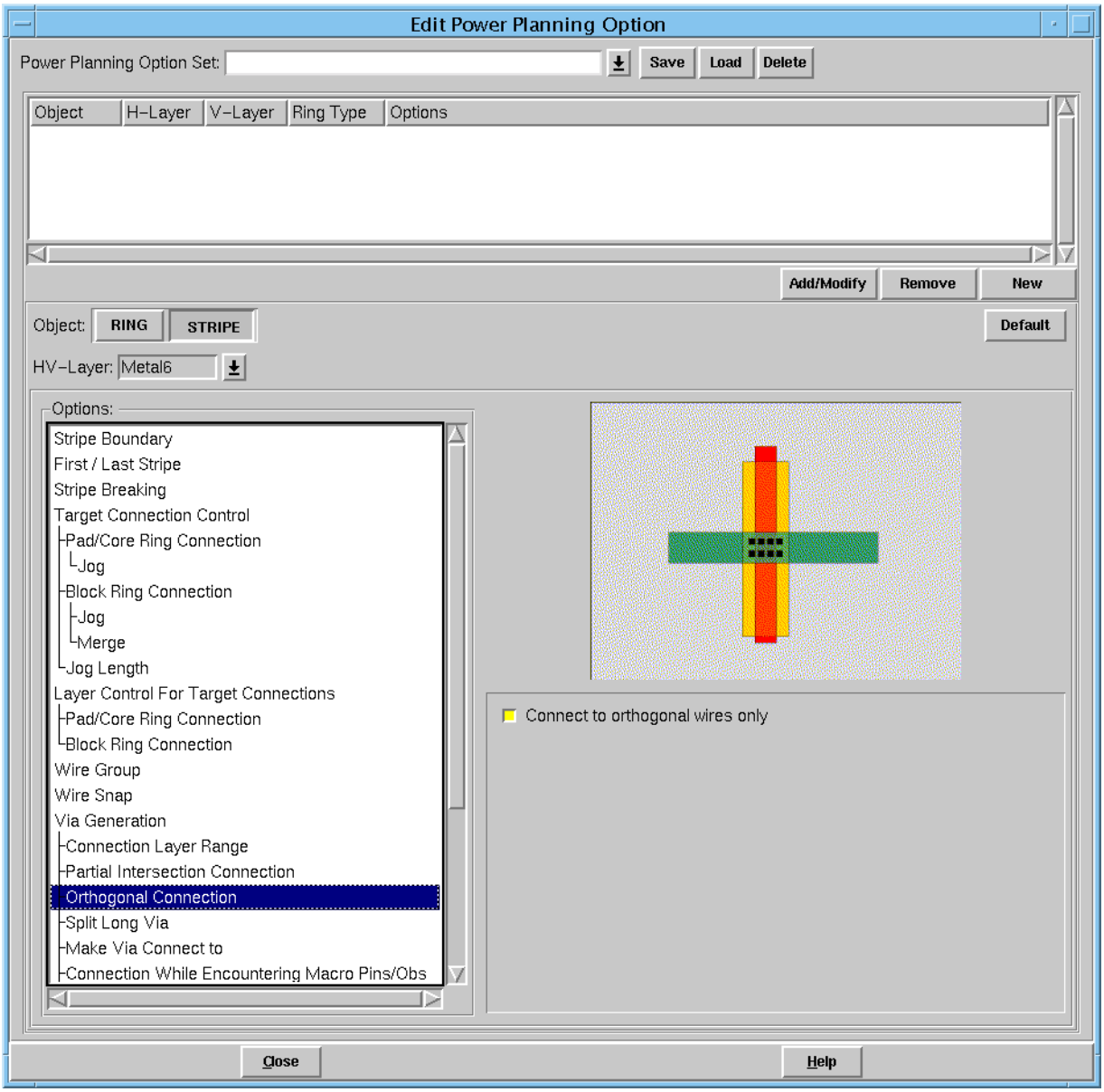
Edit Power Planning Option – STRIPE – Partial Intersection Connection

➤ To open the Partial Intersection Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Partial Intersection Connection* from the display list.



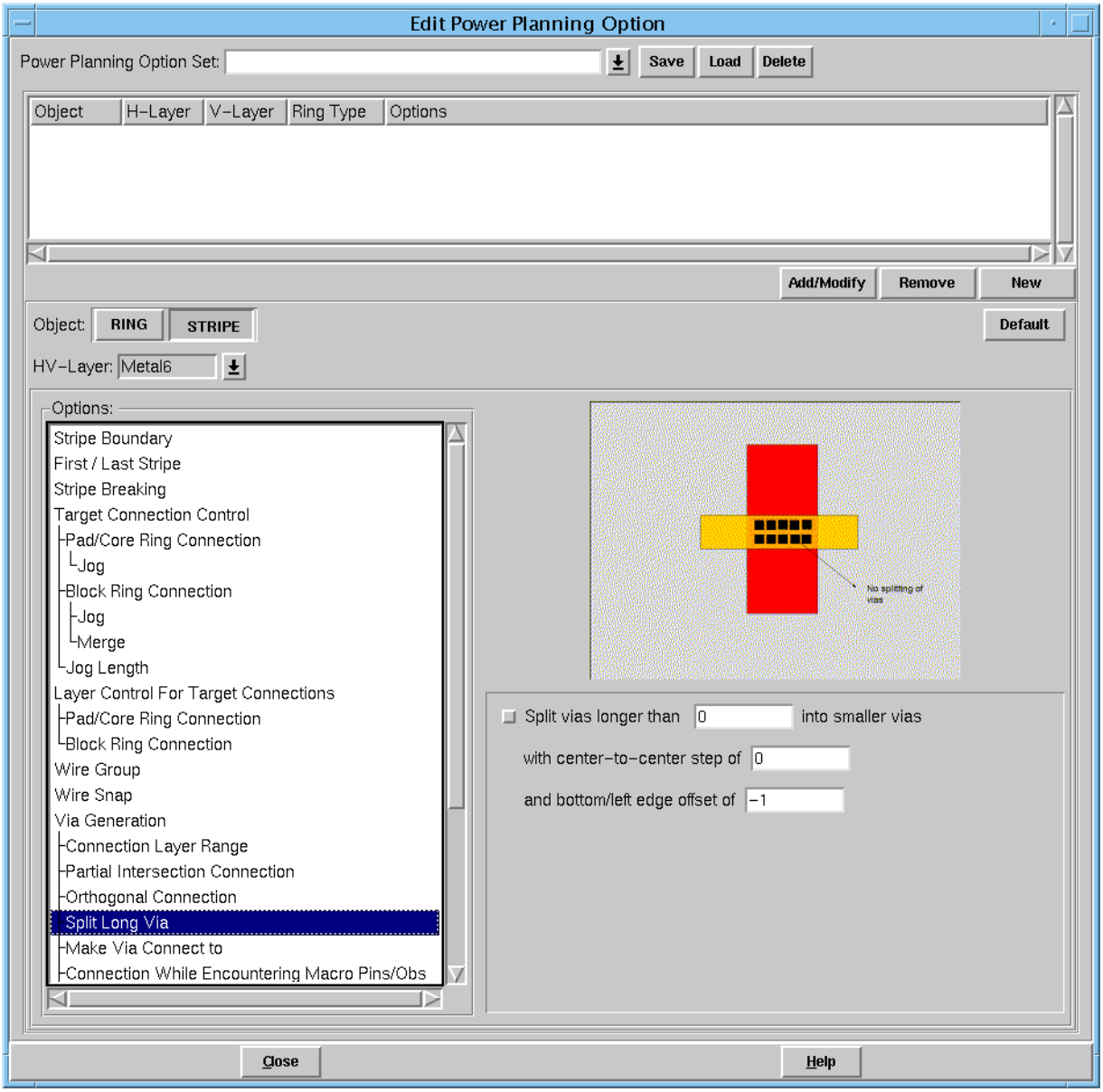
Edit Power Planning Option – STRIPE – Orthogonal Connection

➤ To open the Orthogonal Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Orthogonal Connection* from the display list.



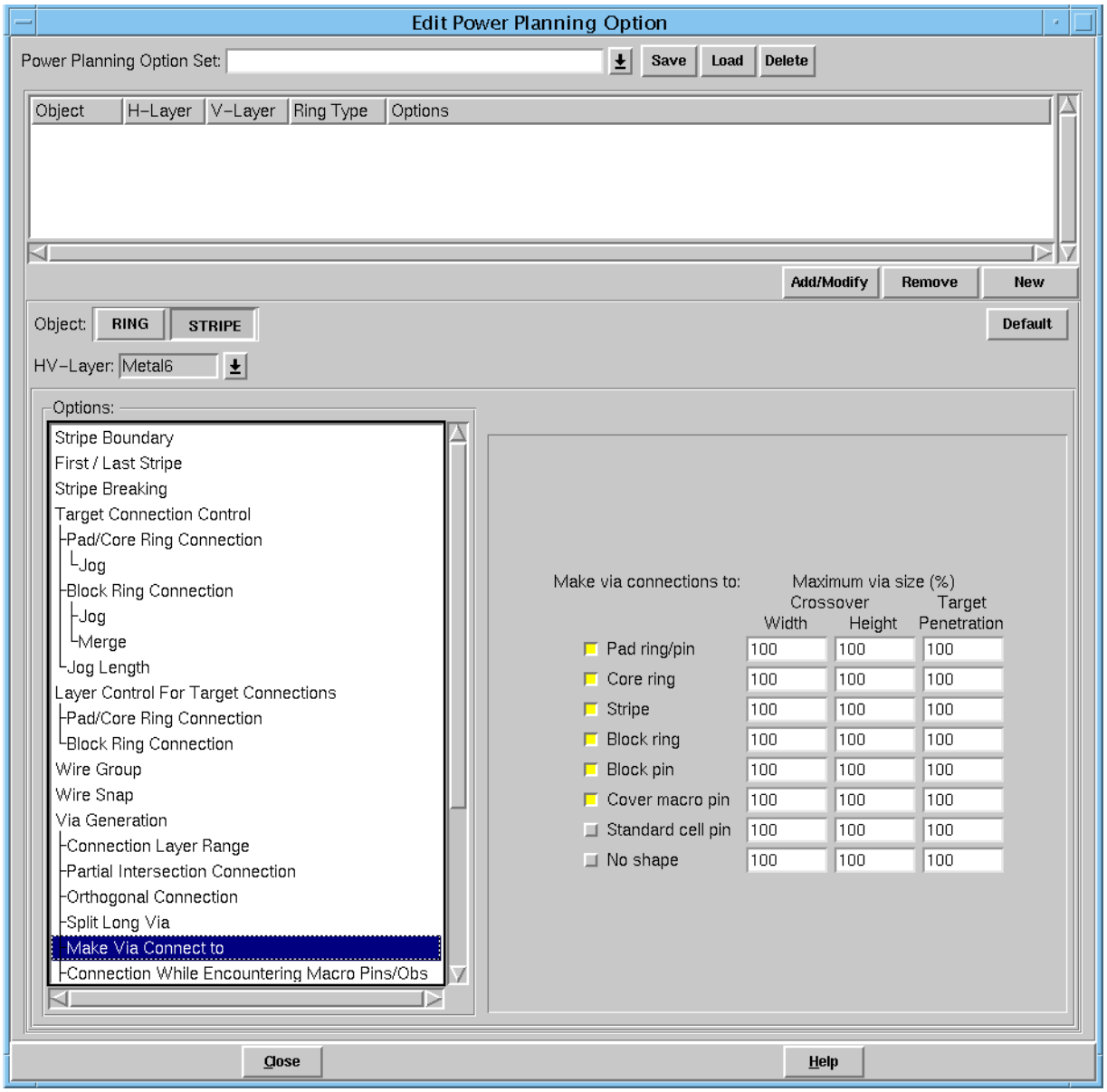
Edit Power Planning Option – STRIPE – Split Long Via

➤ To open the Split Long Via page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Split Long Via* from the display list.



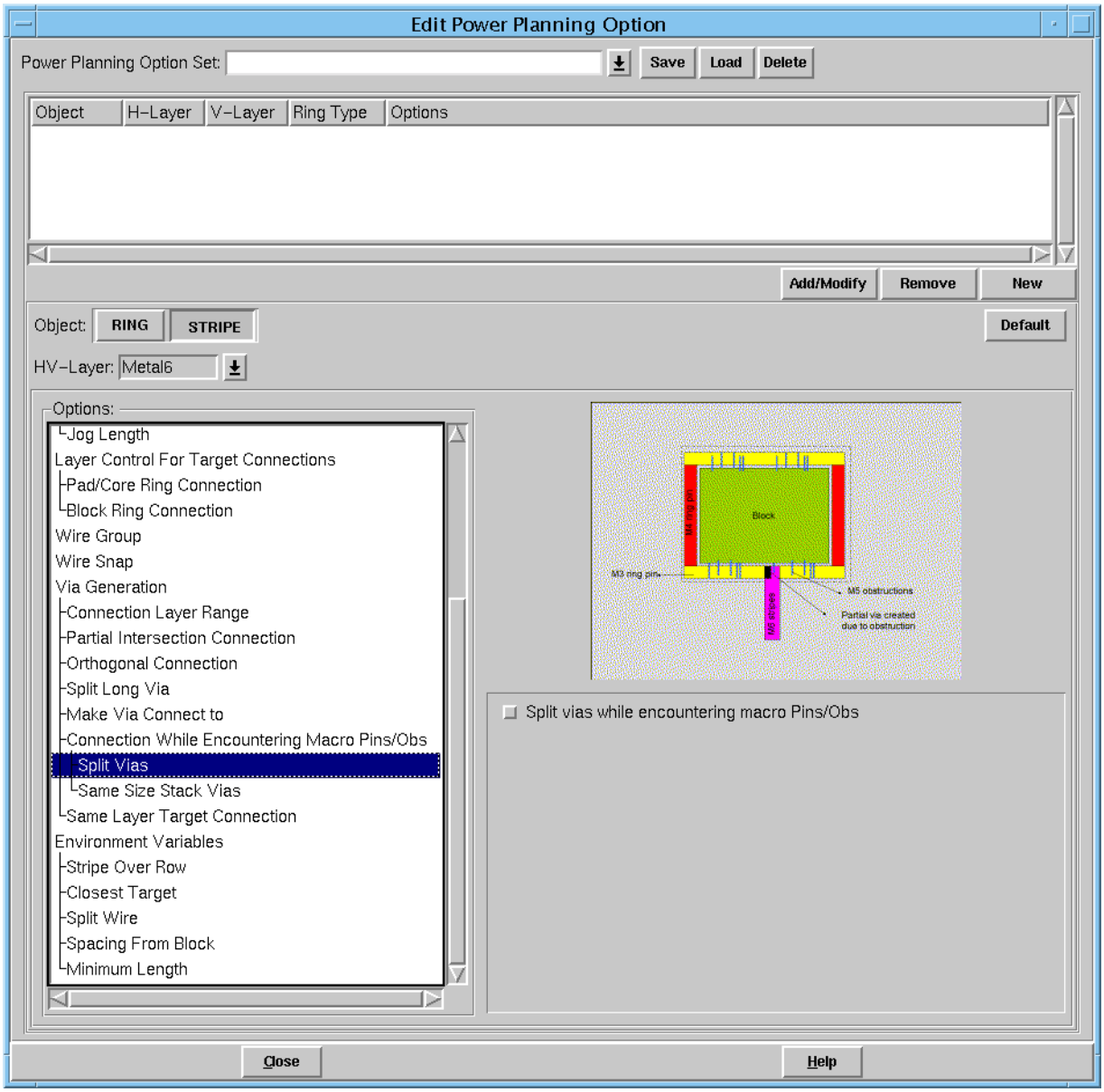
Edit Power Planning Option – STRIPE – Make Via Connect to

➤ To open the Make Via Connection to page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Make Via Connect to* from the display list.



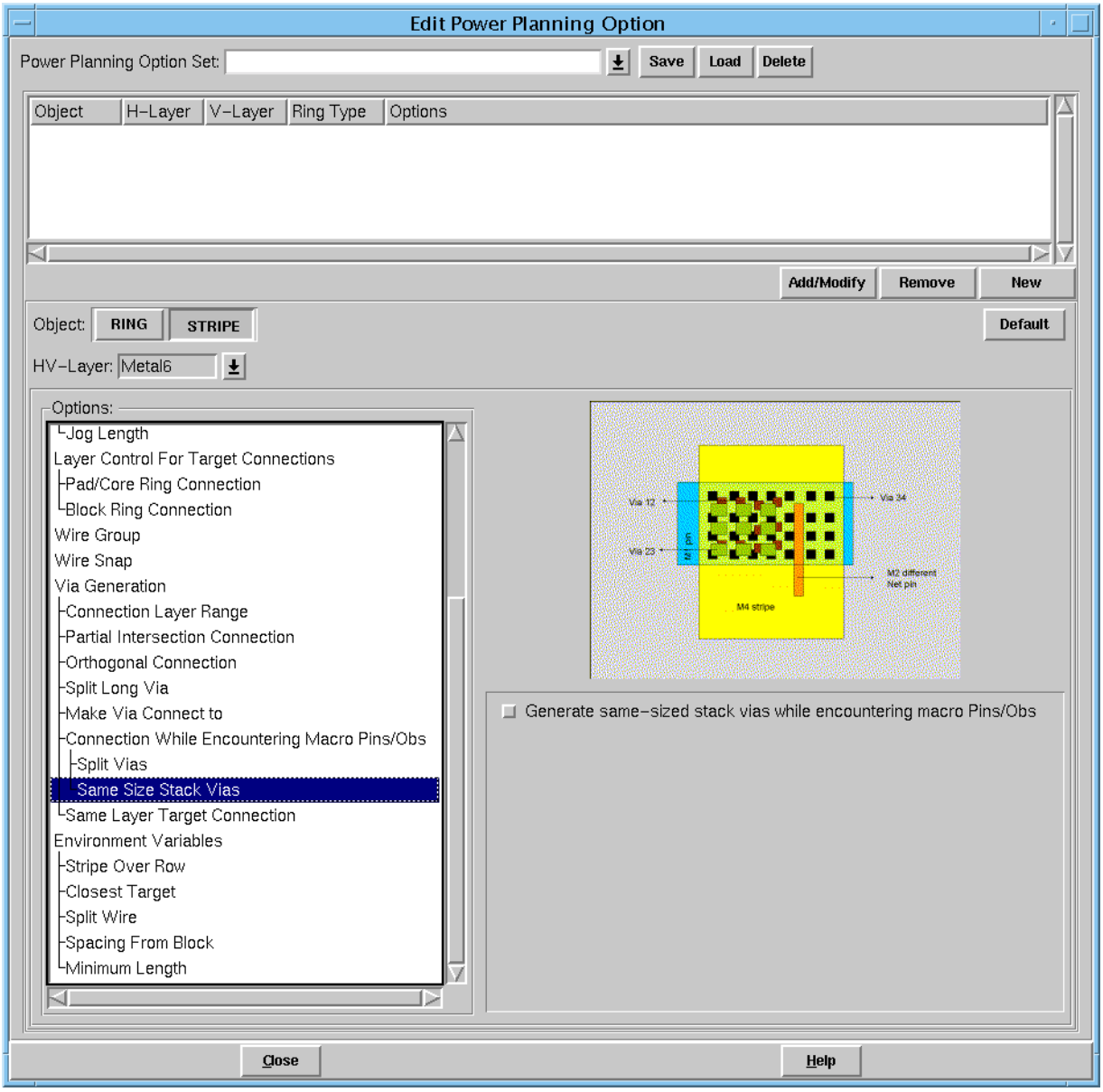
Edit Power Planning Option – STRIPE – Split Vias

➤ To open the Split Vias page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Split Vias* from the display list.



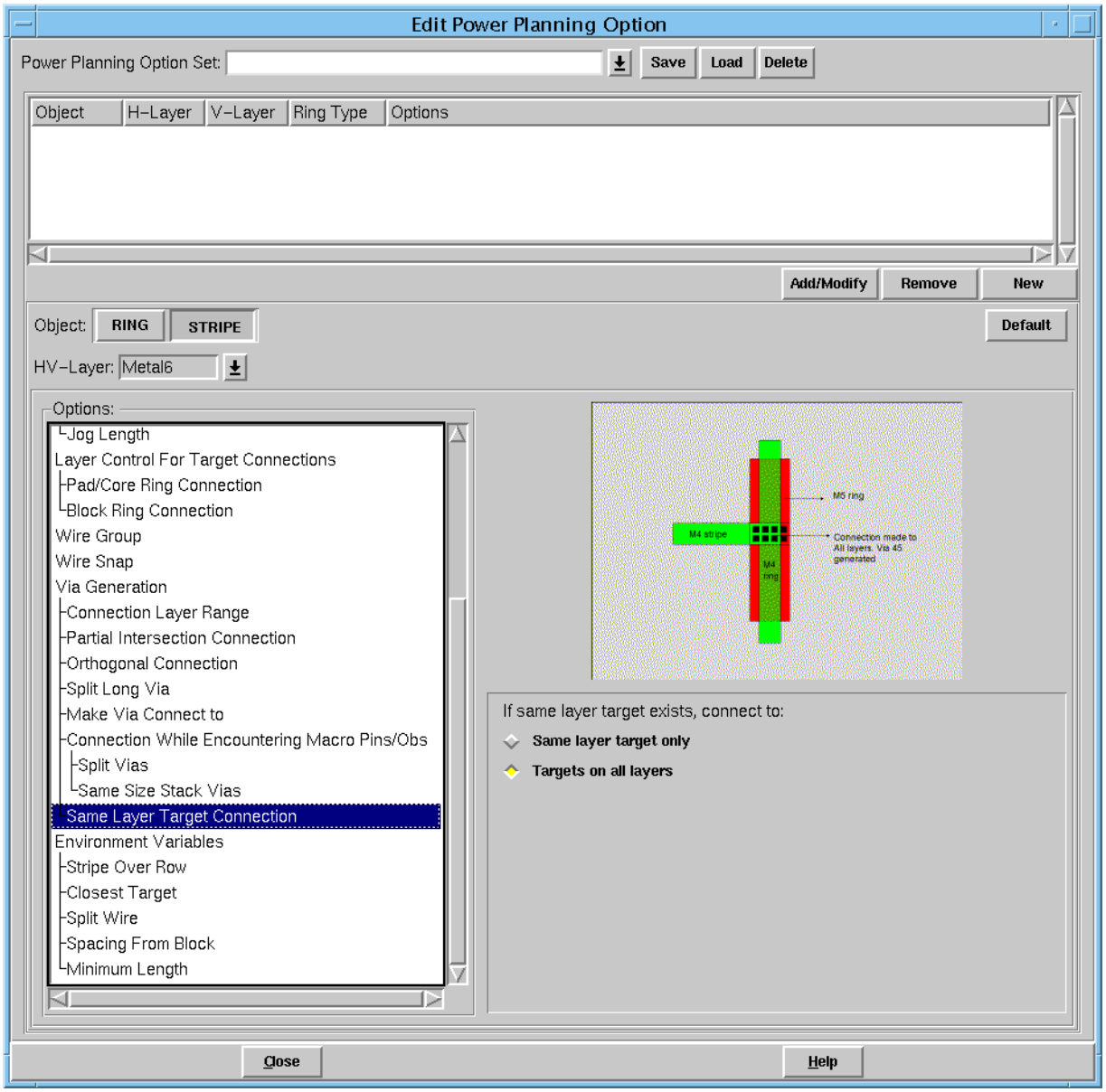
Edit Power Planning Option – STRIPE – Same Size Stack Vias

➤ To open the Same Size Stack Vias page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Same Size Stack Vias* from the display list.



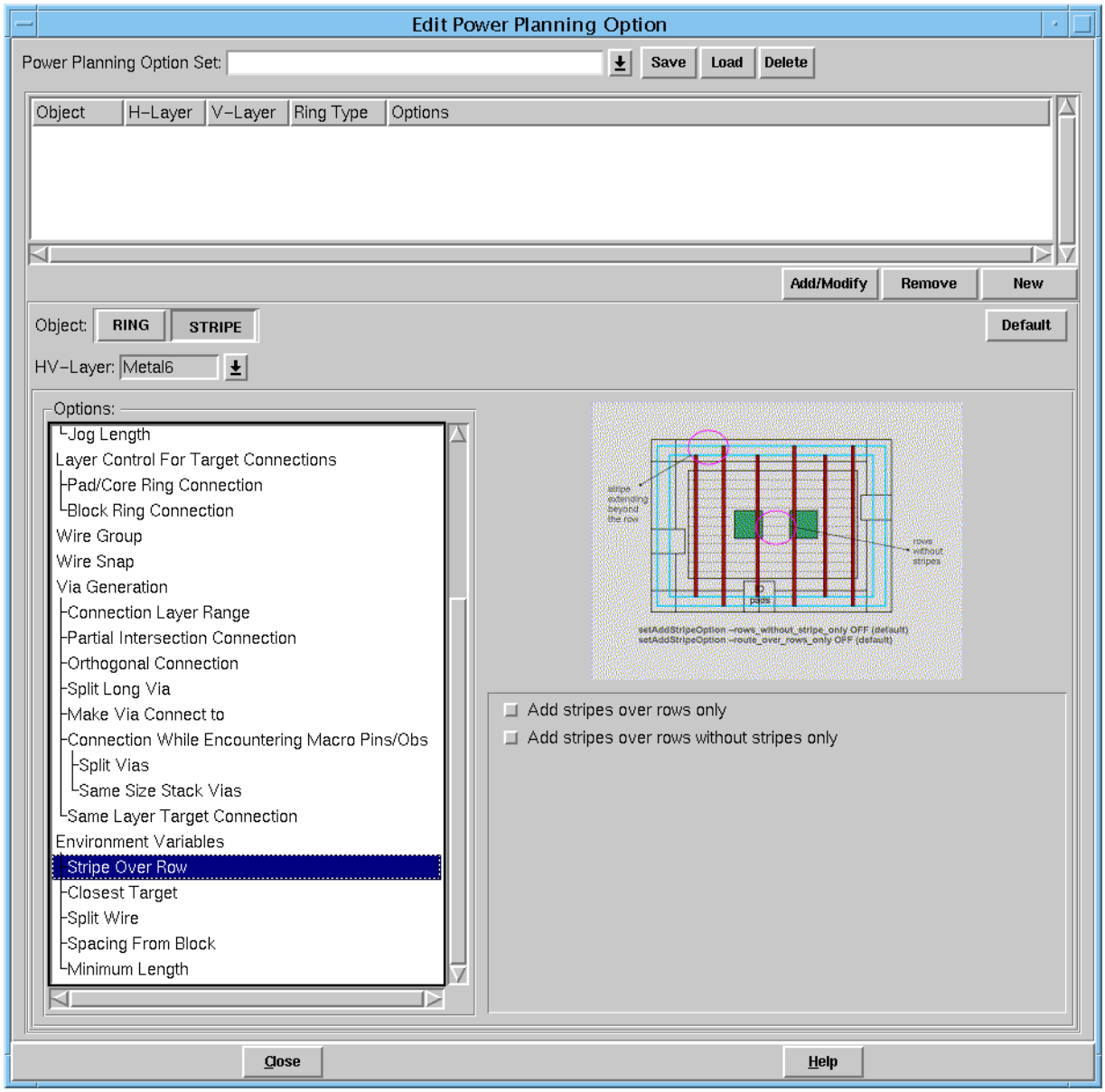
Edit Power Planning Option – STRIPE – Same Layer Target Connection

➤ To open the Same Layer Target Connection page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Same Layer Target Connection* from the display list.



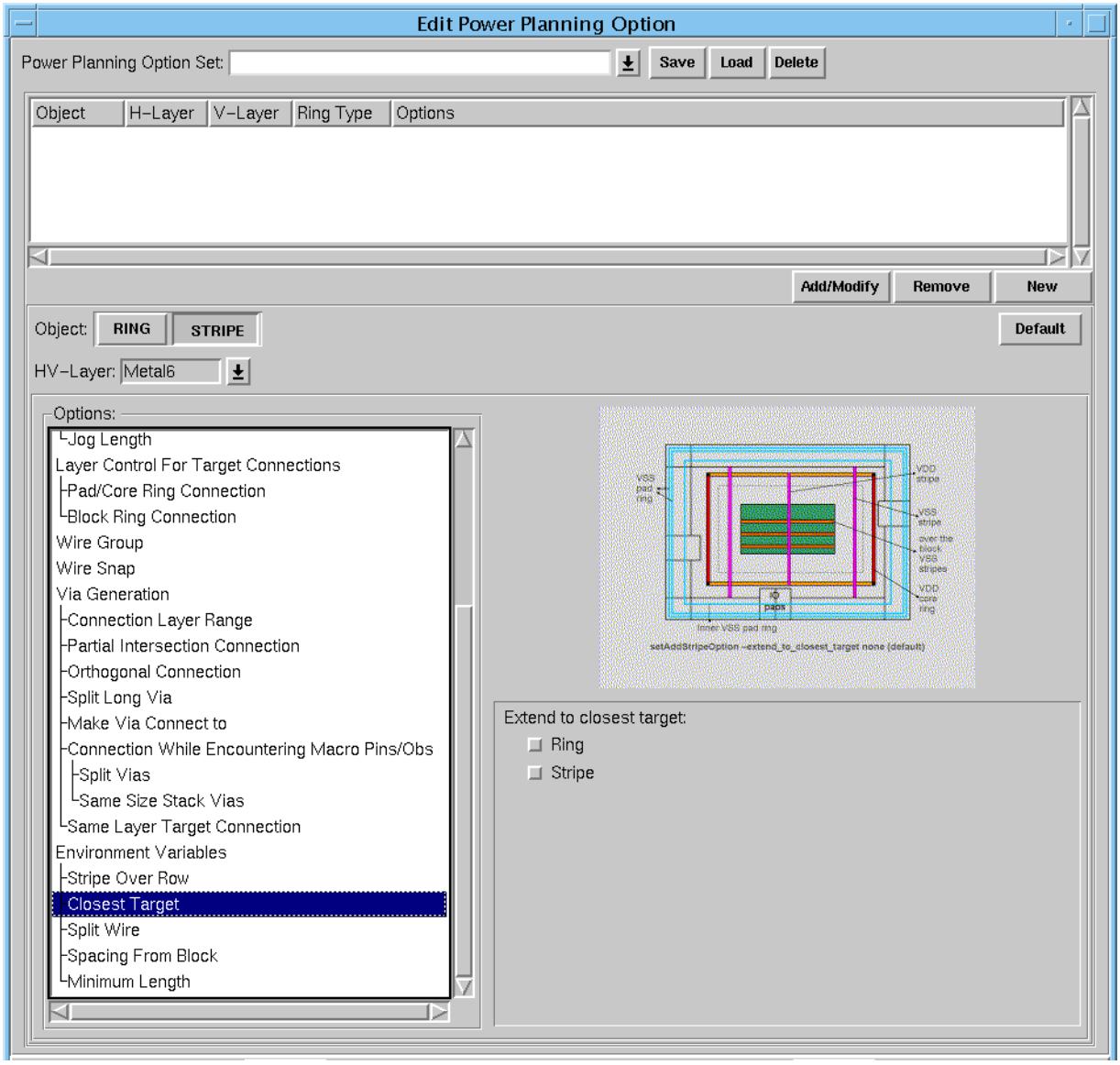
Edit Power Planning Option – STRIPE – Stripe Over Row

➤ To open the Stripe Over Row page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Stripe Over Row* from the display list.



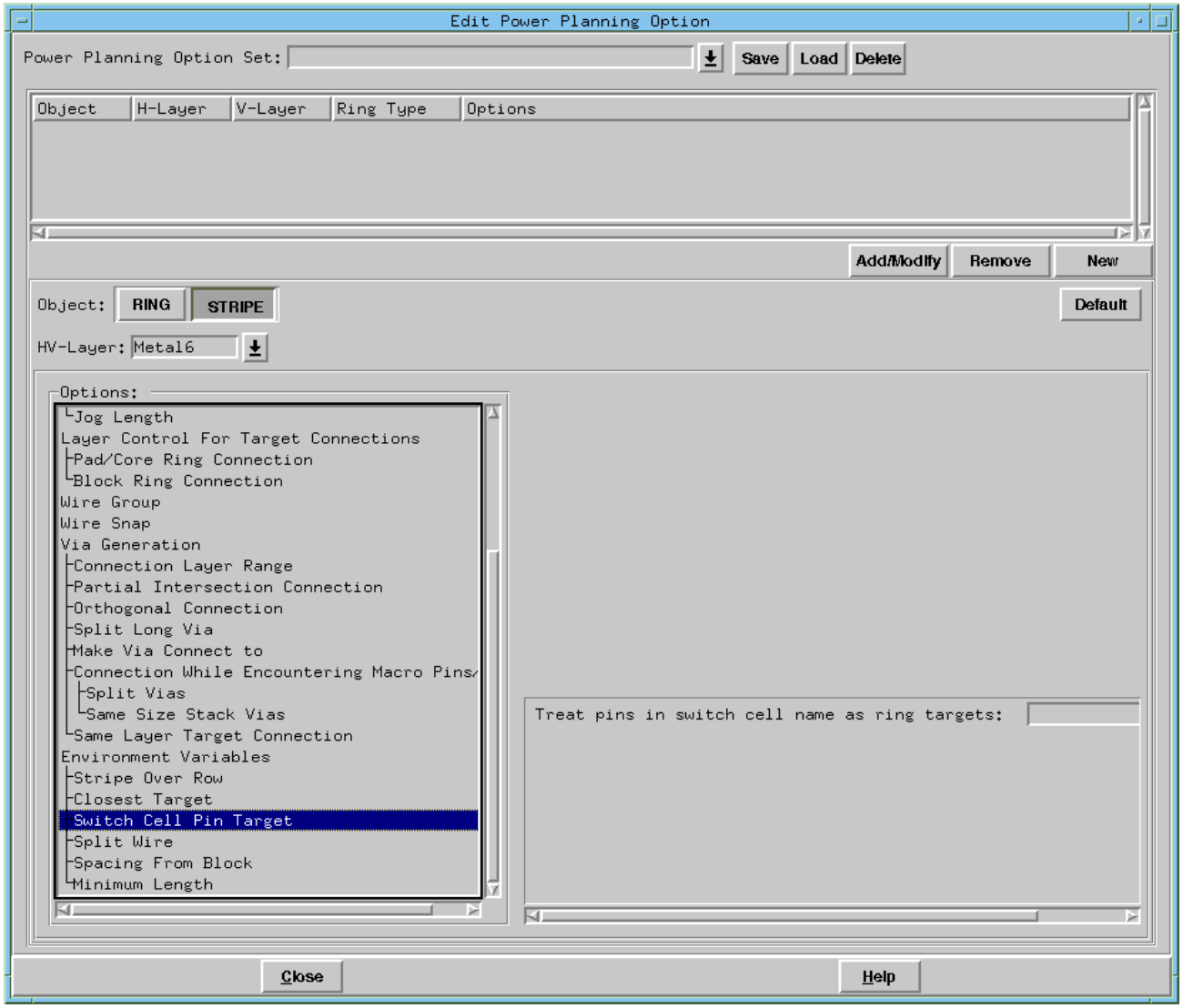
Edit Power Planning Option – STRIPE – Closest Target

➤ To open the Closest Target page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Closest Target* from the display list.



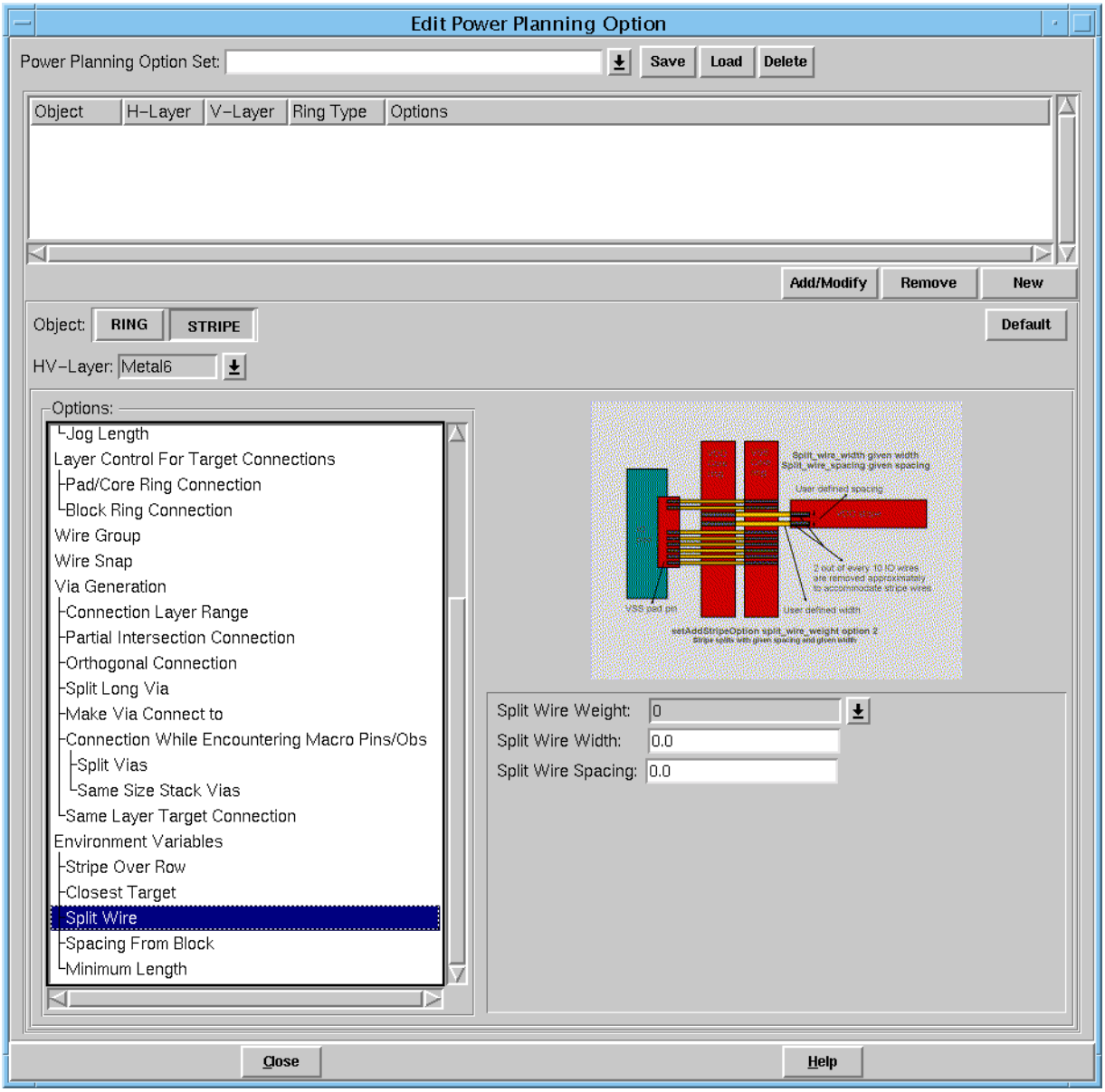
Edit Power Planning Option – STRIPE – Switch Cell Pin Target

➤ To open the Switch Cell Pin Target page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Switch Cell Pin Target* from the display list.



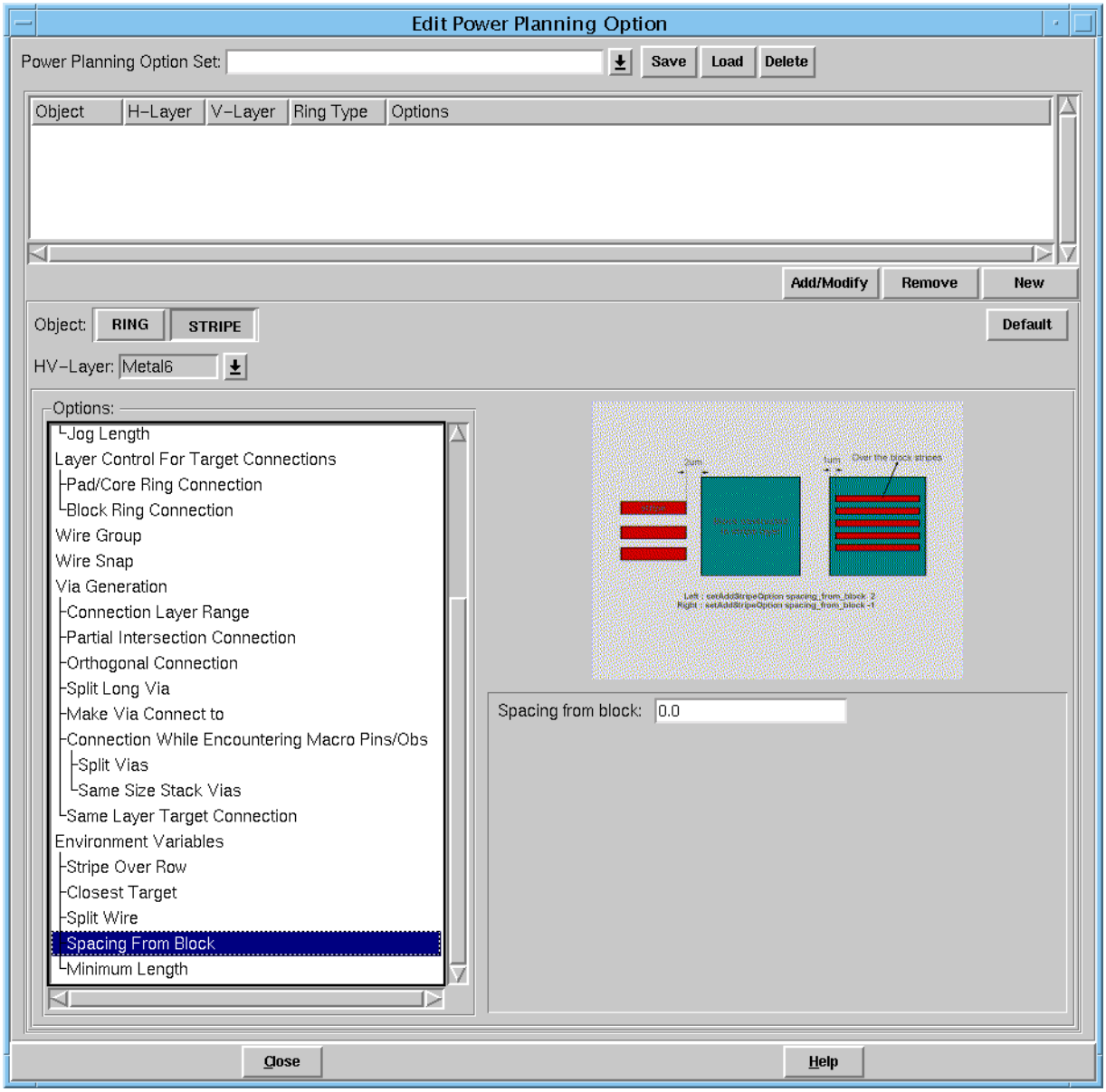
Edit Power Planning Option – STRIPE – Split Wire

➤ To open the Split Wire page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Split Wire* from the display list.



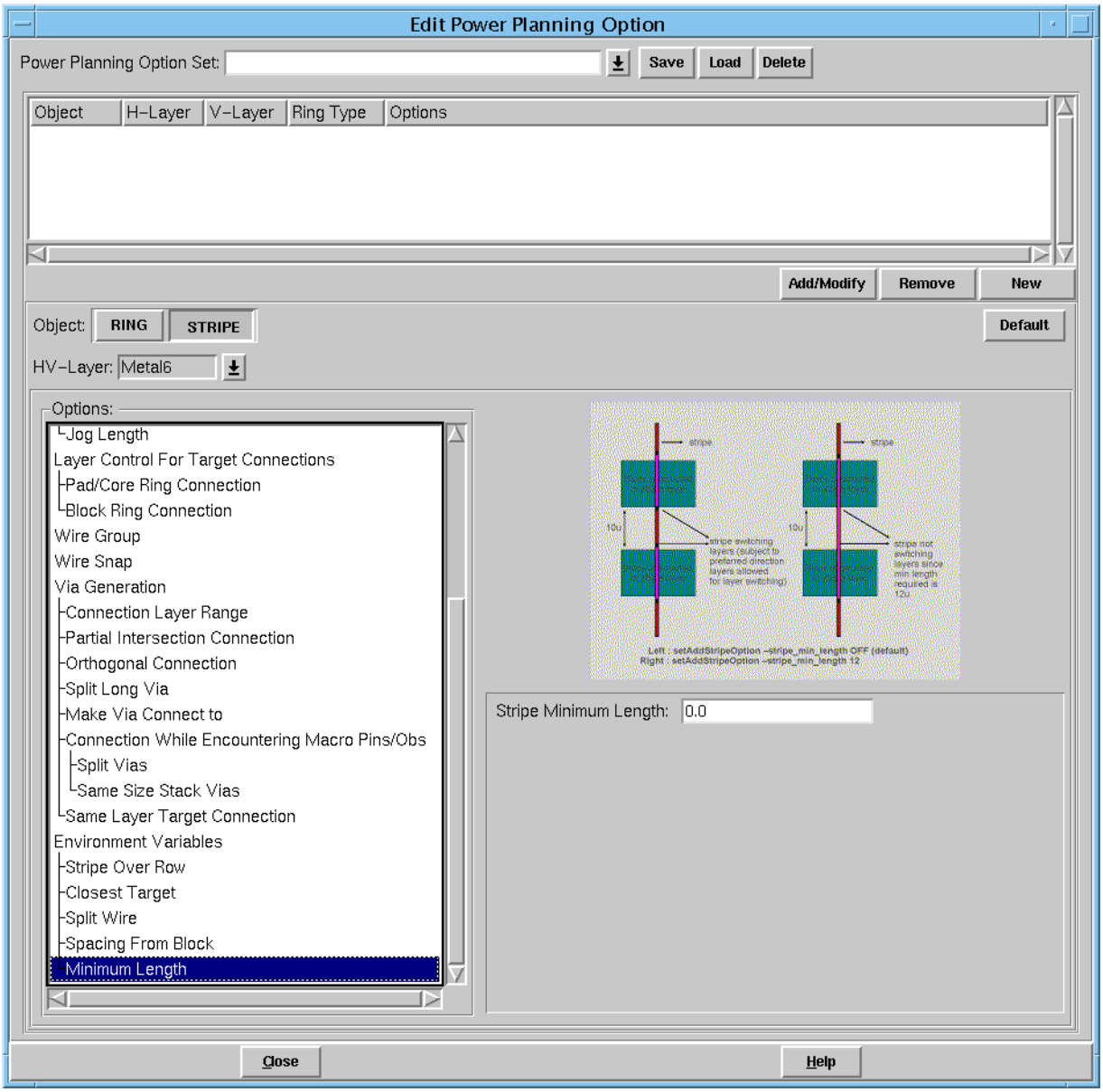
Edit Power Planning Option – STRIPE – Spacing From Block

➤ To open the Spacing From Block page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Spacing From Block* from the display list.



Edit Power Planning Option – STRIPE – Minimum Length

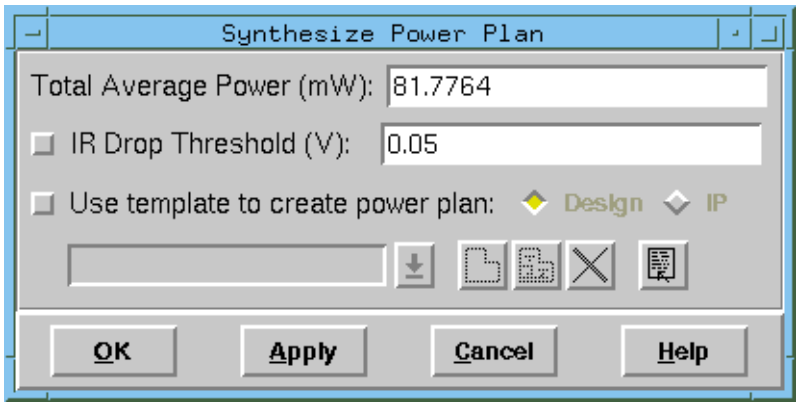
➤ To open the Stripe Over Row page of the Edit Power Planning Option form, choose *Power – Power Planning – Edit Power Planning Option*, select *STRIPE*, then choose *Stripe Over Row* from the display list.



Synthesize Power Plan

The Synthesize Power Plan form lets you create a power structure with a simple power consumption value. You can also optionally specify an IR drop threshold, and optionally select a predefined template for which you can specify the design-specific geometries.

➤ To open the Synthesize Power Plan form, choose *Power – Power Planning – Synthesize Power Plan*.



Synthesize Power Plan Fields and Options

Total Average Power (mW)

Specifies the total average power value for the design. The automatic power planning (APP) software provides an estimate of this power value based on the power constructs in the timing library files (`.libs`) and the capacitance table. This power value is propagated to the synthesize power planning (SPP) functionality to create the power plan.

Note: You should update this power value if the power value is known or if a more accurate power value becomes available.

IR Drop Threshold (V) Specifies the IR drop threshold for the design.

Use template to create power plan

Controls the ability to specify or create a template for creating a power structure.

Design Selects a predefined IP library template to be used when creating the power planning structure.

	IP	Selects a predefined design template to be used when creating the power planning structure. The power planning software analyzes design data to create the proper power structure at the design level.
New icon	Opens the Edit Power Plan Template form.	
Open icon	Opens the Edit Power Plan Template form and displays information on the currently selected template file.	
Delete icon	Deletes the currently selected template.	
Specify template parameter icon	Displays the Specify Template Parameter form.	

Related Text Command

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `synthesizePowerPlan`

Related Topics

For information on the following topics, see “Power Planning and Routing” in the *Encounter User Guide*.

- Automatic Power Planning (APP)
- Creating a Template

Edit Power Plan Template

Use the Edit Power Plan Template form to create and instantiate templates to be used for automatic power planning (APP).

Open the Edit Power Plan Template form:

1. Choose *Power – Power Planning – Synthesize Power Plan*.
2. On the Synthesize Power Plan form, select *Use template to create power plan*.
3. Click the *Design* radio button.
4. Click the *New* icon.

The Edit Power Plan form contains the following pages:

- Edit Power Plan Template – Design
- Edit Power Plan Template – IP Block

Edit Power Plan Template – Design

The *Design* page of the Edit Power Plan Template form lets you specify the configuration of rings and stripes for your design as a whole, or for regions (for example, power domains) of your design.

Note: When you open the *Design* page of the Edit Power Plan Template form, the power planning software displays the first region template that appears in the *Design Template Hierarchy* frame.

Changing the Routing Direction of Stripes

You can change the routing direction of stripes by right-clicking on the layer name in either of these forms:

- *Stripe* panel of the *Design* page

*	Indicates the default setting.
direction	Indicates the routing direction of the stripe.

- *Stripe* panel of the *IP Block* page

*	Indicates the default setting.
direction	Indicates the routing direction of the stripe.

Changing the Stripe Pattern

You can change the stripe pattern over power/ground pins of blocks by right-clicking on the layer name on this form:

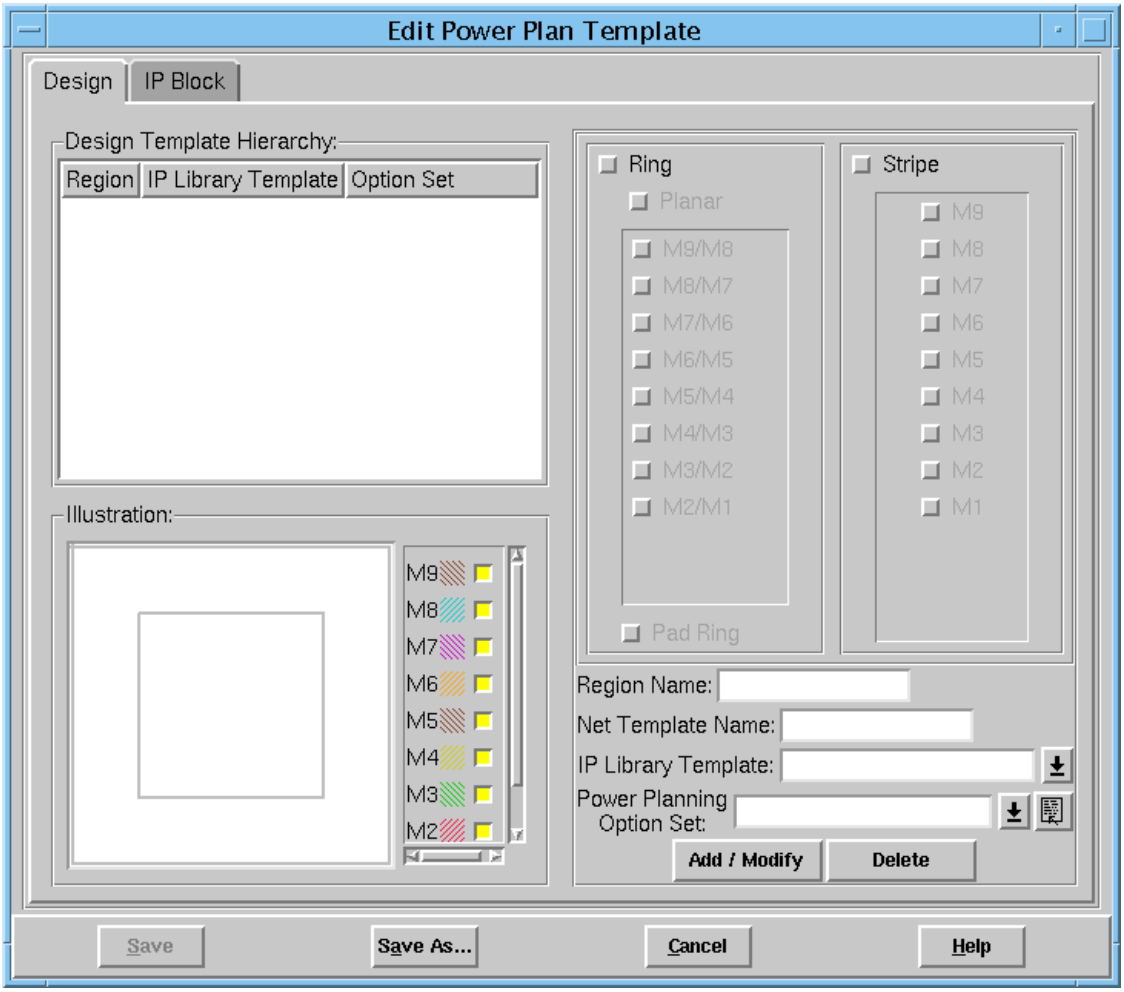
- *Stripe* panel of the *IP Block* page

*	Indicates the default setting.
direction	Indicates the routing direction of the stripe.
set pattern	Indicates the stripe pattern. The default is to use the width and pitch values specified by the user. You can set the stripe pattern for a particular layer to the pin pattern of any other layer. If you do not specify stripe width, the power planning software uses the pin shape to determine the stripe width.

To open the *Design* page of the Edit Power Plan Template form:

1. Choose *Power – Power Planning – Synthesize Power Plan*.
2. On the Synthesize Power Plan form, select *Use template to create power plan*.
3. Click the *New* icon.

   The Edit Power Plan Template form appears, showing the *Design* page:



Edit Power Plan Template – Design Fields and Options

Design Template Hierarchy

Displays the templates you need to successfully build the power structure(s) for a design.

Region

Indicates the template(s) used to build the power structures for the top level of the design and/or for the power domains.

Important

A *region* can be the top level of the design, or any power domain in the design.

You can use a region template to build power structures either at the top level or for other power domains in the design. You can have a region template for the top level and also have region templates for other power domains.

The region template itself serves as the default net template for all power/ground nets in the region to which the region template has been applied.

However, you can also create a net template within a region template if a power/ground net needs a power structure that differs from the default power structure.

Single-click a region name to select it. The region name appears in the *Region Name* field, and the *Net Template Name* field—both fields are in the lower-left quadrant. You can now configure the region template.

Double-click a region name to load the region template and to display the configuration in the upper right quadrant. If this region template has an IP library template, that IP library template is displayed in the *IP Block* page after you click the region name.

IP Library Template

Indicates the name of the IP template library that contains the template configuration of IP blocks that can be used in the region.

You can view—but not modify—the IP template configuration by clicking the *IP Block* tab.

Option Set

Indicates the name of the option set that contains the ring, stripe, and via configurations to be used for the region.

Illustration

Displays a graphic that shows the configuration of the rings and stripes that you specified with the options in the lower left quadrant of this form for the regions listed to the left of this illustration.

Ring

When selected, allows you to define ring characteristics for a design or a power domain in the design.

The ring characteristics depend on how you associate the region template with the Template Instantiation form:

- If you associate a region template with the top level of a design, that region template's ring will be a core ring.
- If you associate a region template with a power domain, that region template's ring will be a domain ring.

Planar

If selected, each side of the core ring is on a single layer, even though two of the sides will be in the non-preferred direction. The layer selection list below this field contains single layers.

If deselected, each side of the core ring is on the layer in the preferred routing direction. The layer selection list below this field contains layer pairs. For example, if you select `M6/M5`, the top and bottom segments of the ring are added to layer `M5`, (the preferred direction for horizontal wires), and the left and right segments are added to `M6` (the preferred direction for vertical wires). This is the default. You can change the routing direction by right-clicking the layer name.

Note: You can specify both non-planar and planar rings for the power structures in your design, but you can only view one such configuration at a time by clicking *Planar*.

Pad Ring

Select this option to create a pad ring on each layer that contains pad cells/pins.

Note: *Pad Ring* is effective only if you associate a region template with the top level of your design.

Stripe

Specifies that stripes are to be added to the region on the selected layers.

Right-click a layer name to choose the routing direction for that layer.

Region Name

Provide the name of the region with the ring or stripe configuration that you want to apply to power/ground nets at either the top level or for the power domain.

Cadence recommends that you

1. Create the region template for the top level of the design.
2. Use the power domain name as the region name if you know which power domain should use this template.

Net Template Name

Provide the name of a net in this field if the net template applies to a specific net.

If you do not specify a net name here, the power planning software uses the region name as the net template name (after you click *Add/Modify*) to indicate that the region template's configuration will apply to all nets in that region.

A region can contain one or more net-based templates.

You can display net-based templates in *Design Template Hierarchy* by clicking on + in the *Region* area.

Note: The name you specify here does not have to match the net name exactly. The name you specify serves as an identifier for mapping the net template to the real net during instantiation.

IP Library Template

Provide the name of the IP library template you want to use for a region.

Select an IP library template from the pull-down menu. (All IP library templates were created on the *IP Block* page of this form.)

Power Planning Option Set

Indicates the name of the option set that contains the ring, stripe, and via configurations to be used for the region.

Select a power planning option set from the pulldown menu.

To create a new power planning option set, click the *create/edit option set* icon.

Add / Modify	Adds a newly configured region to the *Region* list or modifies an existing region.
Delete	Removes a region from *Region* list.
Save	Saves the current configuration by overwriting an existing template. The power planning software displays a warning, which asks you to confirm that you want to overwrite the existing template.
Save As	Saves the current configuration to a new template. The power planning software displays the Specify Template Name form in which you enter the new template name.

Related Command

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `synthesizePowerPlan`

Related Topics

For information on the following topics, see “Power Planning and Routing” in the *Encounter User Guide*.

- Automatic Power Planning (APP)
- Creating a Template

Edit Power Plan Template – IP Block

The *IP Block* page of the Edit Power Plan Template form lets you specify the configuration of rings and stripes for IP blocks (hard macros) that are listed in the LEF file.

To open the *Design* page of the Edit Power Plan Template form:

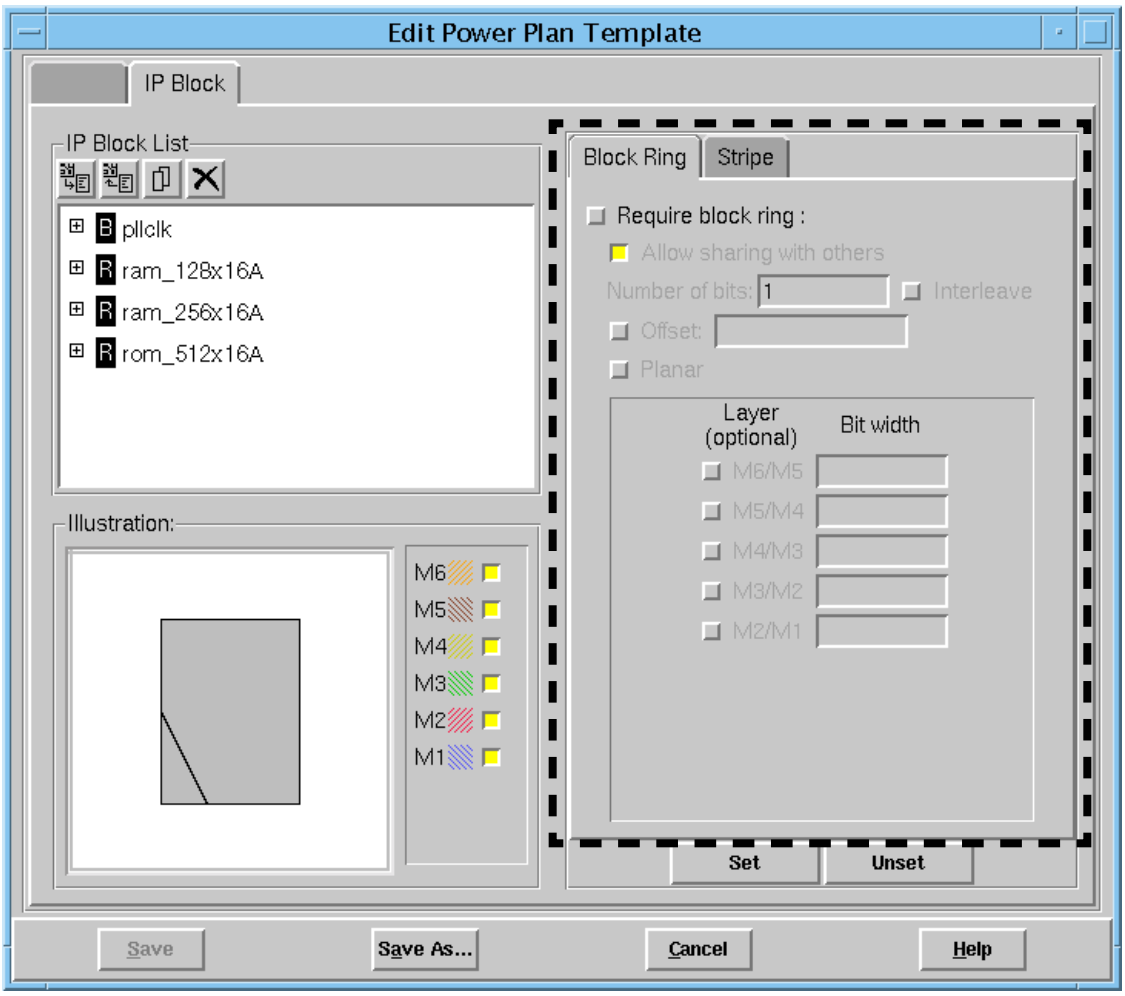
1. Choose *Power – Power Planning – Synthesize Power Plan*.
2. On the Synthesize Power Plan form, select *Use template to create power plan*.
3. Click the *IP* radio button.
4. Click the *New* icon.

Note: When you open the *IP Block* page of the Edit Power Plan Template form, the power planning software displays the first IP block template that has been configured.

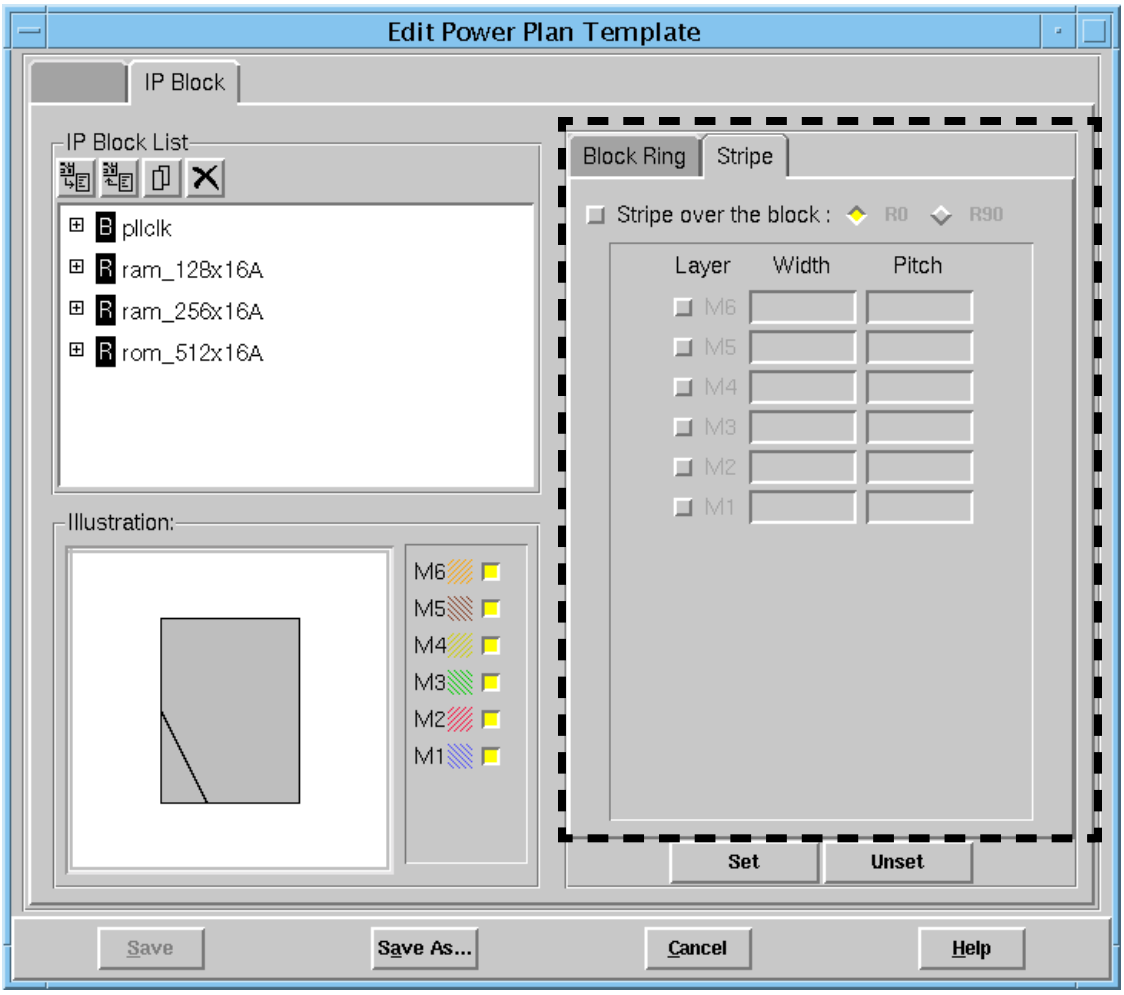
The right side of the *IP Block* page has two pages:

- Block Ring Page
- Stripe Page

Block Ring Page



Stripe Page



Edit Power Plan Template – IP Block Fields and Options

IP Block List

The list of IP blocks (hard macros) defined in the LEF file for the design. You can specify the ring and stripe configuration for items you select from the list. To specify multiple items, hold the `Shift` key or `Control` key while clicking the item. You can also select multiple items by scrolling down the list while holding the mouse button.

When you configure an IP block, its name is displayed in bold blue text.

The following information is available for each block in the list:

	B indicates that this block might need a block ring. *D* indicates a duplicate IP block that contains the IP template that is to be applied to instances with special power structure requirements. *R* indicates that the block already contains a ring pin, and probably does not need a block pin.
highlight block for selected instance	After you select an IP block in the Encounter main window, click this icon to highlight the corresponding IP block in *IP Block List.*
highlight instance for selected block	After you highlight an IP block in *IP Block List*, click this icon to highlight the corresponding IP block in the Encounter main window. By using this icon, you can decide whether a particular instance requires a special power structure because of the instance's placement location.
duplicate block and its template	Creates a duplicate IP block and IP library template for an IP block instance. Such duplicate templates serve as instance-based templates. Use this icon to create a duplicate IP template for an IP block instance that requires a different power structure than other instances of the IP block. The name of the duplicate IP block is `original_IP_block_name:#X` where *X* is a number, beginning with `1`. For example, the first three duplicates of the IP block `pllclk` are `pllclk:#1`, `pllclk:#2`, and `pllclk:#3`. Initially, the duplicate IP blocks have the exact template configuration as the original IP block, to which you can make modifications to account for the special requirements of various power structures. Each duplicate IP block is marked with a white-on-black *D* icon in *IP Block List*. IP blocks with + have duplicate IP blocks. Click the + to see the list of duplicate IP blocks.

delete duplicated block and its template

Removes duplicate IP blocks from *IP Block List*.

Note: Clicking this icon removes *only* duplicate IP blocks. Use *Unset* to remove an IP template configuration for an IP block.

Illustration

Displays a graphic that shows the configuration of the rings and stripes that you specified with the options in the lower left quadrant of this form for the blocks listed to the left of this illustration.

Block Ring

Require block ring

If this choice is selected, block rings are created around the blocks you select in the *IP Block List*. If deselected, rings are not created around the specified IP blocks.

Allow sharing with others

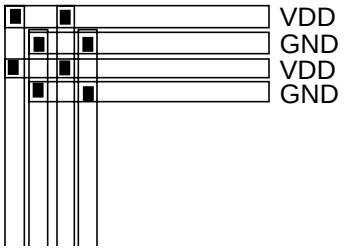
If this choice is selected, the block ring around the blocks you select in the *IP Block List* can be shared with other blocks that are in close proximity (and if those blocks are allowed to share rings with other blocks). If deselected, a discrete ring is created around each block you select in the *IP Block List*.

Number of bits

The number of rings of each specified net to be included in the wire group.

Interleave

If this choice is selected, wires for different nets are grouped as shown in the following figure.



If this choice is deselected, wires for the same net are grouped together. This option is deselected by default.

Offset

If this choice is selected, the block ring is offset from the block by the value specified in the text entry field. You must specify a value in the text entry field if you select this option. If deselected, the block ring is automatically offset from the block by the default value, which is obtained from the maximum spacing value in the LEF file for any selected layer.

Planar

If selected, each side of the core ring is on a single layer, even though two of the sides will be in the non-preferred direction. The layer selection list below this field contains single layers.

If deselected, each side of the core ring is on the layer in the preferred routing direction. The layer selection list below this field contains layer pairs. For example, if you select `M6/M5`, the top and bottom segments of the ring are added to layer `M5`, (the preferred direction for horizontal wires), and the left and right segments are added to `M6` (the preferred direction for vertical wires). This is the default. You can change the routing direction by right-clicking the layer name.

Note: You can specify both non-planar and planar rings for the power structures in your design, but you can only view one such configuration at a time by clicking *Planar*.

Layer (optional)

Specify one or more layer pairs on which block rings are to be created for the specified IP blocks. If you do not specify a layer pair, the software automatically selects the layer pair for the block as follows:

- If the top-most block pin layer is above top-most global stripe layer, the layer pair is the block pin layer and the layer below.
- If the top-most block pin layer is at or below the top-most global stripe layer, the block ring layer is two layers below top-most global stripe layer.

Note: The top-most block ring layer is always at or above the bottom-most pin layer.

Bit width

Represents the width of each bit for the block ring on the specified layer pair. You must specify a width for each layer pair you select. If you want the software to automatically determine the width of the block ring, you must deselect all *Layer* options.

Stripe

Stripe over the block

If this choice is selected, stripes are created over the blocks you select in *IP Block List.*

Note: For each block you specify with *R0* options and only one layer, you must also specify *R90* options.

R0

Select this option, then specify *Layer*, *Width*, and *Pitch* values for blocks you select in the *IP Block List* when they are placed in the design in an unrotated position.

R90

Select this option, then specify *Layer*, *Width*, and *Pitch* values for blocks you select in the *IP Block List* that are rotated 90 degrees when placed in the design.

Layer

Represents the layer on which the stripes are created. The preferred routing direction for the layer is based on the layer definition in the LEF file.

Width

Represents the width, in micrometers, of the stripes to be created over the blocks selected in the *IP Block List*.

Pitch

Represents the distance (pitch), in micrometers, from the edge of the first stripe of the set to the same edge of the first stripe of the next set, for stripes to be created over the blocks selected in the *IP Block List*. By default, the pitch is $2W + 3S$, where W is the width and S is the spacing.

Set

Associates the values specified in the *Block Ring* and *Stripe* sections of this page with the blocks selected in the *IP Block List*. The name of each block that was selected when you clicked the *Set* button appears in bold blue text.

Unset

Removes the association of the values specified in the *Block Ring* and *Stripe* sections of this page from the blocks selected in the *IP Block List*. The name of each block that was selected when you clicked the *Unset* button returns to plain black text.

Save

Saves the current configuration by overwriting an existing template.

The power planning software displays a warning, which asks you to confirm that you want to overwrite the existing template.

Save As

Saves the current configuration to a new template.

The power planning software displays the Specify Template Name form in which you enter the new template name.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `synthesizePowerPlan`

Related Topics

For information on the following topics, see “Power Planning and Routing” in the *Encounter User Guide*.

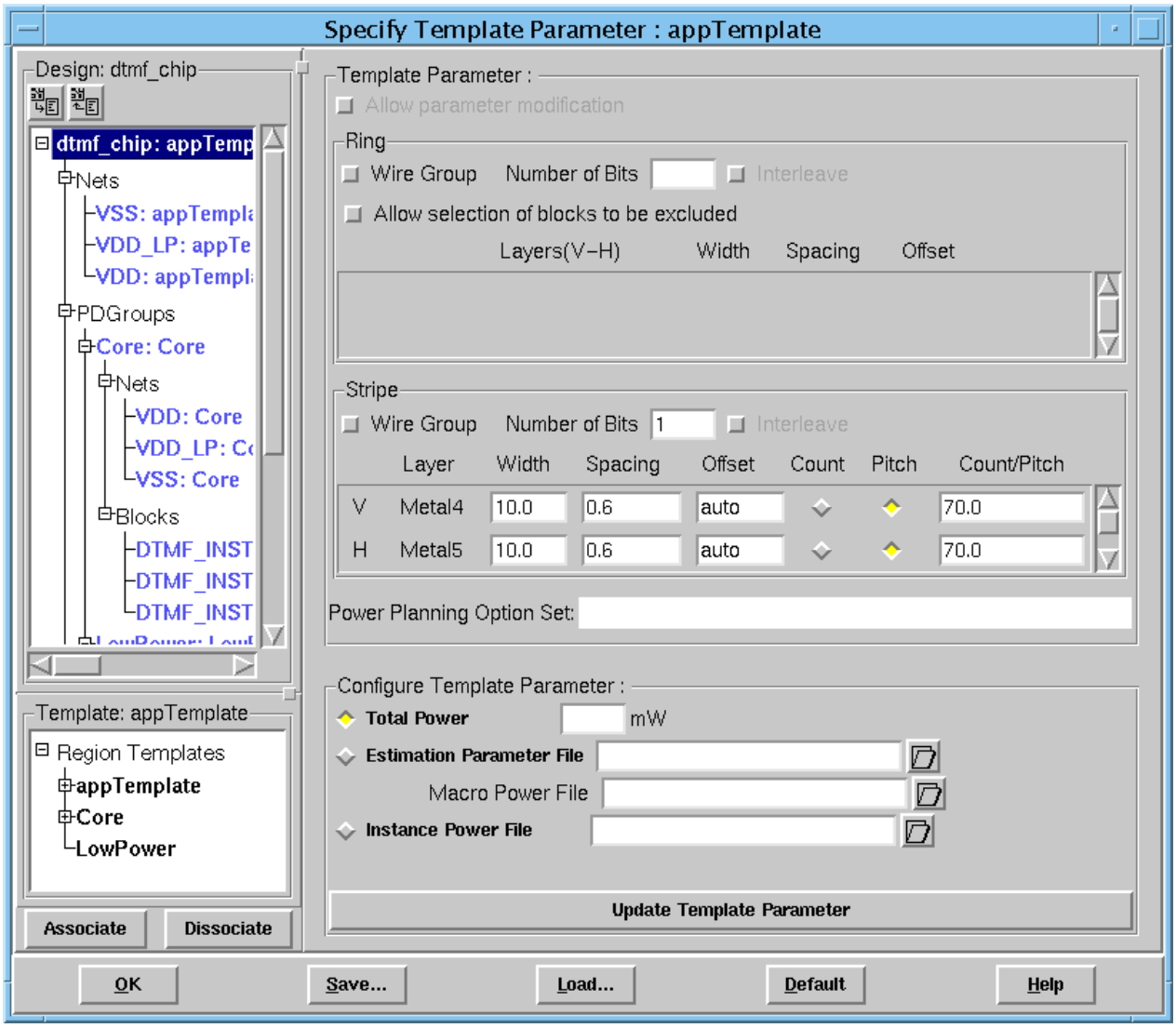
- Automatic Power Planning (APP)
- Creating a Template

Specify Template Parameter

The Specify Template Parameter form lets you specify the exact geometries of rings and stripes in the template.

To open the Specify Template Parameter form:

1. Choose *Power – Power Planning – Synthesize Power Plan*.
2. On the Synthesize Power Plan form, click the *Specify template parameter* icon.



General Description of Specify Template Parameter Form Features

The following table highlights the typographic conventions in the *Design* and *Template Parameter* windows of the Specify Template Parameter form.

Regular weight type	Nets, power domain groups, blocks, net templates, block templates.
Greyed-out regular weight type	Design objects that do not need to be associated with a template, or which do not yet need to be associated with a template.
Bold black type	Design objects for which templates are available, but that have not yet been associated with a template.
Bold blue type	Any design object that has had a template associated with it.

Associating a Region Template with a Top-level Design or Power Domain

When you associate a region template with a top-level design or with a power domain, the power planning software performs the following tasks:

- Analyzes design data, floorplan data, and cell library data (along with power consumption) to determine the initial ring and stripe parameters.
- Assigns the region template to the nets for instantiation, and the nets are automatically tagged with the default region template name.
- Automatically associates instance blocks with IP block templates when an IP block template for the instance blocks exists and instances are tagged with the IP block template name.

When you click on a net in *Design*, all available and appropriate templates (region and net templates) are highlighted in *Template*.

- If a net requires a template other than the region template, you can associate that net with another template, and the net will be tagged with that template name. The power planning software performs analysis on the net to apply the ring and stripe parameters.
- If you dissociate a net from its net-based template, the net uses the region template. If you dissociate the net from the default region template, the power planning software assumes that the net does not require a power structure.
- If you want to reapply the default region template to a net, associate the net with its region template. The net will now have the current ring and stripe parameters associated with

its “parent” component. You can use this method to apply newly modified ring and stripe parameters of a parent component onto a net.

When you click an instance in *Design*, its default cell template and duplicates are highlighted for association with a template.

- Depending on how the instance is placed in the design, a power structure that you defined for one of the duplicates might be more appropriate for the instance. Associate the instance with that duplicate.

General Observations on the Template Instantiation Form

- You can configure the template used by the design component with a set of specific parameters if you double click on the design component (design, power domain, and net).
- Nets that use the same template topology might have different parameters.
- Modifications of ring/stripe parameters for a design component that uses a specific region template automatically propagate down to nets that are tagged with the same region template. Click *Allow parameter modification* to define specific parameter values for a particular net.
- The option *Allow selection of blocks to be excluded* under *Ring* can only be used at the top level of the design.

  Note: Select blocks before using this option.
- Rings can have multiple width and spacing values to allow different widths at different ring legs. If you move your cursor to *Width* or *Spacing*, the following text appears:

  {common} or {vertical horizontal} or {Left Bottom Right Top}

  Enter one value if the width or spacing values are the same for all ring legs.

  Enter two values (separated by spaces) if the width of a ring’s vertical segment have a different width than the horizontal segments.

  Enter four values (separated by spaces) if each ring segment has a unique value.

Specify Template Parameter Fields and Options

Design

Displays power/ground components for the design, including both power/ground nets at the top level of the design, and power/ground nets for power domains.

Important

When you click a component in *Design*, all available and appropriate templates for that component are displayed in *Template*.

Template

Displays all possible templates for the design.

Associate

Associates a region template either with a power domain or with the top-level design.

To associate a region template with a power domain, highlight the power domain and region template, and click *Add*. The power domain (or other design component) is tagged with the template name.

Important

You cannot associate a “child” component to a template before you have associated a child component’s “parent” with a template.

Dissociate

Dissociates a region template from a power domain. To dissociate a region template from a power domain, highlight the power domain and region template, and click *Delete*.

Allow parameter modification

Allows net-specific modification of ring and stripe information.

By default, the power planning software propagates ring and stripe information from the power domain down for all nets within the power domain.

If you want to set specific ring and stripe values for individual nets, click this option and revise the values as needed.

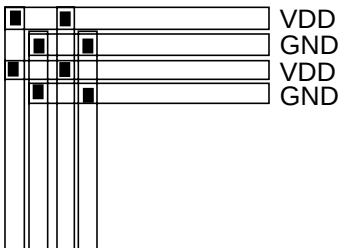
Ring

If you selected the *Ring* option on the *Design* page of the Edit Power Plan form, you can specify values for each ring layer you selected.

Wire Group If selected, multiple wires from the same net are grouped together and via arrays are generated as if they were one wire. If deselected, wire groups are not used. This is the default.

Number of Bits The number of wires for each net in the wire group.

Interleave If selected, wires for different nets are grouped as shown in the following figure.



If deselected, wires for the same net are grouped together. This option is deselected by default.

Allow selection of blocks to be excluded

If selected, the design display area highlights the blocks that are to be excluded from the core ring. You can modify the blocks in the design display area that are to be excluded from the core ring. Deselect a block to include it from the core ring and select a block to exclude it from the core ring.

Layers The list of planar layers or non-planar layer pairs that you selected on the *Design* page of the Edit Power Plan Template form.

Width The width, in micrometers, for each side of the core rings.

Spacing The edge-to-edge spacing, in micrometers, between rings for each side of the ring.

Offset The distance, in micrometers, of the outer edge of the core ring from the edge of the core area.

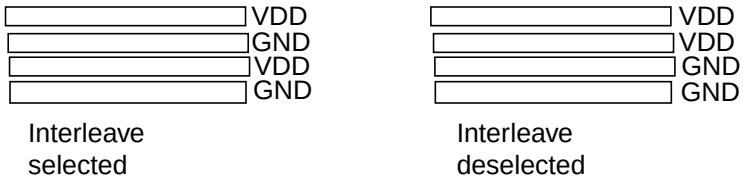
Stripe If you selected the *Stripe* option on the *Design* page of the Edit Power Plan Template form, you can specify values for each layer you selected.

Wire Group If selected, multiple wires from the same net are grouped together and via arrays are generated as if they were one wire. If deselected, wire groups are not used. This is the default.

Number of Bits The number of wires for each net in the wire group.

Interleave

The style of the wire groups. The following illustration shows the difference in how wires are created:



Layer

The layer on which the stripe is to be created. The *V* or *H* to the left of each layer name indicates whether the stripes on that layer are to be vertical or horizontal.

Width

The width, in micrometers, of each stripe.

Spacing

The edge-to-edge spacing, in micrometers, between stripes in each set.

Offset

The distance, in micrometers, of the stripe from the core boundary of the design. The value of *auto* indicates that the stripes are distributed evenly so that the offset from the left and right edges to the first and last stripe set are the same.

Count

If selected, the value in the *Count/Pitch* field indicates the number of stripes on that layer.

Pitch

If selected, the value in the *Count/Pitch* field indicates the distance, in micrometers, of a stripe edge from the corresponding stripe edge of the next set of stripes.

Count/Pitch

If you select *Count* for a stripe layer, this value is the number of stripes on the layer or the distance between a set of stripes. If you select *Pitch* for a stripe layer, this value is the distance between a set of stripes.

Default: *Pitch*

Power Planning Option Set

Indicates the name of the option set that contains the ring, stripe, and via configurations to be used for the region.

Total Power

Optimizes the values for ring and stripe parameters based on the total power consumption value (in milliwatts) that you specify in the text entry field.

Estimation Parameter File

Optimizes the values for ring and stripe parameters based on the power consumption values in the Estimation Parameter File that you select.

Macro Power File

Optimizes the values for ring and stripe parameters based on the power consumption values in the Macro Power File that you select. The macro power file contains data about macro cell power consumption, it is used in conjunction with the estimation parameter file.

Instance Power File

Optimizes the values for ring and stripe parameters based on the power consumption values in the Instance Power Data File that you select.

Update Template Parameter

Click this button to update the values for ring and stripe parameters. Values are best estimated based on the options you selected on this page.

Related Text Commands

For information on the following commands, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `synthesizePowerPlan`

Related Topics

For information on the following topics, see “Power Planning and Routing” in the *Encounter User Guide*.

- Automatic Power Planning (APP)
- Creating a Template
- Instantiating a Template

Add Rings

Use the Add Rings form to create power rings for specified nets around the core boundary or selected power domains, blocks, and groups of core rows. The Add Rings form contains the following three pages:

- *Add Rings – Basic* on page 833
- *Add Rings – Advanced* on page 840
- *Add Rings – Via Generation* on page 844

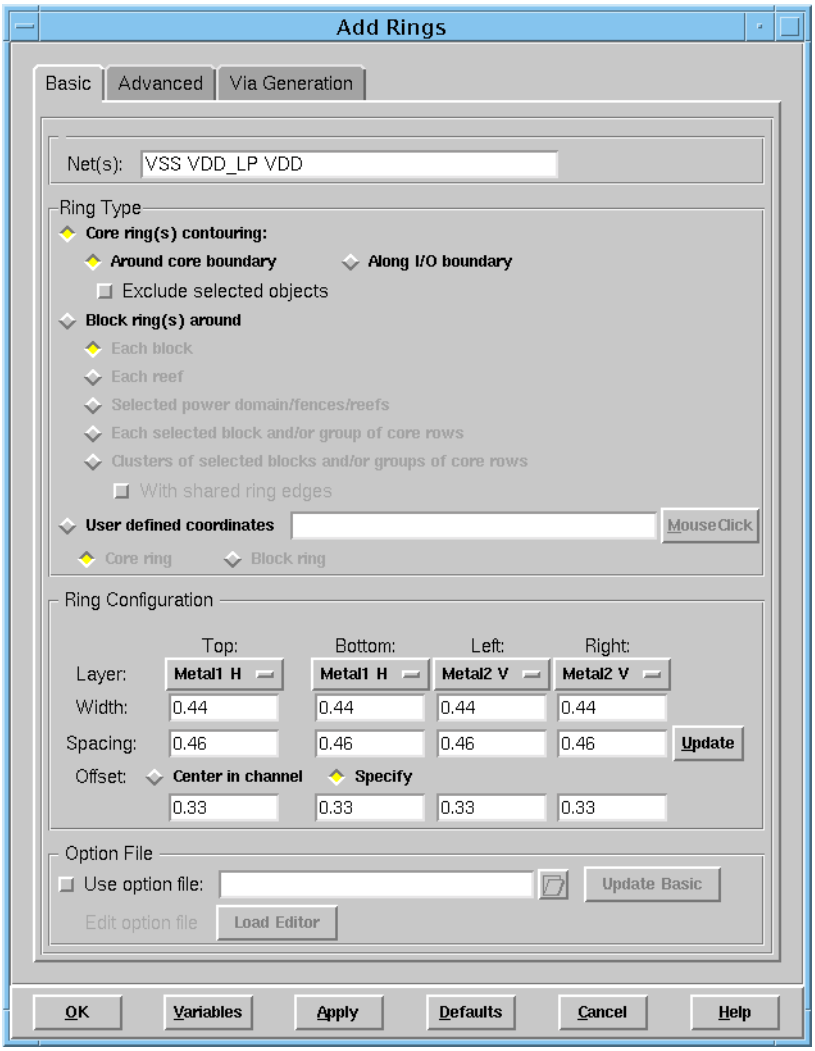
You can access the following form from the Add Rings form:

- Add Ring Environment Variables

Add Rings – Basic

The *Basic* page of the Add Rings form lets you specify the net names for the power rings to be created, as well as the type of rings and their configuration.

➤ To open the *Basic* page of the Add Rings form, choose *Power – Power Planning – Add Rings*, then click the *Basic* tab.



Add Rings – Basic Fields and Options

Net(s)	The net names for power rings to be created.

Ring Type

Specifies the type of ring to be created. You can specify only one type at a time. For example, if you need both core rings and block rings, create core rings first, then select this form again to create block rings.

Select one of the following options:

Core Ring(s) contouring

Creates core rings that follow either the contour of the core boundary or contour around the I/O boundary. Select one of the following options:

Around core boundary

Creates core rings that contour around blocks or rows in the core area of the design, including cores that are rectilinear. This is the default.

Use the options in the Ring Configuration panel to either center the ring in the channel between the core boundary and the I/O area, or offset each side of the ring by a specific distance from the core boundary.

Along I/O boundary

Creates core rings that contour the I/O area.

Use the options in the Ring Configuration panel to either center the ring in the channel between the core boundary and the I/O area, or offset each side of the ring by a specific distance from the I/O boundary.

Exclude selected objects

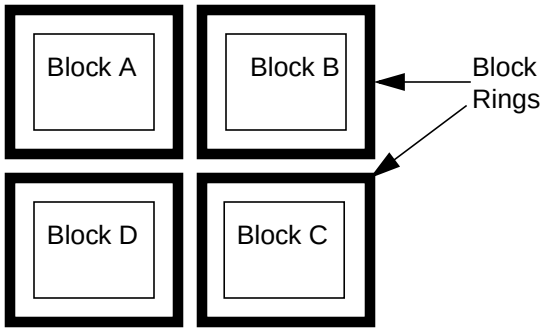
If selected, creates a ring that contours the core boundary while contouring around the selected objects so that they are outside of the ring. If deselected, all objects in the core area are enclosed within the core ring. This is the default.

Block ring(s) around

Creates block rings that follow the contour of the specified objects. Choose one of the following options:

Each Block

Creates a separate ring around each block in the design. Rings are created as shown in the following illustration.

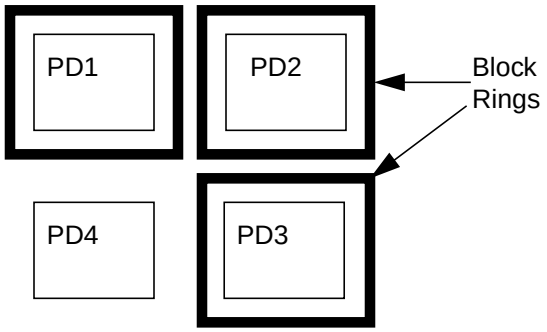


Each Reef

Creates a separate ring around each reef in the design. Reefs are used in flipchip designs.

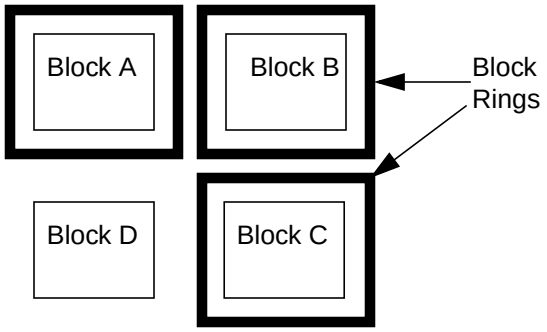
Selected power domain/fences/reefs

Creates a separate ring around each power domain selected in the design display area, around the fence that surrounds a soft block, or around a reef of bumps. If both a power domain and a fence are selected, the power domain takes precedence. For example, if you select PD1, PD2, and PD3, rings are created as shown in the following illustration.



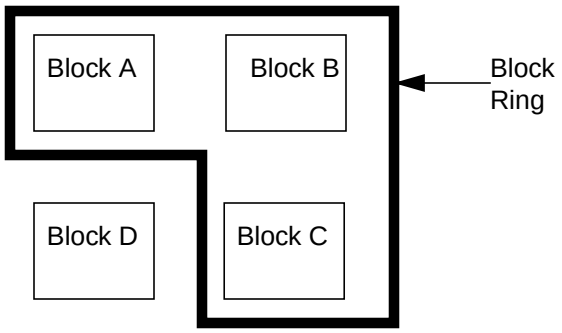
Each selected block and/or group of core rows

Creates a separate ring around each block and each group of core rows that is selected in the design display area. For example, if you select Block A, Block B, and Block C, block rings are created as shown in the following illustration.



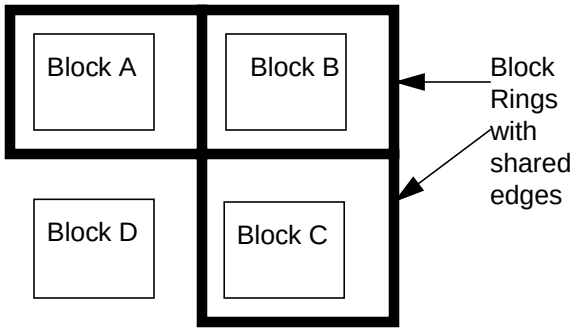
Cluster of selected blocks and/or groups of core rows

Treats all the blocks and groups of core rows selected in the design display area as a single cluster and creates a ring around the cluster. For example, if you select Block A, Block B, and Block C, a ring is created as shown in the following illustration.



With shared ring edges

Treats all the blocks and groups of core rows selected in the design display area as a single cluster and creates rings with shared ring edges around the cluster. To enable this option, you must first select *Cluster of selected blocks/groups of core rows*. For example, if you select Block A, Block B, and Block C, block rings with shared edges are created as shown in the following illustration.



User defined coordinates

Creates a ring that has the same number of corners as the number of x and y coordinates that you specify. You must specify the coordinates in a linear sequence. For example, you cannot specify the coordinates in a sequence such as bottom left, top right, bottom right, top left. For more information, see Creating a Ring with User Defined Coordinates.

Mouse Click Click this button, then move the cursor to the design display area. Click the points to define the corners of the ring. A temporary image shows the location of the ring wires that will be created. When you press the *Esc* key, the *User Specified Coordinates* text entry field is automatically populated with the coordinates of the area you selected.

Core ring The ring has the shape `RING`. This is the default.

Block ring The ring has the shape `BLOCKRING`.

Ring Configuration — The configuration of the rings to be created. Specify options to meet the requirements of your design.

- *Layer* — Use the pull-down menus to select the layer to use for each side of the ring(s) being created.
- *Width* — Use the text entry fields to specify the width, in microns, of the ring segments for each side ring(s).
- *Spacing* — Use the text entry fields to specify the edge-to-edge spacing, in microns, between rings for each side of the ring.
- *Update* — Click this button to automatically update the values in the *Spacing* fields. If spacing values in the *Spacing* fields are less than the values from the LEF file for a particular width, the values in the *Spacing* fields are increased to prevent minimum spacing violations.
- *Offset* — Controls how core rings are offset from the core area. Select one of the following options:
  - *Center in channel* — Specifies that the core ring is centered in the channel between the I/O area and the core area. This option is not available for block rings.
  - *Specify* — Select this option, then use the text entry boxes to specify the distance, in microns, between the edge of the inner ring and the boundary of the referenced object (blocks, rows, power domains, I/O area or core area) for each side of the ring. If you specify a negative number, the ring is created inside of, rather than surrounding, the referenced object.

    Note: For core rings, you can choose between this option and the *Center in channel* option. For block rings, you must specify offset values.

Option File

Use option file	Instructs the power analysis software to use an option file. **Note:** When you click this option, the *Via Generation* tab becomes inactive.
Update Basic	Updates data on the *Basic* tab with the contents of the option file you have specified.
Load Editor	Opens the Edit Power Planning Option form.

Related Text Commands

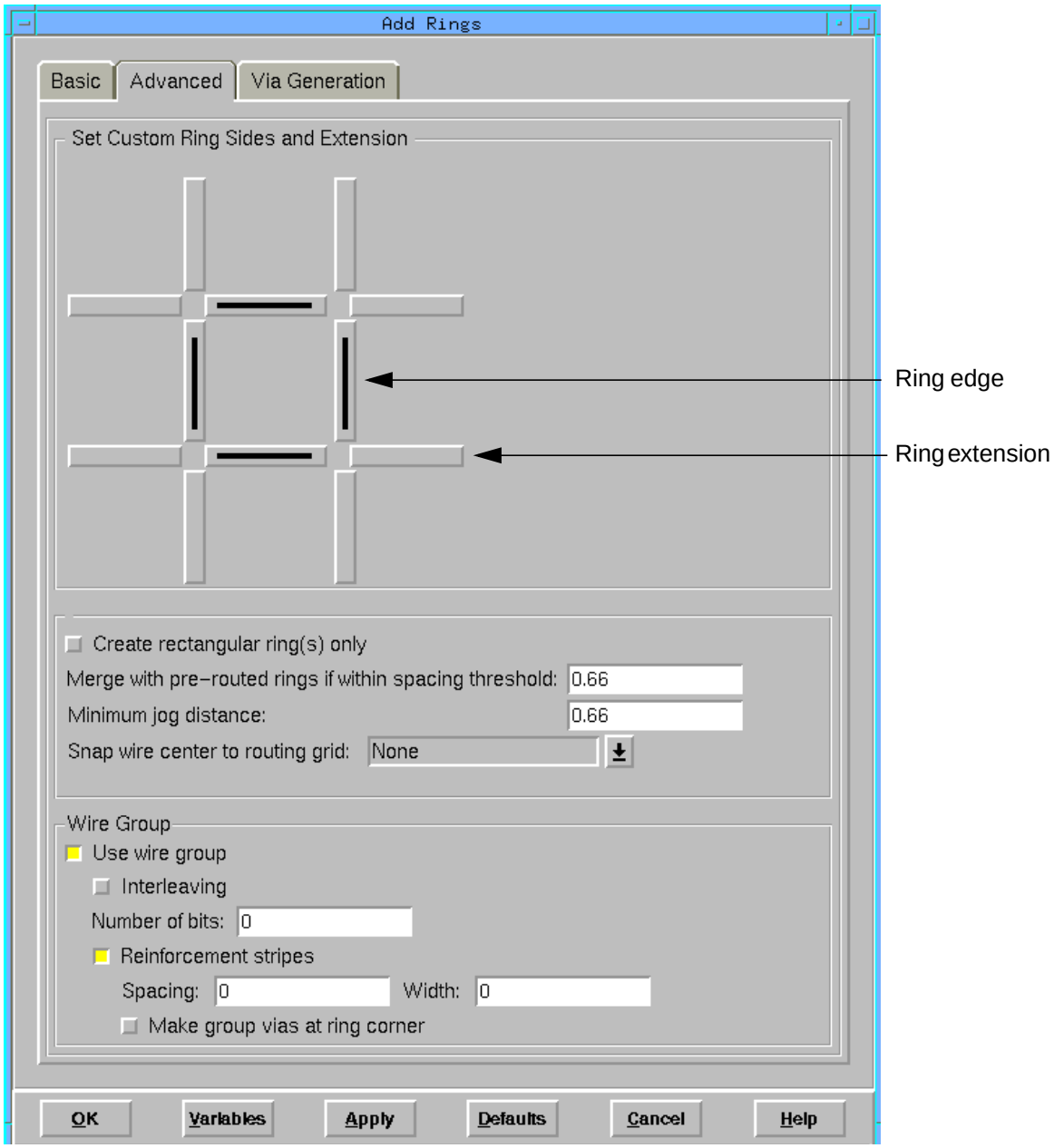
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addRing`

Add Rings – Advanced

The Advanced page of the Add Rings form lets you limit which sides of a ring are to be created and which sides are to be extended to connect to existing power structures. This page also provides options for you to customize rings to meet your design needs.

➤ To open the Advanced page of the Add Rings form, choose *Power – Power Planning – Add Rings*, then click the *Advanced* tab.



Add Rings – Advanced Fields and Options

Set Custom Ring Sides and Extension

(Optional) Allows you to create rings in any configuration. Click a ring edge bar to select or deselect one or more edges to indicate where rings segments are to be created. Click an extension bar to select or deselect one or more of the eight strips (above, below, or to the sides of the ring edges) to indicate the direction in which you want to extend the ring. The ring is extended in those areas until encountering a legal target. By default, all edges are selected and all extensions are deselected.

Create rectangular ring(s) only

If selected, the software does not create rectilinear rings. If deselected, the software can create either rectangular or rectilinear rings. This is the default.

Merge with pre-routed rings if within spacing threshold

(Optional) The minimum spacing, in microns, allowed between ring segments before they can be merged. If spacing is less that this value, rings are merged.

Minimum jog distance

(Optional) The minimum jog distance, in microns, allowed (to follow the contour of the object that the ring surrounds) before the jog is straightened. If the ring would need to jog a distance equal to or less than this value in order to follow the contour of the object, the ring will not jog.

Snap wire center to routing grid

Control the snapping of the center of the sides of the rings to the routing grid. Choose one of the following:

None	Does not snap the wires. This is the default.
Grid	Snaps the centers of the wires to the routing grid of the same layer as the wire.
Half_Grid	Snaps the centers of the wires to the half-routing grid. The half-routing grid is a virtual grid with the tracks at the center of every two adjacent tracks of the routing grid.
Either	Snaps the centers of the wires to the closer of the routing grid or half grid track.

Use wire group

If selected, multiple wires from the same net will be grouped together and via arrays generated as if they were one wire. Cadence recommends that you select this option to provide stronger connections for the rings. If deselected, wire groups are not used. This is the default.

Note: For stripes to connect to rings using wire groups, you must select *Use wire group* in both the Add Rings and Add Stripes forms.

The following figure shows difference in the connections.

Interleaving

The following figure shows the difference in connections with interleaving power and ground wires. This option is deselected by default.

Number of bits

The number of bits specifies how many of each specified net are to be included in the wire group. The *Nets* field (on the *Basic* tab) is automatically populated with the same quantity of net names as specified in the *Number of bits* field. For example, if you have two nets, `VDD` and `VSS`, and you specify 3 in the *Number of bits* field, the *Nets* field is populated as follows if you also select *Interleaving*:

```
VDD VSS VDD VSS VDD VSS
```

Reinforcement stripes

If selected, adds reinforcement stripes to the wire group corners. Encounter automatically computes the number of reinforcement stripes that are added based on the *Spacing* and *Width* values that you provide.

The following figure shows the difference in connections when adding reinforcement stripes in the horizontal and vertical directions. This option is deselected by default.

Spacing

Specifies the amount of spacing, in user units, between the reinforcement stripes.

Width

Specifies the width, in user units, of each reinforcement stripe.

Make group vias at ring corners

If selected, creates group vias for the wire group corners along with reinforcement stripes placed in the horizontal and vertical directions. This option must be used in conjunction with the *Reinforcement stripes* option and is deselected by default.

Related Text Commands

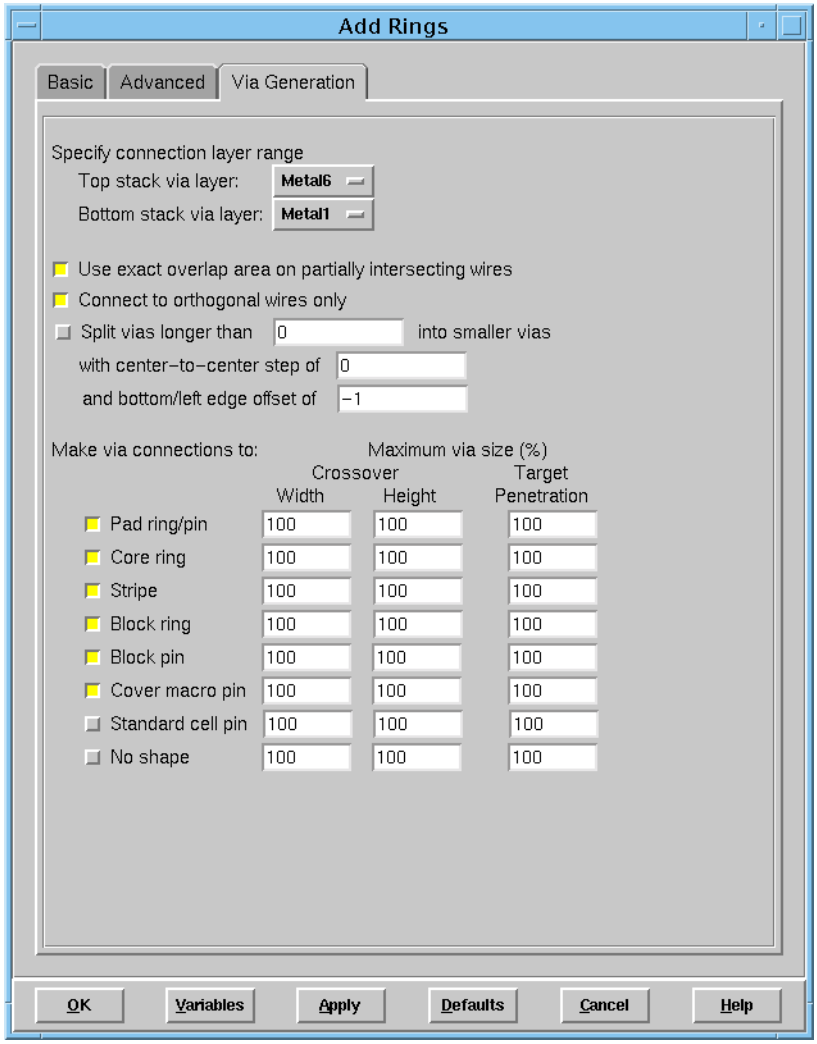
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addRing`

Add Rings – Via Generation

The Via Generation page of the Add Rings form lets you specify how vias connect to the power rings.

➤ To open the Via Generation page of the Add Rings form, choose *Power – Power Planning – Add Rings*, then click the *Via Generation* tab.



Add Rings – Via Generation Fields and Options

Top stack via layer — The highest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Bottom stack via layer

The lowest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Use exact overlap area on partially intersecting wires

If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.

Note: This option does not apply when both of the objects at the crossover are rings or stripes, or at the crossover of a ring and stripe. In these cases, the software always generates full-size vias.

Connect to orthogonal wires only

Creates vias *only* for orthogonal wires and pin intersections.

Default: On

Split vias longer than X *into smaller vias with center-to-center step of* Y *and bottom/left edge offset of* Z

Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers).

Default: Off

Make via connections to

Select the types of wires or pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made. By default, vias can connect to each of the following types of wire or pin:

- *Pad ring/pin*
- *Core ring*
- *Stripe*
- *Block ring*
- *Block pin*
- *Cover macro pin*
- *Standard cell pin*
- *No shape*

Note: Vias can only connect to wires labeled as *No shape* if you select this option.

Crossover Width

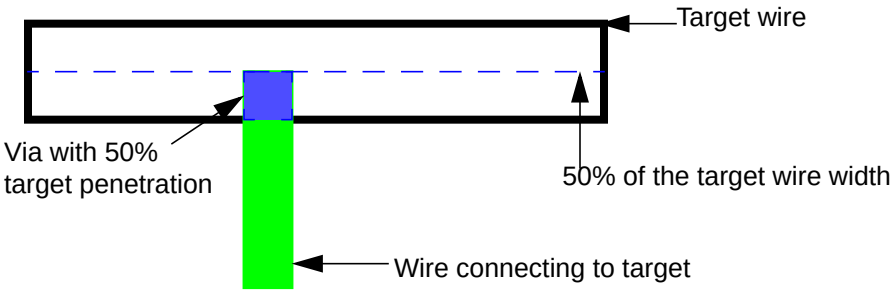
The maximum width of a crossover via, specified as a percentage of a full-size via.

Crossover Height

The maximum height of a crossover via, specified as a percentage of a full-size via.

Target penetration (%) Specifies a smaller size for vias connecting to targets of a particular wire or pin type.

By default, if a wire or pin is a target to which a via can be connected, the via is a full-sized. If you want the via to be smaller, you can specify a value in this field for each wire type. Only a single dimension of the via will be scaled. For example, if you specify a value of 50, the via will be full-sized in one dimension (the width of the wire that crosses the ring), but only half the width in the other dimension (the width of the target wire).



Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addRing`

Add Ring Environment Variables

Use the Add Ring Environment Variables form to set global values used by the power planning software during the creation of power rings.

➤ To open the Add Ring Environment Variables form, choose *Power – Power Planning – Add Rings*, then click the *Variables* button at the bottom of the form.

Add Rings Environment Variables Fields and Options

Consider both rings and stripes as targets

Select this option if you want rings to consider both rings and stripes as targets. Deselect this option if you want stripes to be ignored as targets.

Consider pad rings as targets

If you select this option, rings to consider pad rings as targets. Deselect this option if you want rings to ignore pad rings as targets.

Extend over row

If you select this option, the cut row is not considered a blockage by the power planning software, which generates the ring over the cut row. If you deselect this option, the cut row is considered a blockage and the ring is not generated over the row.

Ignore rows

If you select this option, the power planning software ignores all rows (cut rows and native rows) when core rings or block rings are created. Deselect this option to create rings that do not ignore rows.

Avoid shorts

Select this option to prevent a ring or a ring segment from being created if it would cause a DRC violation to occur. Deselect this option to enable the creation of rings that cause a DRC violation.

Skip crossing trunk

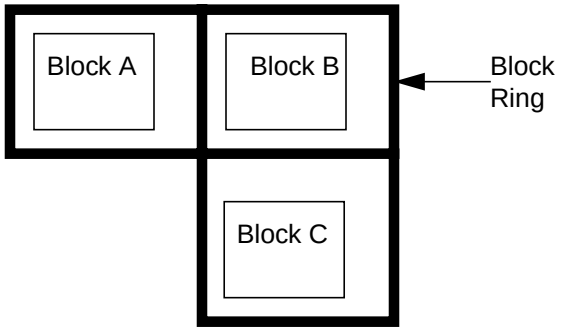
Controls whether ring edges of a particular orientation are shared or removed, when used in conjunction with the *Cluster of selected blocks and/or groups of core rows* option along with the *Shared ring edges* option on the *Basic* page of the Add Rings form.

Note: For best results when using this option, create block halos and issue the `cutCoreRow` command prior to the using the Add Ring software.

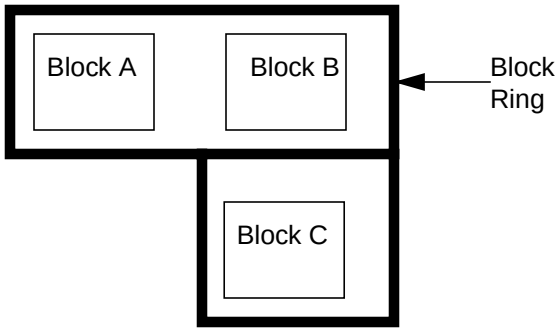
Select one of the following options:

None

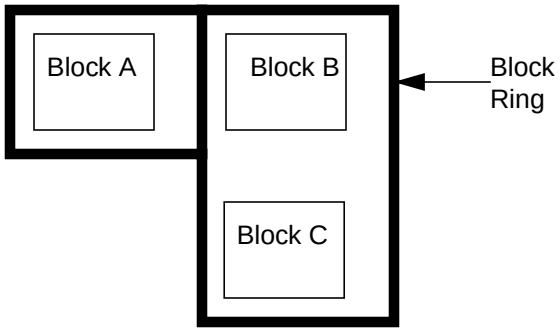
Maintains all sections of rings. Rings are created as shown in the following illustration:



Vertical Removes the vertical portion of rings (shared or inside edges). Rings are created as shown in the following illustration:



Horizontal Removes the horizontal portion of rings (shared or inside edges). Rings are created as shown in the following illustration:



Note: After you click *OK* or *Apply*, the settings in this form remain as you set them until you either specifically reset them or you close the software.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `setAddRingOption`

Add Stripes

Use the Add Stripes form to create power stripes within the specified range. If block rings are encountered, the stripes connect to the block rings. If an obstruction is encountered, the stripe connects to the last stripe on the same net; otherwise the stripe stops at the core row boundary.

The Add Stripes form contains the following three pages:

- *Add Stripes – Basic*
- *Add Stripes – Advanced*
- *Add Stripes – Via Generation*

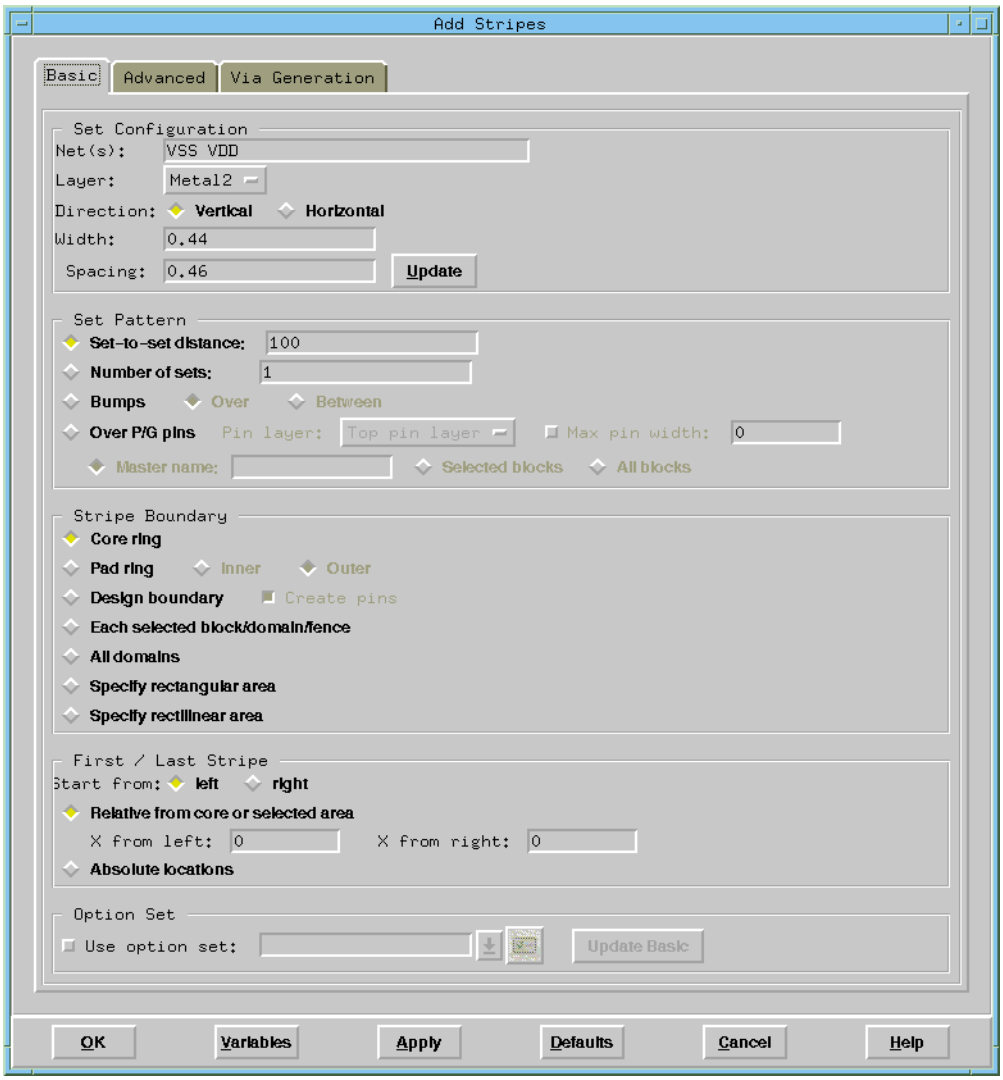
You can access the following form from the Add Stripes form:

- Add Stripe Environment Variables

Add Stripes – Basic

Use the *Basic* page of the Add Stripes form to specify the nets, layers, direction, and other configuration options for power stripes that you add to the design.

➤ To open the *Basic* page of the Add Stripes form, choose *Power – Power Planning – Add Stripes*, then click the *Basic* tab.



Add Stripes – Basic Fields and Options

Set Configuration

The configuration of the stripe set to be created. Specify options to meet the needs of your design.

Net(s)

The net name(s) for which stripes must be created. The number of net names determines the number of stripes within each set of stripes. The first net in the name list is created first and corresponds to the left or bottom stripe of the set. Separate multiple net names with a space.

Note: This field is ignored if you specify *All domains* in the *Stripe Boundary* panel.

Layer

The layer to use to create stripes. By default, the software uses the first vertical routing layer or the second horizontal routing layer in the technology file to populate the form.

Note: When you select a layer, the *Direction* buttons below *Layer* indicate the preferred direction of the layer you have selected.

Direction

The stripe orientation. You can specify only one direction at a time. If you need both vertical and horizontal stripes, create stripes in one direction first, then select this form again to create stripes in the other direction.

Choose one of the following options:

Vertical — Creates vertical stripes with the attributes specified by the selected options. This is the default.

Horizontal — Creates horizontal stripes with the attributes specified by the selected options.

Width

The width, in microns, of the stripes. You can specify a different width for each net within a set. If the number of widths specified does not match the number of net names, the last specified width is used for the unmatched nets.

Spacing

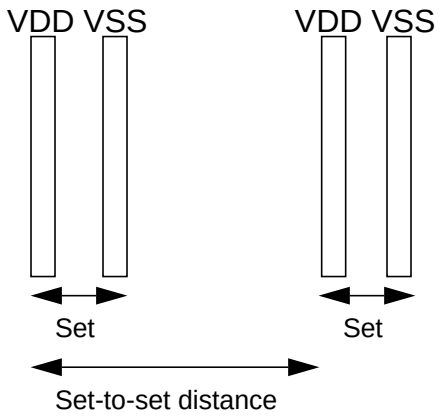
The edge-to-edge spacing, in microns, between stripes in each set. You can specify different spacing rules between each pair of stripes. For *N* number of stripes in a set, *N* – 1 number of spacing rules must be to specified. If fewer values are specified, the last specified spacing is used for the unmatched stripe pairs.

Update (Optional) Automatically updates the values in the *Spacing* fields. If spacing values in the *Spacing* fields are less than the values from the LEF file for a particular width, the values in the *Spacing* fields are increased to prevent minimum spacing violations.

Set Pattern Controls the spacing between stripes. Choose one of the following options:

Set-to-set-distance

The distance (pitch), in microns, from the edge of the first stripe of the set to the same edge of the first stripe of the next set. The number of sets is derived from the stripe range and pitch. The value entered must be a positive number, in microns. The following diagram shows the locations from which this distance is measured for a set that contains two stripes.



Number of sets The number of stripe sets to be created. The set-to-set distance is derived from the stripe range and number of sets you specify in this field.

Bumps Determines the generation of stripes in relation to bumps.

- *Over* indicates that stripes should be generated over bumps.
- *Between* indicates that stripes should be generated between bumps.

Default: *Over*

Over P/G pins Generates stripes over power/ground pins in a standard cell or block.

- *Pin layer* indicates the layer on which the stripe is generated.

  Default: Top pin layer of the standard cell or block

  - *Master Name* indicates instances of the standard cell (or block) master over which the stripes should be generated. This is the default setting.
  - *Selected blocks* allows you to use the Encounter main window display to select instances for which to generate stripes.
  - *All blocks* specifies that stripes should be generated over all blocks.

- *Max pin width* indicates that only pins less than or equal to this maximum pin width setting will be considered when generating stripes over pins. This is available only when *Over P/G pins* is enabled.

  Default: off

Stripe Boundary Controls the region over which stripes are to be created. Select one of the following options:

Core ring Stripes are created within the area enclosed by the core ring.

Pad ring

Stripes are created within the area enclosed by the pad ring. If you select this option, you must also select one of the following options to indicate stripe behavior for multiple pad rings of the same net:

- *Inner* indicates that stripes stop at the pad ring closest to the core area.
- *Outer* indicates that stripes stop at the pad ring closest to the design boundary.

Design Boundary

Stripes are created within the design boundary.

Create pins

Note: If selected, create I/O pins for each stripe. Any overlap with existing I/O pins at the design boundary are flagged as warnings after stripes are created. This is the default. If deselected, pins are not created.

Each selected block/domain/fence

Stripes are created only for the selected block or power domain, or for a fence surrounding a soft block. For power domains, these stripes start and stop at the power ring that surrounds the selected power domain boundary. For fences, these stripes start and stop at the fence. If both a power domain and a fence are selected, the power domain takes precedence. If deselected, stripes are created in the manner that you specify with the other options on this form, treating the power domain boundary as a block. This is the default.

All Domains

Stripes are created over all power domains for each power and ground net within each power domain. Stripes start and stop at each power domain boundary or rings around the domain, and ignore any values that you specify in the Net(s) field.

Specify rectangular area

Stripes are created within the exact rectangular area indicated by the coordinates.

Specify rectilinear area

Stripes are created within the exact rectilinear area indicated by the coordinates.

First / Last Stripe

Controls the location of the first and last stripe. Select one of the following options:

Start from

For vertical stripes:

- *left* indicates that stripes should be generated from left to right, taking the left offset into account.
- *right* indicates that stripes should be generated from right to left, taking the right offset into account.

  Default: *left*

For horizontal stripes:

- *bottom* indicates that stripes should be generated from bottom to top, taking the bottom offset into account.
- *top* indicates that stripes should be generated from top to bottom, taking the top offset into account.

  Default: *bottom*

Relative from core or specified area

The distance, in microns, of the start point of the stripes from the stripe boundary. If the boundary is the core ring, pad ring, or design area, the first and last stripe start at the core area. This is the default.

For vertical stripes, enter the distance from the left side of the boundary for the first stripe and the distance from the right side of the boundary for the last stripe.

For horizontal stripes, enter the distance from the top of the boundary for the first stripe and the distance from the bottom of the boundary for the last stripe.

Absolute locations

The exact x and y coordinates where the first and last stripes must be created.

For vertical stripes, enter the X coordinates for the first stripe and the last stripe in the text entry fields.

For horizontal stripes, enter the Y coordinates for the first stripe and the last stripe in the text entry fields.

Option File

Use option file Instructs the power analysis software to use an option file.

Note: When you click this option, the *Advanced* and *Via Generation* tabs become inactive.

Update Basic Updates data on the *Basic* tab with the contents of the option file you have specified.

Load Editor Opens the Edit Power Planning Option form.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addStripe`

Related Topics

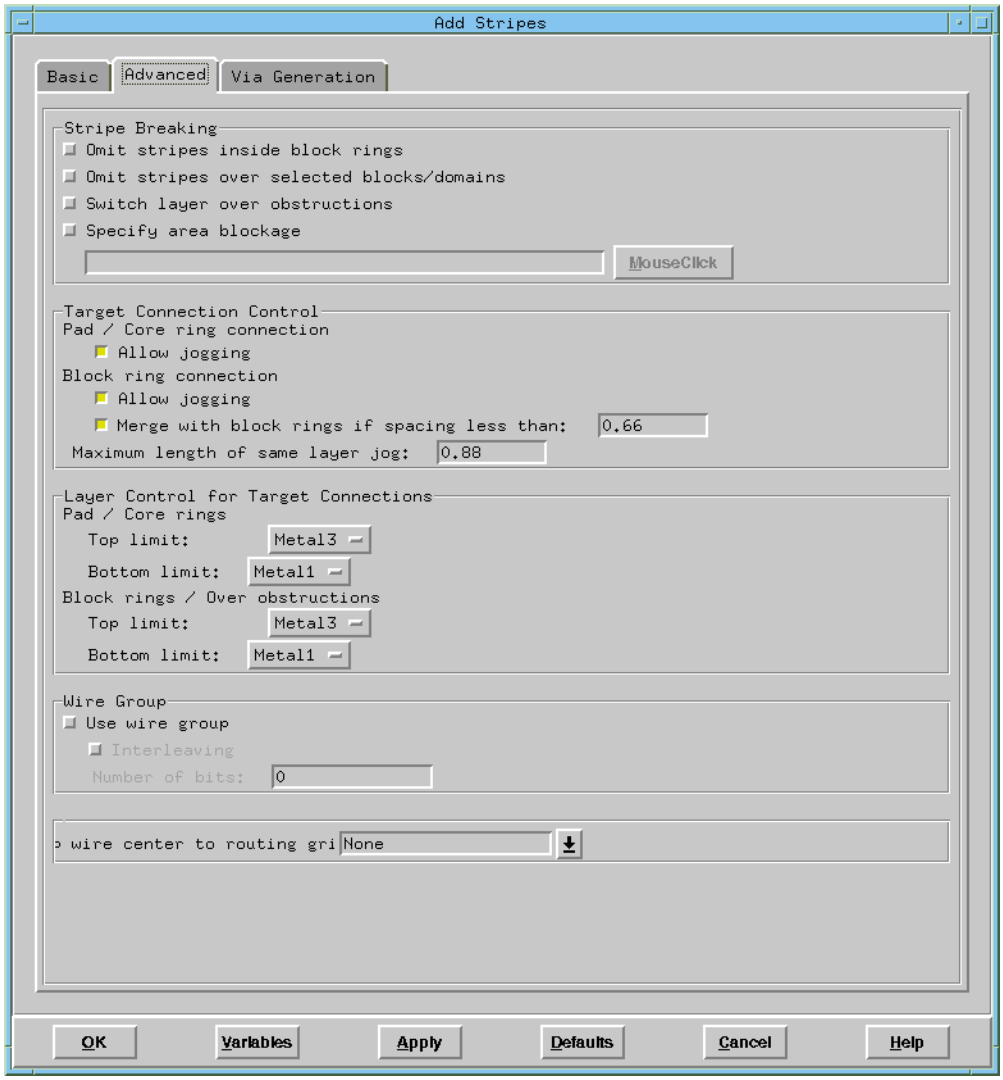
For information on the following topic, see “Power Planning and Routing” in the *Encounter User Guide*.

- Adding Stripes to Power Domains

Add Stripes – Advanced

Use the Advanced page of the Add Stripes form to limit the area in which stripes can be created as well as specify the behavior of stripes when they are near rings, obstructions, rows, or design boundaries.

1. Choose *Power – Power Planning – Add Stripes*, then click the *Advanced* tab.



Add Stripes – Advanced Fields and Options

Omit stripes inside block rings

If selected, stripes stop whenever a block ring is encountered and restart on the other side of the if block rings. If deselected, stripes are created over block rings.

Note: This option applies only to block rings that surround a block, and does not apply to block rings that surround rows or standard cells. If the block is a ring macro, the stripe will break at the ring pin inside the block ring.

Omit stripes over selected blocks/domains

If selected, stripes break whenever a selected block or power domain is encountered, then restart on the other side of the block or power domain. Stripes are created over unselected blocks and power domains. If deselected, stripes are created over all blocks and power domains.

Switch layer over obstructions

If selected, stripes switch layers, are routed over obstructions, and then continue on the original layer.

Default: Off

Specify area blockage

Specifies a rectilinear area blockage that restricts the addition of any stripes to this region. Select this option, then specify the blockage coordinates.

Tip

Clicking on the mouse icon and moving the cursor to the design display area enables you to use the mouse to specify the blockage coordinates.

Default: Off

Pad/Core ring connection: Allow jogging

If selected, stripes can jog in order to connect with a pad ring or core ring (default). If deselected, stripes do not jog to make these connections.

Block ring connection: Allow jogging

If selected, stripes can jog in order to connect with a block ring (default). If deselected, stripes do not jog to make these connections.

Block ring connection: Merge with rings if spacing less than

If selected, you can specify the threshold, in microns, for merging stripes. If the threshold spacing between the stripe and ring is smaller than the value specified, the stripe jogs to connect to the nearby ring. The default value of this field is the same as the value in the *Spacing* field on the *Basic* page of this form. If deselected, stripes do not merge with block rings.

Maximum length of same layer jog

The maximum length, in user units, that a stripe can jog on the same layer before switching to an adjacent layer. For example, if you specify a value of `2` user units, and an obstruction causes a stripe on layer `M4` to jog for `3` user units, the jog will occur on layer `M3` or `M5`. However, if an obstruction causes the stripe to jog for only `1` user unit, the jog occurs on layer `M4`.

Layer Control for Target Connections

Controls the layers that stripes can switch to when encountering rings. Choose a top and bottom layer for each of the following types of rings:

Pad/Core rings	Stripes that encounter a pad or core ring can only switch to layers within the range you select. By default, both the *Top Limit* and *Bottom Limit* are set to two layers above and below the stripe layer.
Block rings / Over obstructions	Stripes that encounter a block ring can only switch to layers within the range you select. By default, both the *Top Limit* and *Bottom Limit* are set to two layers above and below the stripe layer

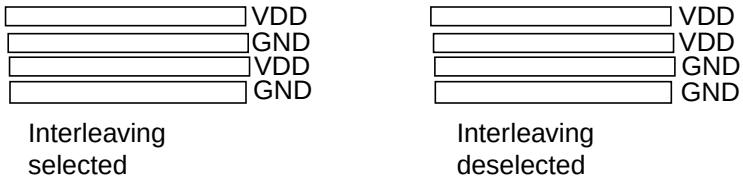
Use wire group

If selected, permits the use of wire groups for buses, based on a property set in the DEF. If deselected, wire groups are not used. This is the default.

Note: For stripes to connect to rings using wire groups, you must select *Use wire group* in both the Add Rings and Add Stripes forms.

Interleaving

The style of the wire groups. The following illustration shows the difference in how wires are created:



Number of bits

The number of nets that are to be included in the wire group. The *Nets* field (on the *Basic* tab) is automatically populated with the same quantity of net names as specified in the *Number of bits* field. For example, if you have two nets, VDD and VSS, and you specify 6 in the *Number of bits* field, the *Nets* field is populated as follows:

```
VDD VSS VDD VSS VDD VSS
```

Snap wire center to routing grid

Controls how wires snap to the grid. Select one of the following options from the pulldown menu:

None	Does not snap the wires. This is the default.\
Grid	Snaps the centers of the wires to the routing grid of the same layer as the wire.
Half_Grid	Snaps the centers of the wires to the half-routing grid. The half-routing grid is a virtual grid with the tracks at the center of every two adjacent tracks of the routing grid.
Either	Snaps the centers of the wires to the closer of the routing grid or half grid track.

Related Text Commands

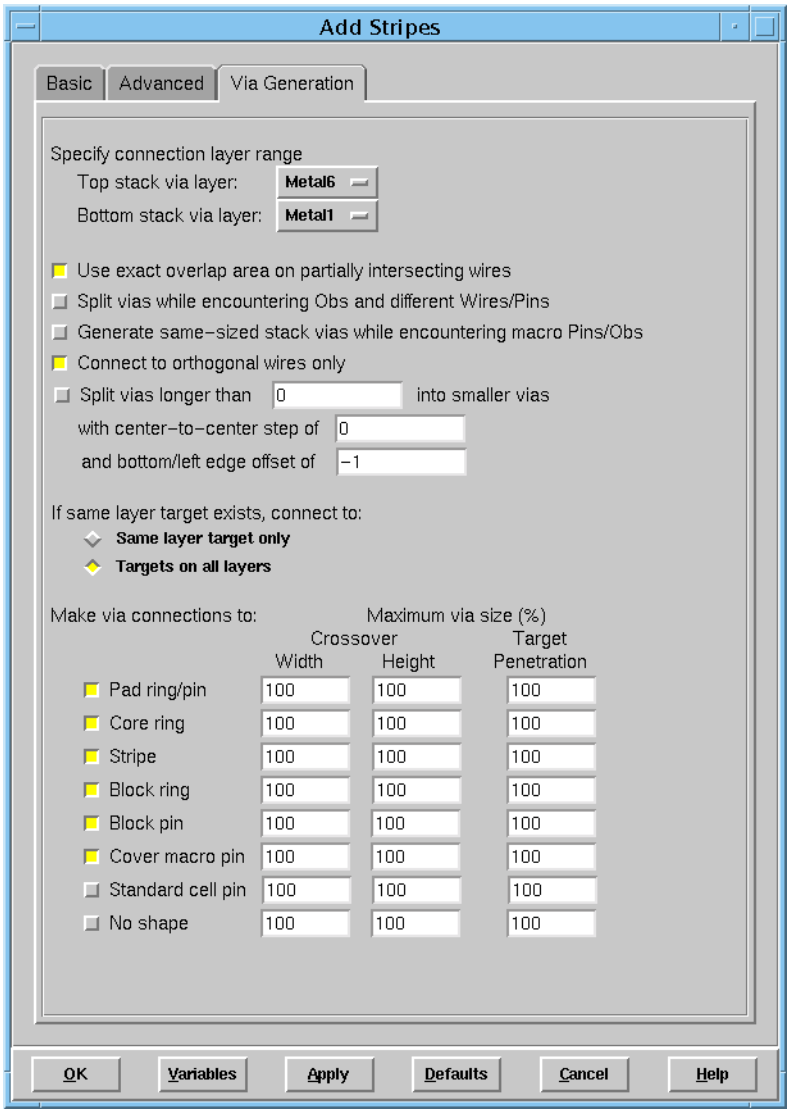
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addStripe`

Add Stripes – Via Generation

Use the Via Generation page of the Add Stripes form to specify how vias connect to the power stripes.

➤ To open the Via Generation page of the Add Stripes form, choose *Power – Power Planning – Add Stripes*, then click the *Via Generation* tab.



Add Stripes – Via Generation Fields and Options

Top stack via layer
The highest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Bottom stack via layer
The lowest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Use exact overlap area on partially intersecting wires

If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.

Note: This option does not apply when both of the objects at the crossover are rings or stripes, or at the crossover of a ring and stripe. In these cases, the software always generates full-size vias.

Split vias while encountering Obs and different Wires/Pins

If selected, two or more partial vias can be created at the crossover between a stripe and any target (pin or wire) if an obstruction (macro obstruction; wire or pin on a different net) prevents the creation of a full-size via. This may be useful, for example, if several metal obstructions partially obstruct the area where a full-size via would normally be placed. This option permits the creation of partial vias that would not violate the process rules, in the open areas. If deselected, one via of the maximum size will be created.

Default: Off

Generate same-sized stack vias while encountering macro Pins/Obs

If selected, the software always generates same-sized stacked vias. If deselected, the software trims the vias as needed to meet the DRC rules.

Connect to orthogonal wires only

Creates vias *only* for orthogonal wires and pin intersections.

Default: On

Split vias longer than X *into smaller vias with center-to-center step of* Y *and bottom/left edge offset of* Z

Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers).

Default: Off

If same layer target exists, connect to

Same layer target only — Prevents the creation of vias to connect to other layers when a target exists on the same layer. This only applies when targets of multiple layers of the same net are stacked on top of one another. If a target does not exist on the same layer, vias are generated to connect to targets on other layers.

Targets on all layers — Allows the creation of vias to connect to other layers when a target exists on the same layer.

Make via connection to — Select the types of wires or pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made. By default, vias can connect to each of the following types of wire or pin:

- *Pad ring/pin*
- *Core ring*
- *Stripe*
- *Block ring*
- *Block pin*
- *Cover macro pin*
- *Standard cell pin*
- *No Shape*

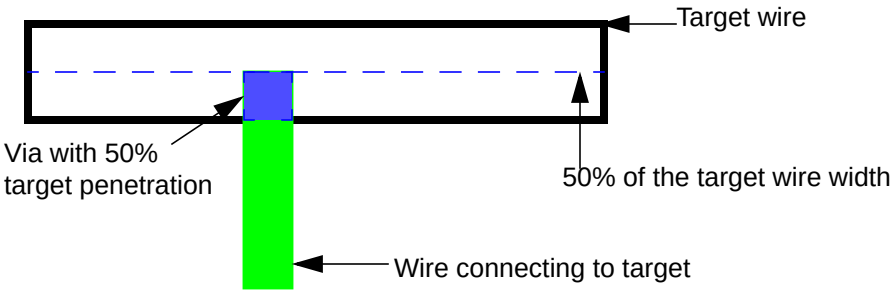
Note: Vias can only connect to wires labeled as *No shape* if you select this option.

Crossover Width — The maximum width of a crossover via, specified as a percentage of a full-size via.

Crossover Height The maximum height of a crossover via, specified as a percentage of a full-size via.

Target penetration (%) Specifies a smaller size for vias connecting to targets of a particular wire or pin type.

By default, if a wire or pin is a target to which a via can be connected, the via is a full-sized. If you want the via to be smaller, you can specify a value in this field for each wire type. Only a single dimension of the via will be scaled. For example, if you specify a value of 50, the via will be full-sized in one dimension (the width of the wire that crosses the ring), but only half the width in the other dimension (the width of the target wire).



Related Text Commands

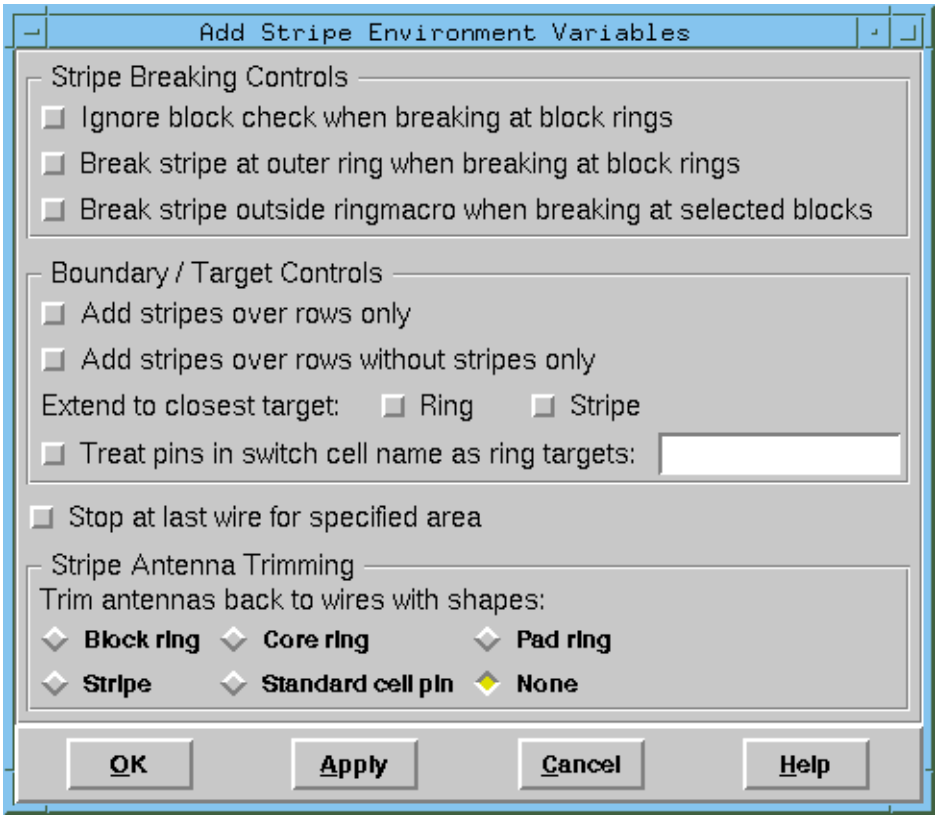
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addStripe`

Add Stripe Environment Variables

Use the Add Stripe Environment Variables form to set global values used by the power planning software during the creation of power stripes.

➤ Choose *Power – Power Planning – Add Stripes*, then click the *Variables* button at the bottom of the form.



Add Stripe Environment Variables Fields and Options

Ignore block check when breaking at block rings

If you select this option, when a stripe encounters a ring, the software does not check whether that ring is surrounding a block. If you deselect this option, when a stripe encounters a ring, the software automatically checks whether a block is enclosed within the ring.

Default: Off

Note: This option only works in conjunction with the following options on the *Advanced* page of the Add Stripes form:

- *Omit stripes within block rings*
- *Omit stripes over selected blocks/domains*

Break stripe at outer ring when breaking at block rings

If selected, when a stripe encounters nested block rings that are not in the same wire group, the stripe breaks at the outer ring. If deselected, the stripe breaks at the innermost ring.

Default: Off

Note: This option only works in conjunction with the following options on the *Advanced* page of the Add Stripes form:

- *Omit stripes within block rings*
- *Omit stripes over selected blocks/domains*

Break stripe outside ring macro when breaking at selected blocks

If selected, breaks the stripe a small distance outside the block and does not connect to the ring pins, if the selected block has ring pins. If you do not select this option, the stripe connects to the ring pins.

Default: Off

Note: This option only works in conjunction with the following option on the *Advanced* page of the Add Stripes form:

- *Omit stripes over selected blocks/domains*

Add stripes over rows only

If selected, stripes can be created only over rows within the boundary specified in the *Stripe Boundary* panel of the *Basic* page of this form. If deselected, stripes are created over the boundary.

Default: Off

Add stripes over rows without stripes only

If selected, stripes are created only over row clusters without stripes. If deselected, stripes are generated as specified by the other options in the Add Stripes form.

Default: Off

Note: This option is useful when you have already run the `addStripe` command and need to run it again to create stripes in areas in which stripes were not generated.

Extend to closest target

If selected, stripe antennas are extended to the closest ring or stripe. If deselected, stripes stop at the boundary specified on the *Basic* page of the Add Stripes form.

Default: Off

Treat pins in switch cell name as ring targets

Treats the specified switch cell as a ring. Pins in the switch cell can then be used as targets for stripes. If the switch cell is in the core area, the software treats it as a block ring. If the switch cell is outside of the floorplan row, the cell is treated as a core ring, and used as the stripe boundary.

Default: Off

Stop at last wire for specified area

If selected, the stripe antennas are trimmed back to the closest wire or pin of the same net.

Default: Off

Note: This option is only available if you select *Specify Area* on the *Basic* page of the Add Stripe form.

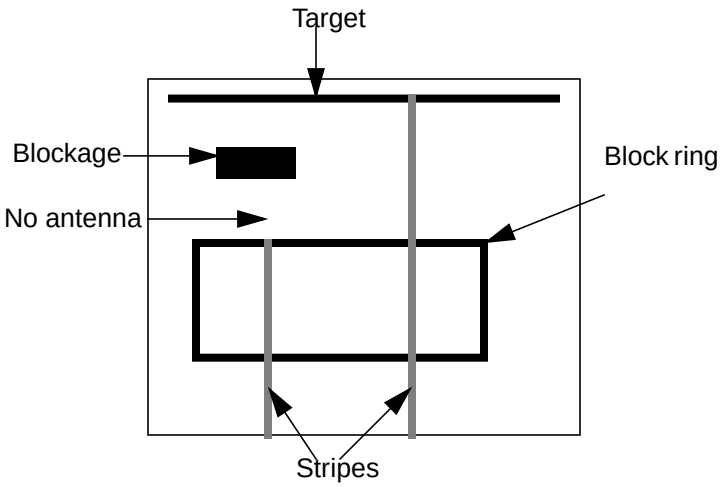
Trim antennas back to wires with shapes

Prevents stripes from creating antennas when a wire of the specified shape is the last target before a blockage that prevents connection to another target. Select one of the following shapes:

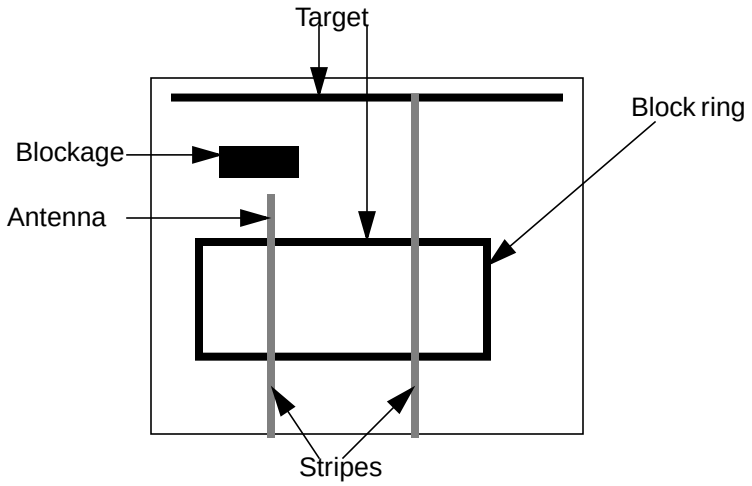
- *Block ring*
- *Core ring*
- *Pad ring*
- *Stripe*
- *Standard cell pin*
- *None*

Default: None

The following figure illustrates this option if you select *Block ring*.



If you select *None*, stripes extend to the blockage, leaving an antenna between the last connection and the blockage. The following figure illustrates this option.



Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `setAddStripeOption`

Add XStripes

Use the Add XStripe form to create diagonal power routes and stripes for Encounter X designs. You can create any combination of Manhattan and diagonal power and ground routing. You can add diagonal stripes on diagonal routing layers only, and only in the preferred routing direction of the layer. When stripes encounter a local preferred direction routing (LPDR) area, they automatically change direction to conform to the local preferred direction in that area.

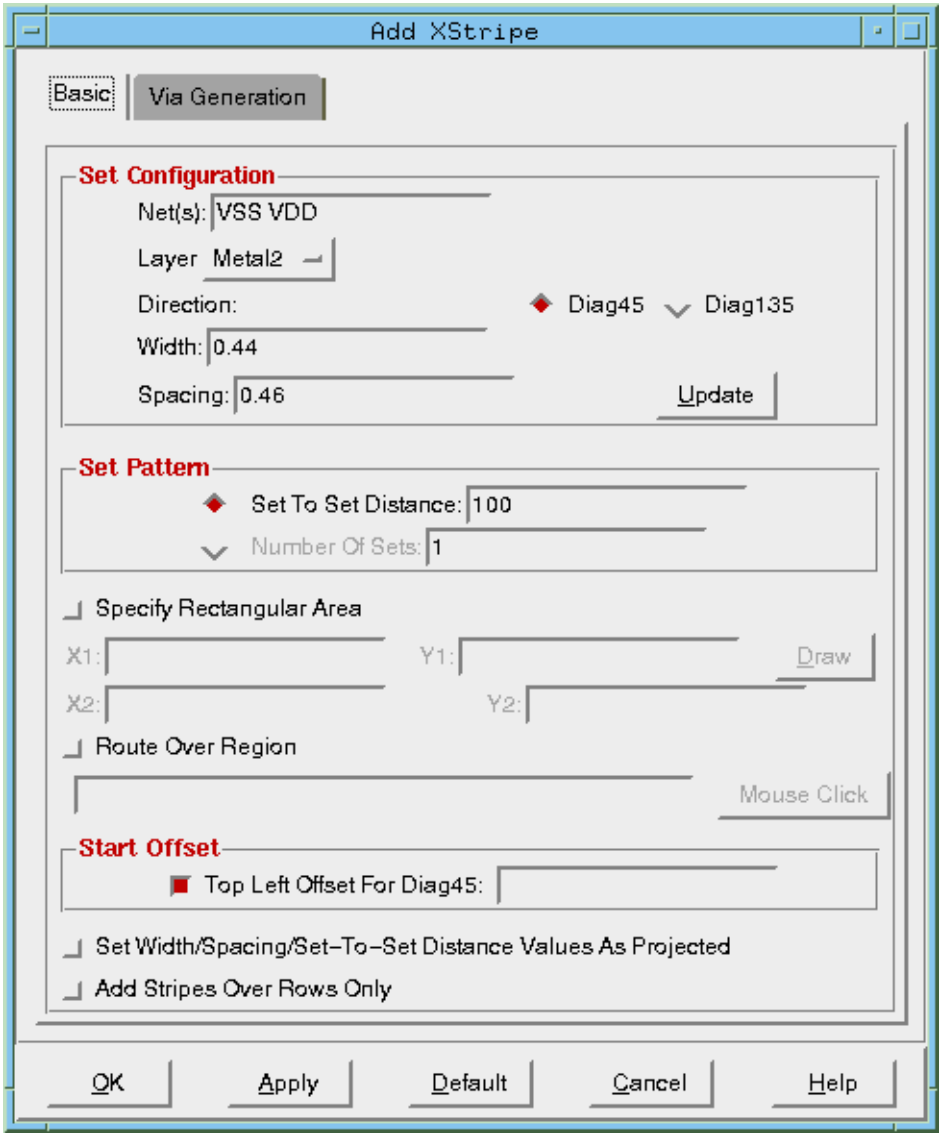
The Add XStripe form contains the following two pages:

- *Add XStripes – Basic*
- *Add XStripes – Via Generation*

Add XStripes – Basic

Use the *Basic* page of the Add XStripe form to specify the nets, layers, direction, and other configuration options for diagonal power routes and stripes that you add to the Encounter X design.

➤ To open the *Basic* page of the Add XStripe form, choose *Power – Power Planning – Add XStripes*, then click the *Basic* tab.



Add XStripes – Basic Fields and Options

Set Configuration

The configuration of the diagonal stripe set to be created. Specify options to meet the needs of your design.

Net(s)

The net name(s) for which diagonal stripes must be created. The number of net names determines the number of diagonal stripes within each set of diagonal stripes. The first net in the name list is created first and corresponds to the left or bottom diagonal stripe of the set. Separate multiple net names with a space.

Layer

The layer to use to create diagonal stripes. By default, the software uses the first vertical routing layer or the second horizontal routing layer in the technology file to populate the form.

Note: When you select a layer, the *Direction* buttons indicate the preferred direction of the layer you have selected.

Direction

The diagonal stripe orientation. You can specify only one direction at a time. If you need both 45-degree and 135-degree diagonal stripes, create diagonal stripes in one direction first, then select this form again to create diagonal stripes in the other direction.

Choose one of the following options:

Diag45 — Creates 45-degree diagonal stripes with the attributes specified by the selected options. This is the default.

Diag135 — Creates 135-degree diagonal stripes with the attributes specified by the selected options.

Width

The width, in microns, of the diagonal stripes. You can specify a different width for each net within a set. If the number of widths specified does not match the number of net names, the last specified width is used for the unmatched nets.

Spacing

The edge-to-edge spacing, in microns, between diagonal stripes in each set. You can specify different spacing rules between each pair of diagonal stripes. For *N* number of diagonal stripes in a set, *N* – 1 number of spacing rules must be specified. If fewer values are specified, the last specified spacing is used for the unmatched diagonal stripe pairs.

Update

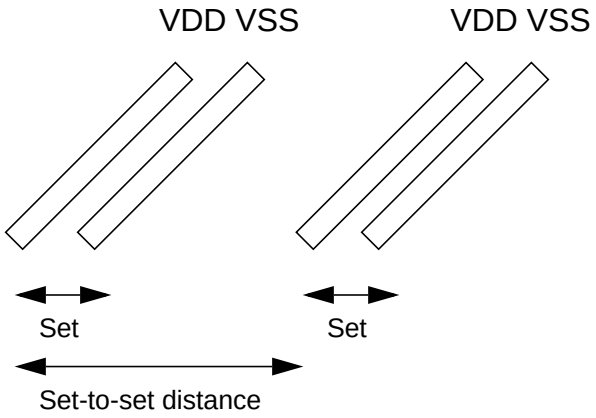
(Optional) Automatically updates the values in the *Spacing* fields. If spacing values in the *Spacing* fields are less than the values from the LEF file for a particular width, the values in the *Spacing* fields are increased to prevent minimum spacing violations.

Set Pattern

Controls the spacing between diagonal stripes. Choose one of the following options:

Set To Set Distance

The distance (pitch), in microns, from the edge of the first diagonal stripe of the set to the same edge of the first diagonal stripe of the next set. The number of sets is derived from the diagonal stripe range and pitch. The value entered must be a positive number, in microns. The following diagram shows the locations from which this distance is measured for a set that contains two 45-degree diagonal stripes.



Number of sets

The number of diagonal stripe sets to be created. The set-to-set distance is derived from the diagonal stripe range and number of sets you specify in this field.

Specify Rectangular Area

Creates diagonal stripes within the exact rectangular area indicated by the coordinates.

Route Over Region

Limits the region in which to create diagonal stripes to the rectangular area bounded by the coordinates you specify.

Top Left Offset For Diag45

Specifies the top left offset in microns for 45-degree diagonal stripes.

Set Width/Spacing/Set-To-Set Distance Values As Projected

Uses the specified width, spacing, and set to set distance values provided by the software.

Add Stripes Over Rows Only

If selected, diagonal stripes can be created only over rows within the boundary. If deselected, stripes are created over the boundary.

Default: Off

Related Text Commands

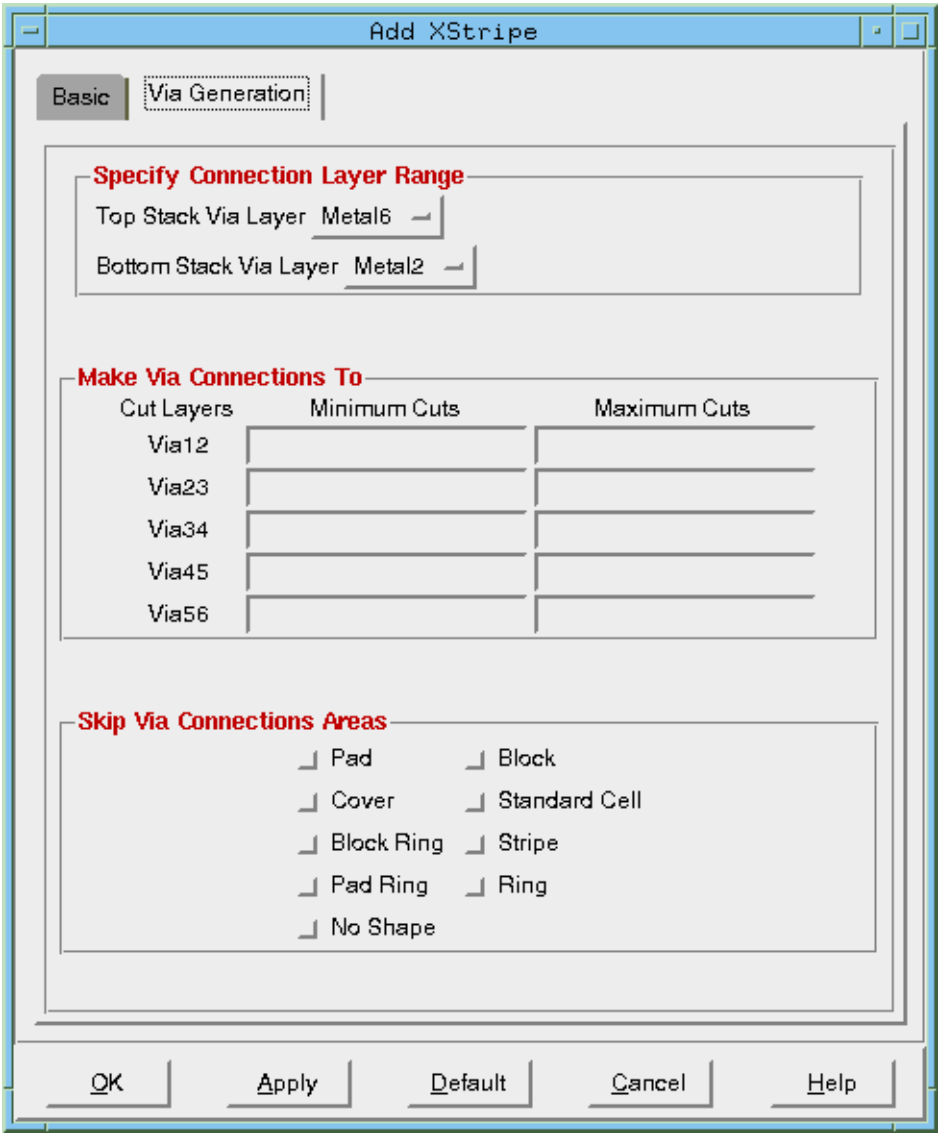
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addXStripe`

Add XStripes – Via Generation

Use the *Via Generation* page of the Add XStripe form to limit the area in which diagonal stripes can be created as well as specify the behavior of diagonal stripes when they are near rings, obstructions, rows, or design boundaries.

➤ To open the *Via Generation* page of the Add XStripe form, choose *Power – Power Planning – Add XStripes*, then click the *Via Generation* tab.



Add XStripes – Via Generation Fields and Options

Top stack via layer
Specifies the highest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Bottom stack via layer
Specifies the lowest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Make Via Connections To

Specifies the minimum and maximum cuts allowed for the specified via cut layers.

Skip Via Connections Areas

Disables the via generation software from making via connections to the following types of wires or pins that you select:

- *Pad*
- *Cover*
- *Block Ring*
- *Pad Ring*
- *No Shape*
- *Block*
- *Standard Cell*
- *Stripe*
- *Ring*

Related Text Commands

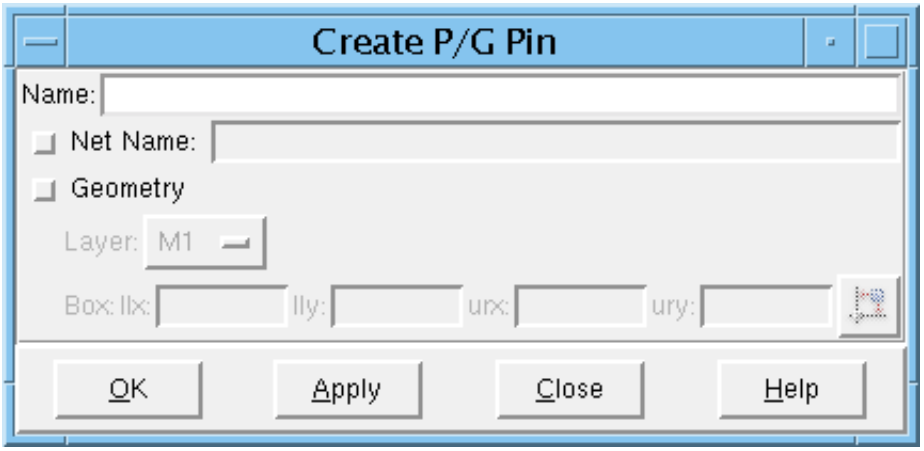
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `addXStripe`

Create P/G Pin

Use the *Create P/G Pin* form to create a power/ground pin as per the specified coordinates of the physical shape.

➤ To open the *Create P/G Pin* form, choose *Power – Power Planning – Create P/G Pin*.



Create P/G Pin Fields and Options

Name	Specifies the name of the power/ground pin.
Net Name	Specifies the name of the net to which the power/ground pin will be attached.
Geometry	Specifies the geometry of the physical pin: the layer on which to create it, and the location.
Layer	Specifies the layer on which the power/ground pin will be created. The layer id should be a numerical number, ranging from `1` to `7`.
Box	Specifies the location of the P/G pin. Specify the coordinates or select them in the artwork window.
	llx — Specifies the lower-left x coordinate of the power/ground pin.
	lly — Specifies the lower-left y coordinate of the power/ground pin.

urx	Specifies the upper-right x coordinate of the power/ground pin.
ury	Specifies the upper-right y coordinate of the power/ground pin.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `createPGPin`

Edit Power Vias

Use the Edit Power Vias form to add, modify, and delete power vias.

The Edit Power Vias form contains the following two pages:

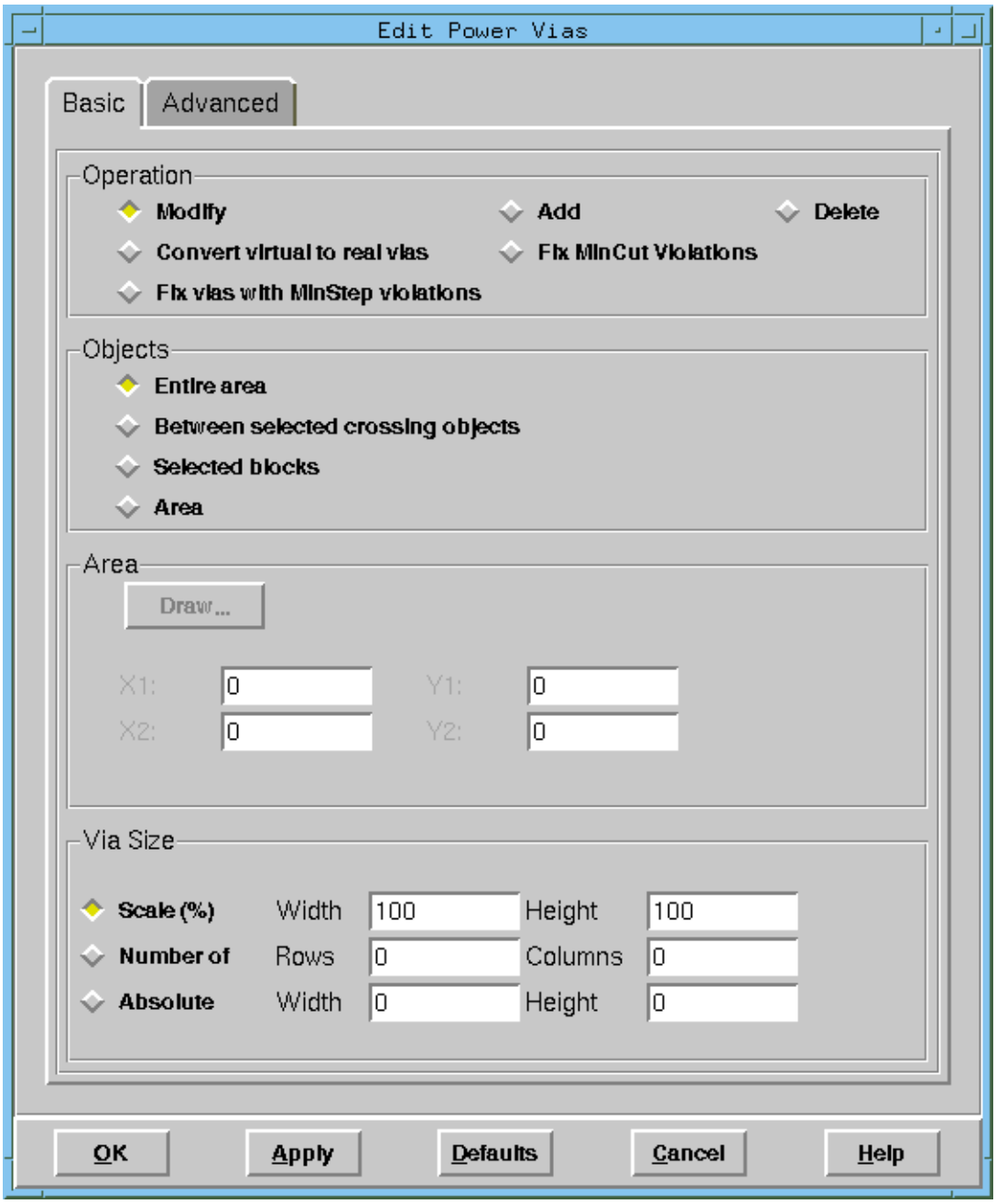
- Edit Power Vias – Basic on page 883
- Edit Power Vias – Advanced on page 887

Edit Power Vias – Basic

Use the *Basic* page of the Edit Power Vias form to add power vias to the design or to perform one of the following actions on existing power vias:

- Modify
- Delete
- Convert virtual vias created by the Automatic Power Planning (APP) software to real vias
- Fix vias that are not in compliance with the LEF `MINIMUMCUT` rule

➤ To open the *Basic* page of the Edit Power Vias form, choose *Power — Power Planning — Edit Power Via*, then click the *Basic* tab.



Edit Power Vias – Basic Fields and Options

Operation

The action that will be performed by the software. Select one of the following actions:

Modify Changes the size of existing vias.

Add Generates new vias.

Delete Removes existing vias.

Convert virtual to real vias

Changes virtual vias created by the power planning software into real vias.

Fix MinCut Violations

Updates existing vias that violate the LEF `MINIMUMCUT` rule.

Fix vias with MinStep violations

Updates existing vias that violate the LEF `MINIMUMSTEP` rule.

Objects

The vias that will be affected by the selected operation. Select one of the following options:

Entire Area Adds, modifies, or deletes all power vias in the design.

Between selected crossing objects

Adds, modifies, or deletes power vias between the selected objects and wires crossing those objects.

Selected Blocks

Adds, modifies, or deletes power vias between the selected blocks and wires crossing those blocks.

Area Adds, modifies, or deletes power vias within the coordinates specified in the *Area* panel.

Area

If you select *Area* in the *Objects* panel, you can either manually enter the coordinates for the area or use the mouse to automatically populate the coordinate fields.

	Draw	(Optional) click *Draw* and then drag the cursor in the design display area to populate the coordinates.
Via Size	The size of the via to be added or the size to which an existing via is to be modified to. **Note:** This section is only available if you select *Add* or *Modify* in the *Operation* panel. Select one of the following options:	
	Scale (%)	The percentage values by which to scale the via dimensions. Use the text entry fields to specify values for both width and height.
	Number of	The number of cuts per row and per column.
	Absolute	The width and height of the added or modified vias.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `editPowerVia`

Related Topics

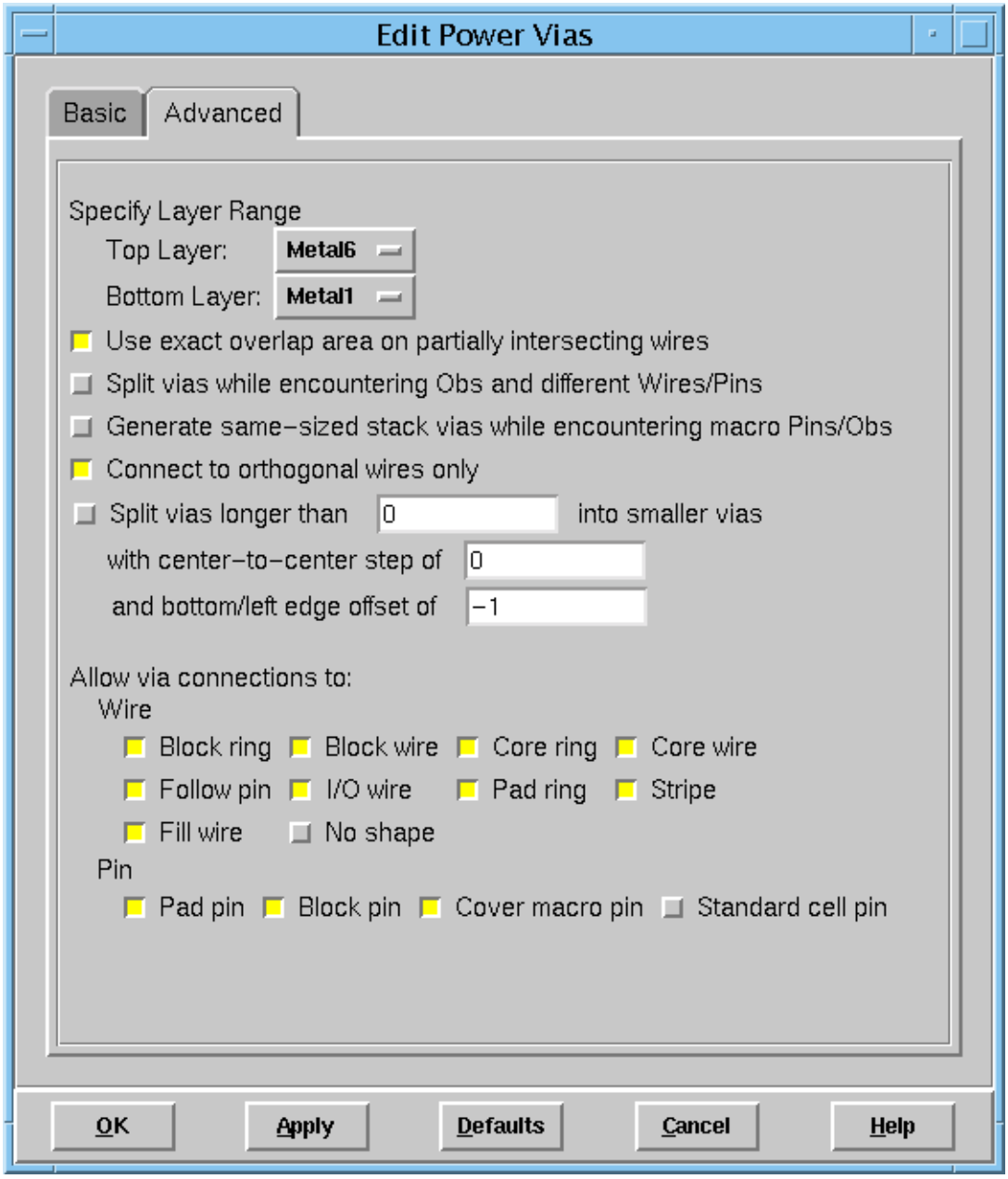
For information on the following topics, see “Power Planning and Routing” in the *Encounter User Guide*.

- Fixing LEF MINIMUMCUT Violations
- Fixing LEF Minimum Spacing Violations

Edit Power Vias – Advanced

Use the Advanced page of the Edit Power Vias form to specify a range of layers on which vias can be created, as well as the types of wires to which vias can connect.

➤ To open the Advanced page of the Edit Power Vias form, choose *Power — Power Planning — Edit Power Via*, then click the *Advanced* tab.



Edit Power Vias – Advanced Fields and Options

Top layer

The highest metal layer to which vias can connect. This limits the generation of vias to targets in the specified range.

Bottom layer

The lowest metal layer to which vias can connect. This limits the generation of vias to targets in the specified range.

Use exact overlap area on partially intersecting wires

If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.

Note: This option does not apply when both of the objects at the crossover are rings or stripes, or at the crossover of a ring and stripe. In these cases, the software always generates full-size vias.

Split vias while encountering Obs and different Wires/Pins

If selected, two or more partial vias can be created at the crossover between a stripe and any target (pin or wire) if an obstruction (macro obstruction; wire or pin on a different net) prevents the creation of a full-size via. This may be useful, for example, if several metal obstructions partially obstruct the area where a full-size via would normally be placed. This option permits the creation of partial vias that would not violate the process rules, in the open areas. If deselected, one via of the maximum size will be created.

Default: Off

Generate same-sized stack vias while encountering macro Pins/Obs

If selected, the software always generates same-sized stacked vias. If deselected, the software trims the vias as needed to meet the DRC rules.

Connect to orthogonal wires only

Creates vias *only* for orthogonal wires and pin intersections.

Default: On

Split vias longer than X *into smaller vias with center-to-center step of* Y *and bottom/left edge offset of* Z

Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers).

Default: Off

Allow via connections to

Select the types of wires or pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made. By default, vias can connect to each of the following types of wire or pin:

- *Block ring*
- *Block wire*
- *Core ring*
- *Core wire*
- *Follow pin*
- *I/O wire*
- *Pad ring*
- *Stripe*
- *Fill wire*
- *No shape*
- *Pad pin*
- *Block pin*
- *Cover macro pin*
- *Standard cell pin*

Note: Vias can only connect to wires labeled as *No shape* if you select this option.

Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `editPowerVia`

Repair Power Stripes

Once your design has power stripes, you can regenerate power stripes at the same locations in your design when you move blocks or make other changes to the floorplan. You should regenerate stripes whenever you move a hard block because connections to blockages and pins inside the block might violate design rules governing spacing or shorts.

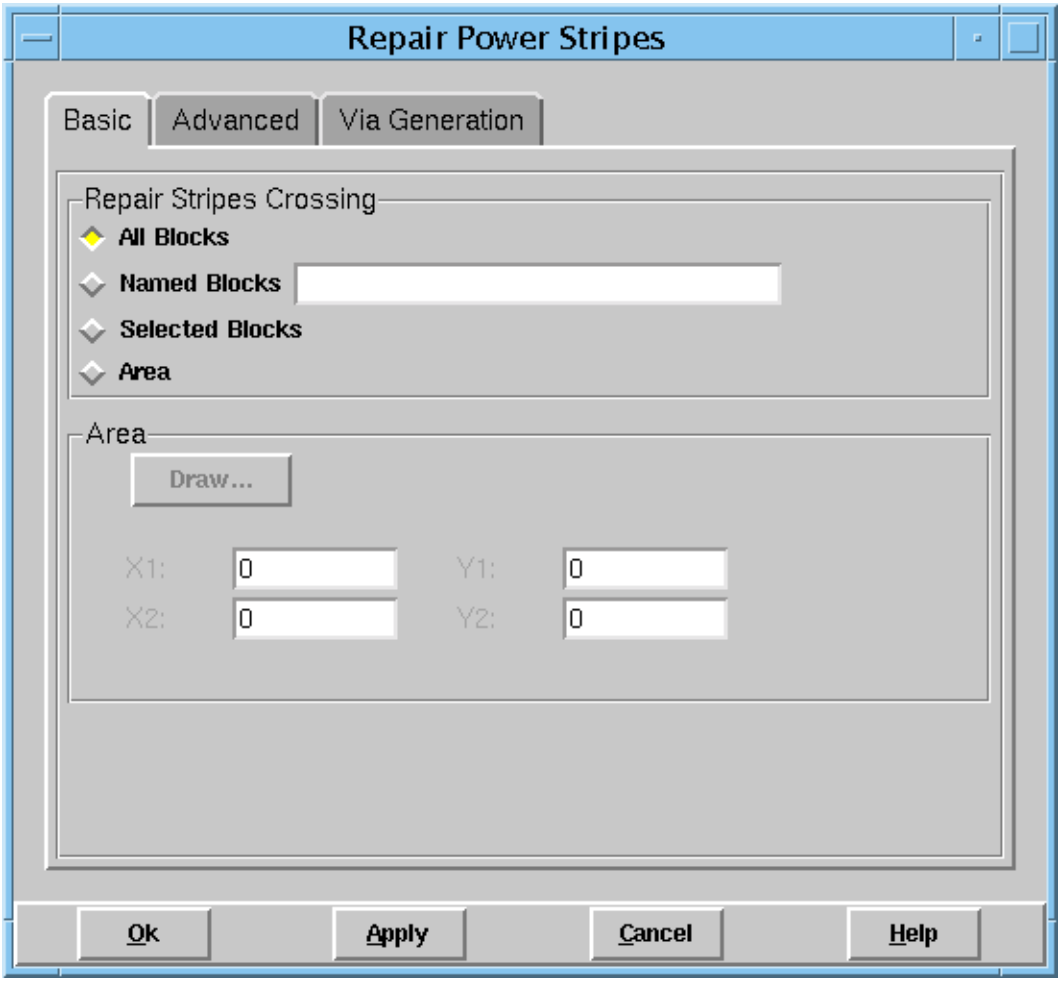
The Repair Power Stripes form contains the following three pages:

- Repair Power Stripes – Basic on page 891
- Repair Power Stripes – Advanced on page 893
- Repair Power Stripes – Via Generation on page 895

Repair Power Stripes – Basic

Use the *Basic* page on the Repair Power Stripes form to specify the types of stripes to be repaired as well as the area in which repairs are to be made.

➤ To open the *Basic* page of the Repair Power Stripes form, choose *Power – Power Planning – Repair Power Stripes*, then click the *Basic* tab.



Repair Power Stripes – Basic Fields and Options

Repair Stripes Crossing

The location of the stripes to be repaired. Select one of the following options:

All Blocks	Repairs stripes crossing all blocks in your design.
Named Blocks	Repairs violations on stripes crossing the blocks you specify. If you specify multiple blocks, separate the block names with a space.
Selected Blocks	Repairs violations on blocks you select in the design display area.
Area	Repairs violations within the specified coordinates.
Draw	Click this button, then drag the mouse within the design display area. The coordinates are automatically populated.

Related Text Commands

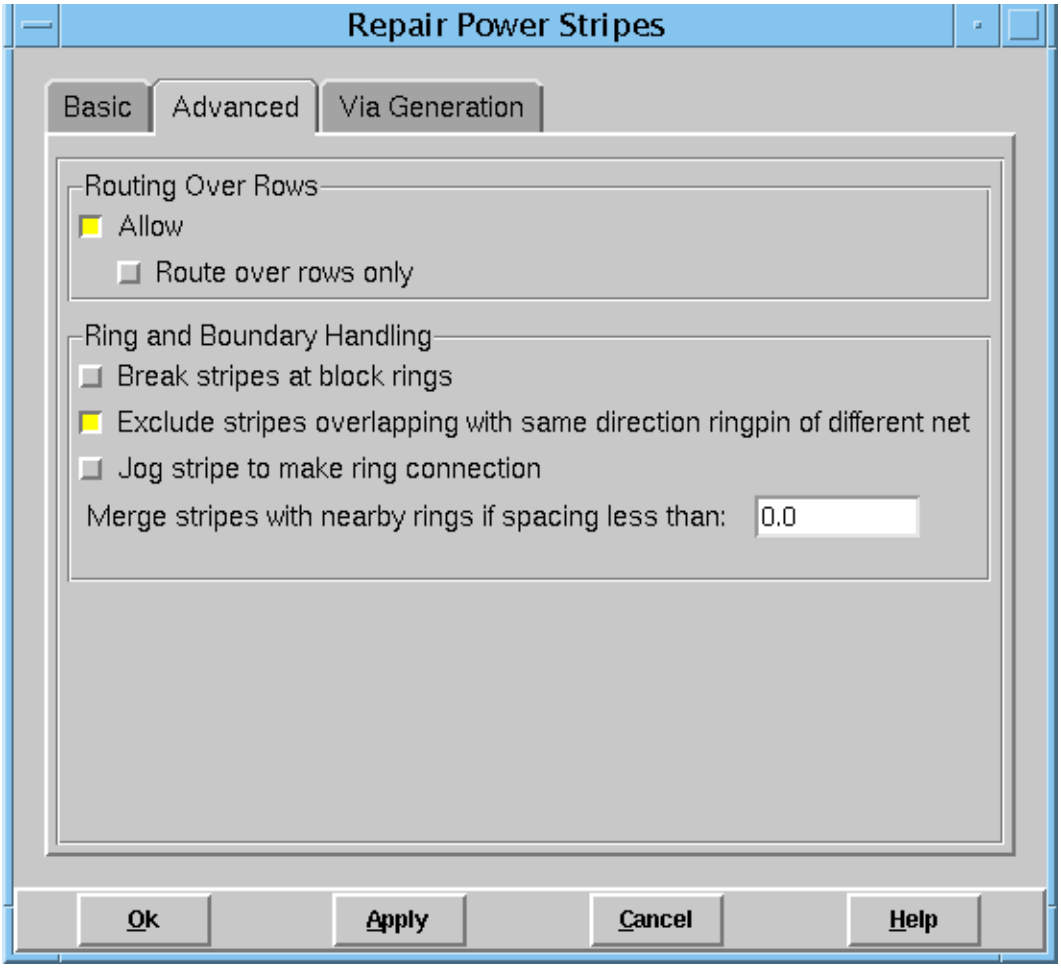
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `repairPowerWire`

Repair Power Stripes – Advanced

Use the Advanced page of the Repair Power Stripes form to specify whether stripes are to be repaired when they are near rings or over rows, as well as when merging should occur.

➤ To open the Advanced page of the Repair Power Stripes form, choose *Power – Power Planning – Repair Power Stripes*, then click the *Advanced* tab.



Repair Power Stripes – Advanced Fields and Options

Routing Over Rows: Allow

If selected, stripes can be repaired over rows. If deselected, stripes are not repaired over rows.

Route over rows only

If selected, stripes can be created only over rows within the boundary specified in the Add Stripes form. If deselected, stripes can be created over rows outside the boundary.

Break stripes at block rings

If selected, stripes break at block rings based on obstruction layers inside the block. If block rings are encountered and there are no obstructions within the block of the same layer as the stripe, the stripes break and connect to the block rings.

Exclude stripes overlapping with same direction ringpins

If selected, stripes are prevented from overlapping with same direction ring pins of a different net. This is the default. If deselected, stripes can overlap with same direction ring pins of a different net. I

Jog stripe to make ring connection

If selected, stripes can jog in order to connect with a ring. If deselected, stripes do not jog to make these connections. This is the default.

Merge stripes with nearby rings if spacing less than

Specify the threshold, in microns, for merging stripes. If the threshold spacing between the stripe and ring is smaller than the value specified, the stripe jogs to connect to the nearby ring. The default value of this field is the same as the value in the *Spacing* field on the *Basic* page of this form.

Related Text Commands

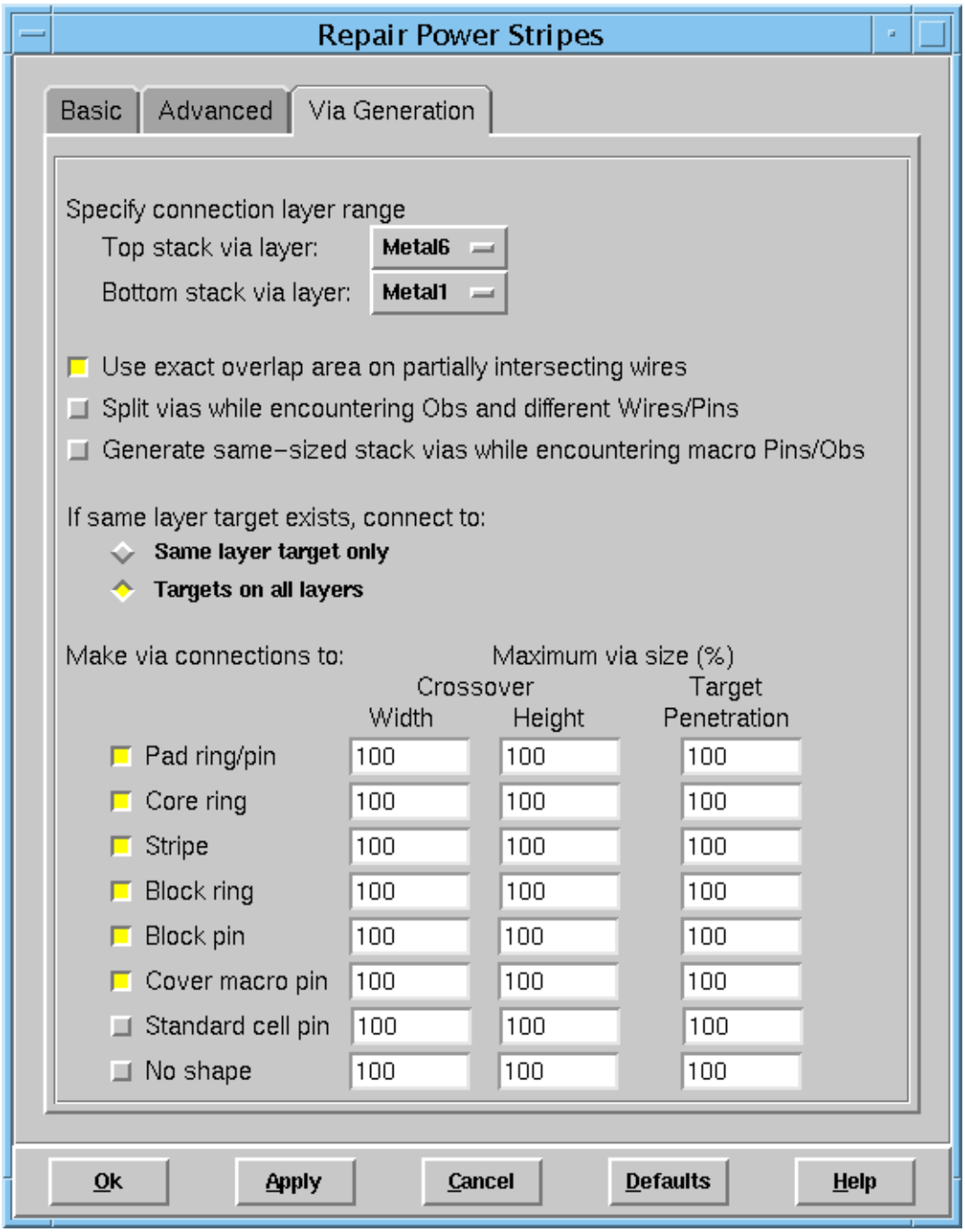
For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `repairPowerWire`

Repair Power Stripes – Via Generation

Use the *Via Generation* tab on the Repair Power Stripes form to specify how vias connect to repaired power stripes.

➤ To open the Via Generation page of the Repair Power Stripes form, choose *Power – Power Planning – Repair Power Stripes*, then click the *Via Generation* tab.



Repair Power Stripes – Via Generation Fields and Options

Top stack via layer
The highest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Bottom stack via layer
The lowest metal layer to which stacked vias can connect. This limits the generation of vias to targets in the specified range.

Use exact overlap area on partially intersecting wires

If selected, the software can generate partial vias of the exact size of the overlap area. If deselected, the software always generates full-size vias.

Note: This option does not apply when both of the objects at the crossover are rings or stripes, or at the crossover of a ring and stripe. In these cases, the software always generates full-size vias.

Split vias while encountering Obs and different Wires/Pins

If selected, two or more partial vias can be created at the crossover between a stripe and any target (pin or wire) if an obstruction (macro obstruction; wire or pin on a different net) prevents the creation of a full-size via. This may be useful, for example, if several metal obstructions partially obstruct the area where a full-size via would normally be placed. This option permits the creation of partial vias that would not violate the process rules, in the open areas. If deselected, one via of the maximum size will be created.

Default: Off

Generate same-sized stack vias while encountering macro Pins/Obs

If selected, the software always generates same-sized stacked vias. If deselected, the software trims the vias as needed to meet the DRC rules.

If same layer target exists, connect to

Same layer target only
Prevents the creation of vias to connect to other layers when a target exists on the same layer. This only applies when targets of multiple layers of the same net are stacked on top of one another. If a target does not exist on the same layer, vias are generated to connect to targets on other layers.

Targets on all layers Allows the creation of vias to connect to other layers when a target exists on the same layer.

Make via connection to Select the types of wires or pins for which via connections are permitted. Deselect the types of wires or pins to which via connections are not to be made. By default, vias can connect to each of the following types of wire or pin:

- *Pad ring/pin*
- *Core ring*
- *Stripe*
- *Block ring*
- *Block pin*
- *Cover macro pin*
- *Standard cell pin*
- *No Shape*

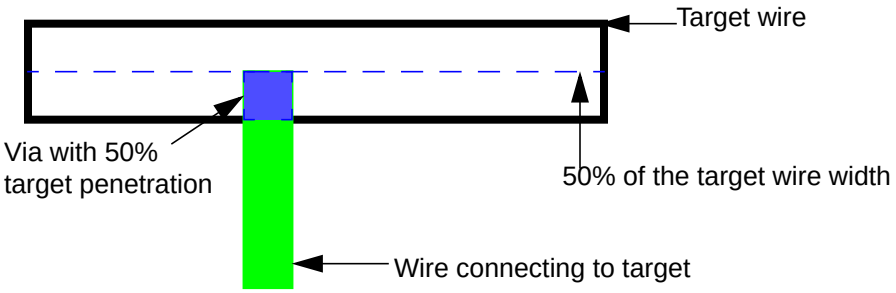
Note: Vias can only connect to wires labeled as *No shape* if you select this option.

Crossover Width The maximum width of a crossover via, specified as a percentage of a full-size via.

Crossover Height The maximum height of a crossover via, specified as a percentage of a full-size via.

Target penetration (%) Specifies a smaller size for vias connecting to targets of a particular wire or pin type.

By default, if a wire or pin is a target to which a via can be connected, the via is a full-sized. If you want the via to be smaller, you can specify a value in this field for each wire type. Only a single dimension of the via will be scaled. For example, if you specify a value of 50, the via will be full-sized in one dimension (the width of the wire that crosses the ring), but only half the width in the other dimension (the width of the target wire).



Related Text Commands

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `repairPowerWire`

Optimize Power Plan

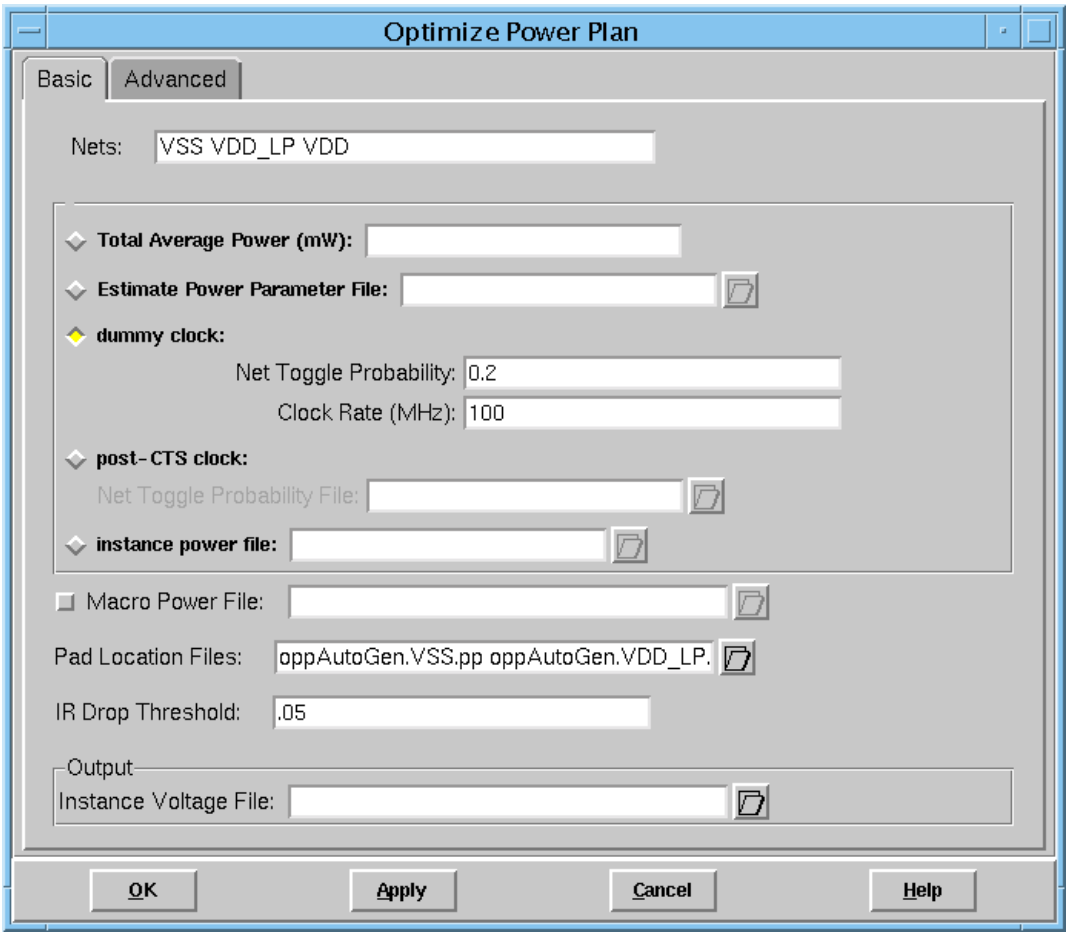
Use the Optimize Power Plan form to initiate an automatic “what-if” IR drop and electromigration analysis feedback loop for power planning.

The Optimize Power Plan form contains the following pages:

- Optimize Power Plan – Basic
- Optimize Power Plan – Advanced

Optimize Power Plan – Basic

➤ To open the Optimize Power Plan – *Basic* page, choose *Power – Power Planning – Optimize Power Plan*, then click *Basic*.



Optimize Power Plan – Basic Fields and Options

Nets
The power net name or list of names to be analyzed.

Total Average Power (mW)
The total average power for the chip or the block.

If you specify a value in the field, the software runs area-based rail analysis. You do not need an instance power file to run in this mode.

Estimate Power Parameter File

The name of a file that contains parameters used by the software to estimate power consumption. This provides a more accurate estimate than using a *Total Average Power* value. For more information, see Running Power Analysis in Simple Estimate Mode in the "Power Analysis" chapter of the *Encounter User Guide*.

dummy clock

Performs power analysis on all nets, including clock nets, toggling at a specified clock rate and a specified toggle probability for all nets.

Note: If you choose this option, you must also specify values for *Net Toggle Probability* and *Clock Rate (MHz)*.

Net Toggle Probability

Percentage of nets toggling in the entire design, including all the clock nets.

Default: `0.2`.

Clock Rate (MHz)

The rate at which the net toggles, in megahertz.

Default: `100`

post-CTS clock

Performs power analysis with clock nets at a set clock rate (in megahertz) for each clock domain, and a set toggle probability (in percent) for the clock's data paths. This means that all the nets on a clock path toggle at the clock rate, but only a percentage of the clock's data paths toggle in each clock cycle.

For example, if the *Clock Rate* value is `300` and the *net toggle probability* value is `0.2` (20%), then the clock path nets toggle at 300 MHz, and only 20 percent of the clock's data paths toggle in each cycle. Nets not belonging to a clock domain do not toggle.

Note: If you choose this option, you must also specify a value in the *Net Toggle Probability File* field.

	Net Toggle Probability File — The clock information file created in the Edit Net Toggle Probability form. **Note:** If your clock information is incomplete, you can control the toggle probability for unclocked instances by specifying a value of `_unclocked_` in the *Clock Name* field of the Edit Net Toggle Probability form.
instance power file	Specifies the output instance power file (`filename.power`).
Macro Power File	Specifies a macro power file (`filename.power`). The macro power file contains data about macro cell power consumption. Values for instances that appear in the macro power file take precedence over any values associated with these instances in the following files or calculation methods: ■ *Total Average Power (mW)* ■ *Estimate Power Parameter File* ■ *dummy clock* ■ *post-CTS clock* ■ *instance power file*
Pad Location Files	One or more pad location files. You must specify a separate pad location file for each net in the design.
IR Drop Threshold	Specifies the maximum IR drop value allowed for the design (in volts).
Instance Voltage File	The name of the Instance Voltage File.

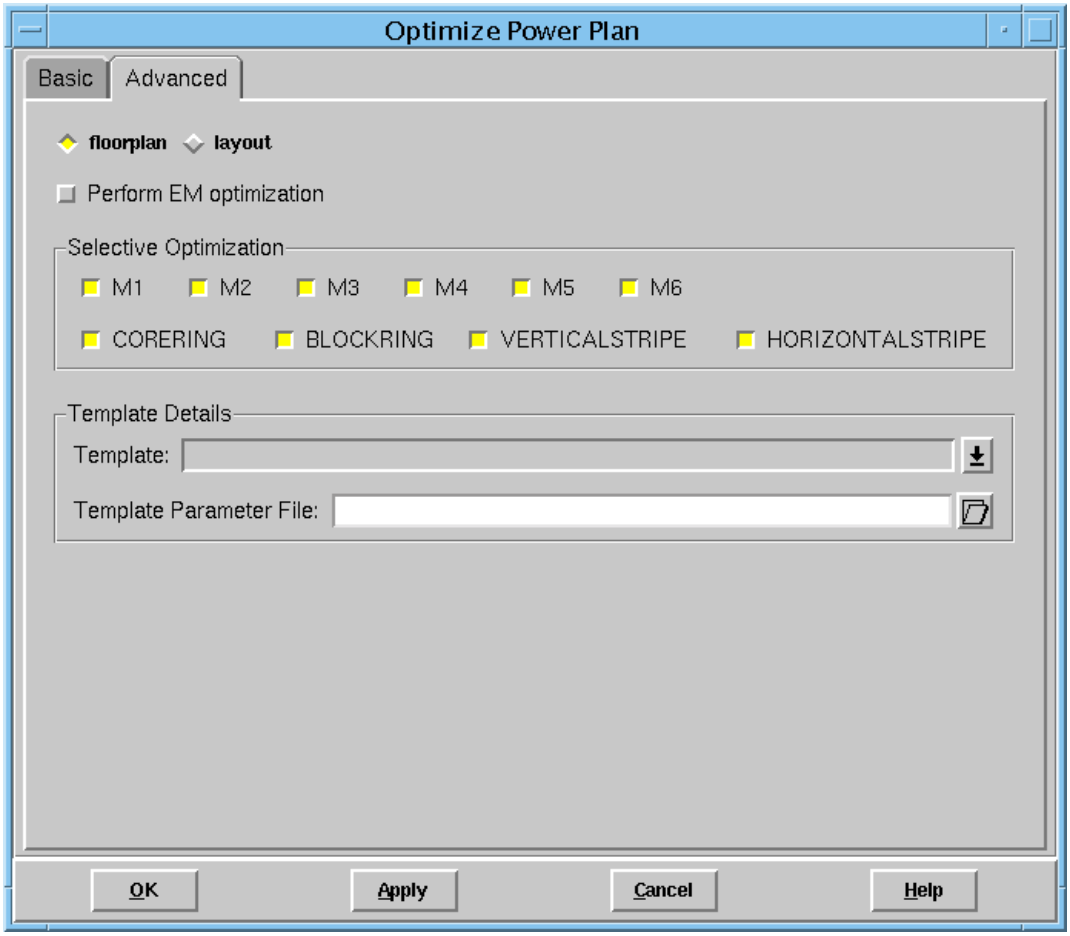
Related Text Command

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

■ `optimizePowerPlan`

Optimize Power Plan – Advanced

➤ To open the Optimize Power Plan – *Basic* page, choose *Power – Power Planning – Optimize Power Plan*, then click *Basic*.



Optimize Power Plan – Advance Fields and Options

floorplan

Runs power analysis early in the floorplanning cycle.

You must perform the following floorplanning steps before running power analysis:

- Create power rings around the core design area.
- Create power stripes over the core design area in both the horizontal and vertical directions.

Power is only analyzed for the instances placed inside the core design area. The power analysis software creates the power rail to connect all the standard cells. The default width of the rail is one-eighth of the height of a standard cell, which can be overwritten using the following Tcl variable:

```
set dbgCellRailWidth microns
```

Note: Power analysis honors followpins generated by SRoute in layout mode only, not in floorplan mode. Power and ground rails and vias generated in floorplan mode are temporary and do not adhere to technology rules, so they should not be used in the design. Power analysis does not create physical rails or vias.

layout

Runs power analysis with the power structures completely designed, when the power stripes actually connect to the power pins of all the blocks and I/O pad instances.

The power design can be done within Encounter using the power planning and SRoute software, or loaded in from the TDF or DEF file.

Perform EM optimization

Performs electromigration optimization concurrently with IR-based optimization.

Default: This option is turned off by default.

Selective Optimization

Selectively optimizes only those items checked.

For example, if you select *M6* and *CORERING*, only core rings on metal layer 6 will be optimized.

Choose from among the following:

- *M1*
- *M2*
- *M3*
- *M4*
- *M5*
- *M6*
- *CORERING*
- *BLOCKRING*
- *VERTICALSTRIPE*
- *HORIZONTALSTRIPE*

Template

Specifies the template used during the synthesize power plan process.

Template Parameter File

Specifies the template parameter file (`.tParam`) created during the synthesize power plan process.

Related Text Command

For information on the following command, see “Power Planning Commands” in the *Encounter Text Command Reference*.

- `optimizePowerPlan`

Power Analysis

The Power Analysis submenu contains the following items:

- Read Activity File

  Opens the Read Activity File form, which contains the following items:

  - Read Activity File – VCD form
  - Read Activity File – TCF form
  - Read Activity File – SAF form

- Set Cell/Instance Power

  Opens the Set Cell/Instance Power form.

- Set Default Switching Activity

  Opens the Set Default Switching Activity form, which contains the following items:

  - Set Default Switching Activity – Global
  - Set Default Switching Activity – Specific

- Set Switching Activity

  Opens the Set Switching Activity form.

- Set Power Analysis Mode

  Opens the Set Power Analysis Mode form.

- Report Power

  Opens the Report Power – Report Power form.

- Write TCF

  Opens the Write TCF form.

- Debug Power

  Opens the Debug Power form.

Read Activity File

The Read Activity File form enables you to read the value change dump (VCD) file, toggle count format (TCF) file, or switching activity format (SAF) file to specify the net activity of the design. The power analysis software uses the net activity information in the activity file as the basis for the power consumption calculation.

Note: To use this feature, you must have a separate license.

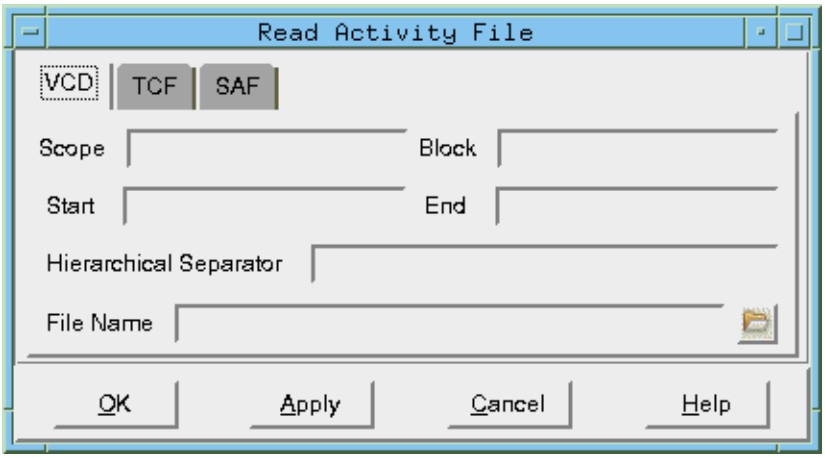
The Read Activity File form contains the following three pages:

- *Read Activity File – VCD*
- *Read Activity File – TCF*
- *Read Activity File – SAF*

Read Activity File – VCD

Use the *VCD* page of the Read Activity File form to read the value change dump (VCD) file to specify the net activity of the design. The power analysis software uses the net activity information in the activity file as the basis for the power consumption calculation.

➤ To open the *VCD* page of the Read Activity File form, choose *Power – Power Analysis – Read Activity File*, then click the *VCD* tab.



Read Activity File – VCD Fields and Options

Scope	Specifies the name of the module within the VCD file associated with the block or other part of the design that you want to analyze. It must include the hierarchical path. Scope refers only to the hierarchy within the VCD file itself, not to the hierarchy in the design.
Block	Specifies the name of the block to map a sub-block VCD file with a block instance at the top-level. Provides the ability to support multiple VCD files based on the block instance names. The specified `module` refers to the hierarchy in the design.

Start	Specifies the start time of the range from the VCD file(s) for the block, level of hierarchy, or other part of the design that you want to analyze. Units in seconds (`s`), milliseconds (`ms`), microseconds (`us`), nanoseconds (`ns`), or picoseconds (`ps`). *Default*: The time unit is defined in the first `.lib` file read during design import.
End	Specifies the end time of the range from the VCD file(s) for the block, level of hierarchy, or other part of the design that you want to analyze. Units in seconds (`s`), milliseconds (`ms`), microseconds (`us`), nanoseconds (`ns`), or picoseconds (`ps`). *Default*: The time unit is defined in the first `.lib` file read during design import.
Hierarchical Separator	Specifies the separator character in the hierarchical net names, bus names, and pin names for the block or other part of the design that you want to analyze. It must be the same as the separator character in the design netlist. *Default*: slash (`/`)
File Name	Specifies the name of the activity file in VCD format.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `readActivityFile`

Related Topics

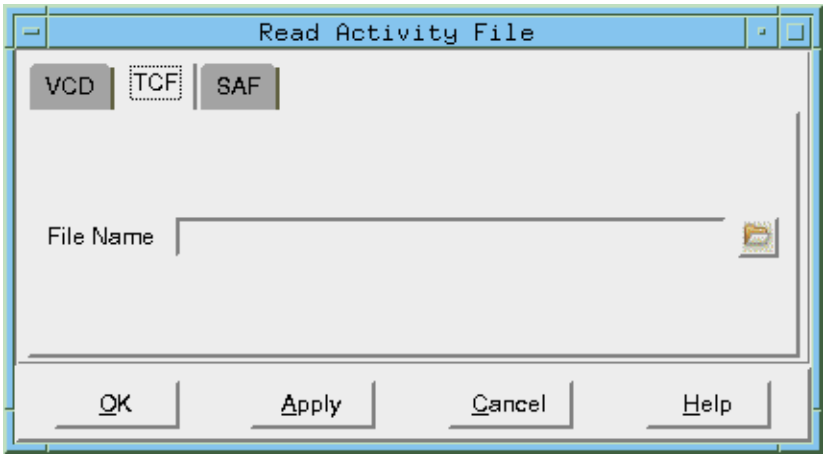
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Read Activity File – TCF

Use the *TCF* page of the Read Activity File form to read the toggle count format (TCF) file to specify the net activity of the design. The power analysis software uses the net activity information in the activity file as the basis for the power consumption calculation.

➤ To open the *TCF* page of the Read Activity File form, choose *Power – Power Analysis – Read Activity File*, then click the *TCF* tab.



Read Activity File – TCF Fields and Options

File Name	Specifies the name of the activity file in TCF format.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `readActivityFile`

Related Topics

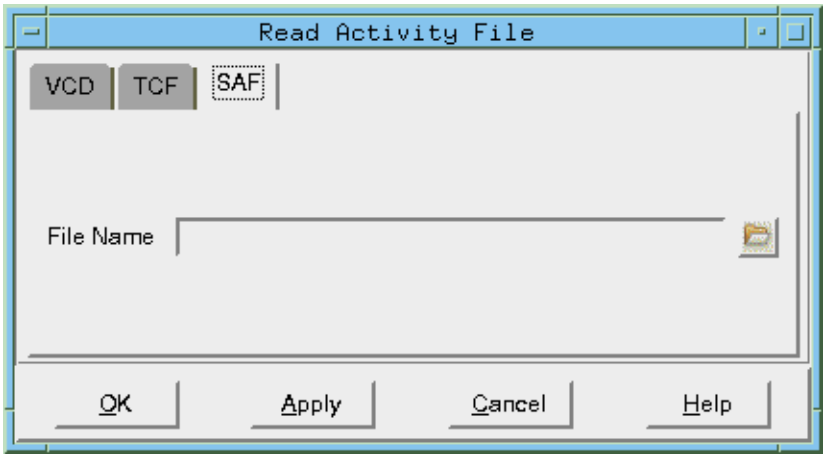
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Read Activity File – SAF

Use the *SAF* page of the Read Activity File form to read the switching activity format (SAF) file to specify the net activity of the design. The power analysis software uses the net activity information in the activity file as the basis for the power consumption calculation.

➤ To open the *SAF* page of the Read Activity File form, choose *Power – Power Analysis – Read Activity File*, then click the *SAF* tab.



Read Activity File – SAF Fields and Options

File Name	Specifies the name of the activity file in SAF format.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `readActivityFile`

Related Topics

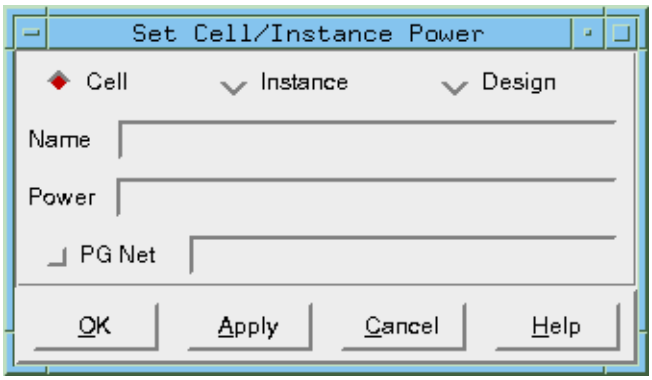
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Set Cell/Instance Power

Use the Set Cell/Instance Power form to set the instance power for a specified cell, hierarchical instance, or top-level design.

➤ To open the Set Cell/Instance Power form, choose *Power – Power Analysis – Set Cell/Instance Power*.



Set Cell/Instance Power Fields and Options

Cell	Specifies the cell or hierarchical instance (cell or leaf level) name for which to set the power.
Instance	Specifies the cell or hierarchical instance (cell or leaf level) name for which to set the power.
Design	Specifies the cell or hierarchical instance (cell or leaf level) name for which to set the power. *Default*: Sets the power for the top-level design if the `-type` parameter is not specified.
Name	Specifies the cell, hierarchical instance (cell or leaf level), or top-level design name for which to set the power.
Power	Specifies the power value assigned to a cell, instance, or top-level design. Units are in watts (`w`), milliwatts (`mw`), microwatts (`uw`), nanowatts (`nw`), or picowatts (`pw`). *Default*: milliwatts

PG Net	Specifies the name of the power net for which the power is being specified.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `setPower`

Related Topics

For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Set Default Switching Activity

The Set Default Switching Activity form enables you to specify the switching activity for all primary inputs, nets, and other devices in the design whose activity has not been previously defined through user attributes, the toggle count format (TCF) file, the value change dump (VCD) file, or the tracing of the clock network.

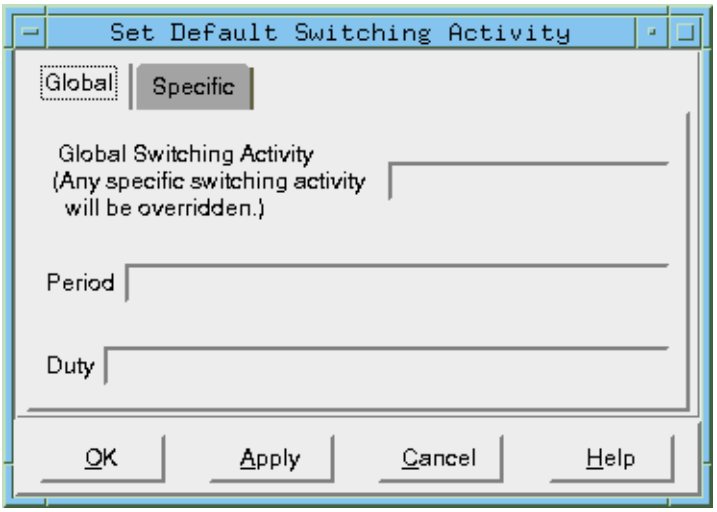
The Set Default Switching Activity form contains the following two pages:

- *Set Default Switching Activity – Global*
- *Set Default Switching Activity – Specific*

Set Default Switching Activity – Global

Use the *Global* page of the Set Default Switching Activity form to specify the average number of times that all unswitched nodes switch in a clock cycle.

➤ To open the *Global* page of the Set Default Switching Activity form, choose *Power – Power Analysis – Set Default Switching Activity*, then click the *Global* tab.



Set Default Switching Activity – Global Fields and Options

Global Switching Activity

Specifies the average number of times that all unswitched nodes switch in a clock cycle. Enter any positive number between 0 and 1. There is no default value.

Period	Specifies the period that the activity is referenced to. If not specified, the software uses the fastest clock in the design. If no clock is specified, the software generates an error and prompts you to enter one. Units in seconds (`s`), milliseconds (`ms`), microseconds (`us`), nanoseconds (`ns`), or picoseconds (`ps`). **Note:** If you enter the period as a negative number, the software reverts back to using the default frequency. *Default*: The time unit is defined in the first `.lib` file read during design import.
Duty	Specifies the duty cycle. **Note:** You must specify the *Period* when assigning a duty. *Default*: `0.5` (equivalent to a 50 percent duty cycle)

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `setDefaultSwitchingActivity`

Related Topics

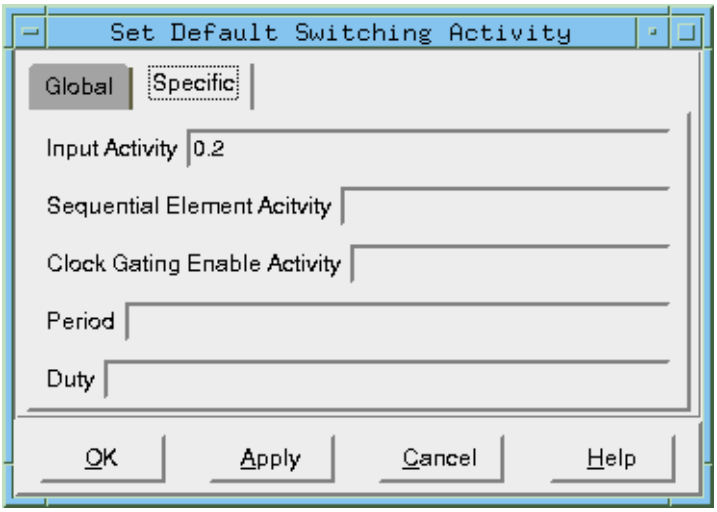
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Set Default Switching Activity – Specific

Use the *Specific* page of the Set Default Switching Activity form to specify the switching activity for all primary inputs, nets, sequential elements, clock gating, and other devices in the design whose activity has not been previously defined through user attributes, the toggle count format (TCF) file, the value change dump (VCD) file, or the tracing of the clock network.

➤ To open the *Specific* page of the Set Default Switching Activity form, choose *Power – Power Analysis – Set Default Switching Activity*, then click the *Specific* tab.



Set Default Switching Activity – Specific Fields and Options

Input Activity

Specifies the average number of times that a primary input switches in a clock cycle. Enter any positive number between 0 and 1.

Default: `0.2` (switches once every five clock cycles)

Note: If you use this option in conjunction with the *Global Switching Activity* option (*Global* tab), the global switching activity takes precedence.

Sequential Element Activity

Specifies the average number of times that a sequential element switches in a clock cycle. Enter any positive number between 0 and 1.

Clock Gating Enable Activity

Specifies the average number of times that a clock-gating cell switches in a clock cycle. Enter any positive number between 0 and 1.

Period

Specifies the period that the activity is referenced to. If not specified, the software uses the fastest clock in the design. If no clock is specified, the software generates an error and prompts you to enter one. Units in seconds (`s`), milliseconds (`ms`), microseconds (`us`), nanoseconds (`ns`), or picoseconds (`ps`).

Note: If you enter the period as a negative number, the software reverts back to using the default frequency.

Default: The time unit is defined in the first `.lib` file read during design import.

Duty

Specifies the duty cycle.

Note: You must specify the *Period* when assigning a duty cycle.

Default: `0.5` (equivalent to a 50 percent duty cycle)

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `setDefaultSwitchingActivity`

Related Topics

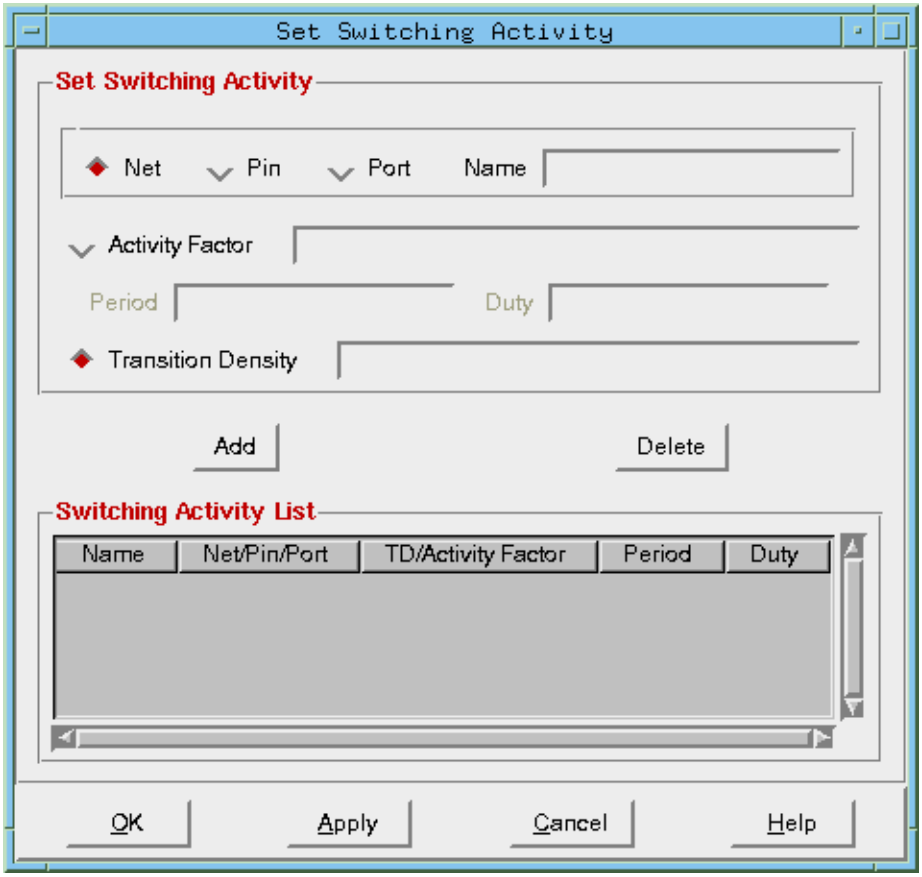
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Set Switching Activity

Use the Set Switching Activity form to specify the switching activity for a specific net, pin, or top-level port.

➤ To open the Set Switching Activity form, choose *Power – Power Analysis – Set Switching Activity*.



Set Switching Activity Fields and Options

Net	Sets the activity for a specified net(s). You must specify the name of the net(s) in the *Name* field.

Pin	Sets the activity for a specified pin(s). You must specify the name of the pin(s) in the *Name* field. Enter the pin names in the following format: `instance-name + default-hierarchy-separator + pin`.
Port	Sets the activity for a specified top-level port(s). You must specify the name of the top-level port(s) in the *Name* field. Enter the port names in the following format: `top-level-port`.
Name	Specifies the name of the net(s), pin(s), or top-level port(s). The *Name* field accepts wildcards (`*`).
Activity Factor	Specifies the average number of times that a net, pin, or top-level port switches in a clock cycle. Enter any positive number between 0 and 1. There is no default value. For example, an activity factor of 0.2 switches once every five clock cycles.
Period	Specifies the period that the activity is referenced to. If not specified, a default frequency is used. If you specify a negative number, the software uses the default frequency. Units are in seconds (`s`), milliseconds (`ms`), microseconds (`us`), nanoseconds (`ns`), or picoseconds (`ps`). **Note:** If you specify the *Period* in conjunction with the *Transition Density*, the software issues a warning and the *Period* is ignored. *Default*: The time unit is defined in the first `.lib` file read during design import. If the time unit is not defined, the software uses the *Period* specified in the Set Default Switching Activity form.
Duty	Specifies the duty cycle. **Note:** You must specify the *Period* when assigning a duty cycle. *Default*: If you do not specify a duty cycle, the software uses the duty cycle specified in the Set Default Switching Activity form.

Transition Density

Specifies the transition density for a specific net, pin, or top-level port. The transition density specifies the number of transitions per second. Enter any positive number between 0 and 1. There is no default value.

Note: If you specify the `-density` parameter in conjunction with the `-period` parameter, the software issues a warning and the `-period` parameter is ignored.

Switching Activity List

Lists all nets, pins, and top-level ports and their assigned transition density, activity factor, period, and duty cycle.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `setSwitchingActivity`

Related Topics

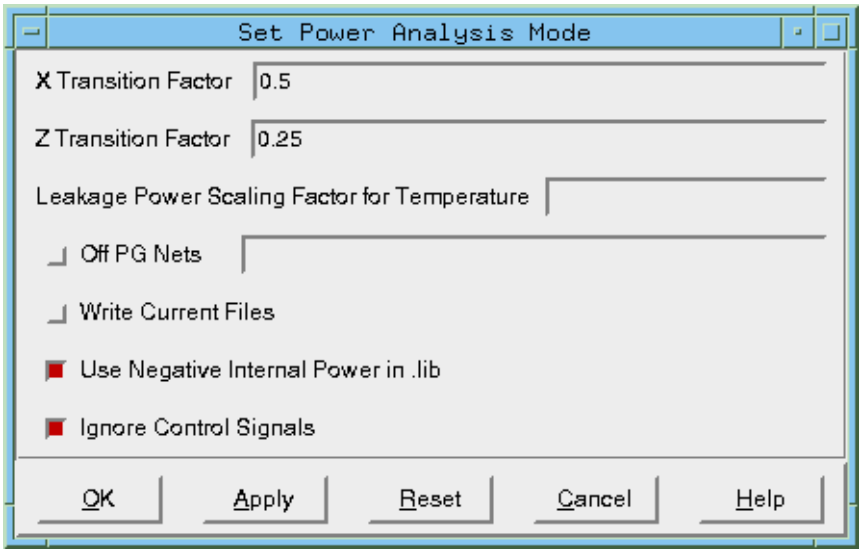
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Set Power Analysis Mode

Use the Set Power Analysis Mode form to set the power analysis mode.

➤ To open the Set Power Analysis Mode form, choose *Power – Power Analysis – Set Power Analysis Mode*.



Set Power Analysis Mode Fields and Options

X Transition Factor

Specifies how to treat the transitions to and from the X state. The transitions to and from the X state are treated as full transitions multiplied by the specified factor.

Default: `0.5`

Z Transition Factor

Specifies how to treat the transitions to and from the Z state. The transitions to and from the Z state are treated as full transitions multiplied by the specified factor.

Default: `.25`

Leakage Power Scaling Factor for Temperature

Performs a linear scaling of the leakage power for temperature in all libraries. This replaces the k-factor for temperature in the `.lib` file. For process and voltage, the scaling will continue to be based on the corresponding k-factors in the `.lib` file.
A *`value`* of 0.8 scales the leakage power in the library to 80 percent. A value of 1.2 scales the leakage power in the library to 120 percent.

Off PG Nets

Specifies which power and ground nets to turn off. The power and ground nets can contain instance hierarchy, if appropriate. The software takes this data into account when analyzing which power switches are turned off.

Note: A net is turned off if all connecting power switches are turned off by control signals. When a net is off, all instances connected to the net will only contribute leakage current to the connecting nets.

Write Current Files

Specifies whether to write out the current data (static UTI) files. When selected, the software writes out the static UTI files.

Use Negative Internal Power in .lib

Specifies whether to use the negative internal power from the `.lib` files during analysis. When deselected, the negative power is treated as zero.
Default: On

Ignore Control Signals

Ignores all control signals.
Default: On

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `setPowerAnalysisMode`

Related Topics

For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Report Power

The Report Power form enables you to report global and specific instance power, clock network power, clock domain power, and net switching power. It also reports the power for power domains and specific power nets.

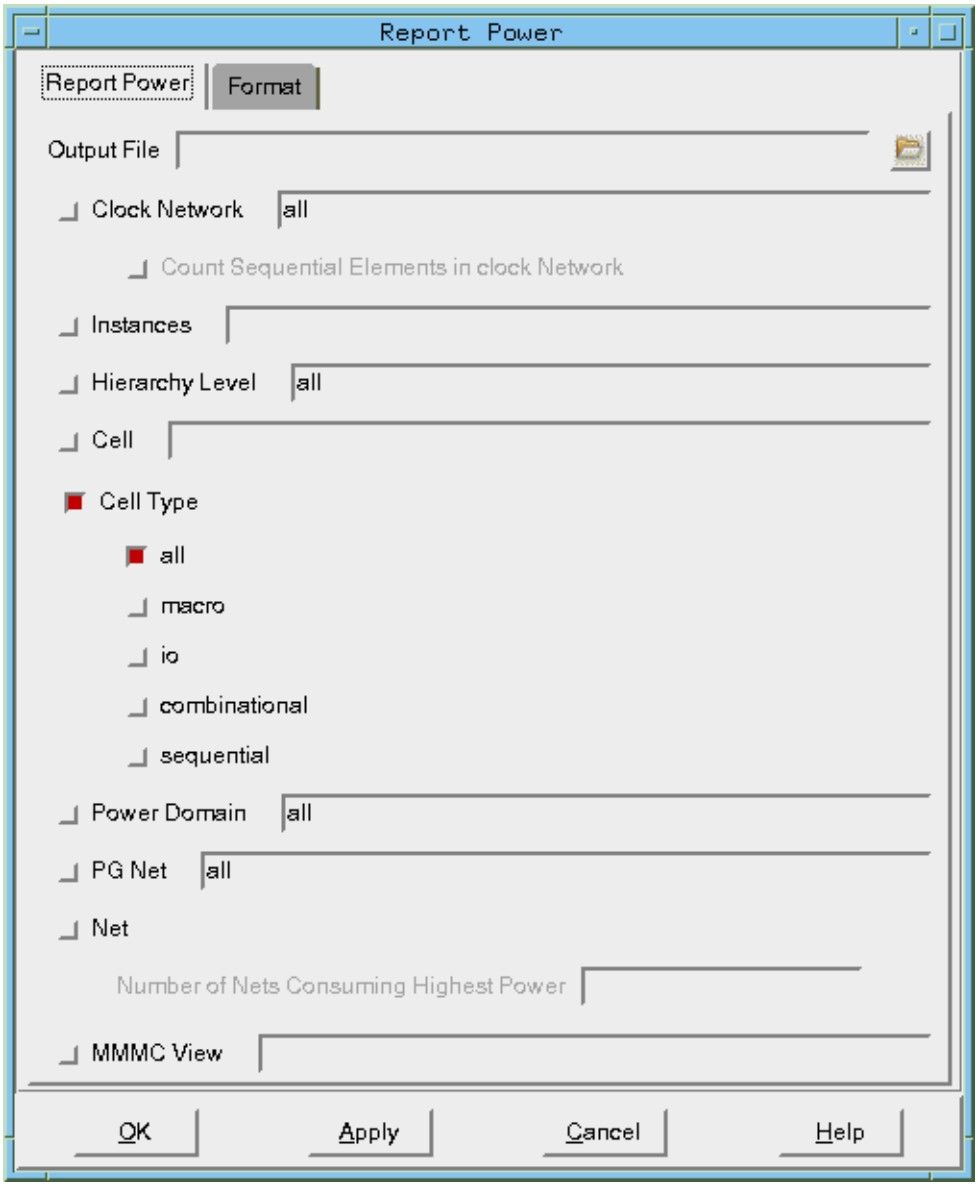
The Report Power form contains the following two pages:

- *Report Power – Report Power*
- *Report Power – Format*

Report Power – Report Power

Use the *Report Power* page of the Report Power form to report on the amount of power consumed in the design.

➤ To open the *Report Power* page of the Report Power form, choose *Power – Power Analysis – Report Power*, then click the *Report Power* tab.



Report Power Fields and Options

Output File

Specifies the name of the report file in which power analysis output information is written. You can include the directory name.

Note: If you do not specify a report file, Encounter directs the power report to the Encounter command line and no power report is written to file.

Clock Network

Specifies the clock nets whose instances are included in the power report. The power report provides the amount of power consumed by each instance connected to each clock net (excludes the data network). It reports only the instances that are part of the clock net.

Default: `all`

Count Sequential Elements in Clock Network

Specifies whether to include leaf flip-flop power in the clock network power report.

Note: When deselected, the leaf flip-flop power is not included in the clock network power report.

Instances

Specifies the instances to include in the power report.
The power report provides the amount of power consumed by a specified list of hierarchical or leaf-level instances. This field accepts wildcards (`*`) for leaf-level instances only.

Hierarchical Level

Specifies the hierarchy level that is included in the power report. You can specify the hierarchy level as a number that corresponds to a specific hierarchy level in the design.
A hierarch level of `0` specifies the top level.

Default: `all`

Cell

Specifies the cells to include in the power report.
This field accepts wildcards (`*`).

Cell Type

Specifies the cell type to include in the power report.

Default: `all`

all	Includes all cell types in the power report.
macro	Includes all macro cells in the power report.
io	Includes all I/O cells in the power report.

	combinational Includes all combinational cells in the power report.
	sequential Includes all sequential cells in the power report.
Power Domain	Specifies the power domains whose instances are included in the power report. The power report provides the amount of power consumed by each instance in each power domain. It reports only the instances that are in a power domain. Use `powerDomainList` to report the power consumed by each instance in a specific power domain. *Default*: `all`
PG Net	Specifies the amount of power consumed by a specified list of power and ground nets. The power report provides the amount of power consumed by each instance that is connected to the specified list of power and ground nets only. **Note:** When using this parameter, CPE will always perform propagation and power calculation. *Default*: `all`
Net	Reports the net switching power, as well as the load capacitance, toggle rate, and switching values for each net in the design. *Number of Nets Consuming Highest Power* Reports the number of nets with the highest net switching power.
MMMC View	Specifies the view that was created using the multi-mode multi-corner (MMMC) `create analysis view` command in Encounter. Power analysis is performed for the specified view. *Default*: Uses the current view in Encounter.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `reportPower`

Related Topics

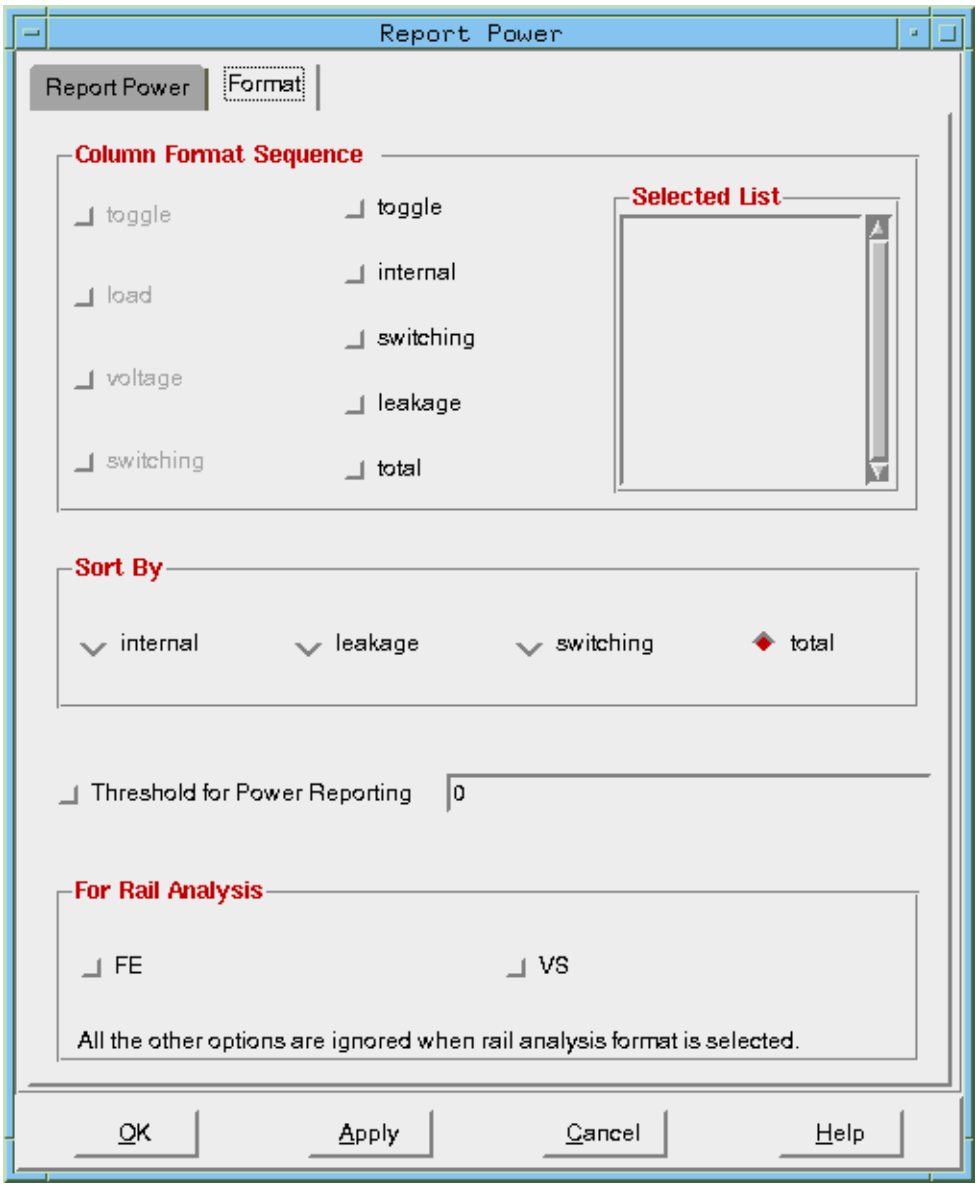
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Report Power – Format

Use the *Format* page of the Report Power form to specify how you want the power data to appear in the report file. It also enables you to select the format of the instance power file that is read by the power-grid analysis tool.

➤ To open the *Format* page of the Report Power form, choose *Power – Power Analysis – Report Power*, then click the *Format* tab.



Report Power – Format Fields and Options

Column Format Sequence

Specifies the order in which the power number columns appear in the power report. The *Selected List* field shows your selections. If you do not specify a column format sequence, the software uses the following default sequence: *toggle*, *internal*, *switching*, *leakage*, and *total*.

Note: For net power, the software uses the following default sequence: *toggle*, *load*, *voltage*, and *switching*.

Sort By

Sorts the instance-based power consumption data by *internal*, *leakage*, *switching*, or *total* power.

Default: `total`

Threshold for Power Reporting

Filters the instances whose total power dissipation is less than the specified value. Units are in milliwatts.

Default: `0`

Set Rail Analysis

Specifies the instance power file format that is read by the power-grid analysis tool.

FE	Reports the instance power file that Encounter uses to perform power-rail analysis.
VS	Reports the instance power file that VoltageStorm uses to perform power-rail analysis.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `reportPower`

Related Topics

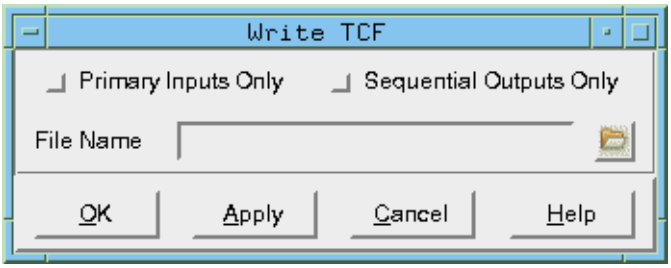
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Write TCF

Use the Write TCF form to write out the propagated switching activity information to a toggle count format (TCF) file. The TCF file contains switching activity information, toggle count information, and the probability of the net or pin being in the logic 1 state.

➤ To open the Write TCF form, choose *Power – Power Analysis – Write TCF*.



Write TCF Fields and Options

Primary Inputs Only

Generates a TCF file that includes only the primary inputs in the design.

Sequential Outputs Only

Includes all the activity for the sequential outputs in the design.

File Name Specifies the name of the output TCF file.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `writeTcf`

Related Topics

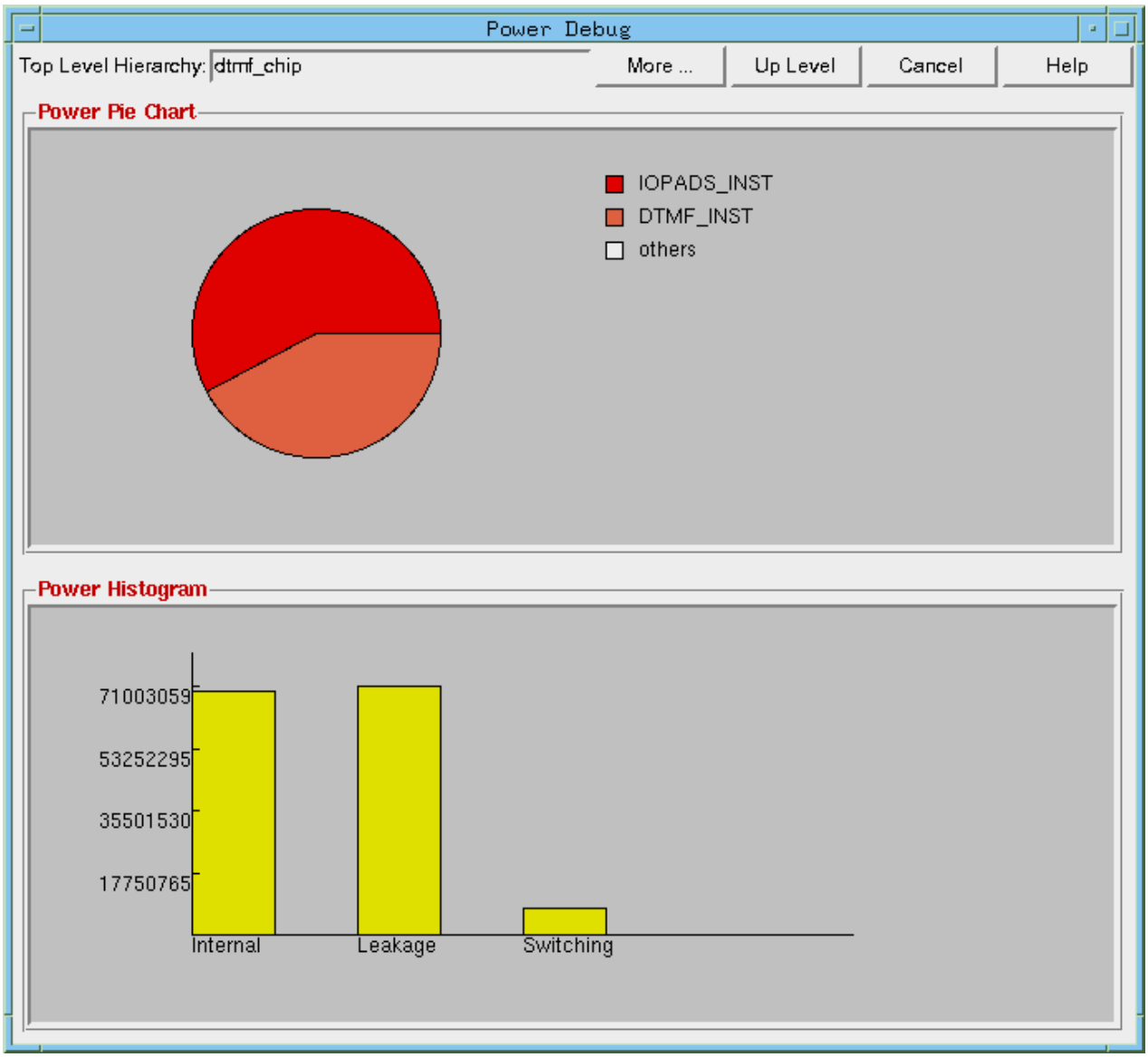
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Debug Power

Use the Power Debug form to display a visual representation of the power reported in the design. This form provides a power pie chart and power histogram to help you debug the high power-consumption areas of the design.

➤ To open the Power Debug form, choose *Power – Power Analysis – Debug Power*.



Debug Power Fields and Options

Top Level Hierarchy	
	Specifies the top-level design.
More	Provides additional power consumption details. You can select from the following list: ■ *By Cell Type* ■ *By Clock Domain* ■ *By Power Domain* ■ *By Power Rail* ■ *By Net* ■ *Net Toggle* ■ *Net Probability*
Up Level	Takes you up a level in the design hierarchy (if applicable).

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- *Performing Static Power Calculation*

Rail Analysis

The Rail Analysis submenu contains the following items:

- Edit Pad Location

  Opens the Edit Pad Location form.

- Edit Net Toggle Probability

  Opens the Edit Net Toggle Probability form.

- Early Analysis
  - Contains the Power Analysis submenu, which opens the following forms:
    - Power Analysis Static Mode form
    - Power Analysis Statistical Mode form
    - Power Analysis Simulation-Based form
  - Contains the Rail Analysis submenu, which opens the Rail Analysis: Average Mode form.

- Sign-off Analysis
  - Opens the VoltageStorm Analysis form.

- Display

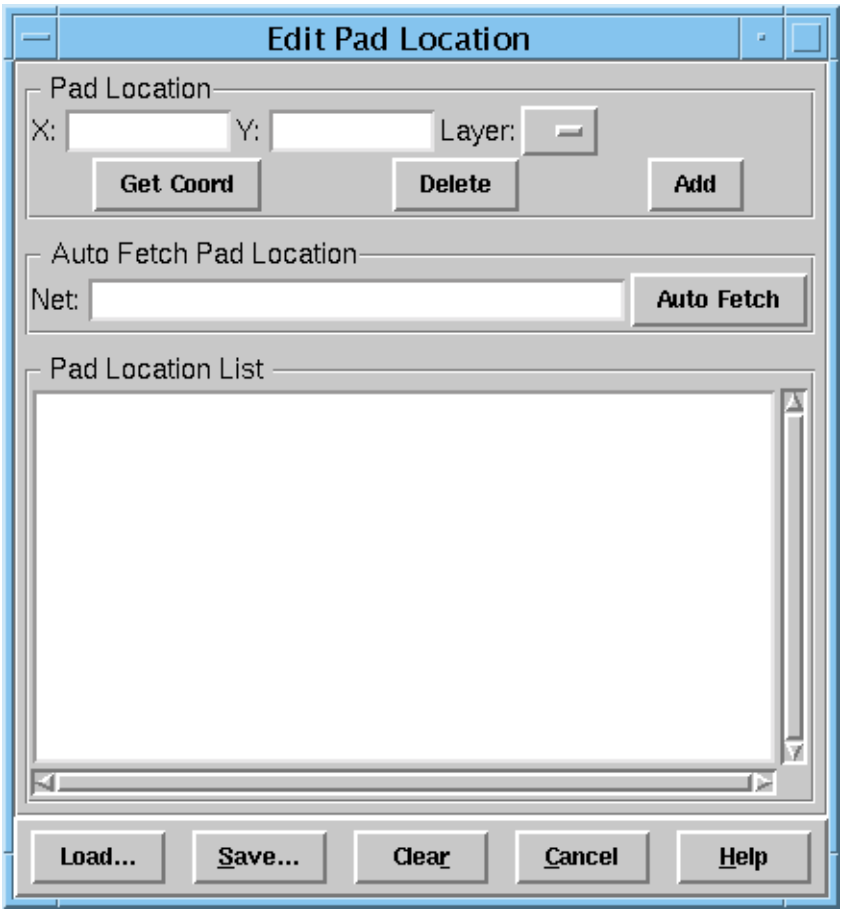
  Opens the Display submenu, which contains the following items:
  - Display Pad Location form
  - Clear Pad Location Display
  - Display Rail Analysis Results form
  - Clear Rail Analysis Display
  - Display Macro I Source Location form
  - Clear Macro I Source Location Display

Edit Pad Location

Use the Edit Pad Location form to create or edit power pad location files (one for each power net) to mark points on the power structures as voltage source reference points. Power pad location files identify the voltage source reference points, such as VCC, VDD, and VSS. You can use these files during all stages of power analysis.

Note: Pad location displays are updated immediately after clicking *Auto Fetch*, *Delete*, or *Add*. The IR drops leading from the pad locations are displayed after running power analysis.

➤ To open the Edit Pad Location form, choose *Power – Rail Analysis – Edit Pad Location.*



Edit Pad Location Fields and Options

Net	The power net or ground net name of the pad cells. **Note:** You can only edit the pad location file for one net at a time.
Pad Location	The *X* and *Y* coordinates of a pad cell.
Layer	The layer that contains the pad cell.
Get coord	Populates the *X* and *Y* coordinates in the *Pad Location* field. Click this button, then click a location in the design display area.
Delete	Removes one or more pad location items from the *Pad Location List*. Highlight the item be removed, then click this button. To highlight multiple items, click them while pressing either the *Shift* or *Control* key.
Add	Adds the *X* and *Y* coordinates of a pad cell to the *Pad Location List*.
Auto Fetch	Automatically populates the *Pad Location List* with the pad locations based on properties defined in the LEF file. For information about setting up a LEF file for use with *Auto Fetch*, see Using Auto Fetch in the *Encounter User Guide*. **Note:** You may need to reissue the `globalNetConnect` command for *Auto Fetch* to function properly if the power pads were not defined in the database at the time that the `globalNetConnect` command was first issued.
Pad Location List	The list of coordinates for pad cells. To populate this field manually, click the *Add* button. To populate this field automatically, click the *Auto Fetch* button.
Load	Opens the Load Pad Location File form. Select a file from this list, then click *Open* to display the pad locations in the *Pad Location List*.
Save	Opens the Save Pad Location File form. Specify a location for the pad location file, then click *OK*. This saves the pad location file, clears the *Pad Location List*, and closes the Save Pad Location form.

Clear	Clears the *Pad Location List*. Once the *Pad Location List* is cleared, you can begin creating a pad location file for a new net. **Note:** Cadence recommends that you use the *Clear* button after you save the pad location file before you use *Auto Fetch* again.

Related Text Commands

For information on the following commands, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `savePadLocation`
- `clearPadLocDisplay`

Related Topics

For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

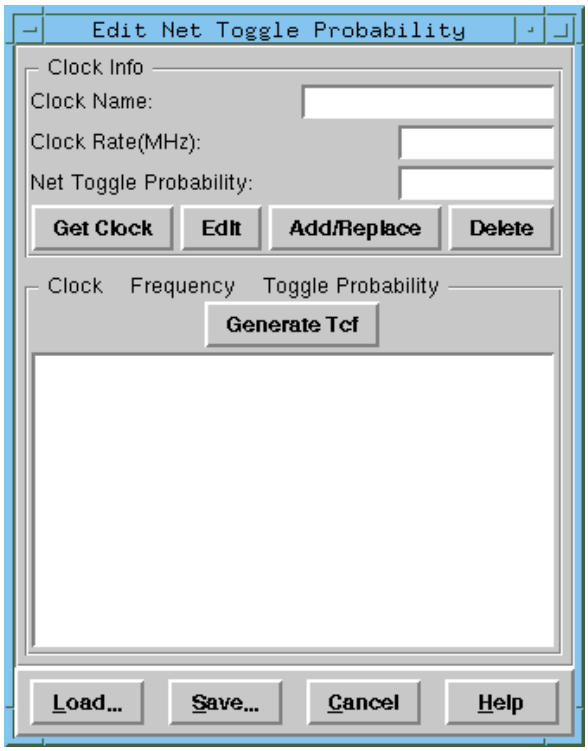
- Creating a Power Pad Location File
- Using Auto Fetch

Edit Net Toggle Probability

Use the Edit Net Toggle Probability form to create or modify a file that contains the clock rate and clock's data path toggle probability.

This form works in conjunction with the Power Analysis Statistical Mode form. It receives the design's clock domain information from the timing constraints file that was read in during design import. The initial information includes the names of all the clocks and clock rate. You can add the toggle probability for each clock domain by editing each clock.

➤ To open the Edit Net Toggle Probability form, choose *Power – Rail Analysis – Edit Net Toggle Probability*.



Edit Net Toggle Probability Fields and Options

Clock Name	The name of the clock to be added to the list. **Note:** For unclocked instances, specify a value of `_unclocked_` in this field.
Clock Rate (MHz)	The rate, in MHz, at which the clock toggles.

Net Toggle Probability

The probability that the nets in the clock domain will toggle.

The default value is `0.2`.

Get Clock

Reads the clock information from the timing constraints file that was loaded during design import, and displays the clock names and their clock rates in the *Clock/Frequency/Toggle Probability* area.

Edit

Modifies the clock information. Information for the clock that is highlighted in the *Clock/Frequency/Toggle Probability* area is displayed in the *Clock Name* and *Clock Rate (MHz)* fields. This allows you to edit the clock rate and net toggle probability.

Important

The specified clock name must be in the timing constraints file.

Add/Replace

Adds or modifies the clock information in the *Clock Name*, *Clock Rate*, and *Net Toggle Probability* text boxes. When adding a clock, make sure the entered clock name exists in the timing constraints file.

Delete

Deletes the clock highlighted in the *Clock/Frequency/Toggle Probability* area.

Generate TCF

Generates a boundary TCF file that contains information about the switching activity of the nets and pins in your design. The switching activity includes the toggle count information and the probability of the net or pin being in the logic 1 state. VoltageStorm uses this switching activity information for power optimization and power analysis in low-power synthesis. When selected, Encounter generates the TCF file and passes this information to VoltageStorm by automatically populating the TCF input field for the Vectorless flow.

Clock/Frequency/Toggle Probability area

Load

Opens the Load Toggle Rate File form. Choose a file, then click *Open*. The file must have the following format:

```
proclock_name clock_frequency toggle_probability
```

The clock names from this file are displayed in the *Toggle Probability List*.

Save	Opens the Save Toggle Rate File form. Enter a filename, then click *Save*. **Note:** This is the filename that you specify in the *Net Toggle Probability File* field of the Power Analysis Statistical Mode form.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `saveToggleProbability`

Power Analysis

The Power Analysis submenu contains the following items:

- *Static*

  This opens the Power Analysis Static Mode form.

- *Statistical*

  This opens the Power Analysis Statistical Mode form.

- *Simulation-Based*

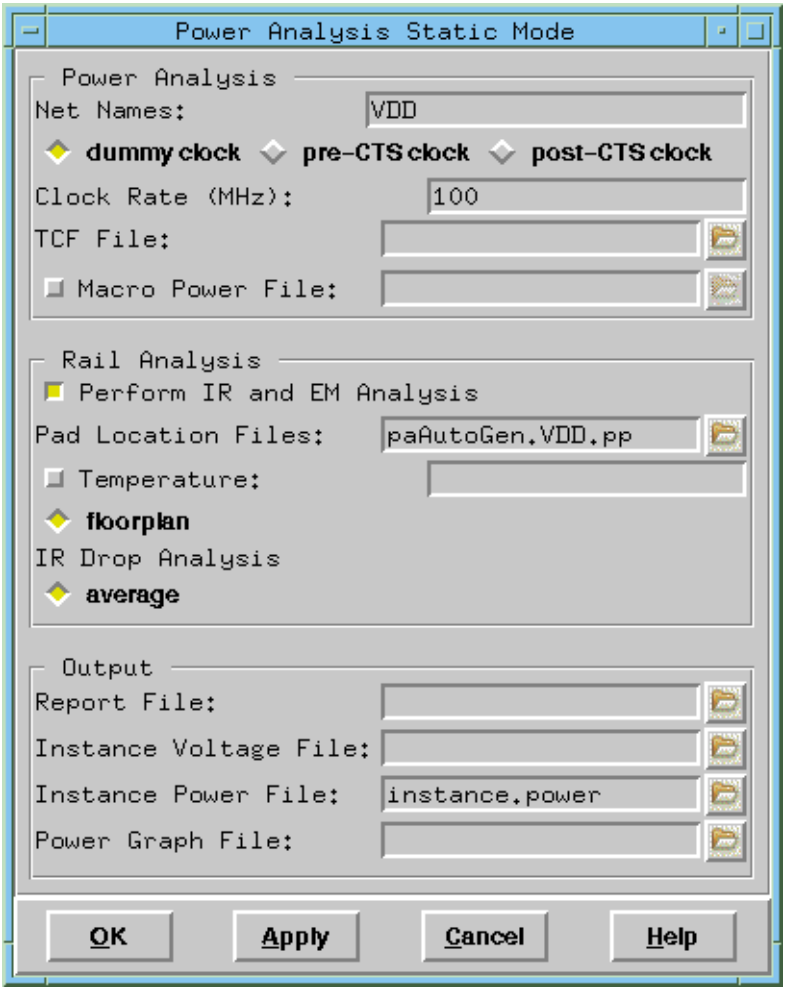
  This opens the Power Analysis Simulation-Based form.

Power Analysis Static Mode

Use the Power Analysis Static Mode form to run power analysis using a TCF file.

When you run power analysis with a TCF file, the power analysis software propagates toggle rates from the primary I/O pins throughout the design for nets that do not have toggle rates specified in the TCF file.

➤ To open the Power Analysis Static Mode form, choose *Power – Rail Analysis – Early Analysis – Power Analysis – Static*.



Power Analysis Static Mode Fields and Options

Net Names

The power net name or list of names to be analyzed.

Tip

If you are running power analysis simultaneously on multiple nets, you must use a separate power pad location file for each net in the design. An error message appears if the number of nets and pad location files does not match. Using multiple net names is useful for analyzing designs that have multiple supply voltages (MSV).

Note: You must specify the power pad location files in the same sequence as the corresponding nets.

dummy clock

Performs power analysis on all nets, including clock nets, toggling at a specified clock rate and a specified toggle probability for all nets.

Note: If you choose this option, you must also specify a value for the *Clock Rate (MHz)* field.

pre-CTS clock

Performs power analysis that is similar to the *post-CTS clock* option, except the switching power for a clock net is not calculated when the number of pins on that clock net is greater than 50. Cadence recommends using pre-CTS clock mode when the clock tree has not yet been built.

post-CTS clock

Performs power analysis with clock nets at a set clock rate (in megahertz) for each clock domain.

Clock Rate (MHz)

Specifies the clock rate in megahertz.

TCF File

Specifies a TCF file (`filename.tcf`).

For more information on TCF file syntax, see *Low Power in Encounter™ RTL Compiler*.

Macro Power File

Specifies a macro power file (`filename.power`).

Perform IR and EM Analysis

If selected, the software automatically performs rail analysis after the completion of power analysis. This is the default. If deselected, prevents the power analysis software from running rail analysis. Deselecting this option also disables the following options on this form:

- *Pad Location File*
- *Floorplan* or *Layout* mode
- *IR Drop Analysis*
- *Instance Voltage File*

Pad Location Files

One or more pad location files.

Note: You must specify a separate pad location file for each net in the design. For more information about this file, see "Edit Pad Location" on page 937.

Temperature

Specifies the temperature (in degrees Celsius) to be used during temperature-dependent resistance extraction. The temperature-dependent resistance coefficient is taken from the capacitance table.

floorplan

Runs power analysis early in the floorplanning cycle.

You must perform the following floorplanning steps before running power analysis:

- Create power rings around the core design area.
- Create power stripes over the core design area in both the horizontal and vertical directions.

Power is only analyzed for the instances placed inside the core design area. The power analysis software creates the power rail to connect all the standard cells. The default width of the rail is one-eighth of the height of a standard cell, which can be overwritten using the following Tcl variable:

```
set dbgCellRailWidth microns
```

Note: Power analysis honors followpins generated by SRoute in layout mode only, not in floorplan mode. Power and ground rails and vias generated in floorplan mode are temporary and do not adhere to technology rules, so they should not be used in the design. Power analysis does not create physical rails or vias.

IR Drop Analysis

Performs IR drop analysis.

average

Displays a gradient of the average IR drop during the entire analysis period. Use this type of analysis to identify potential areas of power deficiency within the design.

Report File

Specifies the name of a general power analysis output file (*filename*.report).

Instance Voltage File

Specifies the output instance voltage file (*filename*.instVoltage).

Instance Power File

Specifies the output instance power file (*filename*.power).

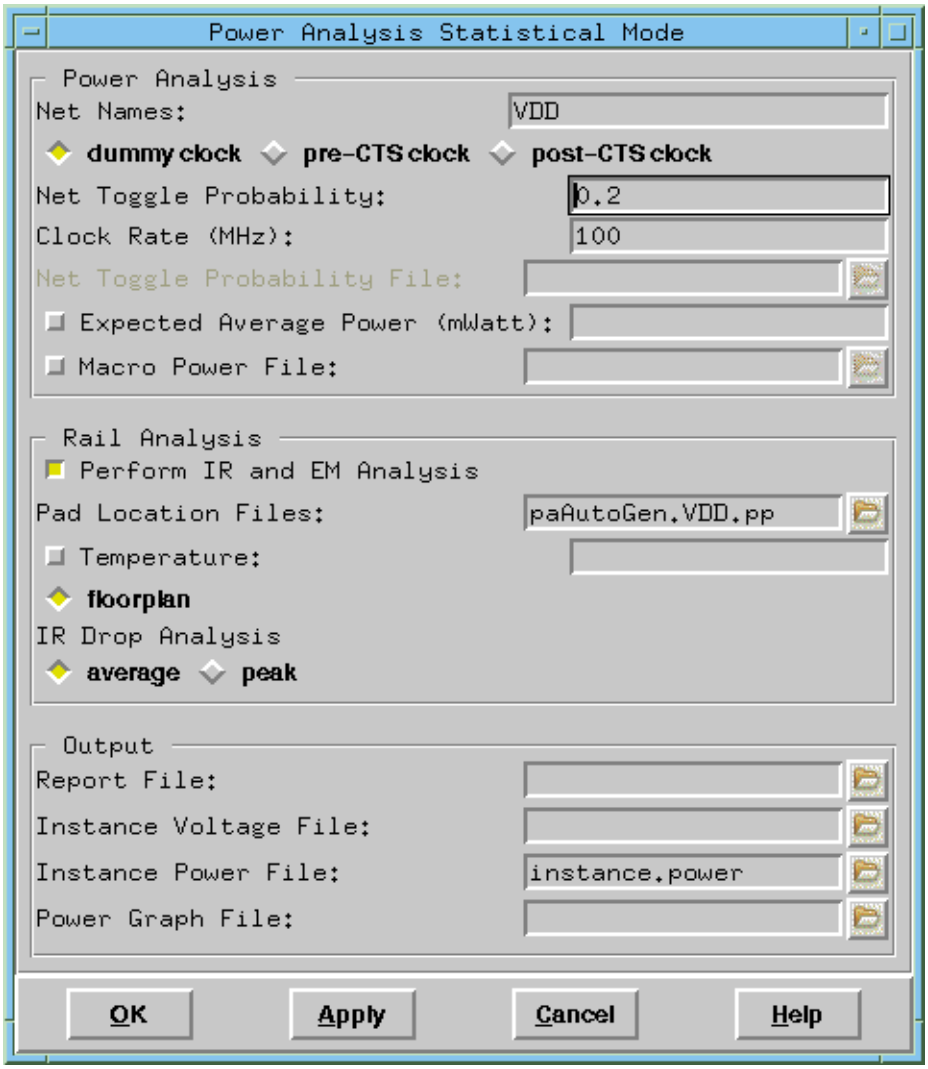
Power Graph File

Specifies the output power graph file (*filename*.pgr).

Power Analysis Statistical Mode

Use the Power Analysis Statistical Mode form to run power analysis for the power or ground nets using the *dummy clock*, *pre-CTS*, or *post-CTS* clock options. You must use statistical analysis to run power analysis if you do not have a VCD file.

➤ To open the Power Analysis Statistical Mode form, choose *Power – Rail Analysis – Early Analysis – Power Analysis – Statistical*.



Power Analysis Statistical Mode Fields and Options

Net Names

The power net name or list of names to be analyzed.

Tip

If you are running power analysis simultaneously on multiple nets, you must use a separate power pad location file for each net in the design. An error message appears if the number of nets and pad location files does not match. Using multiple net names is useful for analyzing designs that have multiple supply voltages (MSV).

Note: You must specify the power pad location files in the same sequence as the corresponding nets.

dummy clock

Performs power analysis on all nets, including clock nets, toggling at a specified clock rate and a specified toggle probability for all nets.

Note: If you choose this option, you must also specify values for the *Net Toggle Probability* and *Clock Rate (MHz)* fields.

pre-CTS clock

Performs power analysis that is similar to the *post-CTS clock* option, except the switching power for a clock net is not calculated when the number of pins on that clock net is greater than 50. Cadence recommends using pre-CTS clock mode when the clock tree has not yet been built.

Note: If you choose this option, you must also specify a value in the *Net Toggle Probability File* field.

post-CTS clock

Performs power analysis with clock nets at a set clock rate (in megahertz) for each clock domain, and a set toggle probability (in percent) for the clock's data paths. This means that all the nets on a clock path toggle at the clock rate, but only a percentage of the clock's data paths toggle in each clock cycle.

For example, if the *Clock Rate* value is `300` and the *net toggle probability* value is `0.2` (20%), then the clock path nets toggle at 300 MHz, and only 20 percent of the clock's data paths toggle in each cycle. Nets not belonging to a clock domain do not toggle.

Note: If you choose this option, you must also specify a value in the *Net Toggle Probability File* field.

Net Toggle Probability

Percentage of nets toggling of nets in the entire design, including all the clock nets.

Default: `0.2`.

Clock Rate (MHz)

The rate at which the net toggles.

Default: `100`

Net Toggle Probability File

The clock information file created in the Edit Net Toggle Probability form.

Note: If your clock information is incomplete, you can control the toggle probability for unclocked instances by specifying a value of `_unclocked_` in the *Clock Name* field of the Edit Net Toggle Probability form.

Expected Average Power (mWatt)

If selected, specify the expected power usage (in milliwatts) in the text entry field. The software does the following:

- Performs power analysis at the clock rate and toggle rate specified in the form.
- Estimates the toggle rate(s) based on the analysis result to meet the milliwatt value entered.
- Performs power analysis with the estimated toggle rate value.

If deselected, the software does not use the *Net Toggle Probability* and *Clock Rate (MHz)* values for *pre-CTS clock* and *post-CTS clock* modes.

Macro Power File

A file that specifies power consumption of macros and instances that do not have power models in the `.lib` or TLF files. This option is particularly useful if you want to specify (rather than have the software calculate) power consumption for one or more specific instances.

You can create a Macro Power file in the following format to specify the power usage of each macro:

```
InstanceName PowerConsumption (in Watts)
```

The following example specifies that the power consumption for the ROM named `DTMF_INST/ROM_INST` is 5mW:

```
DTMF_INST/ROM_INST  0.005
```

Perform IR and EM Analysis

If selected, the software automatically performs rail analysis after the completion of power analysis. This is the default. If deselected, prevents the power analysis software from running rail analysis. Deselecting this option also disables the following options on this form:

- *Pad Location File*
- *Floorplan* or *Layout* mode
- *IR Drop Analysis*
- *Instance Voltage File*

Pad Location Files

One or more pad location files.

Note: You must specify a separate pad location file for each net in the design. For more information about this file, see "Edit Pad Location" on page 937.

Temperature

Specifies the temperature (in degrees Celsius) to be used during temperature-dependent resistance extraction. The temperature-dependent resistance coefficient is taken from the capacitance table.

floorplan

Runs power analysis early in the floorplanning cycle.

You must perform the following floorplanning steps before running power analysis:

- Create power rings around the core design area.
- Create power stripes over the core design area in both the horizontal and vertical directions.

Power is only analyzed for the instances placed inside the core design area. The power analysis software creates the power rail to connect all the standard cells. The default width of the rail is one-eighth of the height of a standard cell, which can be overwritten using the following Tcl variable:

```
set dbgCellRailWidth microns
```

Note: Power analysis honors followpins generated by SRoute in layout mode only, not in floorplan mode. Power and ground rails and vias generated in floorplan mode are temporary and do not adhere to technology rules, so they should not be used in the design. Power analysis does not create physical rails or vias.

average

Displays a gradient of the average IR drop during the entire analysis period. Use this type of analysis to identify potential areas of power deficiency within the design.

peak

Displays a gradient that shows the largest IR drop during the analysis period. Use this type of analysis to identify IR drop that is caused by local switching activity.

Note: In versions 2.2 and earlier, the Encounter software performed only peak IR analysis.

Report File	(Optional) If you specify a filename in the text entry field, the reports for all nets are saved together in the file that you specify. If you do not specify a filename, the software uses the name `powerNetName.report` and creates a separate report file for each net.
Instance Voltage File	The name of the Instance Voltage File.
Instance Power File	The name of the Instance Power file. For more information, see Instance Power Data File.
Power Graph File	The file name to which you want Power Graph information to be written. This information is also written to the Encounter console. For more information, see Power Graph Report.

Related Text Commands

For information about the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `updatePower`

Related Topics

For information about the following topics, see “Power Analysis” in the *Encounter Text User Guide*.

- Running Power Analysis with Encounter
- Instance Voltage File
- Instance Power Data File
- Power Graph Report
- Viewing the Power Graph

Power Analysis Simulation-Based

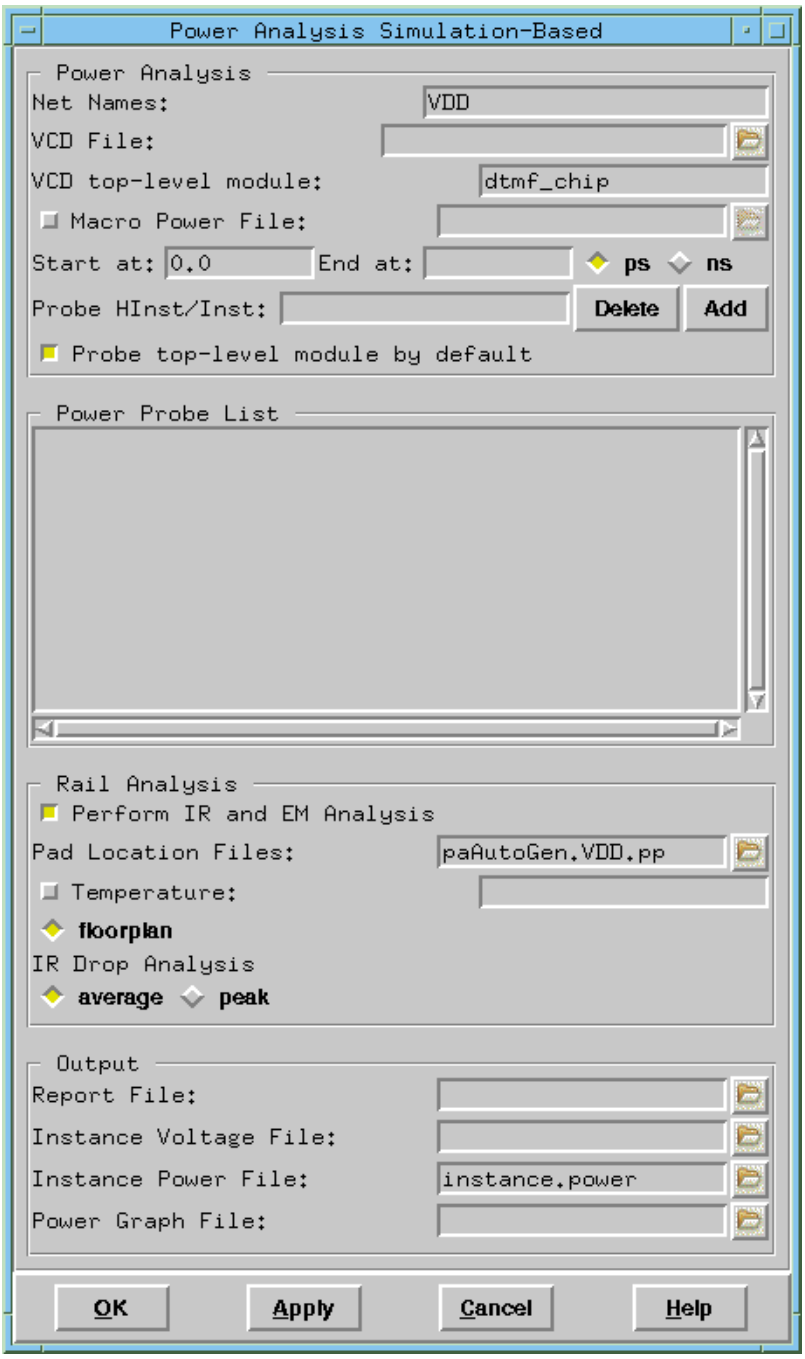
Use the Power Analysis Simulation-Based form to run power analysis using a Verilog VCD file to simulate the design when analyzing power consumption. Running power analysis in simulation-based mode requires the following tasks:

1. Import the design using the *Design – Import Design* menu option.
2. Load the DEF file using the *Design – Load – DEF* menu option.
3. Create or edit the power pad location file using the *Power – Rail Analysis – Edit Pad Location* menu option.
4. Set the `rda_Input` variable. For example:

   ```
   set rda_Input (ui_pwrnet) {vdd VRG_DIG}
   set rda_Input (ui_gndnet) {gnd}
   ```

5. Extract the RC parasitics using the *Timing – Extract RC* menu option.
6. Run power analysis in simulation-based mode.

   To open the Power Analysis Simulation-Based form, choose *Power – Rail Analysis – Early Analysis – Power Analysis – Simulation-Based*.


Power Analysis Simulation-Based
Power Analysis
Net Names:
VDD
VCD File:
VCD top-level module:
dtmf_chip
Macro Power File:
Start at:
0.0
End at:
ps
ns
Probe HInst/Inst:
Delete
Add
Probe top-level module by default
Power Probe List
Rail Analysis
Perform IR and EM Analysis
Pad Location Files:
paAutoGen.VDD.pp
Temperature:
floorplan
IR Drop Analysis
average
peak
Output
Report File:
Instance Voltage File:
Instance Power File:
instance.power
Power Graph File:
OK
Apply
Cancel
Help

Power Analysis Simulation-Based Fields and Options

Net Names

The power net name or list of names to be analyzed.

Tip

If you are running power analysis simultaneously on multiple nets, you must use a separate power pad location file for each net in the design. An error message appears if the number of nets and pad location files does not match. Using multiple net names is useful for analyzing designs that have multiple supply voltages (MSV).

Note: You must specify the power pad location files in the same sequence as the corresponding nets.

VCD File

The name of the Verilog VCD file. This simulation file must contain activity for all nets in the current design. A larger simulation file may also be used by setting the top module to the current design.

VCD top-level module

The VCD top-level module name for the current design. This allows the software to analyze the current design, where the current design is one of the modules in the VCD file.

Note: If the top module name in the VCD file does not match the top cell name in the Encounter database, you must enter the full hierarchical path name for the instance within the VCD file that does match. For example, if the top cell in the Encounter database is `BLOCK_A` and the VCD file uses a top module name of `TEST_TOP`, which has an instance of `BLOCK_A` named `block_a_inst`, specify the value `TEST_TOP/block_a_inst` in this field.

Macro Power File

A file that specifies power consumption of macros and instances that do not have power models in the `.lib` or TLF files. This option is particularly useful if you want to specify (rather than have the software calculate) power consumption for one or more specific instances.

You can create a Macro Power file in the following format to specify the power usage of each macro:

```
InstanceName PowerConsumption (in Watts)
```

The following example specifies that the power consumption for the ROM named `DTMF_INST/ROM_INST` is 5mW:

```
DTMF_INST/ROM_INST  0.005
```

Start at

The start time of the period for which you want to analyze the power. If you do not specify a value in this field, the VCD file is analyzed from the beginning.

Note: The VCD file is usually very large; you need to analyze only a small portion of the VCD file to get a meaningful IR drop value and an average power value.

End at

The end time of the period for which you want to analyze the power. If you do not specify a value in this field, the VCD file is analyzed to the end.

Note: The time between `$dumpoff` and `$dumpon` is subtracted from total elapsed time. The elapsed time is time difference between the first time point and the last time point specified in the VCD file.

ps

The time period is measured in picoseconds.

ns

The time period is measured in nanoseconds.

Probe Hist/Inst

Probes power for a particular hierarchical instance or leaf instance.

Probe top-level module by default

Creates the instantaneous power waveform for the entire design. To probe an instance of the design, add the hierarchical name of the instance to the *Power Probe List*.

Delete

Removes the selected an instance name from the *Power Probe List* area.

Add

Adds the instance name in the *Probe Hist/Inst* field to the *Power Probe List*.

Power Probe List

A list of hierarchical instances or leaf instances. Power analysis is performed on the entire design, and a separate power number is generated for those instances included in the *Power Probe List*.

Perform IR and EM Analysis

If selected, the software automatically performs rail analysis after the completion of power analysis. This is the default. If deselected, prevents the power analysis software from running rail analysis. Deselecting this option also disables the following options on this form:

- *Pad Location File*
- *Floorplan* or *Layout* mode
- *IR Drop Analysis*
- *Instance Voltage File*

Pad Location Files

One or more pad location files.

Note: You must specify a separate pad location file for each net in the design. For more information about this file, see "Edit Pad Location" on page 937.

Temperature

Specifies the temperature (in degrees Celsius) to be used during temperature-dependent resistance extraction. The temperature-dependent resistance coefficient is taken from the capacitance table.

floorplan

Runs power analysis early in the floorplanning cycle.

You must perform the following floorplanning steps before running power analysis:

- Create power rings around the core design area.
- Create power stripes over the core design area in both the horizontal and vertical directions.

Power is only analyzed for the instances placed inside the core design area. The power analysis software creates the power rail to connect all the standard cells. The default width of the rail is one-eighth of the height of a standard cell, which can be overwritten using the following Tcl variable:

```
set dbgCellRailWidth microns
```

Note: Power analysis honors followpins generated by SRoute in layout mode only, not in floorplan mode. Power and ground rails and vias generated in floorplan mode are temporary and do not adhere to technology rules, so they should not be used in the design. Power analysis does not create physical rails or vias.

average

Displays a gradient of the average IR drop during the entire analysis period. Use this type of analysis to identify potential areas of power deficiency within the design.

peak

Displays a gradient that shows the largest IR drop during the analysis period. Use this type of analysis to identify IR drop that is caused by local switching activity.

Note: In versions 2.2 and earlier, the Encounter software performed only peak IR analysis.

Report File

(Optional) If you specify a filename in the text entry field, the reports for all nets are saved together in the file that you specify. If you do not specify a filename, the software uses the name `powerNetName.report` and creates a separate report file for each net.

Instance Voltage File

The name of the Instance Voltage File.

Instance Power File

The name of the Instance Power file. For more information, see Instance Power Data File.

Power Graph File

The file name to which you want Power Graph information to be written. This information is also written to the Encounter console. For more information, see Power Graph Report.

Related Text Command

For information about the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `updatePower`

Related Topics

For information about the following command, see “Power Analysis” in the *Encounter User Guide*.

- Running Power Analysis with Encounter
- Instance Voltage File
- Instance Power Data File
- Power Graph Report
- Viewing the Power Graph

Rail Analysis

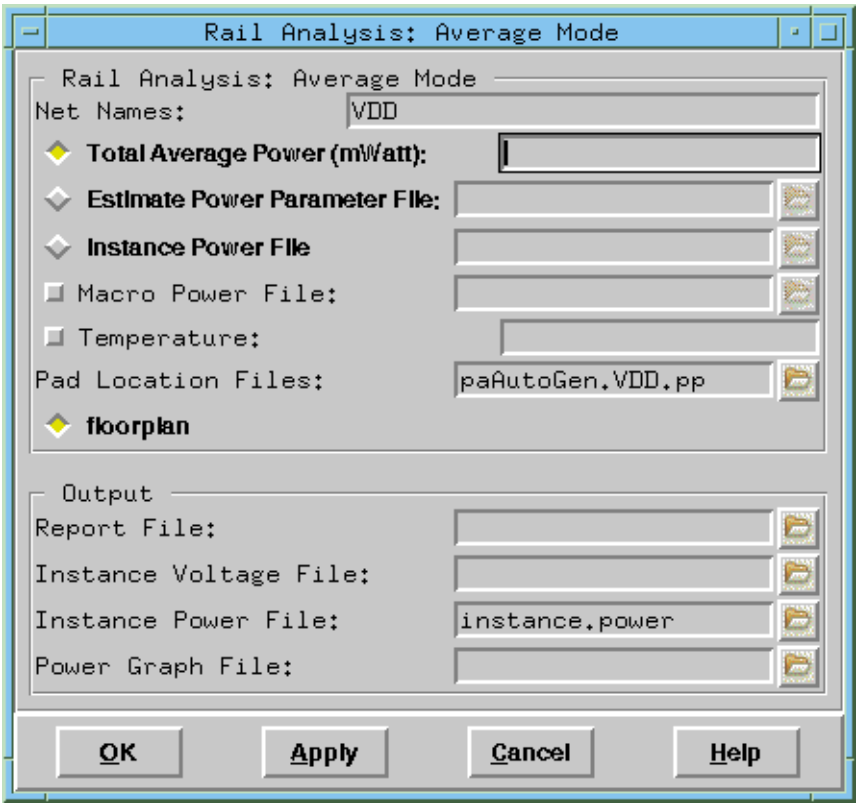
The Rail Analysis submenu opens the Rail Analysis: Average Mode form.

Rail Analysis: Average Mode

The Rail Analysis: Average Mode form enables you to run rail analysis separately, using the results of a previous power analysis run.

Note: You can also use this mode for performing a preliminary estimate of power consumption when no power library is available. This mode requires an input file that contains the estimate information.

➤ To open the Rail Analysis: Average Mode form, choose *Power – Rail Analysis – Early Analysis – Rail Analysis*.



Rail Analysis: Average Mode Field and Options

Net Names

The power net name or list of names to be analyzed.

Tip

If you are running power analysis simultaneously on multiple nets, you must use a separate power pad location file for each net in the design. An error message appears if the number of nets and pad location files does not match. Using multiple net names is useful for analyzing designs that have multiple supply voltages (MSV). For more information about MSV, see Multiple Supply Voltages.

Note: You must specify the power pad location files in the same sequence as the corresponding nets.

Total Average Power (mWatt)

The total average power for the chip or the block.

If you specify a value in the field, the software runs area-based rail analysis. You do not need an instance power file to run in this mode.

Note: The *Total Average Power (mWatt)* field is ignored during rail analysis if either of the following conditions exists:

- The sum of the instance power values in the *Instance Power File* is greater than the value that you specify in the *Total Average Power (mWatt)* field.
- All instances associated with the net for which rail analysis is being performed are defined in the *Instance Power File*.

Estimate Power Parameter File

The name of a file that contains parameters used by the software to estimate power consumption. This provides a more accurate estimate than using a *Total Average Power* value. For more information, see Running Power Analysis in Simple Estimate Mode in the “Power Analysis” chapter of the *Encounter User Guide*.

Instance Power File

An existing file to be used as input for the rail analysis.

Note: This field is optional if you specify a value in the *Total Average Power (mWatt)* field.

Macro Power File

A file that specifies power consumption of macros and instances that do not have power models in the `.lib` or TLF files. This option is particularly useful if you want to specify (rather than have the software calculate) power consumption for one or more specific instances.

You can create a Macro Power file in the following format to specify the power usage of each macro:

```
InstanceName PowerConsumption (in Watts)
```

The following example specifies that the power consumption for the ROM named `DTMF_INST/ROM_INST` is 5mW:

```
DTMF_INST/ROM_INST  0.005
```

Temperature

Specifies the temperature (in degrees Celsius) to be used during temperature-dependent resistance extraction. The temperature-dependent resistance coefficient is taken from the capacitance table.

Pad Location Files

One or more pad location files. Specify a separate pad location file for each net in the design.

floorplan	Runs power analysis early in the floorplanning cycle. You must perform the following floorplanning steps before running power analysis: ■ Create power rings around the core design area. ■ Create power stripes over the core design area in both the horizontal and vertical directions. Power is only analyzed for the instances placed inside the core design area. The power analysis software creates the power rail to connect all the standard cells. The default width of the rail is one-eighth of the height of a standard cell, which can be overwritten using the following Tcl variable: `set dbgCellRailWidth` *`microns`* **Note:** Power analysis honors followpins generated by SRoute in layout mode only, not in floorplan mode. Power and ground rails and vias generated in floorplan mode are temporary and do not adhere to technology rules, so they should not be used in the design. Power analysis does not create physical rails or vias.
Report File	(Optional) If you specify a filename in the text entry field, the reports for all nets are saved together in the file that you specify. If you do not specify a filename, the software uses the name *`powerNetName`*`.report` and creates a separate report file for each net.
Instance Voltage File	The name of the output Instance Voltage File.
Instance Power File (output)	The name of the output Instance Power file. For more information see Instance Power Data File.
Power Graph File	The file name to which you want Power Graph information to be written. This information is also written to the Encounter console. For more information, see Power Graph Report.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

■ `updatePower`

Related Topics

For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- Running Power Analysis in Simple Estimate Mode
- Power Graph Report
- Viewing the Power Graph

Sign-off Analysis

The Sign-off Analysis submenu item opens the VoltageStorm Analysis form.

VoltageStorm Analysis

The VoltageStorm Analysis form enables you to run power analysis using the VoltageStorm PE power integrity verification solution.

Note: To use this feature, you must have a separate license.

The VoltageStorm Analysis form contains the following two pages:

- VoltageStorm Analysis – Basic on page 969
- VoltageStorm Analysis – Advanced on page 978

You can open the following additional forms from the VoltageStorm Analysis form:

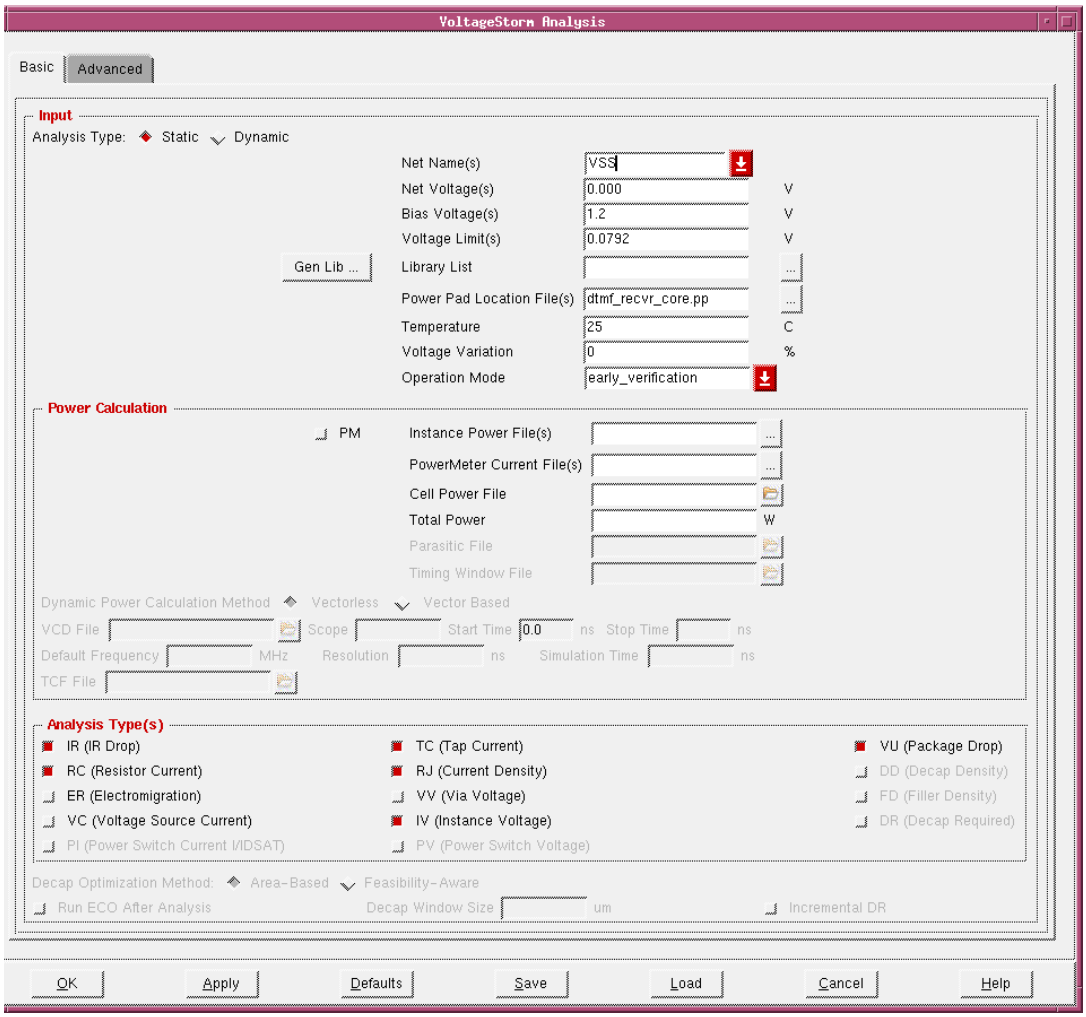
- Library Generation – Basic on page 1348
- Library Generation – Advanced on page 1353
- Cell View Specification on page 985
- Layer Bias Specification on page 988
- Layer Names Maps Specification on page 990

VoltageStorm Analysis – Basic

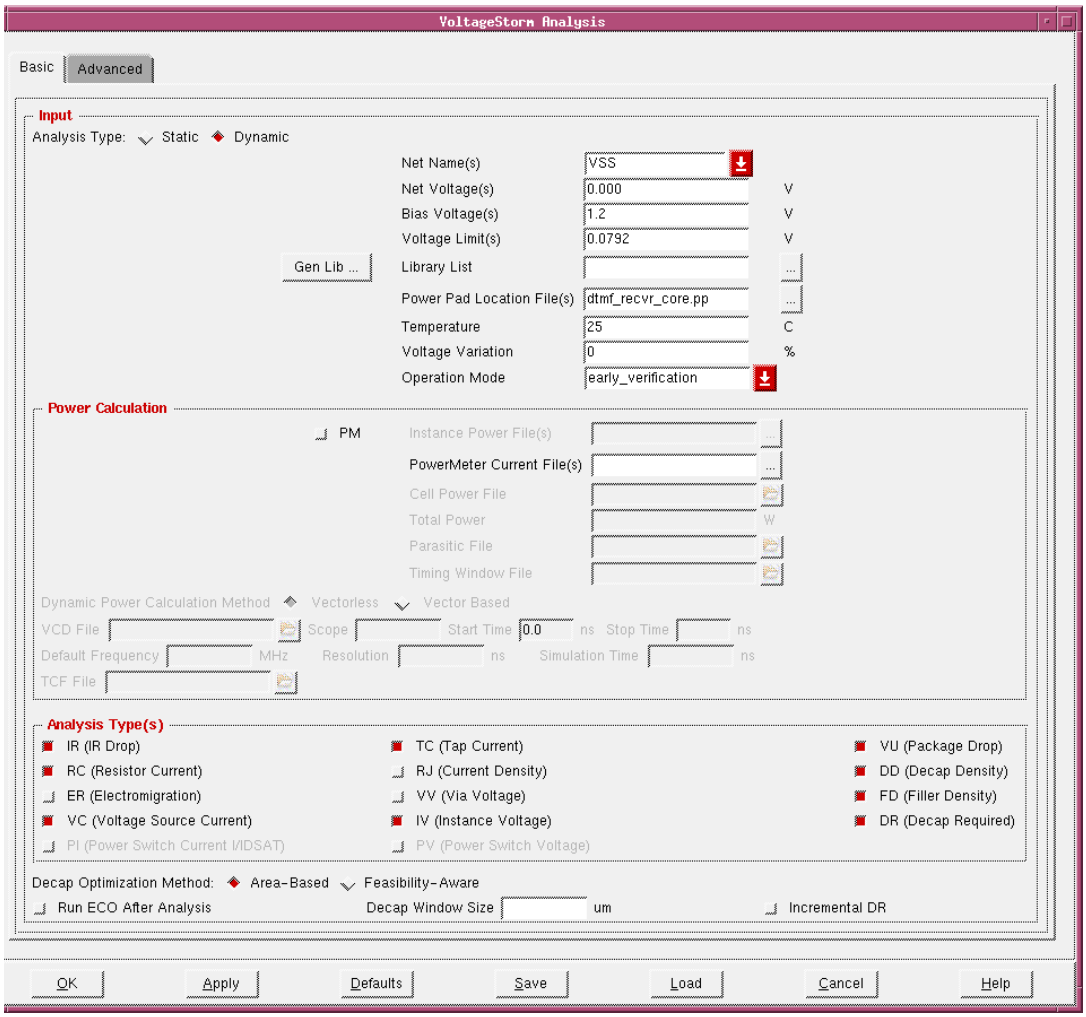
Use the *Basic* page of the VoltageStorm Analysis form to specify input files, select the types of analysis to be done, and to access the Library Generation form.

➤ To open the *Basic* page of the VoltageStorm Analysis form, choose *Power – Rail Analysis – Sign-off Analysis*, then click the *Basic* tab.

The following image shows the *Basic* page with its default, *Static* settings.



The following image shows the *Basic* page with the *Dynamic* settings.



VoltageStorm Analysis - Basic Fields and Options

Analysis Type

Controls the analysis type mode for the VoltageStorm run.

Static

Specifies that VoltageStorm should run in static mode.

This is the default.

Dynamic

Specifies that VoltageStorm should run in dynamic mode.

Net Name

A dropdown list of available net names that you can analyze.

Net Voltage

The voltage of the net.

Bias Voltage

Defines operating bias voltage with which rail analysis is performed.

Note: The bias voltage value is *always* the voltage value for the power net, whether you are analyzing a ground net or power net. For zero voltage (VSS, GND) nets make sure this is assigned correctly, since it will be defaulted to 1.2V.

Important

Cadence strongly recommends that you use this parameter with MSV designs, as the power analysis software provides more accurate results with this parameter.

Voltage Limit

The voltage threshold on the power or ground net. By default, the limit is 10 percent lower than the nominal voltage for the net. Specify the minimum allowed voltage on the power net or the maximum rise on the ground net, depending on which net is being analyzed.

Gen Lib

Opens the Library Generation form.

Library List	The cell libraries or lower level partitions containing power grid views. Click the (...) button next to the field to this field to open the Library Directories form, then use the Library Directories form as follows: **1.** Click a folder icon or type a directory name into the Library Directory field. **2.** Click *Add* to add the directory you selected to the *Library Directories* list. You can add multiple directories to the list. **3.** When you finish adding directories, click *Close* to return to the VoltageStorm Analysis form.
Power Pad Location File	A file that contains power pad locations. For more information, see "Creating a Power Pad Location File" in the *Encounter User Guide*.
Temperature	Specifies a temperature value in degrees Celsius. Default: 25
Voltage Variation	Sets the power pin tolerance limit.
Operation Mode	Specifies the operation mode. When used with the *Voltage Variation* option, you can specify a voltage variation range that is used to characterize the libraries in sign-off mode.
PM	When selected in *Static* mode, Encounter runs PowerMeter analysis using the instance power files that have already been generated. When selected in *Dynamic* mode, Encounter runs PowerMeter analysis to create the PM dynamic current files. When disabled in *Dynamic* mode, Encounter runs PowerMeter analysis using the specified PM dynamic current files that have already been generated. *Default*: Off
Instance Power File	(Optional) An instance power file that was generated during Encounter power analysis. For more information, see "Creating an Instance Power File" in the *Encounter User Guide* **Note:** If you want to run an area-based analysis, leave this field empty.

PowerMeter Current File(s)

Specifies the name(s) of the PowerMeter dynamic current file(s). Use this option to run PowerMeter analysis with the dynamic current files that have already been generated.

Note: This option is available only in dynamic mode and when the *PM* box is disabled.

Cell Power File

(Optional) A file that contains cell power information. For more information, see “Creating a Cell Power File” in the *Encounter User Guide*

Note: If you specify a cell power file, you must also specify a value in the *Total Power* entry field and you cannot specify an instance power file. If you want to run an area-based analysis, specify `/dev/null` (or any other empty file) in this field.

Total Power

(Optional) A value that approximates the total power usage to be used during the analysis. For more information, see “Specifying Power Values” in the *Encounter User Guide*.

Note: If you specify a cell power file, you must provide a value in this field. If you want to run an area-based analysis, you must specify a value in this field.

Parasitic File

Specifies the name of a parasitics file in DSPF or SPEF format.

By default, VoltageStorm automatically extracts parasitics. If you use this option, VoltageStorm uses the parasitics data from the file rather than performing RC extraction to generate the parasitics.

Timing Window File

Specifies the timing window file.

By default, VoltageStorm automatically generates a timing window file. If you specify this option, VoltageStorm uses the specified file rather than generating a timing window file.

Dynamic Power Calculation Method

Vectorless

Specifies that VoltageStorm should calculate dynamic power consumption with a timing-windows-based approach.

Vector Based

Specifies that VoltageStorm should calculate dynamic power consumption using a VCD file.

VCD File	Specifies the name of the VCD file for use in vector-based dynamic power calculation.
Scope	Specifies the design's hierarchical scope to be used in the VCD file.
Start Time	Specifies the starting time to be used in the VCD file.
Stop Time	Specifies the stop time to be used in the VCD file.
Default Frequency	Specifies the operating frequency of the design (in megahertz).
Resolution	Specifies the simulation time step to be used.
Simulation Time	Specifies the total simulation time to be used during power computation.
TCF File	Specifies an external TCF file for the VoltageStorm Vectorless flow. The *TCF File* field is enabled only if the *Dynamic* analysis type and *Vectorless* power method are selected.
Analysis Types	The type of analysis to be performed. Select one or more of the following analysis types. For more information about each type of analysis and report, see the *VoltageStorm Hierarchical PGS Manual.*

IR (IR Drop)	Analyzes and reports IR drop. *Default*: On
RC (Resistor Current)	Analyzes and reports resistor current. *Default*: Off
ER (Electromigration)	Analyzes and reports electromigration risk. *Default*: Off
VC (Voltage Source Current)	Analyzes and reports voltage source current. *Default*: Off
PI (Power Switch Current I/IDSAT)	Analyzes and reports the ratio of current versus the saturation current (IDsat) to see if too much current is flowing through the power switches. This option is activated when you specify a *Switched (ON) Net* for power switch analysis (Advanced form).

TC (Tap Current)	Analyzes and reports tap current. *Default*: Off
RJ (Current Density)	Analyzes and reports relative current density. *Default*: On
VV (Via Voltage)	Analyzes and reports voltages across vias and contacts. *Default*: On
IV (Instance Voltage)	Analyzes and reports instance-based supply voltage. *Default*: Off
PV (Power Switch Voltage)	Analyzes and reports the power-switch voltage by computing the IR drop across each power switch in the design. This option is activated when you specify a *Switched (ON) Net* for power switch analysis (Advanced form). *Default*: Off
VU (Package Drop)	Analyzes and reports on voltage drop across the package. *Default*: Off
DD (Decap Density)	Analyzes and reports on decoupling capacitance density. *Default*: Off
FD (Filler Density)	Analyzes and reports on filler density. *Default*: Off
DR (Decap Required)	Analyzes and reports on decoupling capacitance required. *Default*: Off

Decap Optimization Method

Area-Based	Performs area-based decoupling capacitance optimization. After the successful completion of dynamic IR-Drop and decoupling capacitance analysis, VoltageStorm generates the ECO file (`vs2fe_eco.tcl`) for Encounter that is driven by the area-based `addDeCap` command. When you run the ECO file in Encounter using the `source vs2fe_eco.tcl` command, Encounter swaps the filler cells in the design with decoupling capacitance cells, then checks for DRC violations based on the technology LEF rules for the design. You can use the `reportDeCap` command to generate a report on the newly added decoupling capacitance cells in the design.
Feasibility-Aware	Performs feasibility-aware (also known as placement-aware) decoupling capacitance optimization. This method relies on the available filler cells in the design. During decoupling capacitance optimization in VoltageStorm, the additional capacitance value is computed for each node on the power grid. The analysis searches for available filler cells near the nodes that require additional decoupling capacitance and generates an ECO file that contains the filler instances that should be swapped with decoupling capacitance cells. The ECO file is then sourced again for reanalysis of the power grid. During re-analysis, VoltageStorm swaps the filler cells with decoupling capacitance cells and dynamic IR drop is analyzed to assess the impact of the newly added decoupling capacitance cells.

Run ECO After Analysis

Instructs VoltageStorm to run ECO functionality after power analysis.

Default: Off

Decap Window Size — Specifies the window size setting that VoltageStorm uses when dividing the die area into multiple windows for decoupling capacitance optimization. Units in microns.

Incremental DR — For incremental decoupling capacitance optimization, lets you change the window size after the ECO file is generated. After selecting *Incremental DR* and specifying the new window size in the *Decap Window Size* field, the ECO file is updated with the new window size information. If *Run ECO After Analysis* is selected, Encounter sources the new ECO file.

Save — Opens the Save VoltageStorm Analysis Form File. Specify a location for the file, then click *Save*. This saves the specified VoltageStorm analysis option settings to a VoltageStorm analysis form file (`.vsaf`) for use at a later time. Encounter saves this file as: *`default_filename`*`.vsaf`.
For example: `dtmf_chip.vsaf`. You can rename this file as needed.

Load — Opens the Load VoltageStorm Analysis Form File. Select a `.vsaf` file from this list, then click *Open* to load the VoltageStorm analysis option settings from a previous run.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `runVStorm`

Related Topics

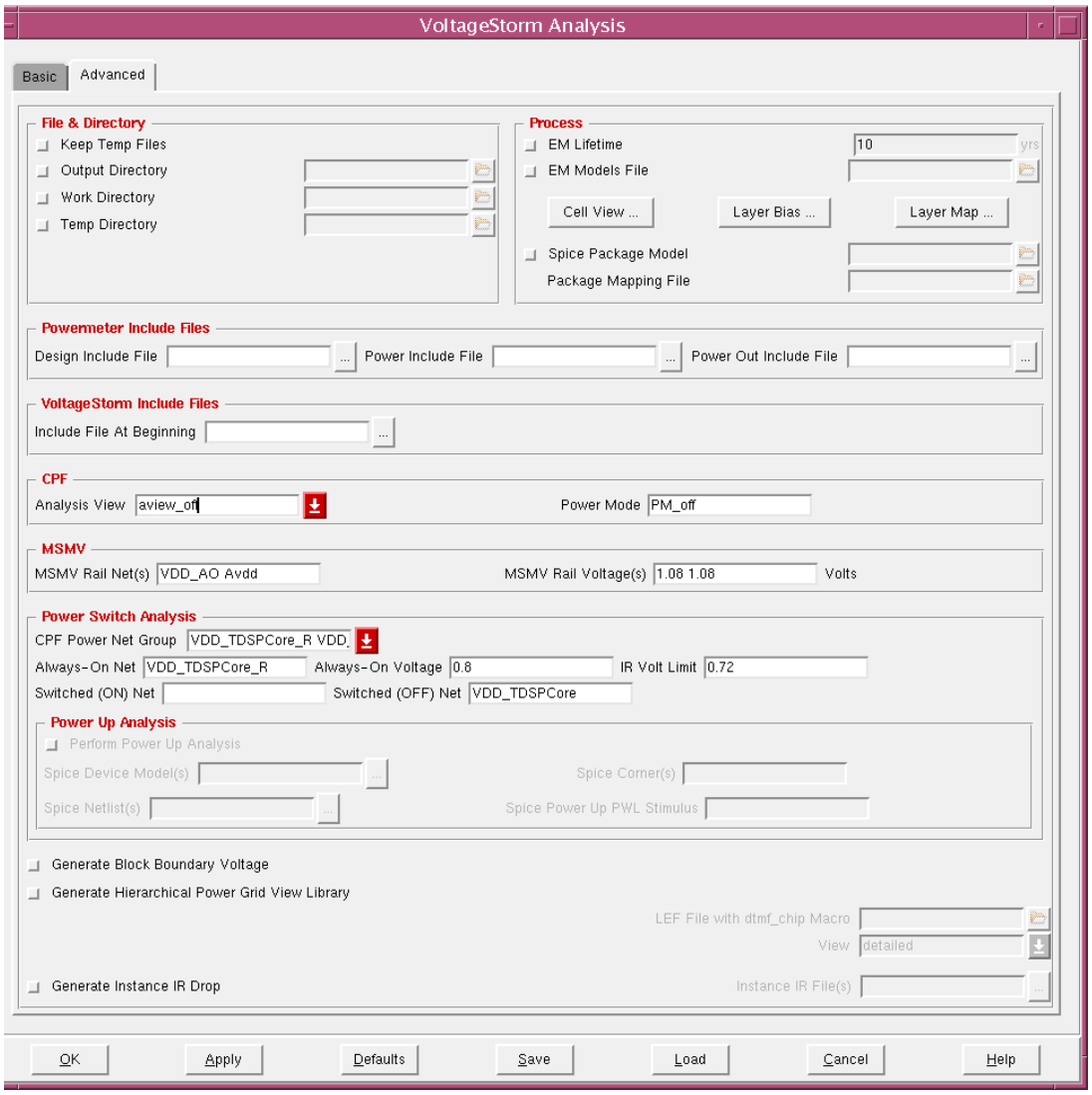
For information on the following topics, see “Power Analysis” in the *Encounter User Guide*.

- Running Power Analysis with VoltageStorm

VoltageStorm Analysis – Advanced

Use the *Advanced* page of the VoltageStorm Analysis form to specify detailed process parameters for EM and to specify inputs for detailed power grid view generation, boundary voltage generation, and instance voltage file generation.

➤ To open the Advanced page of the VoltageStorm Analysis form, choose *Power – Rail Analysis – Sign-off Analysis*, then click the *Advanced* tab.



VoltageStorm Analysis – Advanced Fields and Options

Keep Temp Files	Retains temporary files in your run directory.
Output Directory	Directory in which the VoltageStorm run results directory is created. By default, this directory is created in the current directory.
Work Directory	Directory into which VoltageStorm writes temporary work files. By default, a directory named `work` is created in the current directory and used for this purpose.
Temp Directory	Directory into which VoltageStorm writes temporary files. If you do not specify a location, temporary or unimportant intermediate files are written to the `/tmp` directory. If you do not have write permission to the `/tmp` directory, you must specify another location in order to run VoltageStorm.
EM Lifetime	Expected lifetime of the design, in years. *Default:* `10`
EM Models File	Name of an EM model file to load into the software. This file is the same one used by ElectronStorm and VoltageStorm transistor-level software.
Cell View	Opens the Cell View Specification form. For more information, see "Cell View Specification" on page 985.
Layer Bias	Opens the Layer Bias Specification form. For more information, see "Layer Bias Specification" on page 988.
Layer Map	Opens Layer Names Maps Specification form. For more information, see "Layer Names Maps Specification" on page 990.
Spice Package Model	File containing a SPICE subcircuit describing the package model. This file is generated by Allegro Package SI (also known as APE3D by Cadence) or other package-modeling products.
Package Mapping File	Specifies the name of the package terminal mapping file, which contains the mapping of the terminals of the SPICE subcircuit in the Spice package model file to the locations at the grid or top-level pins.
Design Include File	

Specifies the design include file that contain the PowerMeter command to specify a stimulus pin that the piecewise-linear (PWL) source will be applied to. For example:

```
design rSpiceDeckPWLPin "design or instance:PIN , PWL
( 0 0 400ps 0 600ps 0.8)"
```

Power Include File

Specifies the power include file that contains the PowerMeter command to generate the `static_`*`netname`*`.ptiavg` current data files when performing static power-consumption calculation with PowerMeter. For example:

```
ChipPwr rWriteStaticUTIFiles 1
```

PowerMeter creates a current data file for the following nets:

- Nets defined as power or ground nets in the DEF file
- Nets with three or more connections when more than half of the connections are power or ground nets
- Nets with two connections when both are power or ground nets
- Nets that you define as power rails

Note: PowerMeter does not use the routing data, only the connectivity data. If the net is connected by abutment and you have connectivity described in the DEF file, PowerMeter will generate the current data file. If the connectivity of abutted cells is not in the DEF file, PowerMeter will not see that these cells are connected to a power net and will not generate the current data file.

Power Out Include File

Specifies the power output include file that contains the PowerMeter command to report on the cell types in the design. You can report on the macro, I/O, combinational, sequential, or blackbox cell types. For example:

```
report_power -outfile power.report -cell_type { macro |
io | combinational | sequential | blackbox }
```

VoltageStorm Include Files

Specifies the VoltageStorm include files.

CPFAnalysis View

Specifies an analysis view. Specifies one of aview_off, aview_slow, or aview_fast

CPF Power Mode

Provides the power mode that is assigned to the specified CPF power net group. The drop-down list includes the power modes to control the switched-on or switched-off state of the power switches. This information is then passed to VoltageStorm to perform power switch steady-state analysis.

Note: You must specify the CPF power mode in conjunction with the CPF power net group to perform power switch steady-state analysis with VoltageStorm. See *CPF Power Net Group* for more information.

MSMV Rail Net(s) Specifies the multiple supply multiple voltage nets that are operating at different voltages.

MSMV Rail Voltage(s) Specifies the separate supplies that are used for the power domains operating at different voltages.

Always-On Net Specifies the always-on net.

Note: When the always-on net and switched nets (on and off) are specified and PM is disabled, you must specify multiple PM dynamic current files for each net (Basic form).

Always-On Voltage Specifies the always-on voltage.

IR Volt Limit Specifies the IR voltage limit.

Switched (ON) Net Specifies the switched-on net.

Switched (OFF) Net Specifies the switched-off net.

Perform Power Up Analysis

Specifies whether to enable the power-up analysis of a switched net in the power domain.

Note: To run power-up analysis, you must also specify the *Switched (ON) Net* and enable PowerMeter.

Spice Device Model(s)

Specifies the device SPICE models for power-up analysis. When specifying the device SPICE models, include a space between each SPICE model. The device SPICE models are required to run power-up analysis.

Spice Corner(s)

Specifies the device corners for power-up analysis. When specifying the device corners, include a space between each corner. The device corners are required to run power-up analysis.

Spice Netlist(s)

Specifies the SPICE netlists for power-up analysis. The SPICE netlists are optional if you have already included a detailed-view library (cell library generated by GDS) during analysis. If the LEF-only library was used for analysis, you must provide an external SPICE subcircuit for each cell in the design for power-up analysis.

Spice Power Up PWL Stimulus

Specifies the piecewise-linear (PWL) source that is applied to the traced control pin of the design to power-up the switched net. For example:

```
"0 0 400ps 0 600ps 0.8"
```

You can view the traced stimulus file (`switchedNet.stimulus`) after dynamic power calculation completes. You can also supply a stimulus pin using the *Design Include File*. For example:

```
design rSpiceDeckPWLPin "design or instance:PIN , PWL
( 0 0 400ps 0 600ps 0.8)"
```

Generate Block Boundary Voltage

Generates a `.pp` file including boundary voltages for every hard block in the design. This can be used at a later time for block level analysis.

Generate Hierarchical Power Grid View Library	Generates power grid view libraries during block level analysis. If you select this option, you must also specify the name of a LEF file containing a MACRO statement for the block that is being analyzed. In addition, you can specify *detailed*, *abstract*, or *reduced* as a view type.
Generate Instance IR Drop	Generates instance voltage information for IR-drop aware timing. If you select this option, you must specify the name(s) of the *Instance IR File(s)*.
LEF File with dtmf_chip Macro	
	Specifies the name of the LEF file for the block for which to generate the hierarchical power grid view. For example, if you are analyzing a block named `Block1`, set the value of this parameter to the name of the LEF file that contains a macro statement for `Block1`.
Instance IR File(s)	
	Specifies the name(s) of the instance IR file(s). Use this option with the *Generate Instance IR Drop* option.
Save	Opens the Save VoltageStorm Analysis Form File. Specify a location for the file, then click *Save*. This saves the specified VoltageStorm analysis option settings to a VoltageStorm analysis form file (`.vsaf`) for use at a later time. Encounter saves this file as: *`default_filename`*`.vsaf.` For example: `dtmf_chip.vsaf`. You can rename this file as needed.
Load	Opens the Load VoltageStorm Analysis Form File. Select a `.vsaf` file from this list, then click *Open* to load the VoltageStorm analysis option settings from a previous run.

Related Text Commands

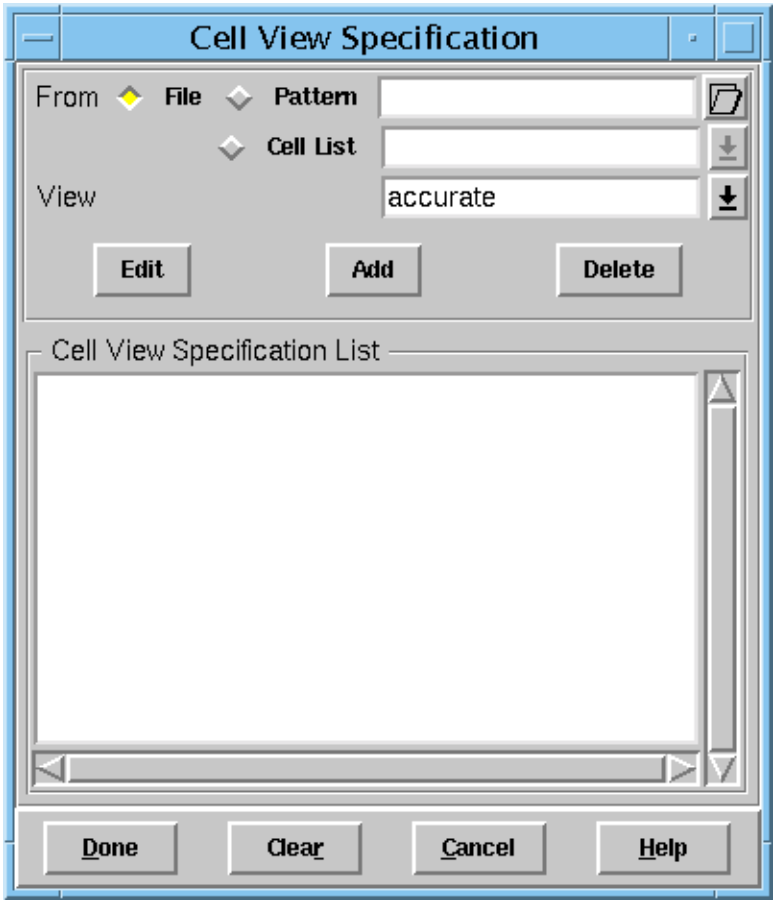
For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `runVStorm`

Cell View Specification

Use the Cell View Specification form to select the power grid view to use in modeling the cell characteristics.

➤ To open the Cell View Specification form, choose *Power – Rail Analysis – Sign-off Analysis*, then click the *Cell View* button on the *Basic* page of the VoltageStorm Analysis form.



Cell View Specification Fields and Options

From	The cells to be used in modeling cell characteristics. Select one of the following options:

File — A file that contains a list of cell names. Select this option and click the folder icon to select a file. All cells contained in the selected file should use the view that you select from the *View* pull-down menu.

Pattern — A pattern of cell names. Select this option and use the text entry field to specify a pattern. Any cell matching the specified pattern should use the view that you select from the *View* pull-down menu. For example, if you specify `*AD*` in this field and you select *port* from the *View* pull-down menu, a cell named `ADDFHX1` matches this pattern, so it uses the `port` view.

Cell List — Specific cells. Select this option and choose a cell from the drop down list. Only the named cell should use the view that you select from the *View* pull-down menu.

View

The type of view grid to be created. Detailed information about view types is available in the *VoltageStorm Hierarchical PGS Manual*.

Select one of the following options:

abstract — Creates an abstract power grid view.

accurate — Creates an accurate power grid view.

fast — Creates a fast power grid view.

floorplan — Creates a floorplan power grid view.

port — Creates a port power grid view.

reduced — Creates a reduced power grid view.

detailed — Creates a detailed power grid view.

Cell View Specification List

The list of each cell, pattern, or file along with its associated power grid view. Use the following buttons to update this list:

Edit — Populates the *From* and *View* fields with the selected item on the list.

Add	Appends the list with the information in the *From* and *View* fields.
Delete	Removes the selected item from the list.

Related Text Commands

For more information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `runVStorm -useCellView` *`type name view`*

The following VoltageStorm command provides equivalent or additional functionality:

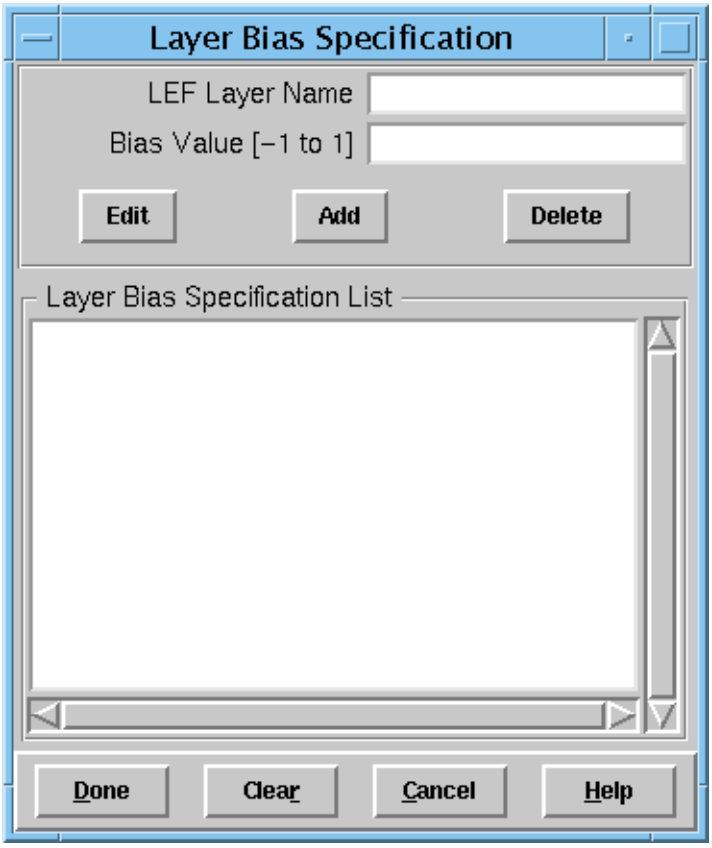
- `use_cell_view`

For more information, see the *VoltageStorm Hierarchical PGS Manual*.

Layer Bias Specification

Use the Layer Bias Specification form to adjust the size of wires within a layer to better match the widths expected when moving to silicon.

➤ To open the Layer Bias Specification form, choose *Power – Rail Analysis – Sign-off Analysis*, then click the *Layer Bias* button on the *Basic* page of the VoltageStorm Analysis form.



Layer Bias Specification Fields and Options

LEF Layer Name	The name of the LEF layer.
Bias Value [-1 to 1]	Changes the widths of wires. A positive value decreases the size and a negative value increases the size.
Edit	Populates the *LEF Layer Name* and *Bias Value [-1 to 1]* fields with the values of the item you selected in the *Layer Bias Specification List*.

Add	Adds the specified layer and associated bias value to the *Layer Bias Specification List.*
Delete	Removes the selected item from the *Layer Bias Specification List.*
Layer Bias Specification List	
	A list of LEF layer names and associated bias values.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `runVStorm -layerBias lefLayer value`

Note: The following VoltageStorm command provides equivalent or additional functionality:

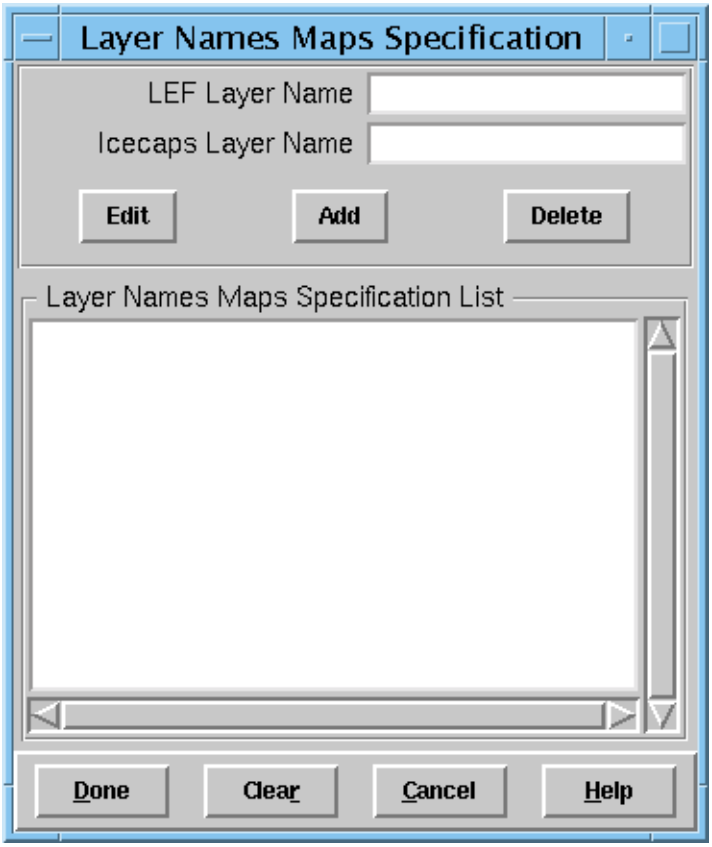
- `layer_bias`

For more information, see the *VoltageStorm Hierarchical PGS Manual*.

Layer Names Maps Specification

Use the Layer Names Maps Specification form to provide mapping information to the software if the layer names used in the `icecapts.tch` file are different from those used in the LEF and DEF files.

➤ To open the Layer Names Maps Specification form, choose *Power – Rail Analysis – Sign-off Analysis*, then click the *Layer Map* button on the *Basic* page of the VoltageStorm Analysis form.



Layer Names Maps Specification Fields and Options

LEF Layer Name	The name of the LEF layer.
Icecaps Layer Name	The name of the equivalent Icecaps layer
Edit	Populates the *LEF Layer Name* and *Icecaps Layer Name* fields with the values of the item you selected in the *Layer Names Maps Specification List*.

Add	Adds the specified layer and associated bias value to the *Layer Names Maps Specification List.*
Delete	Removes the selected item from the *Layer Names Maps Specification List.*
Layer Names Maps Specification List	
	A list of LEF layer names and associated Icecaps layer names.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `runVStorm -layerMap lefLayer icecapLayer`

Display

Opens he Display submenu, which contains the following forms and commands:

- Display Pad Location
- Clear Pad Location Display
- Display Rail Analysis Results
- Clear Rail Analysis Display
- Display Macro I Source Location
- Clear Macro I Source Location Display

Display Pad Location

Use the Display Pad Location form to display voltage source reference points, such as VCC, VDD, and VSS. These must be displayed before running power analysis. Only one file can be displayed at any time.

➤ To open the Display Pad Location form, choose *Power – Rail Analysis – Display – Display Pad Location*.

Display Pad Location Fields and Options

Pad Location File	The name of the pad location file that was created using the Edit Pad Location form. See "Edit Pad Location" on page 937.
OK	Displays the pad locations contained in the file as yellow circles in the design display area. **Note:** The yellow circles display only in the Physical view.

Related Text Commands

For information on the following command, see "Power Analysis Commands" in the *Encounter Text Command Reference*.

- `displayPadLoc`

Clear Pad Location Display

Use the *Clear Pad Location Display* command to clear the pad location circle markers.

➤ Choose *Power – Rail Analysis – Display – Clear Pad Location Display.*

Note: There is no GUI form associated with this command.

Related Text Commands

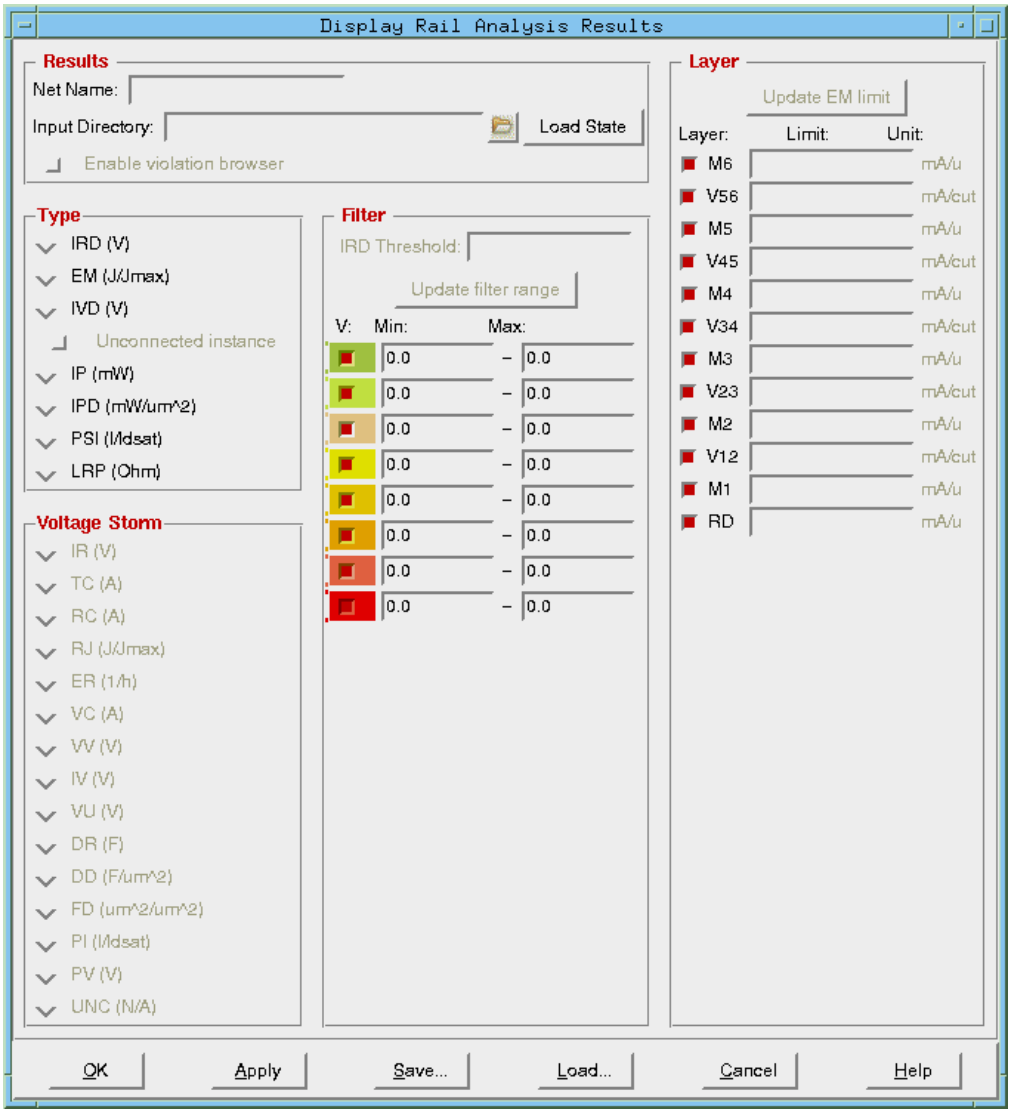
For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

■ `clearPadLocDisplay`

Display Rail Analysis Results

After you run Power Analysis, Rail Analysis, or VoltageStorm, use the Display Rail Analysis Results form to select the type of data results you want to display.

➤ To open the Rail Analysis Results Display form, select *Power – Rail Analysis – Display – Display Rail Analysis Results.*



Display Rail Analysis Results Display Fields and Options

Net Name

The net name for which rail analysis results are to be displayed.

Note: If you are displaying VoltageStorm analysis results, this must be the net for which results exist in the directory specified in the *Input Directory* field.

Input Directory

(Optional) A VoltageStorm results directory. This field is used only if you are displaying VoltageStorm analysis results. For the appropriate binary display files to exist, you must generate this directory using the VoltageStorm Analysis form or the `runVStorm` command prior to using the VoltageStorm Results Display form.

Enable violation browser

Controls the display of certain rail analysis results in the Violation Browser.

When you display *IRD*, *EM*, *IR*, or *RJ* results, all violation layout segments appear as a list in the Violation Browser.

Click one of the items in the list, or click *Select All* to select all items. The browser highlights the violation layout segment(s) and zooms into the violation area if the auto zoom feature is on.

Type

The display type options. Select one of the following:

IRD (V)

Displays the IR drop values by color. The color of the IR drop varies from green (low IR drop) to red (threshold exceeded). For example, if the voltage is 3.3 V and you set the threshold value at 0.33 V, all areas in which the IR is 2.97 V or less are displayed in red.The IR drop is 0 at the power pad locations. You can find the worst IR drop values by looking for areas of red.

Note: The values displayed represent the voltage difference from the DC source point.

EM (J/Jmax)

Displays a map that shows where the wire and via current density limits (EM) are exceeded in the design, as well as where the current density is close to the limit.

Note: To display this information, you must set the EM limits in the *Layer* section of the form.

`DCCURRENTDENSITY` values from the LEF file are used for checking EM violations in the design. If no `DCCURRENTDENSITY` value is specified in the LEF file, each field for a selected layer is populated with the worst EM value for that layer, and the display for those layers appears in the design display area.

When `DCCURRENTDENSITY` is width-dependent, the values are specified as a table in the LEF file. The power analysis software supports only the worst value (smallest current density limit) from that table

Electromigration (EM) is measured as wire and via current density. Constant DC current on narrow wire segments can cause power wires to break, resulting in failure of a chip. EM analysis always reports average current densities in the design. This is different than and independent of IR Drop analysis, in which you can specify either peak or average mode.

IVD (V)

Displays the instance voltage drop (IVD) in volts.

Unconnected Instance

If selected, displays all unconnected instances in white.

IP (mW)

Displays the instance power (IP) in milliwatts.

Provides a color gradient display of relative power distribution among a design's instances.

Instances that exhibit high power consumption are indicated by colors at the red end of the spectrum in the Encounter main window.

Note: You must provide the *Instance Power File* to display the instance power colors in the Encounter main window.

IPD (mW/um^2)

Displays the instance power density (IPD) in milliwatts/micrometers^2. The IPD is obtained by dividing the instance power by the instance area.

Provides a color gradient display of relative power density among a design's instances.

Instances that exhibit high power density are indicated by colors at the red end of the spectrum in the Encounter main window.

Note: You must provide the *Instance Power File* to display the instance power density colors in the Encounter main window.

PSI (I/Idsat)

Displays the power switch current using a ratio of the current (I) versus the saturation current (Idsat).

Provides a color gradient display of relative current distribution for all power switches in the design.

Power switches that exhibit high current consumption are indicated by colors at the red end of the spectrum in the Encounter main window.

LRP (Ohm)	Displays the wire segments with the least resistive paths (LRP) in ohms. The software tags each wire segment with a resistance value generated from the least resistive path. You can plot each wire segment with a color using the *Filter* set.
IR (V)	IR is the actual supply or ground voltage, not the IR drop value from the ideal source voltage; units are in volts.
TC (A)	Tap current is the instance current drawn; units are in amperes.
RC (A)	Resistor current; units are in amperes.
RJ (J/Jmax)	Resistor current density is relative current; the value shown is (current density / max current density).
ER (1/h)	Electromigration risk is the risk that the segment will fail; results are filtered as (1/ mean time to failure) in hours.
VC (A)	Voltage source current is the required supply current at the DC source points; units are in amperes.
VV (V)	Voltages across vias; units are in volts.
IV (V)	Instance IR is instance specific supply and ground voltage, not the IR drop; units are in volts.
VU (V)	Analyzes and reports on voltage drop across the package.
DR (F)	Analyzes and reports on decoupling capacitance required.
DD (F/um^2)	Analyzes and reports on decoupling capacitance density.
FD (um^2/um^2)	Analyzes and reports on filler density.

IRD Threshold

(Optional) An IR drop threshold value. This field is only available when you select *IRD* analysis type. If you don't specify a valid threshold, the software uses a threshold value that is 10% of the bias voltage when updating the filter ranges.

Update filter range

Populates the *Min* and *Max* values with the filter ranges defined in the results file or derived from the value that you specified in the *IRD Threshold* field.

V

The column in which you select or deselect filters. Deselecting a filter hides that range of values within the results display.This can be useful for debugging.

Min

The minimum value for the filter of the corresponding color.

Max

The maximum value for the filter of the corresponding color.

Update EM limit

Updates the electromigration limit values in the *Limit* field. When you click on the *Update EM limit* button, the electromigration limit values specified in the Specify Electromigration Limits form (*Power – Power Planning – Specify Electromigration Limits*) are displayed.

The following guidelines apply:

- If you explicitly specify the electromigration limit values in the Specify Electromigration Limits form, clicking on the *Update EM limit* button displays those values.
- If the LEF file defines the electromigration limit values and you do not explicitly specify the electromigration limit values in the Specify Electromigration Limits form, clicking on the *Update EM limit* button displays the electromigration limit values that are defined in the LEF file.
- If the LEF file does not define the electromigration limit values and you do not explicitly specify the electromigration limit values in the Specify Electromigration Limits form, clicking on the *Update EM limit* button displays the default electromigration limit values of 2 mA/um for the metal layer and 0.2 mA/cut for the via layer.

Note: You can add or update limits only if you select the *EM (J/Jmax)* display option.

Layer

The layers for which you want to display rail analysis.

Note: For *IRD*, you can only select metal layers. For all other display options, you can select metal layers and cut layers.

Limit

The EM limit for the layers for which you want to display rail analysis.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

- `displayRailAnalysisResults`

Clear Rail Analysis Display

Use the *Clear Rail Analysis Display* menu item to clear the rail analysis display. You must clear the display before you can display another rail analysis.

➤ Choose *Power – Rail Analysis – Display – Clear Rail Analysis Display.*

Note: There is no GUI form associated with this command.

Related Text Commands

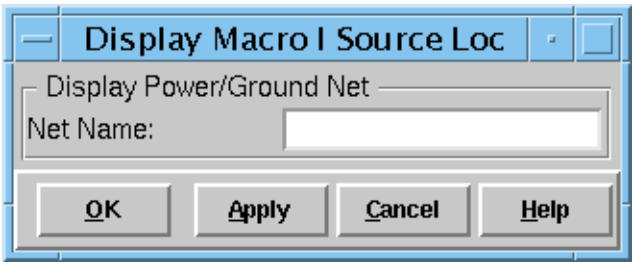
For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

■ `clearRailAnalysisDisplay`

Display Macro I Source Location

Use the Display Macro I Source Location form to display the macro current source location for blocks. (The I in the title of this form stands for *current*.) The power pins of a block are both the power source for the block's contents, and the sinks for the power grid external to the macro.

➤ To open the Display Macro I Source Location form, choose *Power – Rail Analysis – Display – Display Macro I Source Location*.



Display Macro I Source Location Fields and Options

Net Name	The power net name to be displayed.

Related Text Commands

For information on the following command, see "Power Analysis Commands" in the *Encounter Text Command Reference*.

- `displayMacroISourceLoc`

Related Topics

For information on the following topic, see "Power Analysis" in the *Encounter User Guide*.

- Displaying Macro Current Source Locations

Clear Macro I Source Location Display

Use the *Clear Macro I Source Location Display* menu item to clear the macro current source display.

➤ Choose *Power – Rail Analysis – Display – Clear Macro I Source Location Display*.

Note: There is no GUI form associated with this command.

Related Text Commands

For information on the following command, see “Power Analysis Commands” in the *Encounter Text Command Reference*.

■ `clearMacroISourceLocDisplay`

9

Place Menu

- Specify on page 1006
- Place Jtag on page 1015
- Standard Cells on page 1017
- Place Flip Chip I/O on page 1019
- Refine Placement on page 1023
- ECO Placement on page 1026
- Place Spare Cell on page 1028
- Filler on page 1035
- Tie HI/LO on page 1050
- Scan on page 1055
- Check Placement on page 1059
- Display on page 1062

Specify

The *Place* menu's Specify forms enable you to specify and assign spare cells, scan cells, JTAG cells, and placement blockage for power and ground stripes. You must assign these objects before running placement.

The *Specify* submenu provides access to the following features:

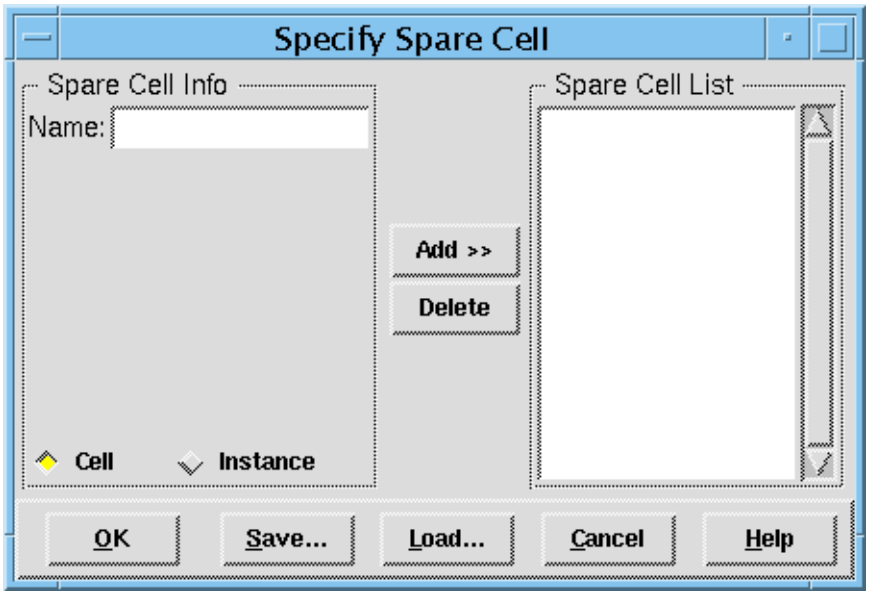
- Spare Cells on page 1007
- Cell Padding on page 1009
- Jtag Cells on page 1011
- Placement Blockage on page 1013

Spare Cells

Use the Specify Spare Cell form to assign cell types or modules that are designated as spare cells in the design.

Note: The module that contains the spare gates should be guided during the floorplanning session to localize the spare gate cell placements.

➤ Choose *Place – Specify – Spare Cells*.



Specify Spare Cells Fields and Options

Name	Specifies the library cell of instance to designate as a spare cell.
Cell	Specifies that *Name* is a library cell. Use this option for for leaf cells (standard cells) only—it cannot be used for spare modules.
Instance	Specifies that *Name* is an instance of a library cell.
Add >>	Adds *Name* to the *Spare Cell List*.
Delete	Removes *Name* from the *Spare Cell List*.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `specifySpareGate`

Tip

For cases where several spare cells are specified, it is faster to use the `specifySpareGate` command than the Specify Spare Cell form.

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Specifying Spare Cells

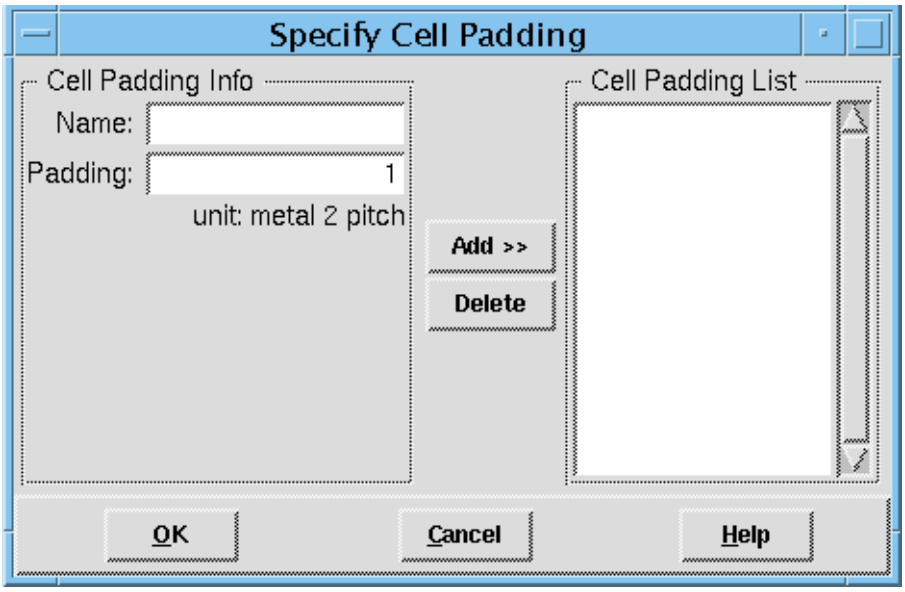
Cell Padding

Use the Specify Cell Padding form to assign cell types, such as clock flip-flops, with a small placement clearance so that a buffer can be inserted during clock tree synthesis. When the cell is placed, this clearance is on the right side of the cell. Cell padding is retained during optimization and CTS. If there are any congestion problems, delete the cell padding.

Use the `deleteAllCellPad` command to remove the padding.

➤ Choose *Place – Specify – Cell Padding*.

Note: You can also save or load the spare cell information to or from the floorplan file.



Specify Cell Padding Fields and Options

Name	Specifies the cell to which to add or delete padding.
Padding	Specifies the numerical value of the padding dimension. The value is multiplied by the *metal2* pitch value to determine the padding dimension. The *metal2* pitch value is read from the technology file. *Default:* one *metal2* pitch.
Add >>	Adds the pad assignment to the *Cell Padding List*.
Delete	Removes the pad assignment from the *Cell Padding List*.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `specifyCellPad`

Related Topics

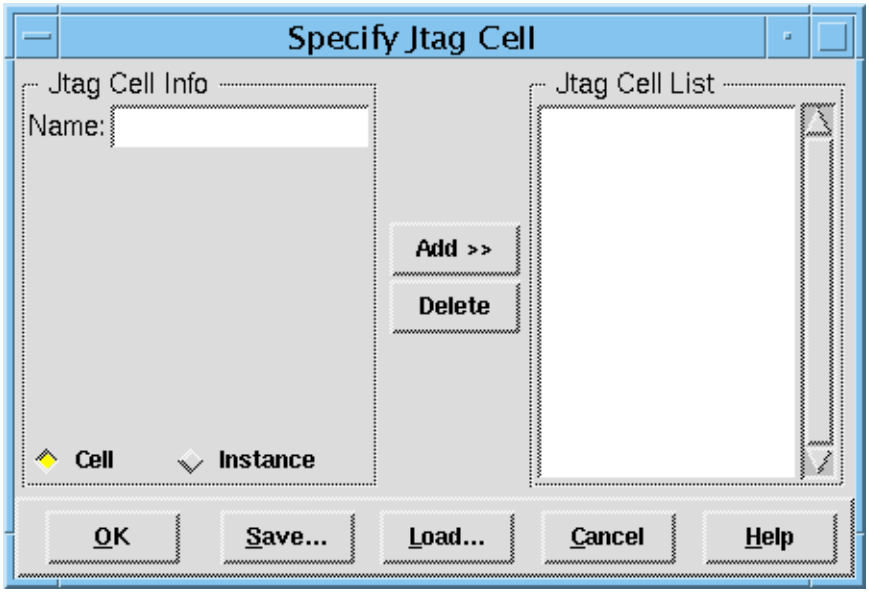
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Specifying Cell Padding

Jtag Cells

Use the Specify Jtag Cell form to specify the modules that contain the JTAG logic. You can also use this form to save and load your specification data.

➤ Choose *Place – Specify – Jtag Cells*.



Specify Jtag Cells Fields and Options

Name	Specifies a cell or instance. If you select *Instance*, you can use the asterisk wildcard (*) character.
Cell	Marks all instances of the specified cell type as JTAG instances.
Instance	Marks an instance as a JTAG instance. You can use a wildcard (*) character for this parameter.
Add >>	Adds *Name* to the *Jtag Cell List*.
Delete	Removes *Name* from the *Jtag Cell List*.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `specifyJtag`

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Running JTAG Placement

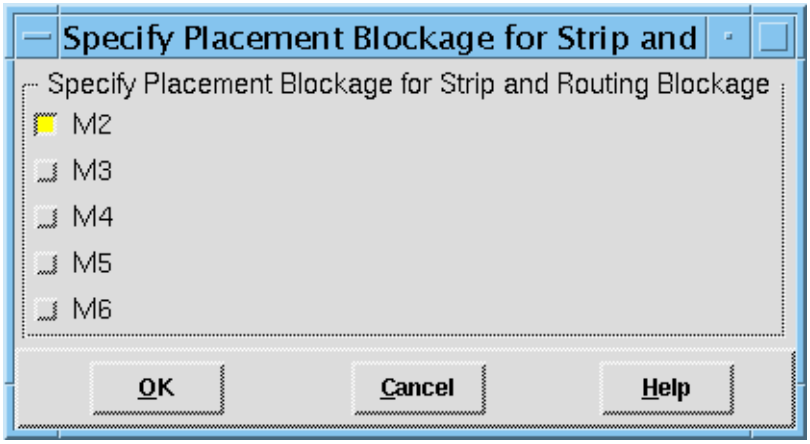
Placement Blockage

Use the Specify Placement Blockage for Strip and Routing Blockage form to treat routing blockage objects and wires with the DEF attribute + `SHAPE STRIPE` on the specified layers as placement blockages so that placement commands do not place cells under them.

Note: Preplaced instances are not moved by the placement commands, even if they violate the specified blockage.

Note: Fillers are still added under preroute wires.

➤ Choose *Place – Specify – Placement Blockage*.



Note: For fine but dense power lines, deselect the metal layers in the form. Cells will be positioned underneath the power stripes, and will not block the interconnection.

Specify Placement Blockage for Strip and Routing Blockage Fields and Options

M2 M3 M4 M5 M6

Specify the metal layer numbers.

The default value is set after the library is read in by the floorplan section, and depends on the number of routing layers in the design.

- In designs with one, two, or three routing layers, preroutes on all layers are treated as obstructions. For example, in a three-layer design, preroutes on M1 M2, and M3 are treated as obstructions by default.
- In designs with more than three routing layers, only M1 and M2 preroutes are treated as obstructions by default. For example, in a five-layer design, preroutes on M1 and M2 are treated as obstructions by default.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `setPrerouteAsObs`

Related Topics

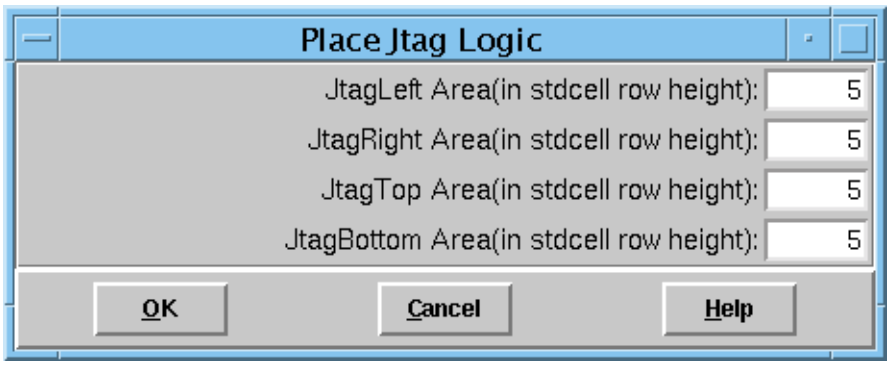
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Guiding Placement With Blockages

Place Jtag

Use the Place Jtag Logic form to place JTAG instances close to their I/O pads.

➤ Choose *Place – Place Jtag*.



Place Jtag Logic Fields and Options

Jtag Left Area	Specifies the standard cell row height for the left side of the JTAG placement area. *Default:* 5 (approximately five times the standard cell height. This creates a temporary placement blockage layer during JTAG placement, and is removed thereafter.
Jtag Right Area	Specifies the standard cell row height for the right side of the JTAG placement area. *Default:* 5 (approximately five times the standard cell height. This creates a temporary placement blockage layer during JTAG placement, and is removed thereafter.
Jtag Top Area	Specifies the standard cell row height for the top of the JTAG placement area. *Default:* 5 (Places the JTAG instance within five standard cell rows at the top of the chip.)
Jtag Bottom Area	Specifies the standard cell row height for the bottom of the JTAG placement area. *Default:* 5 (Places the JTAG instance within five standard cell rows at the bottom of the chip.)

Related Text Commands

For information on the following commands, see the “Placement Commands” chapter in the *Encounter Text Command Reference*.

- `placeJtag`
- `traceJtag`

Related Topics

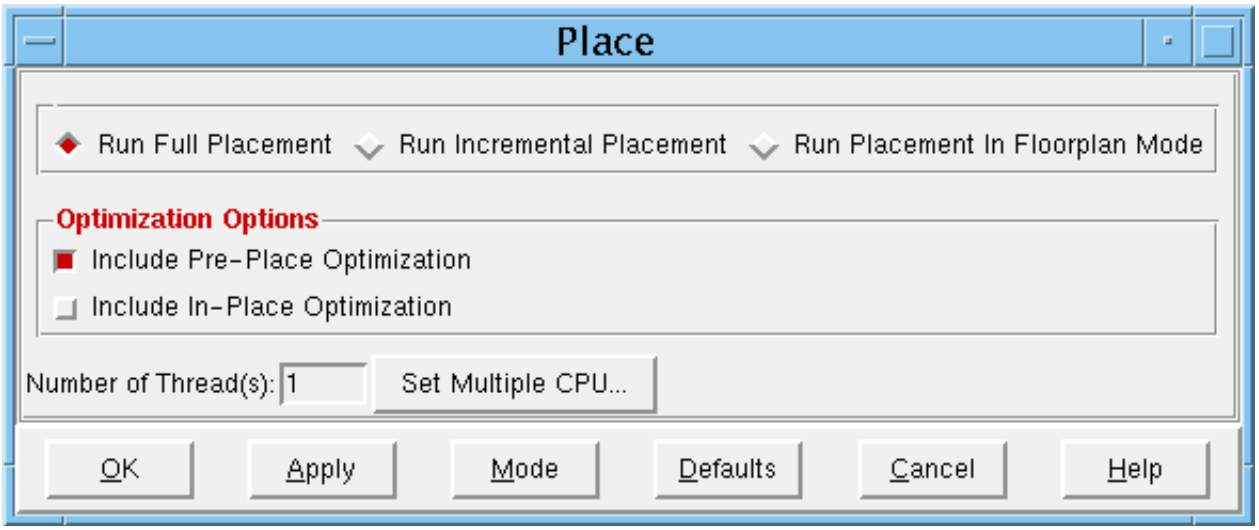
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Running JTAG Placement

Standard Cells

Use the *Place* form to place standard cells in the design based on the global settings for placement, RC extraction, timing analysis, and trial routing. The placement commands consider the modules that were placed (guided) during floorplanning, and take into account the design's hierarchy and connectivity.

➤ Choose *Place – Standard Cells*.



Place Fields and Options

Run Full Placement

Runs placement in timing-driven mode, based on the global settings for placement, RC extraction, timing analysis, and trial routing.
Default: On

Run Incremental Placement

Reruns placement in timing-driven mode while honoring current placement.
Default: Off

Run Placement in Floorplan Mode

Runs a quick placement to gauge the feasibility of the netlist, but might not place components in legal locations. This mode assumes non-timing-driven placement.
Default: Off

Note: In this mode the *Include In-Place Optimization* option is disabled.

Optimization Options
Include Pre-Place Optimization

Simplifies the netlist, for example, by deleting buffer trees, before running placement.
Default: On

Include In-Place Optimization

Runs netlist optimization between placement iterations in order to improve instance placement of timing-critical paths.
Default: Off

Number of Threads

Displays the number of threads to use for multiple-CPU processing.

Note: This is a non-editable field. To edit this field, select *Set Multiple CPU*.

Set Multiple CPU

Opens the Multiple CPU Processing form. For more information, see "Multiple CPU Processing" on page 373.

Related Text Command

For information on the following command, see "Placement Commands" in the *Encounter Text Command Reference*.

- `placeDesign`

Related Topics

For information on the following topics, see "Placing the Design" in the *Encounter User Guide*.

- Placing Standard Cells

Place Flip Chip I/O

Use the Place Flip Chip I/O form to place area and peripheral I/O cells.

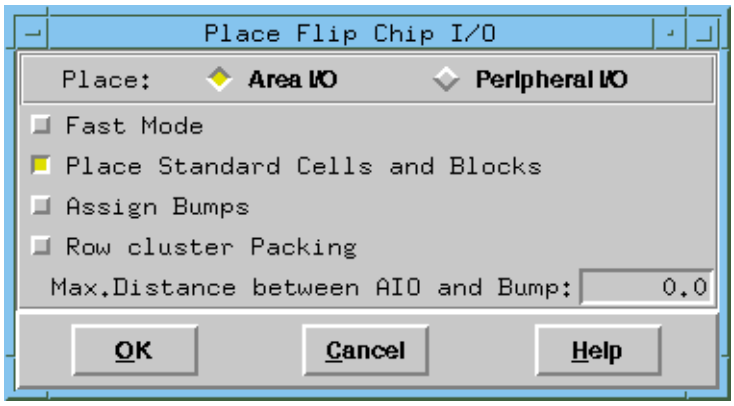
➤ Choose *Place – Place Flip Chip I/O*.

Place Area I/O

➤ Select *Area I/O* to place I/O driver cells.

Important

Load the area I/O library when importing the design. Area I/O rows are also required.



Place Area I/O Fields and Options

Area I/O	Places area I/O driver cells.
Peripheral I/O	See Place Peripheral I/O.
Fast Mode	Runs area I/O placement in fast mode, trading quality for speed.
Place Standard Cells and Blocks	Places standard cell instances and blocks with the area I/O instances. *Default:* On

Assign Bumps

Connects area I/O instances to the nearest unassigned bumps if there are unassigned bumps for area I/O instance connections.

Note: You can also assign bumps after area I/O placement by using the `assignBump` text command.

Row Cluster Packing

Specifies the packing of I/O driver instances within each cluster of rows.

Note: This option is only applicable to designs with clusters of I/O rows.

Max. Distance between AIO and Bump

Specifies the maximum allowable distance between the area I/O instances and the bumps, in microns.

Related Text Commands

For information on the following command, see “Flip Chip Commands” in the *Encounter Text Command Reference*.

- `placeAIO`

Related Topics

For information on the following topic, see “Flip Chip and Area I/O” in the *Encounter User Guide*.

- Flip Chip Flow

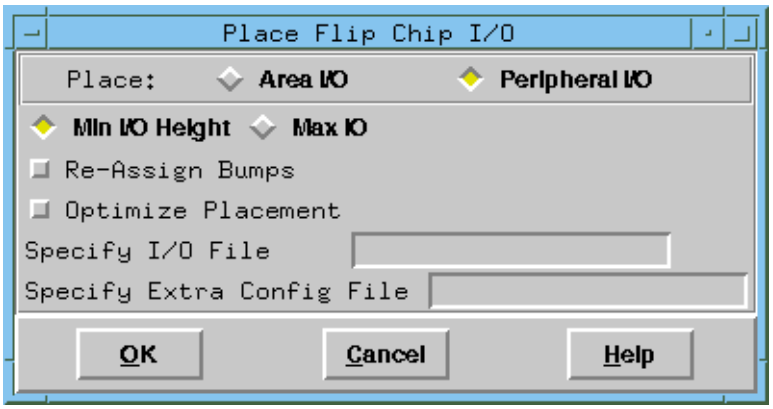
Place Peripheral I/O

➤ Select *Peripheral I/O* to place I/O cells defined as `CLASS PAD AREAIO` on the boundary of the design.

`PAD` cells are placed close to the assign bumps. If the bumps are not assigned, the `PAD` cells are placed close to any unassigned bump in a random order.

Important

Load the peripheral I/O library when importing the design.



Place Area I/O Fields and Options

Area I/O	See Place Area I/O.
Peripheral I/O	Places I/O cells defined as `CLASS PAD AREAIO` on the boundary of the design.
Min IO Height	Specifies the minimum height for the I/O row
Max IO Height	Specifies the maximum height for the I/O row.
Reassign Bumps	Allows signal bumps to be reassigned to improve routing if the I/O cells have been fixed.
Optimize Placement	Allows I/O pads to be moved to improve routing if the bumps have been fixed.
Specify IO File	Specifies the name of a file to control the placement of the I/O cells.

Specify Extra Config File	Specifies an extra configuration file for additional command support.

Related Text Commands

For information on the following command, see “Flip Chip Commands” in the *Encounter Text Command Reference*.

- `placePIO`

Related Topics

For information on the following topics, see Peripheral I/O Flow in the *Encounter User Guide*.

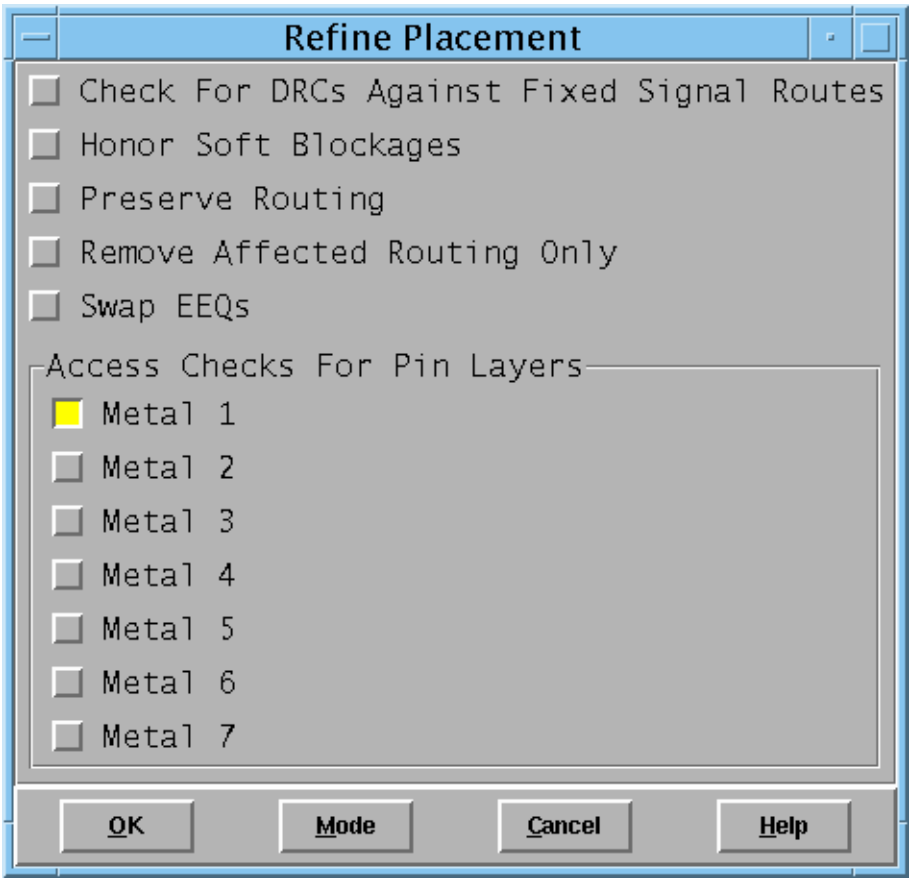
- Place peripheral I/O pads
- Optimize peripheral I/O placement
- Reassign Bumps

Refine Placement

Use the *Refine Placement* form to correct flawed cell locations and report corrections or instance overlap problems.

You do not need a fully placed design in order to refine placement.

➤ Choose *Place – Refine Placement*.



Refine Placement Fields and Options

Check For DRCs Against Fixed Signal Routes

Considers pre-routed `FIXED` signal wires and avoids creating DRC violations between `FIXED` signal wires and instance pins. When this option is not selected, the software ignores `FIXED` signal wires.

Default: Off

Note: Running placement with this option selected might result in longer run time.

Honor Soft Blockages

Specifies that soft blockages will be considered when running the command. Soft blockages are different from density screens (partial blockages). Partial blockages are never considered during `refinePlace`.

Default: Soft placement blockages are considered only during global placement, and are ignored during `refinePlace` and optimization stages.

Preserve Routing

Preserves all routed wires.
Default: Off. Refine Placement removes all wires.

Remove Affected Routing Only

Removes wires connected to moved cells.
Default: Off. Refine Placement removes all wires, whether connected cells were moved or not.

Swap EEQs

Specifies whether master cells can be replaced by EEQ cells during detailed placement to improve routability. After detailed placement, the software reports the number of replacements. EEQ cells are defined in the LEF file.
Default: Off

Access Checks For Pin Layers

Specifies the layers to check for pin access.
Default: 1

Related Text Commands

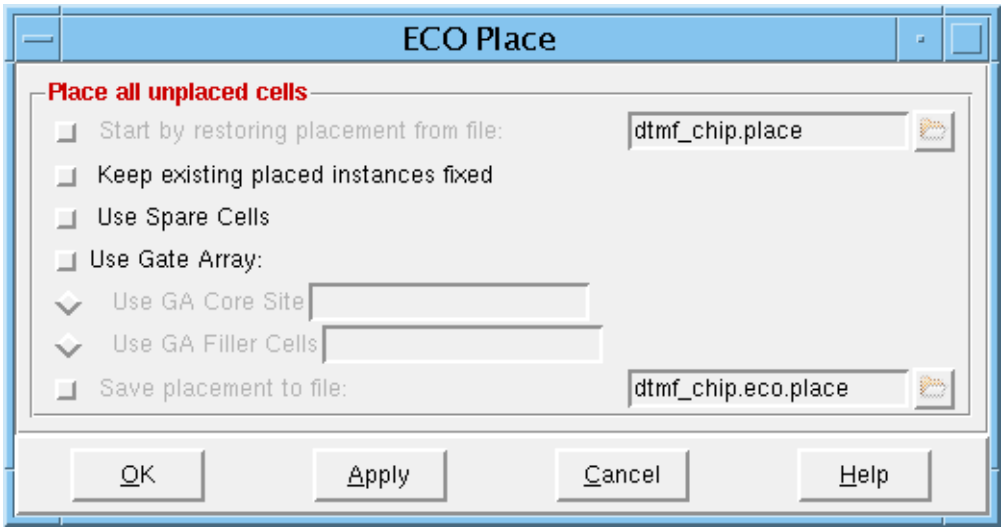
For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `refinePlace`

ECO Placement

Use the ECO Place form to run netlist ECO (Engineering Change Order) placement. You can set global options for incremental placement of standard cells. In a pre-mask flow, this command moves the unplaced standard cells into the core area. In a post-mask flow , the software can map the unplaced cells to the available spare cells. Use this form for minor design changes. The ECO for logic changes should not exceed 20 percent from the previous imported design.

➤ Choose *Place – ECO Placement*.



ECO Place Fields and Options

Start by restoring placement from file:

Restores an existing placement file before placing ECOs. This placement file is saved from the previous netlist that was imported and placed in the Encounter software. Running ECO Placement will change this design as per the new imported netlist. The placement file format must be from the Encounter software.

Keep existing placed instances fixed

Specifies that instances with the PLACED status are not moved.

Use Spare Cells	Maps unplaced cells to spare cells during placement. First, checks whether all unplaced cells match spare cells. Next, chooses a spare cell and changes the connections from the unplaced cell to the selected spare cell. Finally, deletes the unplaced cell. You can use this parameter only for post-mask ECO. This option observes the power domain when selecting the spare cell and maps an unplaced cell to the spare cell in the power domain, based on the instance name of the cell. For example, if module A/B is defined for power domain PD2, this option will map an unplaced cell A/B/inst1 to a spare cell in module A/B.
Use GA Core Cells	Specifies a list of Gate Array (GA) cells. The tool matches the GACoreSite to available spare cells. The tool chooses a spare cell and changes the connections from the unplaced cell to the selected spare cell. You can use this parameter only for post-mask ECO.
Use GA Filler Cells	Specifies a list of Gate Array (GA) filler cells that the tool can replace with GA cells during post-mask ECO. You can only use this parameter in a post-mask ECO flow. The new logic instances adding during a post-mask flow must already be present in the netlist.
Save Placement to file	Specifies the filename to save the placement results.

Related Text Commands

For information on the following command, see “Interactive ECO Commands” in the *Encounter Text Command Reference*.

- `ecoPlace`

Related Topics

For information on the following topic, see “ECO Placement” in the *Encounter User Guide*.

- Running ECO Placement

Place Spare Cell

Use the Spare Cell form to place a group of designated instances together as a spare module, with a constraint in the floorplan file, and distributed across the design by the number of rows and columns. The use of modules helps to ensure that the designated spare instances stay together, and makes it easy to place multiple copies of the group in the design. This can be done after placement.

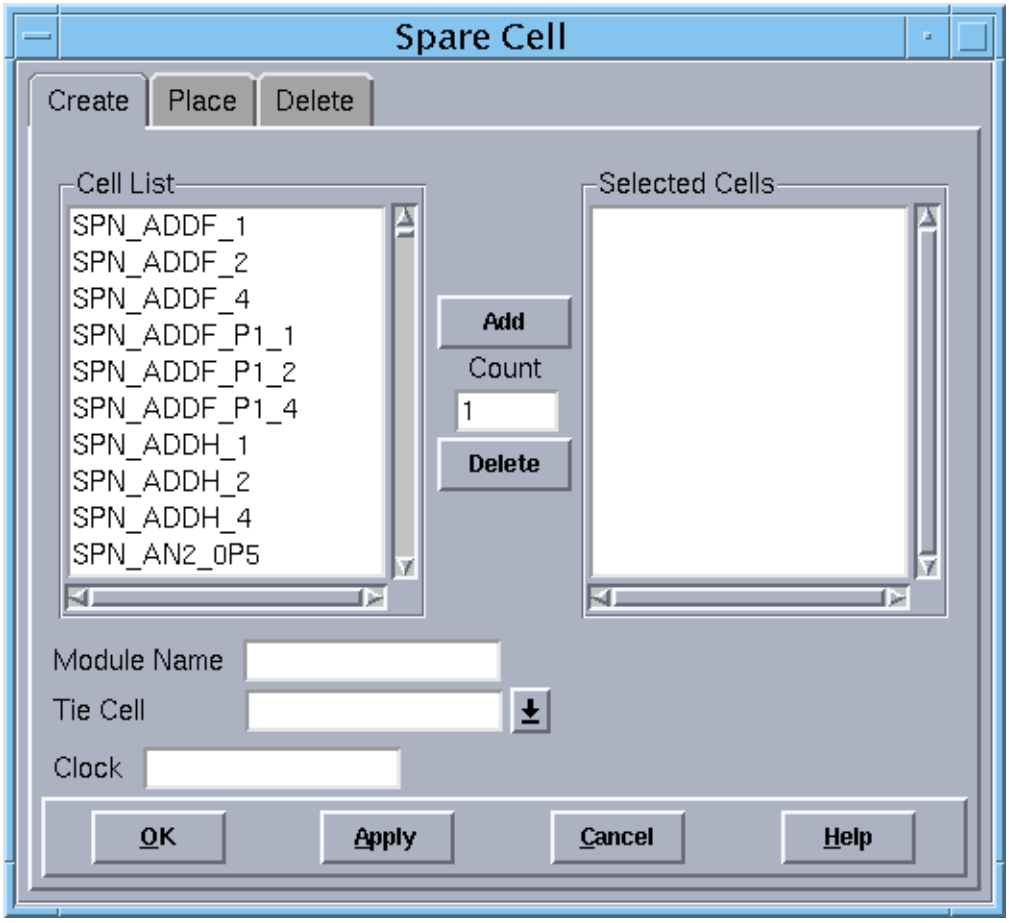
The Spare Cell form contains the following pages:

- Spare Cell - Create on page 1029
- Spare Cell - Place on page 1031
- Spare Cell - Delete on page 1033

Spare Cell - Create

Use the *Create* page of the Spare Cell form to specify the cells to add to a module and to name the module.

➤ Choose *Place – Spare*, then click the *Create* tab.



Spare Cell – Create Fields and Options

Cell List	Displays a list of spare cells that can be added to the module.
Selected Cells	Displays the list of spare cells that are selected to add to the module.
Add	Adds highlighted cells in the *Cell List* to the *Selected Cells* box.

Count	Displays the number of cells in the *Selected Cells* box.
Delete	Removes highlighted cells from the *Selected Cells* box.
Module name	Specifies a name for the spare module to add to the netlist.
Tie Cell	Specifies a tie-high or tie-low cell to add to the spare module.
Clock	Specifies the clock to add to the spare module.

Related Text Commands

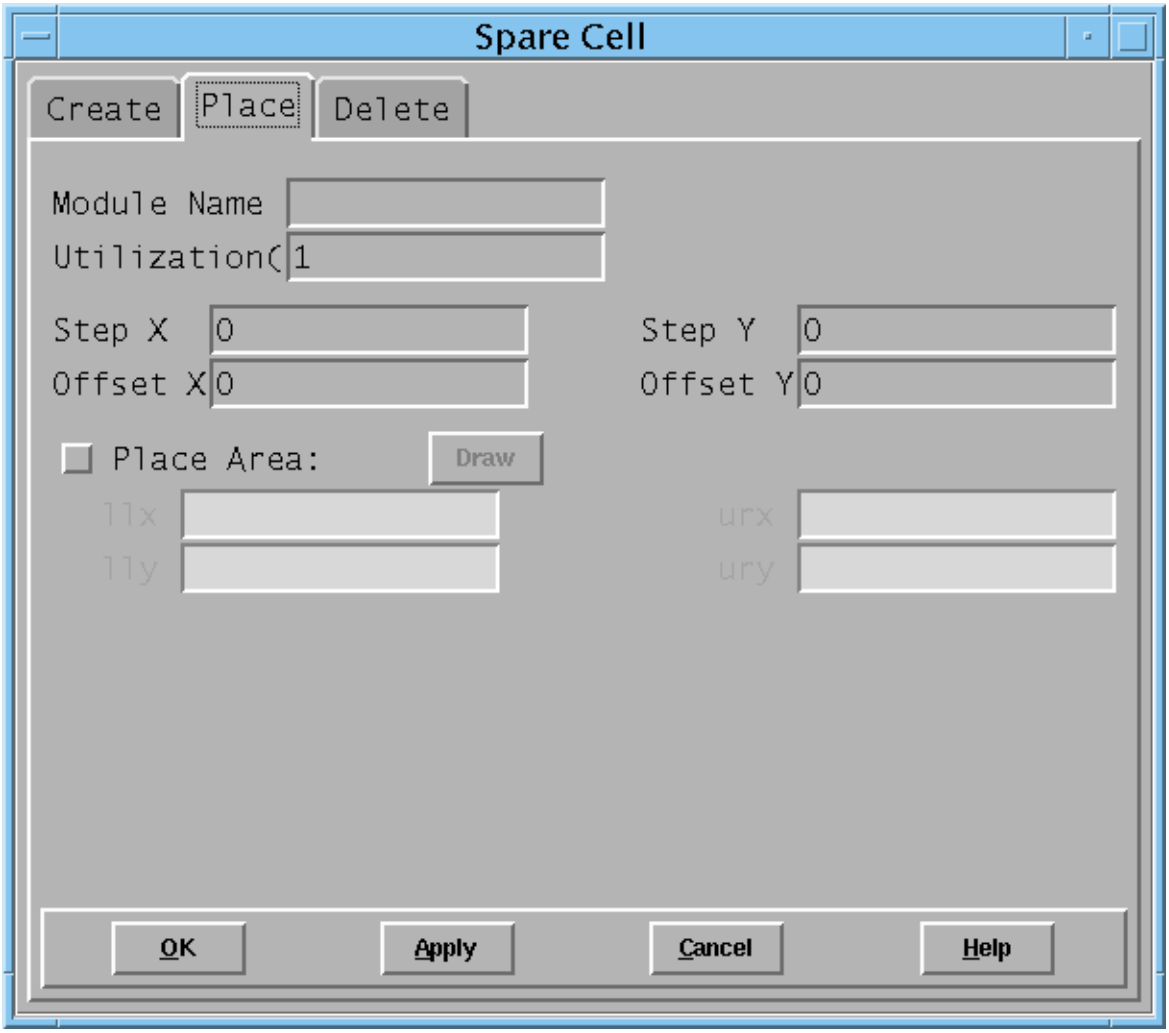
For information on the following commands, see “Placement Commands” in the *Encounter Text Command Reference*.

- `createSpareModule`
- `deleteSpareModule`
- `placeSpareModule`

Spare Cell - Place

Use the *Place* page of the Spare Cell form to instantiate the created spare module and place copies of the spare module across the design. You can place spare modules before or after placement. To place them after placement, the software runs ECO placement.

➤ Choose *Place – Spare*, then click the *Place* tab.



Spare Cell – Place Fields and Options

Module name	Specifies the name of the spare module.

Utilization	Specifies the utilization factor of the spare modules. *Value Range:* More than `0.0` and less than `1.0`
Step X	Specifies the distance, in microns, between the instantiated spare modules along the x axis. The distance must be greater than the spare module bounding box.
Step Y	Specifies the distance, in microns, between the instantiated spare modules along the y axis. The distance must be greater than the spare module bounding box.
Offset X	Specifies the offset along the x axis, in microns, from the left core boundary.
Offset Y	Specifies the offset along the y axis, in microns, from the left core boundary.
Place Area	Specifies an area in the design where the spare modules are placed. You can select the *Draw* button, click in the design display area, and draw a box to retrieve the x and y coordinates.

Related Text Commands

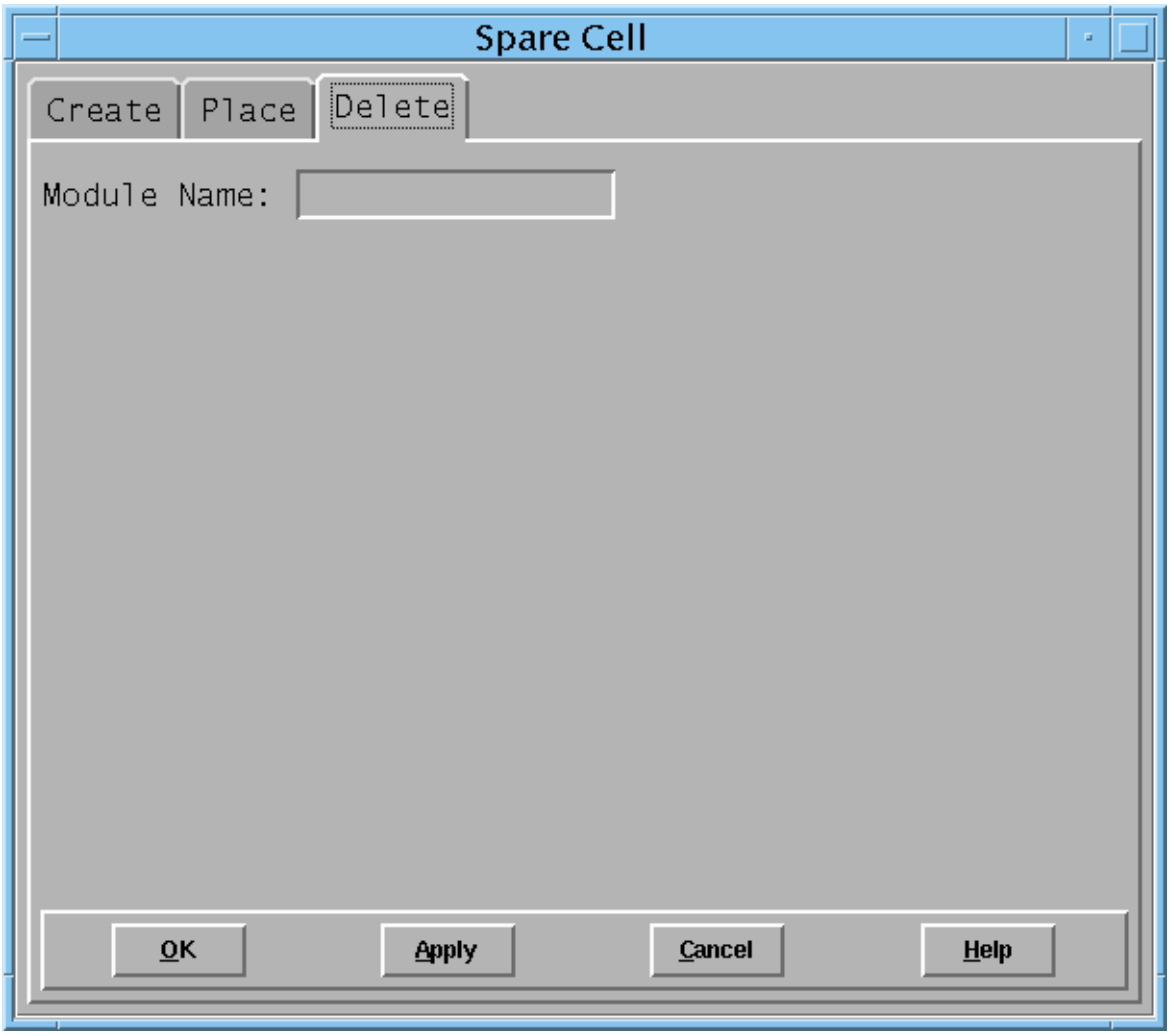
For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `createSpareModule`
- `deleteSpareModule`
- `placeSpareModule`

Spare Cell - Delete

Use the *Delete* page of the Spare Cell form to delete the spare module from the netlist.

➤ Choose *Place – Spare*, then click the *Delete* tab.



Spare Cell - Delete Fields and Options

Module Name	Specifies the name of the spare module.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `createSpareModule`
- `deleteSpareModule`
- `placeSpareModule`

Filler

The *Place* menu's Filler forms enable you to add or delete filler, well tap, end cap, and I/O filler cells.

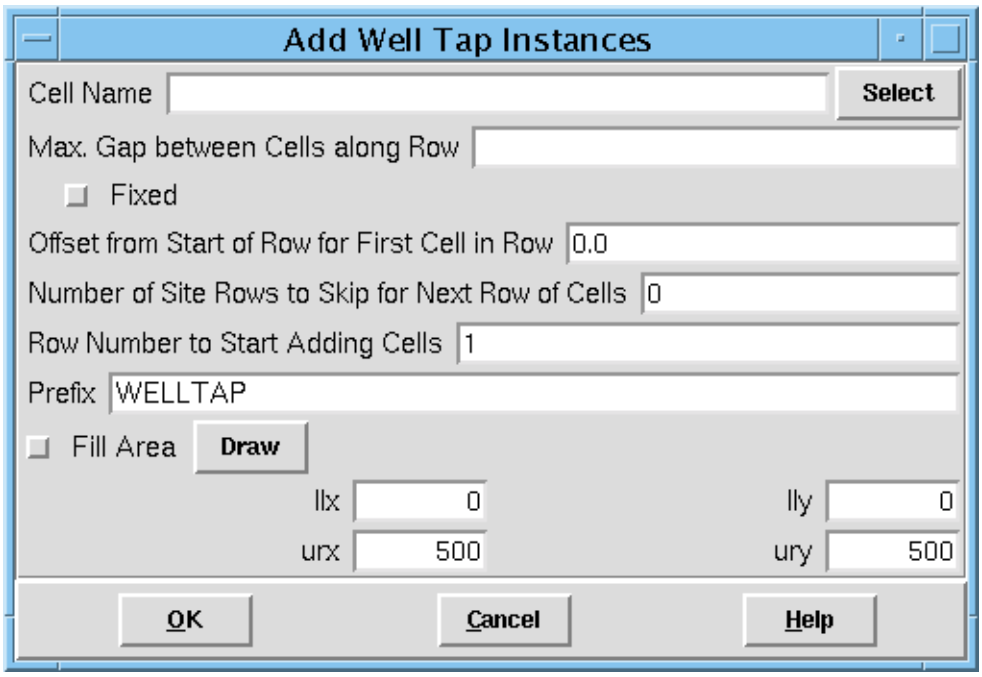
The *Filler* submenu provides access to the following features:

- Add Well Tap on page 1036
- Add End Cap on page 1039
- Add Filler on page 1041
- Delete Filler on page 1044
- Add IO Filler on page 1046
- Delete IO Filler on page 1048

Add Well Tap

Use the Add Well Tap Instances form to place physical-only well-tap cells.

➤ Choose *Place – Filler – Add Well Tap*.



Add Well Tap Instances Fields and Options

Cell Name

Specifies the name of the cell in the technology library of class type `CORE` to use as a well-tap. You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.

Max. Gap between Cells along Row

Specifies the distance, in microns, between two consecutive well-tap cells on a row. If well-tap cells cannot be placed at this gap due to placement blockage, the software will search for a legal location: first towards the previous well-tap, and then away from the specified location. Under no circumstances can the gap between well-taps be less than half of the *Max. Gap* value.

Fixed

Ensures that the specified gap is always maintained. The software does not search for a legal location if it cannot place well-tap cells at the specified *Max. Gap*. Instead, it goes on to place well-tap cells at the next position.

Offset from Start of Row for First Cell in Row

Specifies the offset, in microns, of the first well-tap cell from the start of the site row.
Default: `0` (The first cell on beginning of row is the starting point.)

Number of Site Rows to Skip for Next Row of Cells

Specifies the row number from bottom (or left) on which the well-taps have to be placed.
Default: `1` (Specifies that the first row from the bottom is the starting point.)

Prefix

Specifies the prefix for the placed instances. The generated name for the instance uses this prefix as `prefix_`*`uniqueString`*.
Default: `WELLTAP`

Important

Do not include an underscore at the end of the prefix.

Fill Area

Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction.

You can type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates.

Note: If the area is not defined properly, well-tap instances are not added.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `addWellTap`

Related Topics

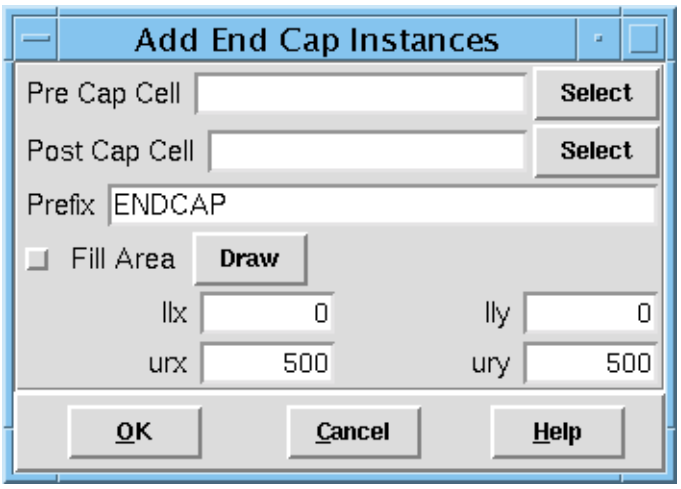
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Filler Cells

Add End Cap

Use the Add End Cap Instances form to place physical-only end-cap cells at the ends of the site rows.

➤ Choose *Place – Filler – Add End Cap*.



Add End Cap Instances Fields and Options

Pre Cap Cell

Specifies the name of the cell in the technology library to use to cap the beginning of each site row.

You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.

Post Cap Cell

Specifies the name of the cell in the technology library to use to cap the end of each site row.

You can type the cell name, or click *Select* to open a list of cells where you can click a cell name and click *OK* to add the cell name to the field.

Prefix

Specifies the prefix for the placed instances. The generated name for the instance uses this prefix as `prefix_`*`uniqueString`*. The default is `ENDCAP`.

Important

Do not include an underscore at the end of the prefix name.

Fill Area

Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction.

You can type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates.

Note: If the area is not defined properly, end cap instances will not be added.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `addEndCap`

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Filler Cells

Add Filler

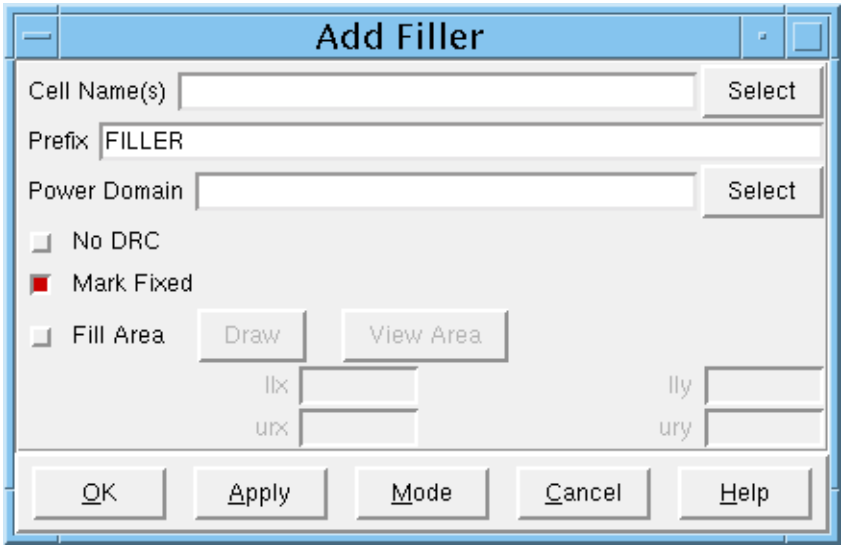
Use the Add Filler form to insert filler cell instances between the gaps of standard cell instances. If the design is routed, the software does DRC checks of the filler cells added to the wires in the design. It does not check adjacent cells. This process ensures that adding filler cells is fast enough to be used many times in the design flow.

To resolve adjacent cell DRC violations created by the insertion of filler cells, run Verify Geometry to mark these violations. Then, use Add Filler with *No DRC* turned off to add more filler cells to replace filler cells that cause violations.

> **Note:** This command resolves only filler-related violations—it cannot resolve net-based violations. To repair net-based violations, reroute the net with violations.

Add Filler recognizes up to five implant layers and attempts to honor implant layer width and spacing rules within each implant layer. If it does not find the correct filler cell to add to an implant layer, it tries to add “no-implant” filler cells. If it cannot add the “no-implant” cells, it inserts a filler cell that is large enough that it does not violate the minimum width rule of the relevant implant layer.

➤ Choose *Place – Filler – Add Filler*.



Add Filler Fields and Options

Cell Name(s)	Specifies the cell name(s) of the filler cell instance. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *Add* includes the cell name(s) to the *Cells List* and *Cell Name(s)* field. Highlighting a cell or cells in the *Cells List* and clicking *Delete* removes the cell name(s) from both areas.
Prefix	Specifies the prefix for the added filler cell instances. *Default:* `FILLER`
Power Domain	Specifies the power domain in which the fillers are to be inserted. If this parameter is not specified, and a list of filler cells is specified with *Cell Name(s)*, the software tries to add fillers to all power domains. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Power Domain List*. Clicking *Add* includes the cell name(s) in the *Cells List* and *Cell Name(s)* field. Highlighting a cell or cells in the *Cells List* and clicking *Delete* removes the cell name(s) from both areas.
No DRC	Disables postroute DRC violation checking against existing net routing. By default, if filler cells are added after routing, the software checks for DRC violations between regular nets and the filler cells. *Default:* Off
Mark Fixed	Marks added fillers as `FIXED`. *Default:* On

Fill Area

Specifies an area to fill. Specify values for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction.

Use *Draw* to click and drag a window around the area in the design display area. This will automatically update the values for the boundaries.

Note: If the area is not defined properly, no filler cells are added.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `addFiller`

Related Topics

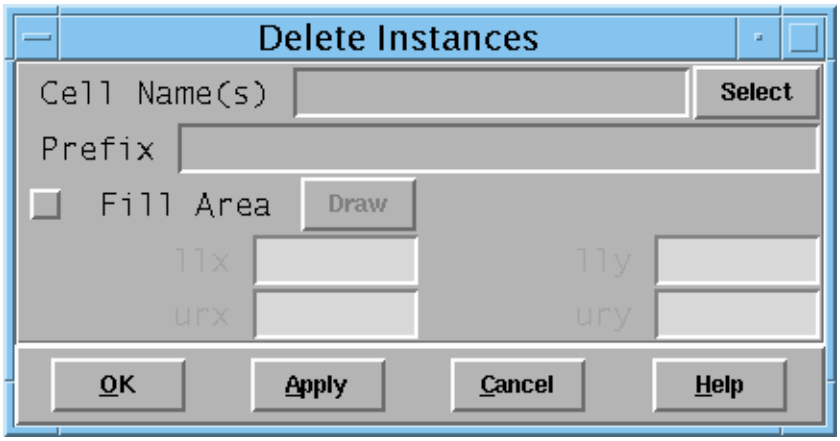
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Filler Cells

Delete Filler

Use the Delete Instances form to remove physical cell instances, filler cells, end-cap cells, and well-tap cells from standard cell rows.

➤ Choose *Place – Filler – Delete Filler*.



Delete Instances Fields and Options

Cell Name

Specifies the cell name, or list of cells, to remove. Separate cell names with spaces.

Type the cell name, or click *Select* to open the a list of cells where you can click a cell name and click *Add* to add the cell name(s) to the field.

Prefix

Specifies the prefix of the filler cell instances to remove.

Important

This command adds an underscore at the end of the provided prefix while checking it against the instance names.

Fill Area

Specifies the coordinates of the bounding box, in microns, for the lower left (*llx*) and upper right (*urx*) boundaries in the x-direction, and the lower left (*lly*) and upper right (*ury*) boundaries in the y-direction. By default, the core box that encloses all core rows is used.

Type in the fields, or click *Draw* and use the left mouse button to drag over an area in the design display area to get the boundary coordinates.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `deleteFiller`

Related Topics

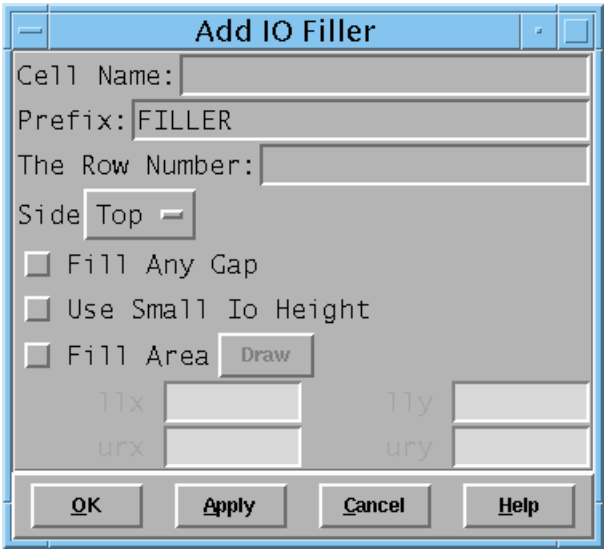
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Filler Cells

Add IO Filler

Use the Add IO Filler form to add I/O instances to the I/O box netlist.

➤ Choose *Place – IO Filler – Add IO Filler*.



Add IO Filler Fields and Options

Cell Name	Specifies the name of the I/O filler cell to add.
Prefix	Specifies the prefix name to be appended for the addedI/O filler instance.
The Row Number	Specifies the row number of the I/O pads (in multiple ring I/O pads) to insert the fillers.
Side	Specifies the side as the Top, Bottom, Left, or Right side of the I/O box. *Default:* By default, the top side is used.
Fill Any Gap	If selected, forces the I/O filler instance into a gap even though the gap (clearance) is not large enough.

Use Small IO Height

Specifies that the filler cell should be inserted between I/O pads only when the smallest I/O pad has the same height as the height of the filler cell.

For example, consider that there are I/O pads A, B, C, D, and E. Out of these, A, B, and E are the same height, and C and D have a height double that of A, B, and E. Assume that you want to insert an I/O filler cell F, which has the same height as A, B, and E.

If you do *not* specify this option, the cell F will be inserted between A and B, B and C, C and D, and D and E. If you specify this option, the cell F will be inserted between A and B, B and C, and D and E. However, the cell will not be inserted between C and D, because both C and D have a height different from F.

Fill Area

Specifies the lower-left and upper-right x and y coordinates of the range where I/O filler cells are added. The values are in micrometers.

Draw

You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the range where I/O filler cells will be added.

Related Text Commands

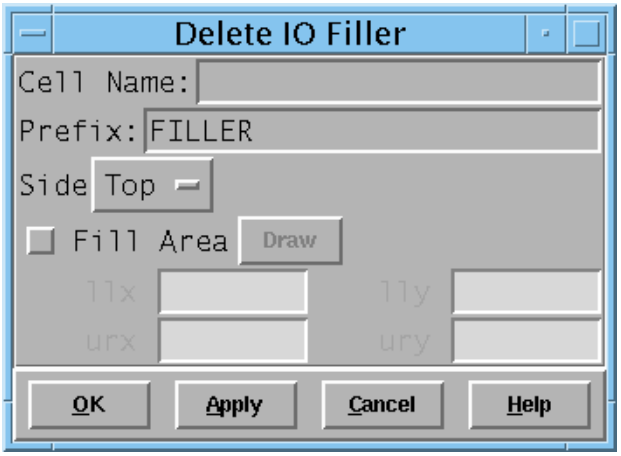
For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `addIoFiller`

Delete IO Filler

Use the Delete IO Filler form to delete I/O filler cell instances from the design.

➤ Choose *Floorplan – IO Filler – Delete IO Filler*.



Delete IO Filler Fields and Options

Cell Name	Specifies the name of the I/O filler cell to delete.
Prefix	Specifies the prefix name of the I/O filler instance to be removed.
Side	Specifies the side as the Top, Bottom, Left, or Right side of the I/O box where the I/O filler cells will be removed. *Default:* By default, the top side is used.
Fill Area	Specifies the lower-left and upper-right x and y coordinates of the range where I/O filler cells are to be deleted. The values are in micrometers. *Draw* — You can click the *Draw Box* button to physically draw a box in the design window corresponding to the coordinates of the range where I/O filler cells will be added.

Related Text Commands

For information on the following command, see “Floorplan Commands” in the *Encounter Text Command Reference*.

- `deleteIoFiller`

Tie HI/LO

Use the Place menu's Tie HI/LO forms to add or delete tie high or tie low cells from the design and connect tie-off pins of netlist instances to tie-off pins of added instances.

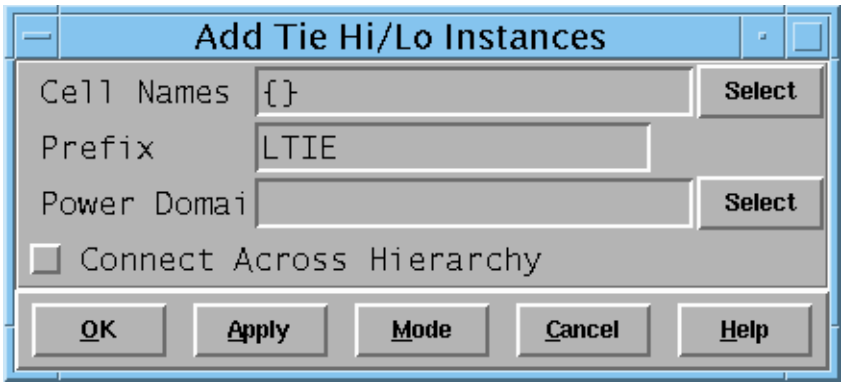
The *Tie HiLo* submenu provides access to the following features:

- Add on page 1051
- Delete on page 1053

Add

Use the Add Tie Hi/Lo Instances form to add instances of specified tie-off cells to the logical hierarchy of the design and connect the tie-off pins of netlist instances to the tie-off pins of the added instances. Thus, these instances provide the connectivity between the tie-high and tie-low pins of the netlist instances to power and ground.

➤ Choose *Place – TieHiLo – Add TieHiLo*.



Add Tie Hi/Lo Instances Fields and Options

Cell Names	Specifies the names of the tie-off cell instances. You can specify a maximum of two tie cells, when one cell is a tie-high driver, and the other a tie-low driver. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *OK* adds the cell name(s) to this field.
Prefix	Specifies the prefix for the added tie-off cell instances. *Default:* `LTIE`
PowerDomain	Specifies the power domain in which the tie-cells are inserted. This identifies the area where to place the tie-cells and connect to the correct power and ground nets. Click *Select* to open a browser to highlight a power domain from the *Selectable Power Domain*. Clicking *OK* adds the power domain name to this field.

Connect Across Hierarchy

Allows the added tie cells to connect to tie pins across hierarchical boundaries, if other constraints, such as maximum fanout and maximum distance, allow it. The port connections are logged to a file named `tiehilo.rpt`.

Default: Off

Related Text Commands

For information on the following commands, see “Placement Commands” in the *Encounter Text Command Reference*.

- `addTieHiLo`
- `deleteTieHiLo`
- `getTieHiLoMode`
- `setTieHiLoMode`

Related Topics

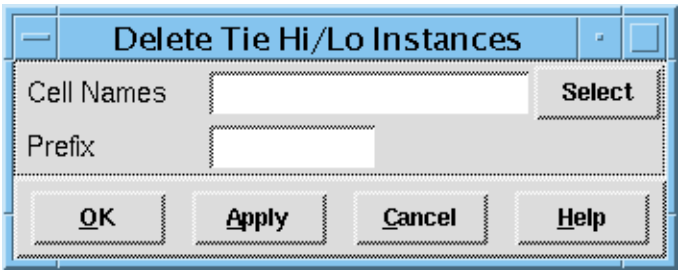
For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Logical Tie-Off Cells

Delete

Use the Delete Tie Hi/Lo Instances form to remove logical tie-off cell instances from the netlist and reconnect the tie input pins.

➤ Choose *Place – TieHiLo – Delete TieHiLo*.



Delete Tie Hi/Lo Instances Fields and Options

Cell Names	Specifies the names of the tie-off cell instances to delete. Click *Select* to open a browser to highlight a cell, or cells, from the *Selectable Cells List*. Clicking *OK* adds the cell name(s) to this field.
Prefix	Specifies the prefix of the instances to delete.

Related Text Commands

For information on the following commands, see “Placement Commands” in the *Encounter Text Command Reference*.

- `addTieHiLo`
- `deleteTieHiLo`
- `getTieHiLoMode`
- `setTieHiLoMode`

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Adding Logical Tie-Off Cells

Scan

Use the *Place* menu's Scan forms to reorder or delete scan cells.

The *Scan* submenu provides access to the following features:

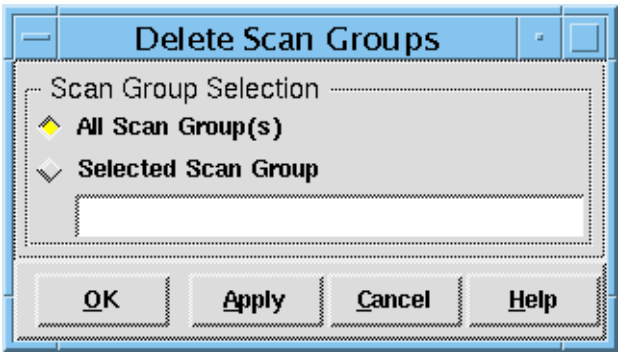
- Delete on page 1056
- Reorder on page 1057

Delete

Use the Delete Scan Groups form to unassign scan cell groups.

Note: Scan groups are sometimes called scan partitions.

➤ Choose *Place – Scan – Delete*.



Delete Scan Groups Fields and Options

All Scan Group(s)	Unassigns all scan groups.
Selected Scan Group	Unassigns a particular scan group.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `deleteScanCell`

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

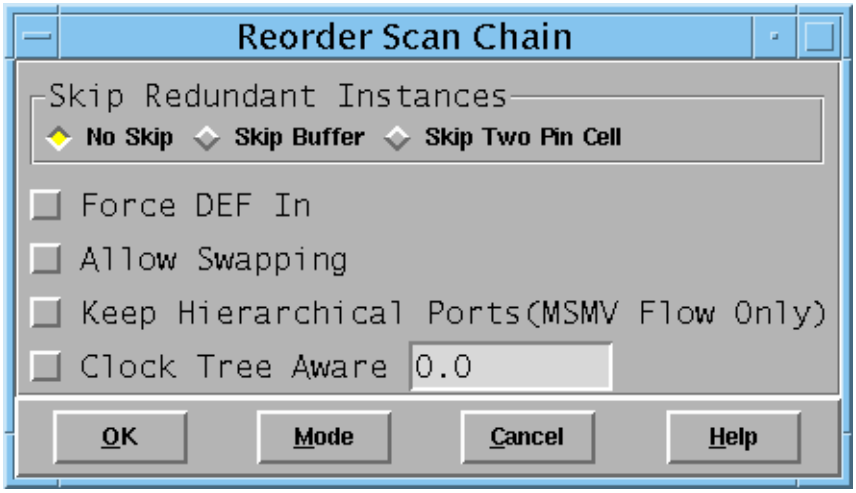
- Scan Cell Functionality

Reorder

Use the Reorder Scan Chain form to reorder the scan edge order for scan groups. Reordering the groups eases connection constraints on the scan instances without constraining the placement of the scan instances.

Note: Scan groups are sometimes called scan partitions.

➤ Choose *Place – Scan – Reorder*.



Reorder Scan Chain Fields and Options

Force DEF In

Ignores netlist mismatches and performs scan reordering using the sequence in the DEF file loaded by the `defIn` command as the initial order of scan elements. This parameter is required for the DEF-in flow for scan reorder when the netlist does not match the sequence of scan elements in the DEF file.

If this parameter is not specified and a netlist mismatch with the DEF file occurs, scan reorder stops and the software exits with an error message.

Skip Redundant Instances

Specifies the way that scan reordering handles buffers and inverters in the scan chain.
Default: No Skip

Select one of the following options:

No Skip	Does not remove buffers or inverters after scan chain reordering.
Skip Buffer	Skips the buffers in the scan chain. If a buffer or inverter is not connected elsewhere in the design, the software removes the buffer.
Skip Two Pin Cell	Skips buffers and inverters in the scan chain. If a buffer or inverter is not connected elsewhere in the design, the software removes the buffer or inverter.

Keep Hierarchical Ports (MSMV Flow Only)

Maintains or corrects the hierarchical ports without deleting or inserting shifters, and reorders the remaining scan chain.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `scanReorder`

Related Topics

For information on the following topic, see “Placing the Design” in the *Encounter User Guide*.

- Reordering Scan Chains

Check Placement

Use the Check Placement form to check `FIXED` and `PLACED` cells and blocks for violations, add violation markers to the design display area, and generate a violation report. Use the Violation Browser to see the violation markers.

Rules as to what constitutes a placement violation are different for `FIXED` and `PLACED` cells. For example, `FIXED` cells in obstruction areas are not considered to be violations, but `PLACED` cells are considered to be violations.

Note: The utilization value reported by `checkPlace` and the density value reported by `timeDesign` might differ because `checkPlace` considers padding when calculating utilization but `timeDesign` does not consider padding when calculating density.

You can delete padding by running the `deleteAllCellPad` command before running `checkPlace`.

The command checks for the following violations:

- Region and fence violations (Instances placed outside their region or fence)
- Out of core area violations (Instances placed partly or wholly outside the core area)
- Not placed on placement grid (Instances not on the placement grid, or blocks not on the manufacturing grid)
- Row orientation violations (Instances whose orientation is illegal for their row; may short power to ground)
- Tech site violations (Instances placed on tech sites not matching their cells and instances that do not have rows for their tech sites)
- Overlapping with other instance (Placed instances that overlap with other instances)
- Pin access violations (Instances with at least one signal pin that does not have routing access due to pre-wires)
- Orientation violations (Instances whose orientation is not legal based on its cell symmetry rules)
- Routing/placement blockage violations in the core area (Instances placed in an obstruction created by pre-wires or routing blockage)

  The command does not check fixed blocks.
- Placement blockage violations in the core area (for example, placed instances in an obstruction created by prerouted wires or a routing blockage, placed instances that overlap a placement blockage area).

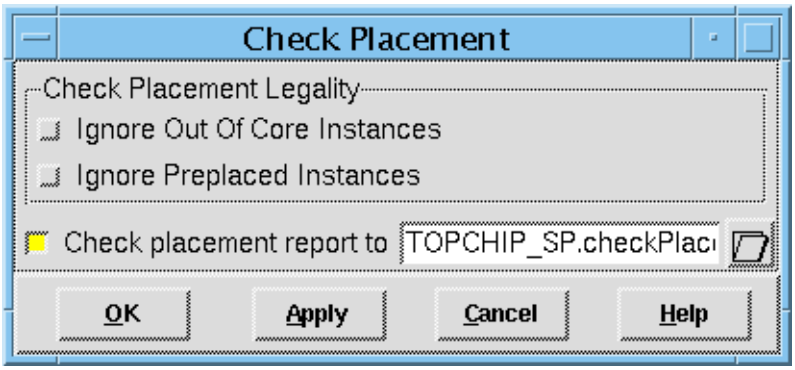
Note: The command does not check fixed instances overlapping placement or routing blockages by default.

- Site orientation violations (Instances whose orientation does not match the tech site orientation)
- Not of fence violations (Instances placed inside a fence to which it does not belong)

In addition to checking for violations, the command reports the following:

- Number of placed instances in the design
- Placement density, in terms of used sites over available sites

➤ Choose *Place – Check Placement*.



Check Placement Fields and Options

Ignore Out of Core Instances

Disables the reporting on instances that are in the area in between the core design boundary area and chip design (head box) area. The instances preplaced in this in between area are assumed to be correct. This also includes I/O pad instances that are outside the core design area.
Default: Off

Ignore Preplaced Instances

Disables reporting on instances that are preplaced within the design (head box) area. This includes placement of instances from loading DEF or TDF placement files.
Default: Off

Check placement report to	Specifies the filename for the check placement report.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `checkPlace`

Display

Use the *Place* menu's *Display* forms and commands to display spare cells and scan cells and remove them from the design display area.

The *Display* submenu provides access to the following features:

- Display Spare Cells on page 1063
- Clear Spare Cells Display on page 1064
- Display Scan on page 1065
- Clear Scan Display on page 1066
- Display Density Map on page 1067

Display Spare Cells

Use the Display Spare Cells command to display the results of placing the spare instances.

➤ Choose *Place – Display – Display Spare Cells*.

There is no GUI form for this command.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

■ `displaySpareCell`

Clear Spare Cells Display

Use the Clear Spare Cells Display command to remove the displayed spare instances.

➤ Choose *Place – Display – Clear Spare Cells Display*.

There is no GUI form for this command.

Related Text Commands

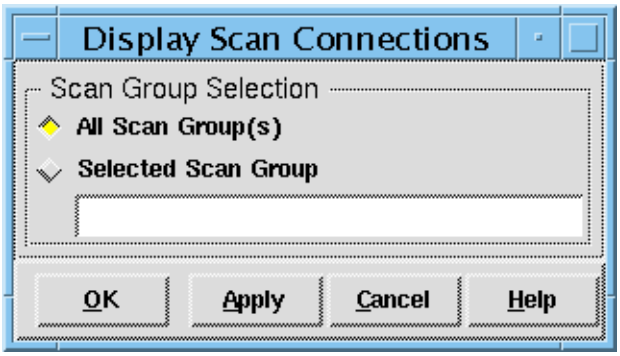
For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

■ `clearSpareCellDisplay`

Display Scan

Use the Display Scan Connections form to display scan cell connections.

1. Set the design display to Physical view.
2. Choose *Place – Display – Display Scan*.



Display Scan Connections Fields and Options

All Scan Group(s)	Displays scan connections of all scan groups. **Note:** Scan groups are sometimes called scan partitions.
Selected Scan Group	Displays scan connections of the specified scan group.

Related Text Commands

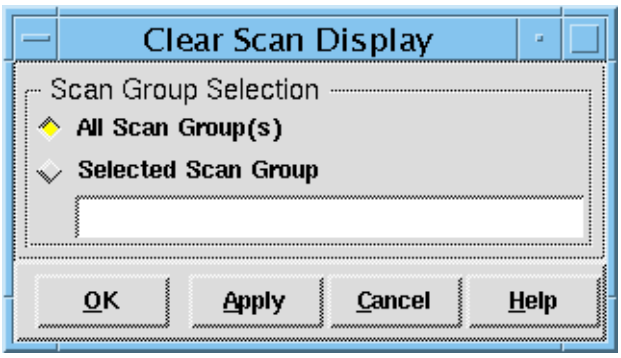
For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

- `displayScanChain`

Clear Scan Display

Use the Clear Scan Display form to clear the display of scan cell connections.

➤ Choose *Place – Display – Clear Scan Display*.



Clear Scan Display Fields and Options

All Scan Group(s)	Removes the display of scan connections of all scan groups. **Note:** Scan groups are sometimes called scan partitions.
Selected Scan Group	Removes the display of scan connections of the specified scan group.

Related Text Commands

For information on the following command, see “Placement Commands” in the *Encounter Text Command Reference*.

■ `clearScanDisplay`

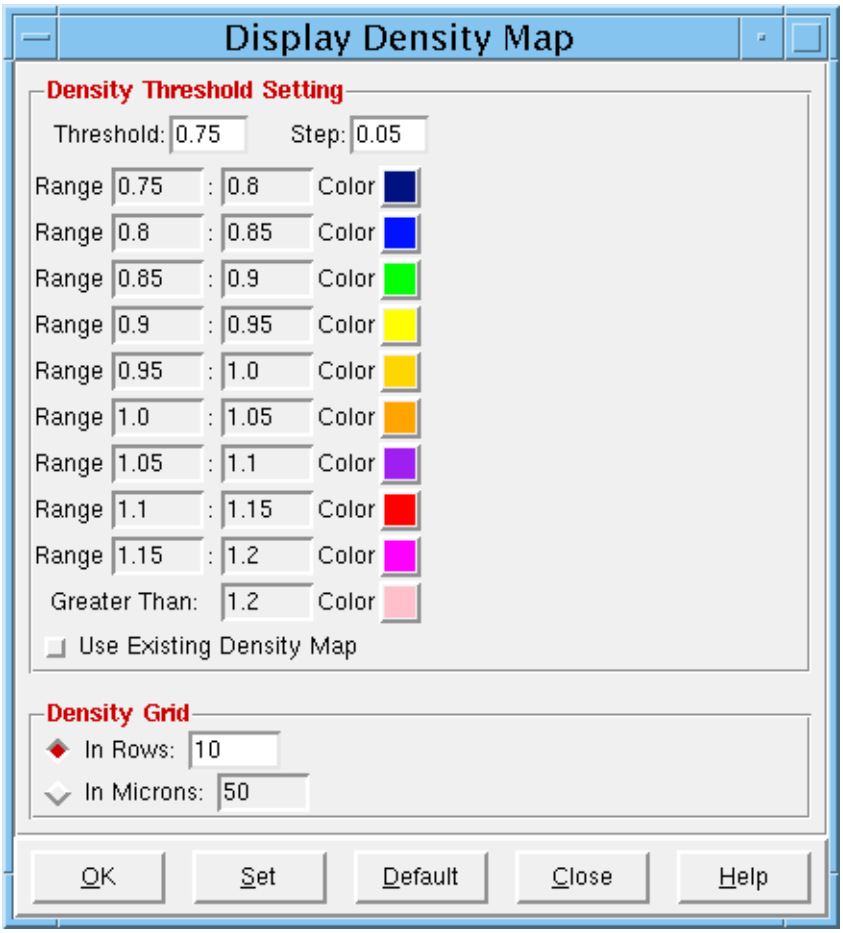
Display Density Map

Use the Display Density Map form to set options for displaying placement density.

Note: Use one of the following methods to turn the display of the density map on or off:

- Select *Density Map* on the list of Visibility toggles in the main Encounter window.
- Clock the All Colors button to open the Color Preferences form, then select the *View Only* tab, and select *Density Map*, in the *Multi-Color Layers* section.

➤ Choose *Place – Display – Display Density Map*.



Display Density Map Fields and Options

Density Threshold Setting
Threshold

Specifies a threshold density value for a grid in the map. Any grid under the threshold value is not displayed. The value must be positive. For example, if the threshold value is 0.75, a grid with placement density of 0.74 is not displayed.
Default: 0.75

Step

Specifies an incremental amount for moving to a higher or lower *Range*.
Default: 0.05

Range

Specifies a decimal value for the highest and lowest placement density to represent with a specified color in the map. Each *Range* is a different density level.

Color

Displays the color for a *Range*. Click the color to open the Density Map Level *level_number* Color form, and change the color by using the slider bars.

Greater Than

Specifies the minimum value for the highest placement density level to display. Any value higher than the value specified is represented by a single color. For example, if the specified value is `1.2`, and the adjacent *Color* is pink, any area with a placement density that is greater than 1.2 is shown in pink in the density map.
Default: `1.2`

Use Existing Density Map

Redraws the screen when you click *OK*, without recalculating the density. Select this option if you change the threshold or the step size, but haven't made any changes to placement.
Default: Off

Density Grid

Specifies the basis for the map grid. Each bin in the map is a square.
Default: In Rows

In Rows

Specifies that the dimensions of the bins are based on the height of a standard cell row. For example, if you specify 12, the dimensions of each bin represent 12 times the standard row height. If you specify a value less than 1, the software uses 1.
Default: 10

In Microns	Specifies that the dimensions of the bins are based on microns. For example, if you specify 45, the dimensions of each bin represent 45 microns. *Default:* 50

Related Text Commands

For information on the following commands, see “Placement Commands” in the *Encounter Text Command Reference*:

- `getDensityMapMode`
- `reportDensityMap`
- `setDensityMapMode`

10

Clock Menu

- Design Clock on page 1072
- Trace Pre-CTS Clock Tree on page 1082
- Clock Tree Browser on page 1093
- Clock Tree Analyst on page 1101
- Display on page 1121
  - Display Clock Tree on page 1122
  - Clear Clock Tree Display on page 1125
- Save Clock Nets on page 1126
- Generate Clock Tree Spice on page 1127
- Clock Mesh on page 1129
  - Edit Clock Mesh Specification on page 1130
  - Synthesize Clock Mesh on page 1152
  - Delete Clock Mesh on page 1155
  - Route Clock Mesh on page 1156
  - Trim Clock Mesh on page 1157
  - Analyze on page 1159
  - Report Clock Mesh on page 1160
  - Display Clock Mesh on page 1162
  - Mode on page 1165

Design Clock

The Synthesize Clock Tree form enables you to run the complete clock tree synthesis process. You can use this form to build clock trees, route clock nets, and resize instances based on CTS mode settings and SDC constraints, and to generate the standard clock skew and timing reports. You also can generate the clock tree specification file necessary for clock tree synthesis.

Note: In order to use the Synthesize Clock Tree form to synthesize clock trees, the design must be placed. If the design is not placed, when you click the *OK* button, the software only loads the clock tree synthesis specification file into the design.

The Synthesize Clock Tree form contains the following subpages:

- Synthesize Clock Tree – Basic on page 1073
- Synthesize Clock Tree – Advanced on page 1079

Related Controls

The Synthesize Clock Tree form contains the following buttons that provide access to related clock tree synthesis functions:

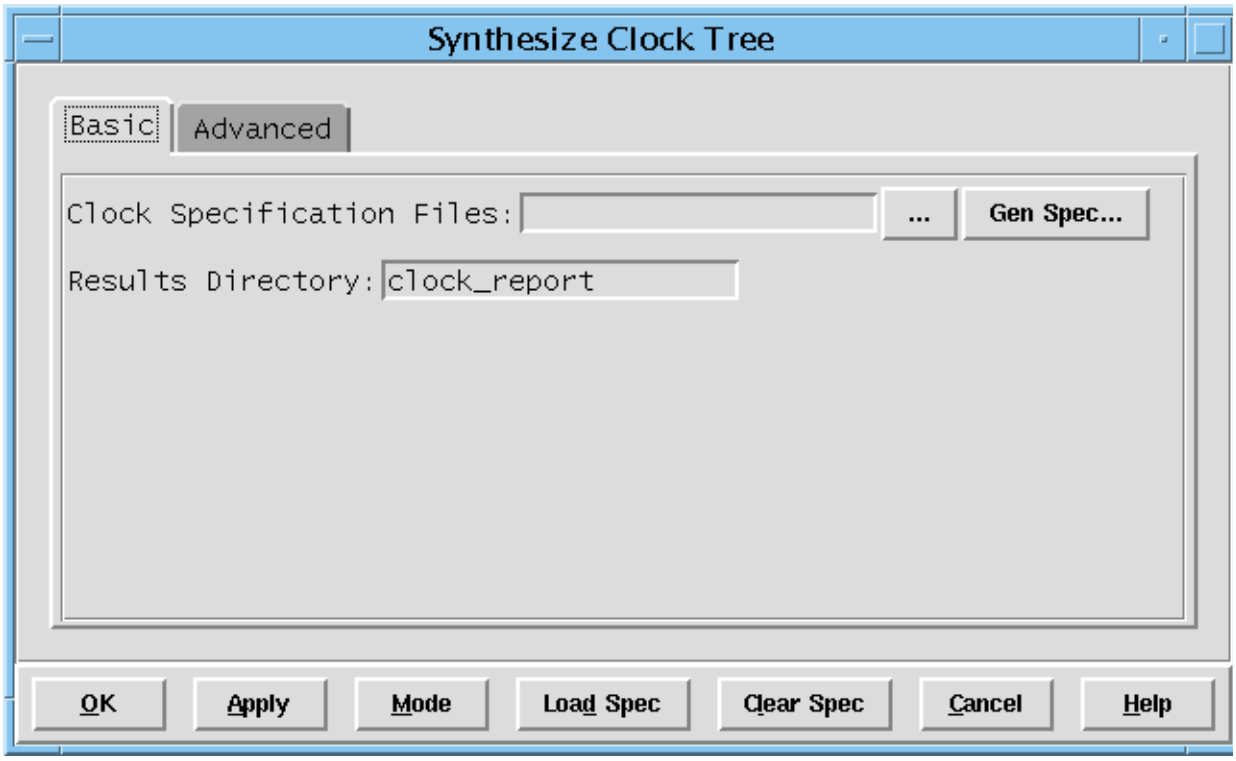
Mode	Opens the *CTS* pages of the Mode Setup form. You can use this form to set global parameters for performing clock tree synthesis.
Load Spec	Loads the clock tree specification file into the design only; the software does not perform clock tree synthesis.
Clear Spec	Removes clock tree information that was loaded when you specified the clock tree specification file.

Synthesize Clock Tree – Basic

Use the *Basic* page of the Synthesize Clock tree form to specify the clock tree specification files to use for clock tree synthesis, and the directory in which to save the resulting reports.

Note: If placement has not been performed, you can use this form only to generate and load a clock tree specification file.

➤ Choose *Clock – Design Clock*.



Fields and Options

Clock Specification Files

Specifies the clock tree specification file to use to drive CTS. You can specify one or more specification files.

... Opens the Clock Specification Files form, which you can use to choose a clock tree specification file.

	Gen Spec...	Opens the Generate Clock Spec form, which you can use to create a clock tree specification file.
Results Directory	Specifies the directory name in which the CTS report files are saved. *Default:* `clock_report`	

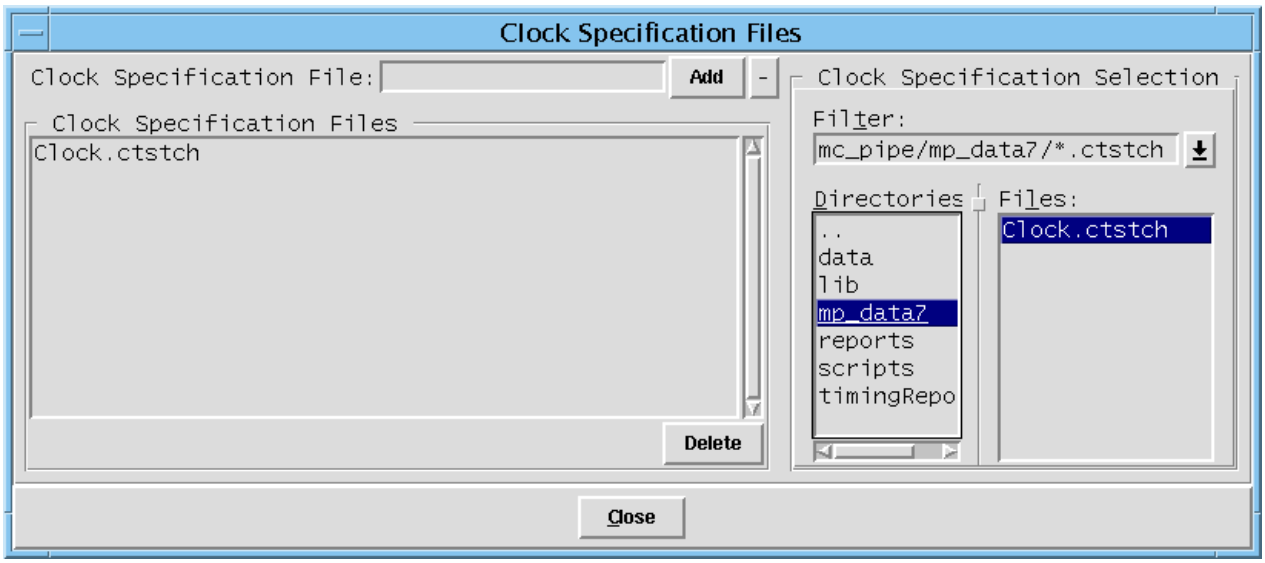
Related Text Commands

- `clockDesign`
- `ckSynthesis`
- `cleanupSpecifyClockTree`
- `setCTSMode`

Clock Specification Files

Use the Clock Specification Files form to choose a clock tree specification file to use for clock tree synthesis.

➤ Choose *Clock – Design Clock*, and click the *...* button next to the *Clock Specification Files* option.



Fields and Options

Clock Specification File

Indicates the name of the file you want to choose.

To choose a file:

1. Click the + button to expand the form so that you can search for clock tree spec files.
2. Double click on the directory name in which you want to search.
3. Double click on the name of the clock tree spec file you want to choose.
4. Click the *Add* button to populate the *Clock Specification Files* field on the Synthesize Clock Tree form.

Related Text Command

- `specifyClockTree`

Generate Clock Spec

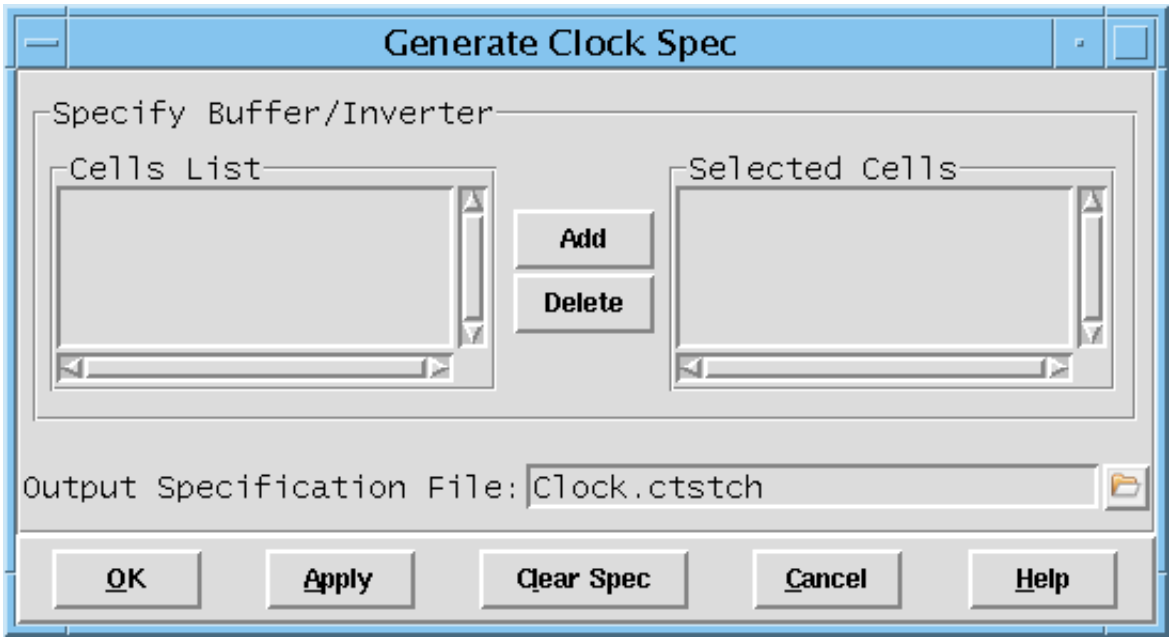
Use the Generate Clock Spec form to create a clock tree specification file.

The clock tree specification file defines the clocks in the design that you want to synthesize. If a design contains several clocks, you can specify any of these clocks in the clock tree specification file, and those clocks will be synthesized during a single CTS run. You can also synthesize an individual clock tree separatelusing its own clock tree specification file.

Important

Timing constraints must be loaded into the Encounter session before using this form.

➤ Choose *Clock – Design Clock*, and click the *Gen Spec...* button.



Fields and Options

Cells List	Specifies the list of buffer and inverter cells to use during automatic, gated clock tree synthesis.

Selected Cells

Lists the available buffer and inverter cells that you can choose to use.

To add a cell to the *Cells List* window, highlight the cell name in the *Selected Cells* window, and click the *Add* button.

To delete a cell from the *Cells List* window, hightlight the cell name in the *Cells List* window and click the *Delete* button.

Output Specification File

Specifies the name of the clock tree specification file to be created.

Default: `Clock.ctstch`

Related Text Commands

- `createClockTreeSpec`

Related Topics

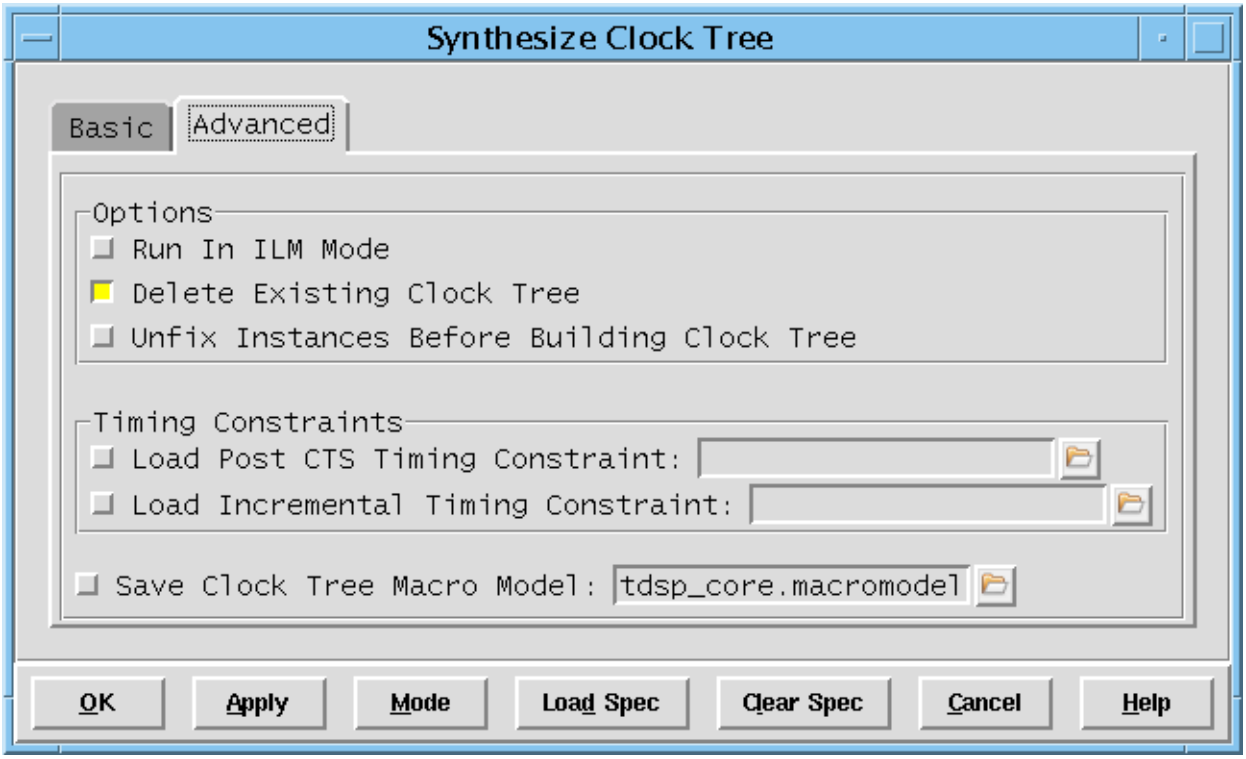
- Creating a Clock Tree Specification File

Synthesize Clock Tree – Advanced

Use the *Advanced* page of the Synthesize Clock Tree form to set requirements for clock tree synthesis.

Note: The options specified on the *Advanced* page can be used only after placement has been performed.

➤ Choose *Clock – Design Clock*, then choose the *Advanced* tab.



Fields and Options

Run In ILM Mode

Performs clock tree synthesis on designs containing interface logic models (ILMs).

Default: Off

Delete Existing Clock Tree

Removes existing clock trees before performing clock tree synthesis.

Default: On

Unfix Instances Before Building Clock Tree

Changes the placement status of all buffers, inverters, flip-flops, and gating cells of the clock tree to `PLACED`, before building the clock tree.

If you do not specify this option, the software sets the placement status for the buffers, inverters, flip-flops, and gating cells of the clock tree to `FIXED`.

Default: Off

Load Post CTS Timing Constraint

Loads the specified post-CTS SDC file after clock tree synthesis, before running timeDesign.

If you specify this option, CTS clears the original SDC file from memory and loads the new SDC file before running `timeDesign -postCTS`.

Note: You can load an incremental SDC file and a post-CTS SDC file together. If you do, CTS clears the original SDC file from memory, loads the new post-CTS file, then loads the incremental file.

Default: Off

Load Incremental Timing Constraint

Loads the specified incremental SDC file.

Use this option to load an incremental SDC file after clock tree synthesis in order to make minor changes, such as changing the `clock_uncertainty` value, or to add the `set_clock_latency` statement.

Note: You can load an incremental SDC file and a post-CTS SDC file together. If you do, CTS clears the original SDC file from memory, loads the new post-CTS file, then loads the incremental file.

Default: Off

Save Clock Tree Macro Model

Saves the macro model information for the clock tree to the specified file.

If you do not specify a name, the software saves the results to the *`design_name`*`.macromodel` file.

Default: Off

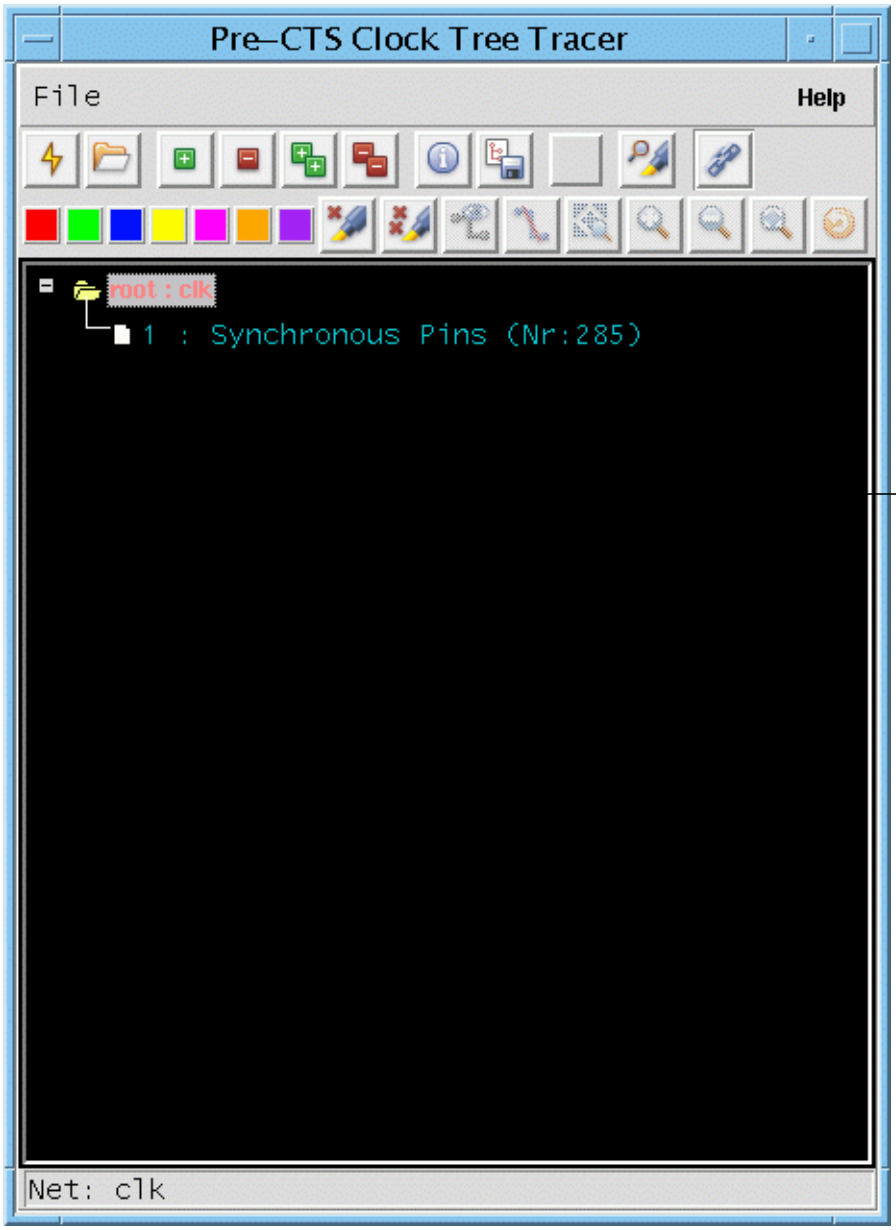
Related Text Commands

- `clockDesign`
- `ckSynthesis`
- `cleanupSpecifyClockTree`
- `setCTSMode`

Trace Pre-CTS Clock Tree

Use the Pre-CTS Clock Tree Tracer to analyze clock trees before performing CTS.

➤ To open the Pre-CTS Clock Tree Tracer, choose *Clock – Pre-CTS Clock Tree Tracer*.



Main tree window

You can perform the following functions with the Pre-CTS Clock Tree Tracer:

- Search for pins and nets.

  You can use an asterisk (`*`) as a wildcard in your searches.

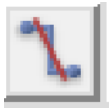
- Highlight pins and nets, and change highlighting colors dynamically.
- Cross-probe pins and nets between the browser and the Physical view.

The browser creates a file (`top_level_cell.cts_trace`) that contains tracing information.

The following table describes the widgets on the Pre-CTS Clock Tree Tracer.

Widget	Description
	Trace Clock Tree—Traces the existing clock tree and displays the clock tree root in the main tree window.
	Load Trace File—Loads an existing clock tree trace file (`top_cell_name.cts_trace`) into the Pre-CTS Clock Tree tracer.
	Expand Current—Expands all objects below the object that is highlighted in the main tree window.
	Collapse Current—Collapses the object that is highlighted in the main tree window.
	Expand All—Expands all objects in the tracer window, whether or not the objects are highlighted.
	Collapse All—Collapses all objects in the tracer window, whether or not the objects are highlighted

Widget	Description
	Query (q)—Displays one of three forms, containing information on the object highlighted in the tracer window: ■ The Clock Info form for highlighted clocks ■ The Synchronous Pins/Excluded Pins form for highlighted synchronous pins or excluded pins ■ The Gate Info form for highlighted gated cells Each of these forms contains a button with which you can display the Attribute Editor. You can also display the Attribute Editor by double-clicking on an object in one of the three forms described above.
	Save Subtree (Ctrl-s)—Saves to a text file all trace information for the highlighted object and all objects below the highlighted object.
	Search Path (s)—Displays the Search form, with which you can search in all clock paths for pins or nets that you specify in the Search form.
	Search & Hilite—Displays the Search & Hilite form, in which you can search for objects in the clock tree and change their highlighting colors.
	Link with layout—Acts as a toggle to display in the Encounter main window any objects that you have highlighted in the tracer window. Clicking this button activates the following widgets: ■ *Show Net (n)* ■ *Hide Net (u)* ■ *Zoom Selected (a)* ■ *Zoom In (z)* ■ *Zoom Out (Z)* ■ *Zoom Fit (f)* ■ *Redraw (r)* ■ *Physical view*

Widget	Description
	Highlight (*1-7*)—Highlights the selected objects in the clock tree with the selected color.
	Dehilite (d)—Removes highlighting from a single object in the tracer window and in the Encounter main window, if *Link with layout* is turned on.
	Dehilite All (D)—Removes highlighting from all objects in the tracer window and in the Encounter main window, if *Link with layout* is turned on.
	Show Net (n)—Displays net flight lines in the Encounter main window.
	*Hide Net (u)*—Turns off the display of net flight lines in the Encounter main window.
	Zoom Selected (a)—Zooms into the selected object in the Encounter main window.
	Zoom In (z)—Zooms into the Encounter main window.
	Zoom Out (Z)—Zooms out of the Encounter main window.
	Zoom Fit (f)—Zooms into the Encounter main window while fitting the entire design within the design display area.
	Redraw (r)—Redraws the Encounter main window.

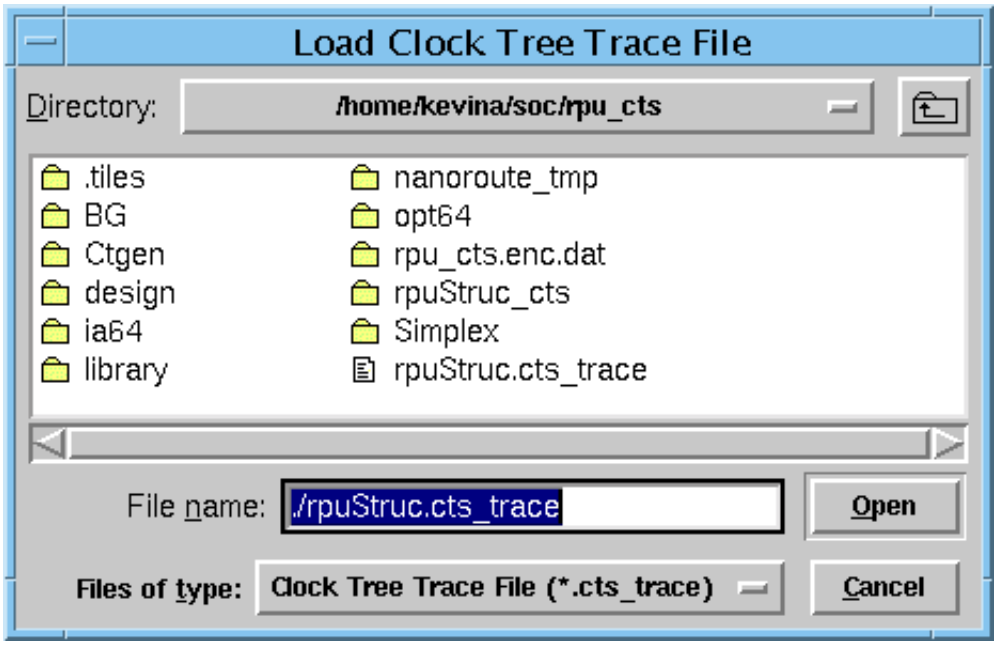
Related Text Commands

- `ckSynthesis -check`

Load Clock Tree Trace File

Use the Load Clock Tree Trace File form to browse for and load a clock tree trace file for use with the Pre-CTS Clock Tree Tracer.

➤ To open the Load Clock Tree Trace File form, click the *Load Trace File* icon in the Pre-CTS Clock Tree Tracer.



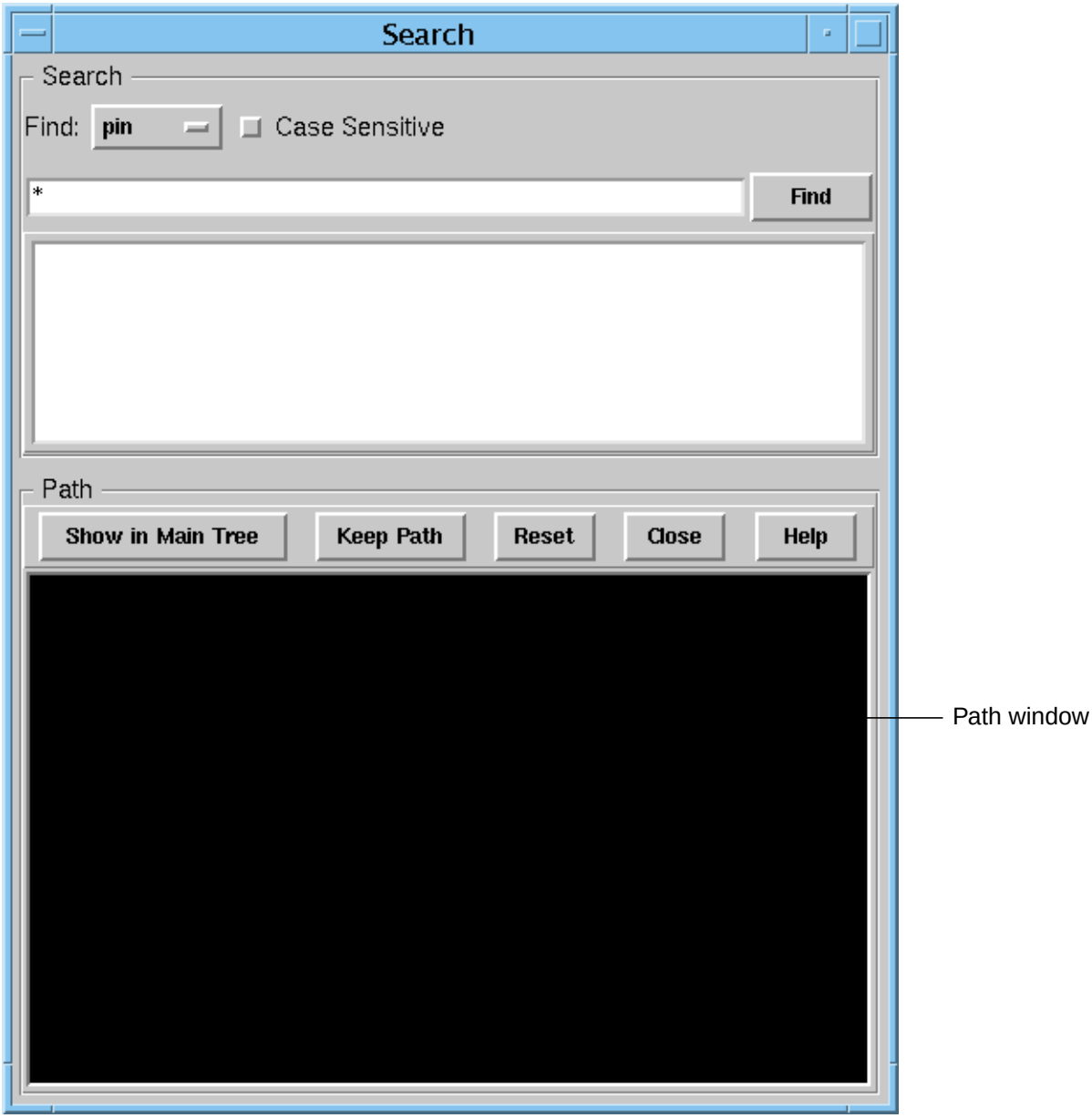
Fields and Options

Directory	Displays the name of the directory from which you started Encounter. Click on the directory icon to choose from a list.
File name	Enter the name of the trace file you want to load.
Files of type	Allows you to display either trace files, or all files in the current directory.

Pre-CTS Clock Tree Tracer Search

Use the Search form from within the Pre-CTS Clock Tree Tracer to search for and highlight pins or nets in your design.

➤ To open the Search form, click the *Search Path (s)* button in the Pre-CTS Clock Tree Tracer.



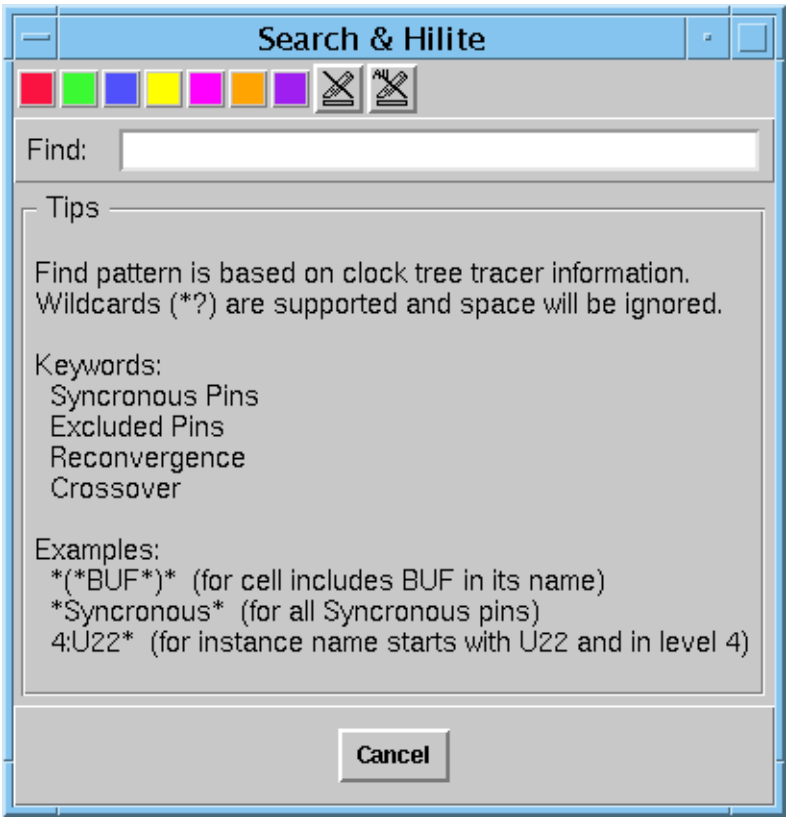
Fields and Options

Find: pin/net	Defines whether to search for pins or nets.
Case Sensitive	Searches for pins or nets based upon capitalization.
Find	Starts the search.
Show in Main Tree	Shows (in the main tree window) the object you have selected in the path window.
Keep Path	Cumulatively preserves the paths you select in the path window.
Reset	Clears all paths in the path window.

Search & Hilite

Use the Search & Hilite form to search for and highlight objects in the tracer window.

➤ To open the Search & Hilite form, click the *Search & Hilite* icon in the Pre-CTS Clock Tree Tracer.



Fields and Options

Find	Accepts character strings on which to search.

Tips

Provides guidelines on how to use the *Find* field:

- Keywords for describing the characteristics of clock objects:
  - Synchronous Pins
  - Excluded Pins
  - Reconvergence
  - Crossover
- Wildcards are supported: * and ?

Determines the color to use when highlighting objects in the tracer window. Clicking on a colored box simultaneously selects and applies the highlighting color to all objects in the tracer window.

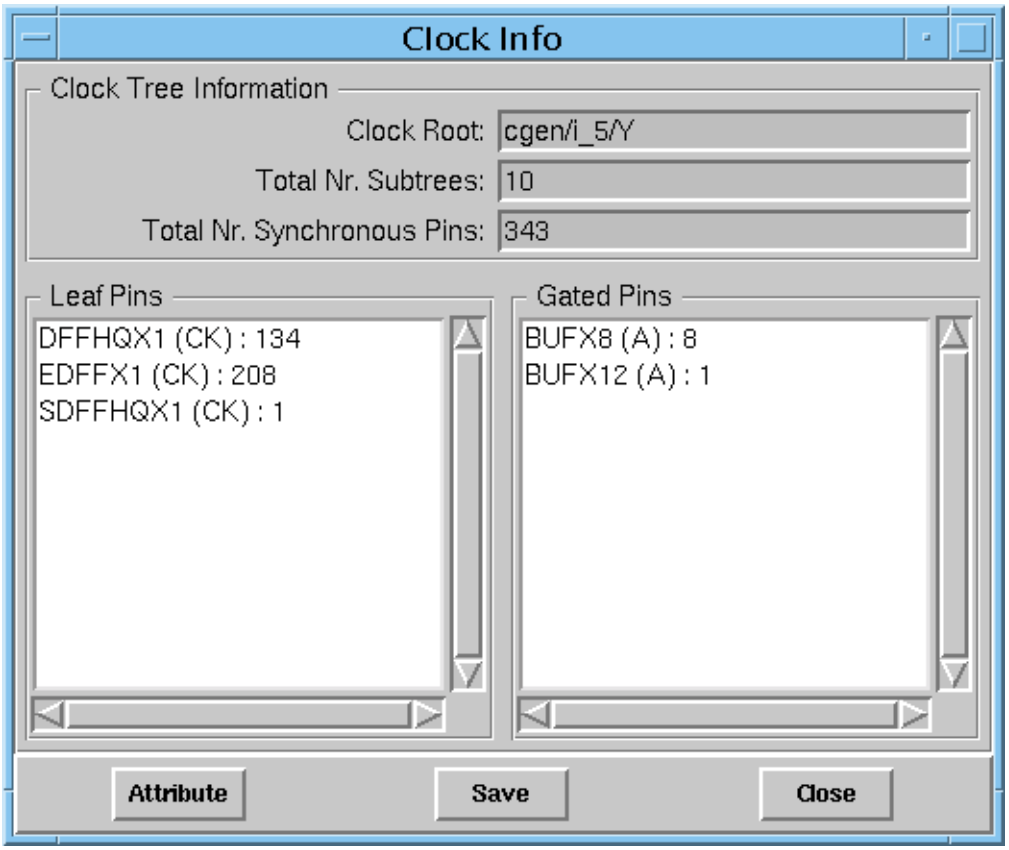
Dehilite (d)—Removes highlighting from a single object in the tracer window.

Dehilite All (D)—Removes highlighting from all objects in the tracer window.

Clock Info

Use the Clock Info form to display information about a clock tree in your design.

➤ To open the Clock Info form, double-click on the root of a clock tree in the Pre-CTS Clock Tree Tracer.



Fields and Options

Clock Root	Displays the name of the clock root.
Total Nr. Subtrees	Displays the number of subtrees in the clock tree.
Total Nr. Synchronous Pins	Displays the number of synchronous pins in the clock tree.

Leaf Pins	Displays the leaf pins in the clock tree. Double-click on a leaf pin to display information about the gated pin with the Attribute Editor.
Gated Pins	Displays the gated pins in the clock tree. Double-click on a gated pin to display information about the gated pin with the Attribute Editor.
Attribute	Opens the Attribute Editor and shows information for the clock root.
Save	Saves the data in the Clock Info form to a user-defined file.
Close	Closes the Clock Info form.

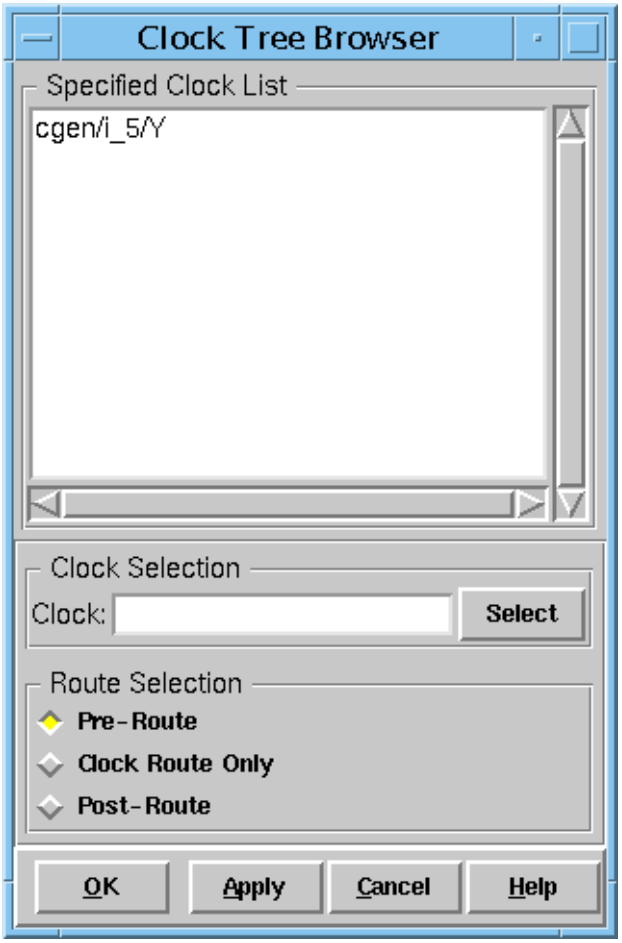
Clock Tree Browser

Use the Clock Tree Browser to view and identify the synthesized clock tree, the added clock buffers, and the added delay elements. In addition, you can control the display of the resulting clock tree, phase delay, and minimum and maximum paths in the Physical view.

Important

If you want to generate a clock tree report for a design on which you have already run clock tree synthesis, and which you have restored during an Encounter session, you must load the design's clock tree specification file with the Specify Clock Tree form.

1. To open the Clock Tree Browser, choose *Clock – Clock Tree Browser*.
2. Highlight an item in the *Specified Clock List*, then click *Select*.



Fields and Options

Route Selection

Selects the routing status of the clock(s) to be displayed.

Choose one of the following:

Pre-Route
Displays clock tree timing analysis results that are based on a CTS Steiner tree.

Clock Route Only
Displays clock tree timing analysis results that are based only on clock tree wires, even if other wires (such as signal net wires) exist in the design.

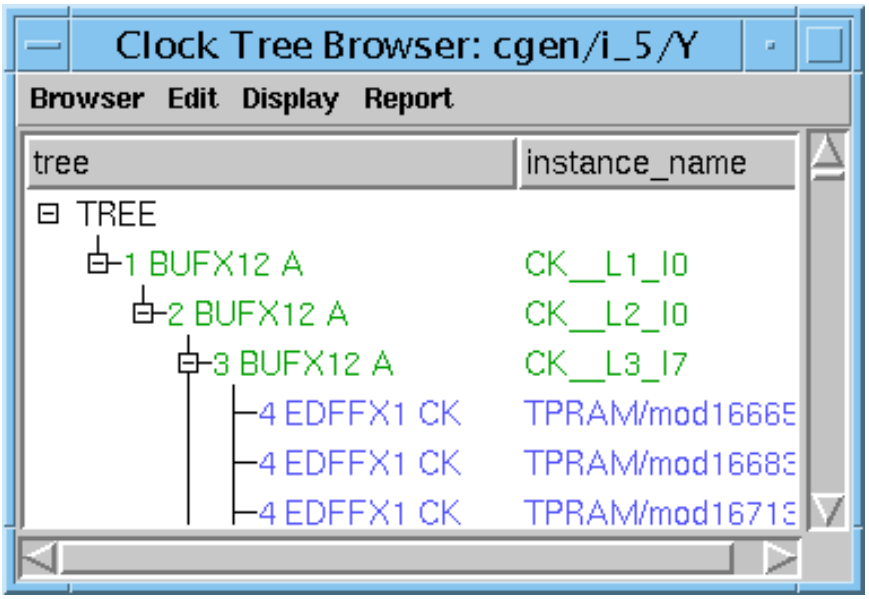
Post-Route
Displays post-routing clock tree timing analysis results based on clock tree wires and signal wires on the specified clock, or on all clocks in the design if no clock is specified.

Note: CTS halts and displays a message if the design has not been routed.

Clock Tree Browser – Clock Tree Diagram

CTS builds the hierarchical clock tree and replaces the original browser display with a diagram of the clock tree.

➤ Select the appropriate options in the Clock Tree Browser form and then click *OK*.



Fields and Options

Browser – Save	Displays the Save Clock Tree Browser form and allows you to specify a file to which you want to save the Clock Tree Browser data.
Edit – Resize	Displays the Select Cell form. Use this form to select a cell to use when resizing an instance in the Clock Tree Browser.
Edit – Insert at input	Inserts buffers, inverters, or clocked leaf instances as close as physically possible to the chosen input. The inserted cell appears at the input of the instance you selected.
Edit – Insert at output	Inserts buffers or inverters as close as physically possible to the chosen output. **Note:** You cannot insert buffers or inverters at the output of flip-flops.

Edit – Delete

Deletes buffers or inverters. Select a buffer or inverter and then select *Edit – Delete*.

Edit – Reconnect

Reconnects clocked leaf instances that have been revised within the browser. The placement of such instances remains the same, but CTS changes the connections between the instances.

Note: You can only reconnect leaf cells. CTS does not refine placement after reconnecting leaf cells.

Edit – Highlight

Highlights selected buffers, inverters, or clocked leaf instances in the Physical view.

Edit – Zoom highlighted

Zooms into selected buffers, inverters, or clocked leaf instances in the Physical view.

Edit – DeHighlight

Dehighlights selected buffers, inverters, or clocked leaf instances in the Physical view.

Display – Expand all

Shows all branches in the clock tree.

Display – Expand to instance …

Opens the *query* form in which you can do the following:

1. Enter an instance name in the *Instance name to expand to* field.
2. Click *OK*.

The browser then searches all branches of the clock tree for the specific instance and expands the display to show all occurrences of the instance you have specified.

The browser displays the path (in red) from the clock root pin to the specified instance(s).

Display – Expand from instance

Opens all branches beginning with the highlighted instance.

Display – Collapse from instance

Closes all branches beginning with the highlighted instance.

Display – Refresh

Updates the colors in the browser.

Display – Trigger Edge Delay

Displays the clock tree histogram.

For more information, see Clock Tree Browser – Clock Tree Histogram on page 1099.

Display – Hide/Show

Provides nine choices:

Instance name	Adds or removes the *instance_name* column that displays the instance names associated with each branch in the clock tree.
Trig edge	Adds or removes the *trig_edge* column that displays the triggering edge type for instances in the clock tree. Hides or shows the *Trig edge* column in the viewer. *Trig edge* refers to *downstream* trigger edges.
Trig edge skew	Adds or removes the *trig_edge_skew* column that displays the triggering edge skew values for instances in the clock tree. Hides or shows the *Trig edge skew* column in the viewer. *Trig edge skew* refers to *downstream* trigger edges.
Rise delay	Adds or removes the *rise_delay* column that reports the downstream rise delays.
Fall delay	Adds or removes the *fall_delay* column that reports the downstream fall delays.
Rise skew	Adds or removes the *rise_skew* column that reports the downstream skew.
Fall skew	Adds or removes the *fall_skew* column that reports the downstream skew.
Input delay	Adds or removes the *input_delay* column that reports the downstream input delays.
Input tran	Adds or removes the *input_tran* column that reports the downstream input transition values.

Display – Physical view	Provides three choices:	
	Phase delay	Displays the phase delays of clock instances. Colors at the red end of the spectrum indicate the greatest phase delay; colors at the blue end of the spectrum indicate the smallest phase delay.
	Min/Max Path	The clock path with minimum delay is blue; the clock path with maximum delay is red.
	Clear display	Clears the clock tree display in the design area.
Report – Instance info	Displays information about a selected instance in the Encounter console.	

Related Text Commands

- `displayClockPhaseDelay`

Clock Tree Browser – Clock Tree Histogram

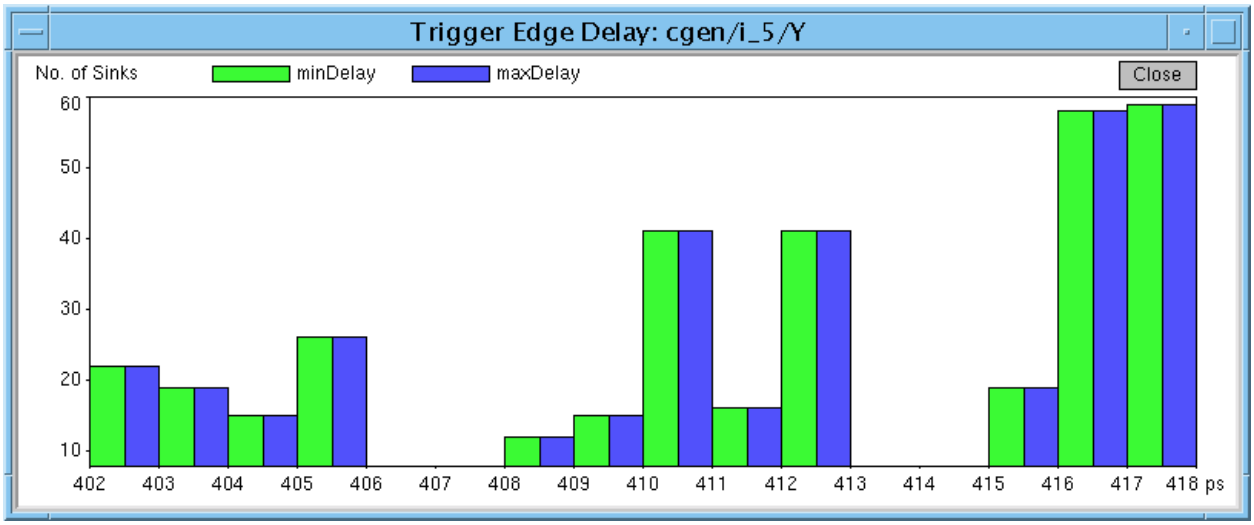
You can display a histogram that reports the distribution of minimum trigger edge delay and maximum trigger edge delay (in picoseconds) for each terminal in a clock.

The vertical axis of the histogram shows the number of sinks that have the delay shown (in picoseconds) on the horizontal axis of the histogram.

The gradation of the picosecond increments in the histogram depends on the range of delay values. The example below shows one-picosecond delay increments; if the range of delay values were greater, the increments would be greater, too.

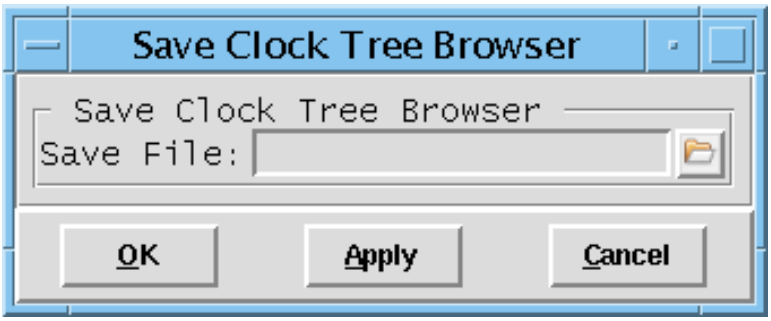
To display the histogram, complete the following step:

➤ In the Clock Tree Browser, select *Display – Trigger Edge Delay*.



Save Clock Tree Browser

The Save Clock Tree Browser form allows you to specify a file in which to save the contents of the Clock Tree Browser.



Fields and Options

Save File	Enter the name of the file for the clock tree browser information.

Clock Tree Analyst

The Clock Tree Analyst tool helps you visualize the logical (pre and post-CTS) and physical views of the clock tree. You can debug the clock tree spec file and better understand the quality of the clock tree synthesis results.

The Clock Tree Analyst tool has the following features.

- The tool display shows a schematic-like representation of the clock tree. You can control the level of details you want to see.
- The results shown in the tool are based on the CTS spec file. You can view `preRoute`, `clkRouteOnly`, or `postRoute` views.
- The units on the horizontal scale of the display represent time, so that distance between two elements indicates delays that you can measure.
- A comprehensive search mechanism enables you to find instances, paths, and reconvergent clocks easily.
- The tool displays several clocks at the same time.
- The tool can display reconvergent and crossover clocks.
- From this tool, you can link to the schematic and the Global Timing Debug tool.

The Clock Tree Analyst Tool contains the following forms and commands:

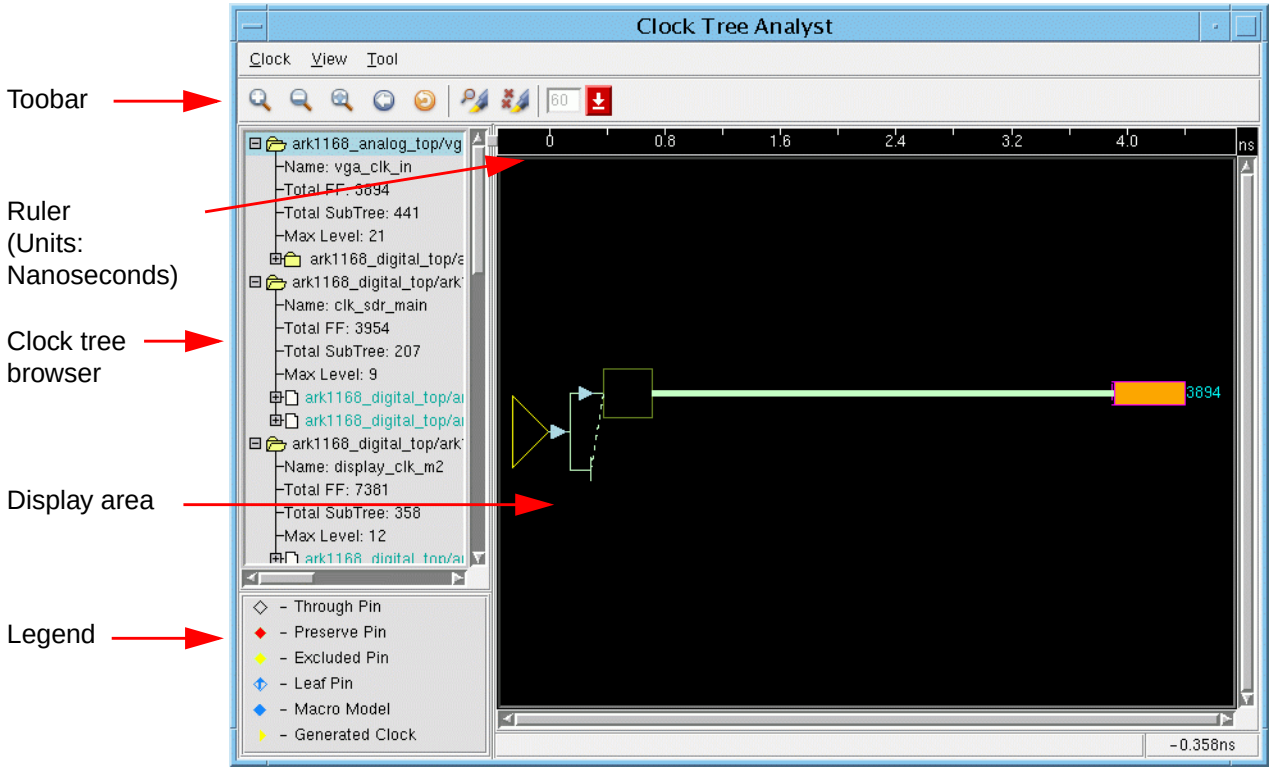
- Clock Tree Analyst Main Window on page 1102
- Clock Tree Analyst – Clock Setup on page 1105
- Clock Tree Analyst – Clock – Preference – Display on page 1107
- Clock Tree Analyst – Clock – Preference – Color on page 1109
- Clock Tree Analyst – Clock – Preference – Color – Set Mixed Color on page 1110
- Clock Tree Analyst – Tool – Find – Instance on page 1111
- Clock Tree Analyst – Tool – List Flip-Flops Not In Any Clock on page 1113
- Clock Tree Analyst – Find – Reconvergence on page 1115
- Clock Tree Analyst – Find – Path on page 1116
- Clock Tree Analyst – Tool – Dump View on page 1118
- Clock Tree Analyst – List Sink on page 1119

Clock Tree Analyst Main Window

Use the Clock Tree Analyst tool to visualize the logical and physical views (pre and post-CTS) of the clock tree.

➤ Choose *Clock Tree Analyst* from the *Clock* menu.

- A pop-up menu displays when you right-click on the main display area, containing the following choices:
  - *Add Ruler*
  - *Delete Ruler*
- A pop-up menu displays when you right-click on an element, containing the following choices:
  - *Expand*
  - *Collapse*
  - *Property*
  - *List Sink*
  - *View Predecessor*
  - *Highlight in Layout*
  - *Back Trace Pin*



Main Window Features

Toolbar — Shows icons for performing the following tasks:

- Zoom in
- Zoom out
- Fit
- Zoom previous
- Redraw
- Find
- Clear highlight

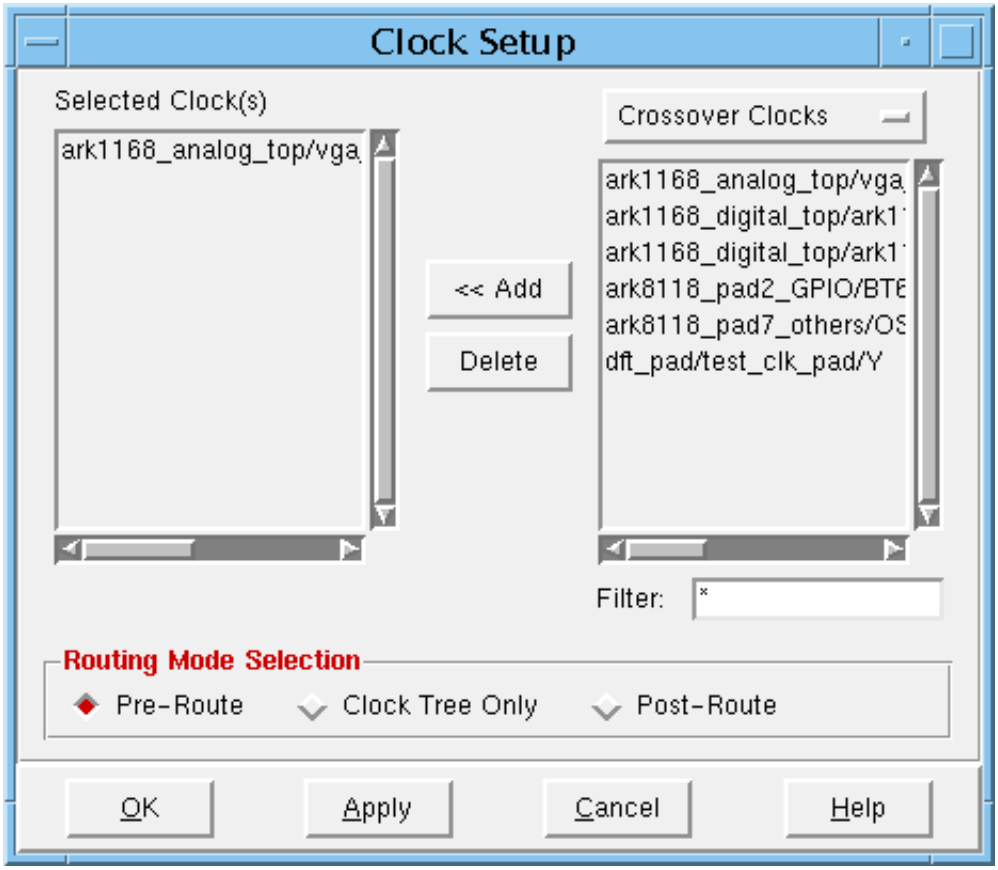
Ruler — Displays time units (in nanoseconds) that measure the delay between elements.

Clock Tree Browser — Displays the information from the clock tree specification file.

Legend	Provides the meaning of the various icons used in the main display.

Clock Tree Analyst – Clock Setup

➤ From the Clock Tree Analyst Main Window, choose Clock Setup from the Clock menu.



Clock Tree Analyst – Clock Setup Fields and Options

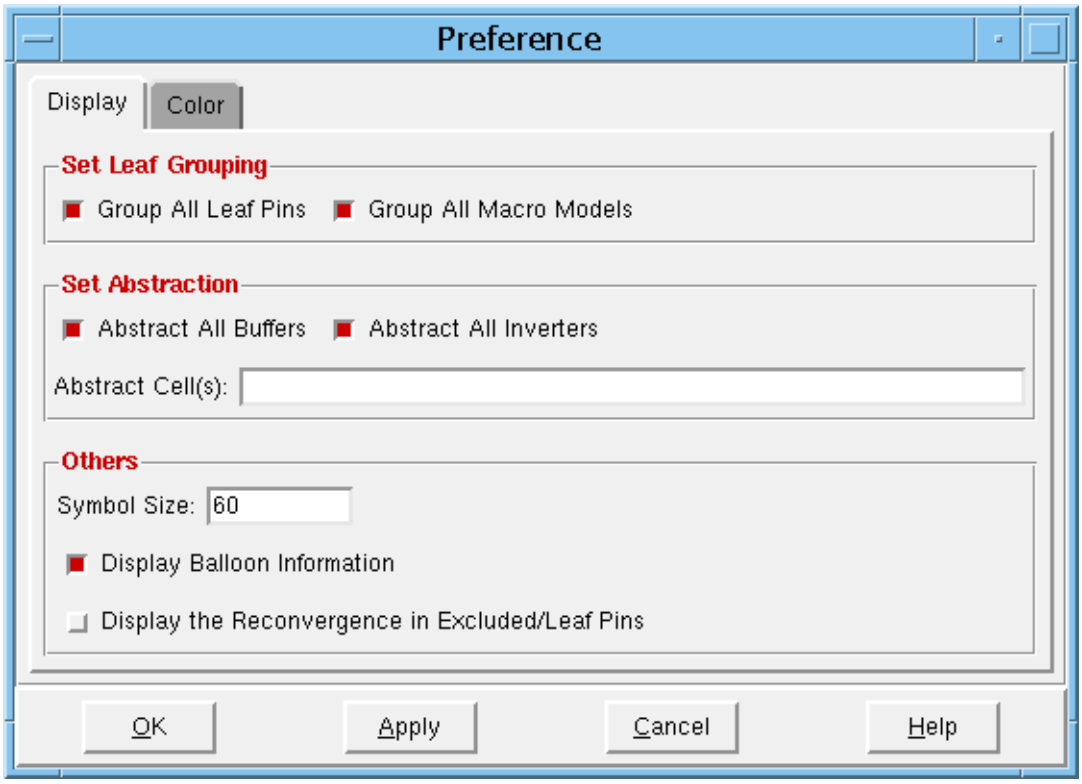
Selected Clocks	Displays the clock tree driven by the selected clocks.
Add	Adds a clock from the list of crossover, pre-route, or all clocks in the clock list
Delete	Deletes a selected clock from the *Selected Clock(s)* list.
Filter	Specifies a filter pattern for selecting clocks for the clock list.
Crossover Clocks (Clock list)	Lists the cross-over clocks shown in the display area. You can add any of these to the *Selected Clock(s)* list.

Clock Group (Clock list)	Lists the clock groups shown in the display area. You can then add any of these to the *Selected Clock(s)* list.
All Clocks (Clock list)	Lists all clocks listed in the CTS spec file. You can then add any of these to the *Selected Clock(s)* list.
Pre-Route	Displays clock tree timing analysis results that are based on a CTS Steiner tree.
Clock Tree Only	Displays clock tree timing analysis results that are based only on clock tree wires, even if other wires (such as signal net wires) exist in the design.
Post-Route	Displays post-routing clock tree timing analysis results based on clock tree wires and signal wires on the specified clock, or on all clocks in the design if no clock is specified.

Clock Tree Analyst – Clock – Preference – Display

Use the Display page of the Clock Tree Analyst – Clock – Preference form to specify the default display content and size requirements.

➤ From the Clock Tree Analyst main window, choose *Preferences* from the *Clock* pulldown menu and click on the *Display* tab



Fields and Options

Group All Leaf Pins	Groups leaf pins.
Group All Macro Models	Groups or ungroups macro models.
Abstract All Buffers	Abstracts buffers, which hides instances from view.
Abstract All Inverters	Abstracts inverters, which hides instances from view.
Abstract Cells	Specifies the cells to abstract.
Symbol Size	Specifies the size (in pixels) of the objects in the display.

Display Balloon Information

Displays or hides the information displayed when you mouse-over an object.

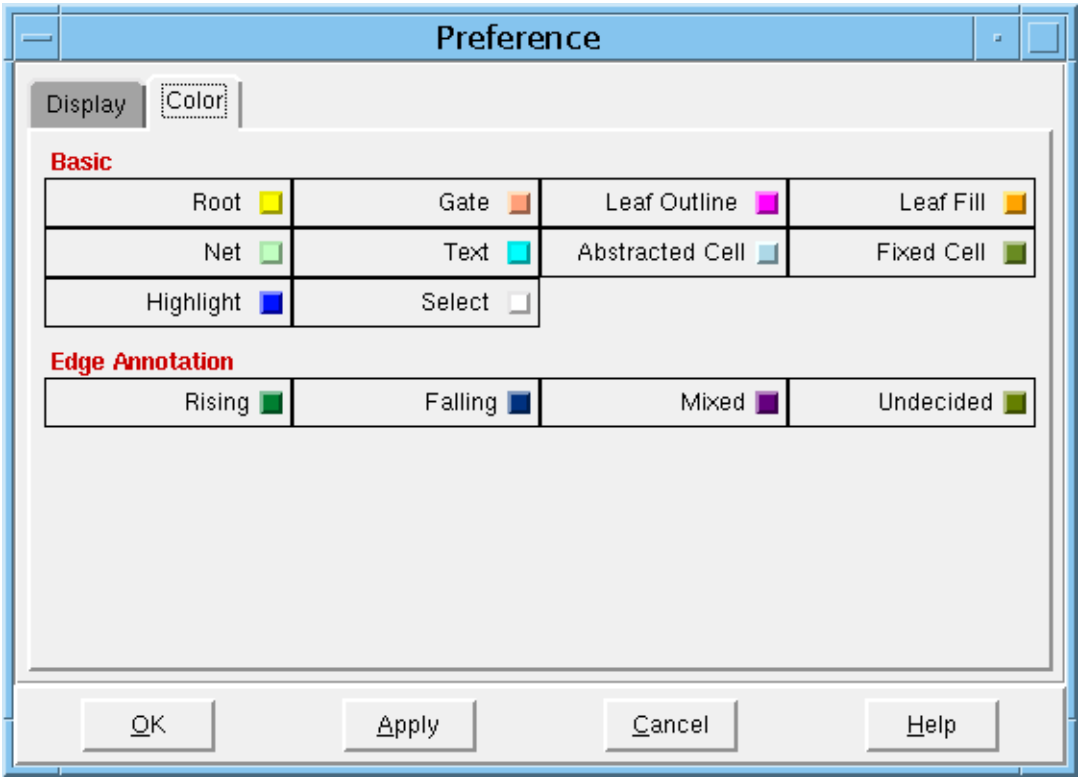
Display the Reconvergence in Excluded/Leaf Pins

Displays reconvergence for this these types of pins.

Clock Tree Analyst – Clock – Preference – Color

Use the Preference – Color form to select a color for the objects and annotations in the Clock Tree Analyst display.

➤ From the Clock Tree Analyst main window, choose *Preferences* from the *Clock* pulldown menu and click on the *Color* tab.



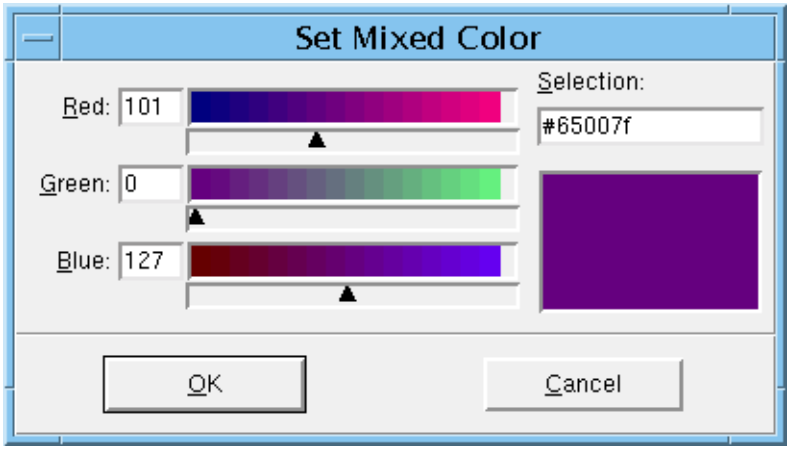
Fields and Options

Basic	Shows the colors defined for displaying, selecting, highlighting objects in the main display. Double-click on any color and use the Set Mixed Color form to change the color. **Note:** If your design contains power domains or partitions, two additional color selections will be displayed: *Power Domain Annotation*, and *Partition Annotation*.
Edge Annotation	Shows colors used in clock edge annotation. Double-click on any color and use the Set Mixed Color form to change the color.

Clock Tree Analyst – Clock – Preference – Color – Set Mixed Color

Use the Set Mixed Color form to create a custom color for the Preference – Color form.

➤ From the Clock Tree Analyst main window, choose *Preference* from the *Clock* pulldown menu and click on the *Color* tab. Double-click on any of the colors.



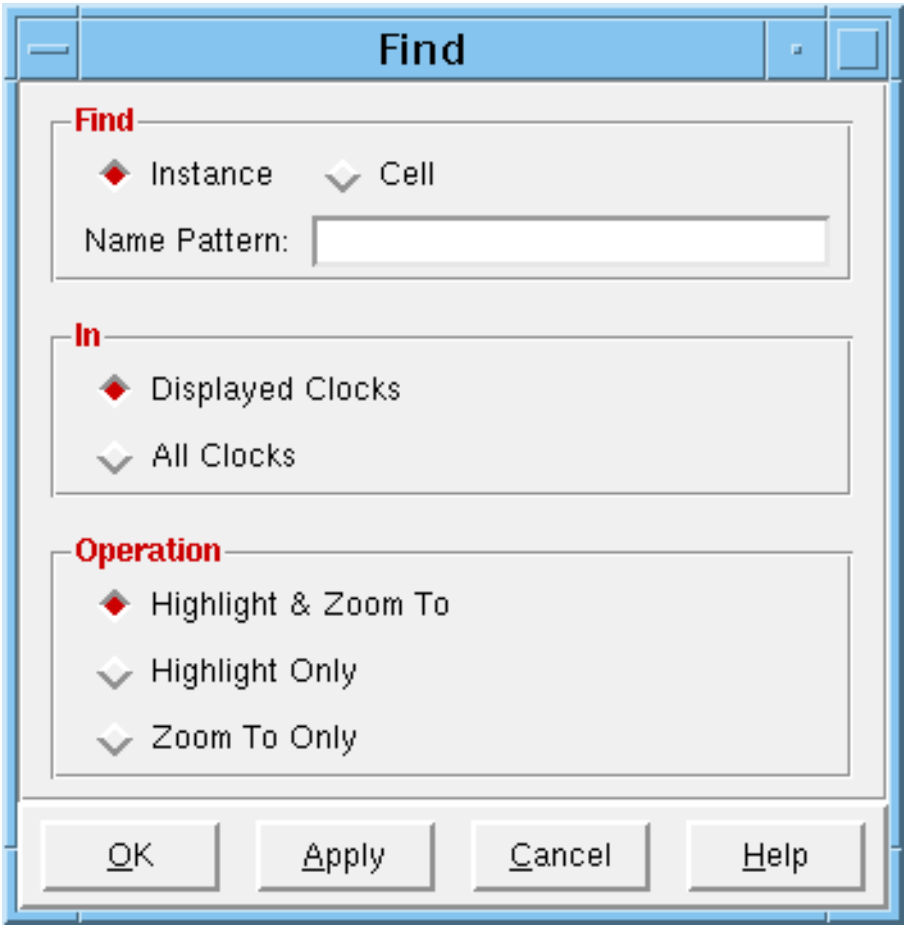
Clock – Preference – Color – Set Mixed Color Fields and Options

Red, Green, Blue	Lets you select the color values that create the custom color. Use the slider to select the values.
Selection	Displays a unique number for the color.
Panel	Displays the custom color.

Clock Tree Analyst – Tool – Find – Instance

Use the Find form to find instances and cells in the clock tree.

➤ From the Clock Tree Analysis main window, choose *Find* from the *Tools* pulldown menu, then select *Instance*. Or, click the Find icon in the Clock Tree Analyst toolbar.



Fields and Options

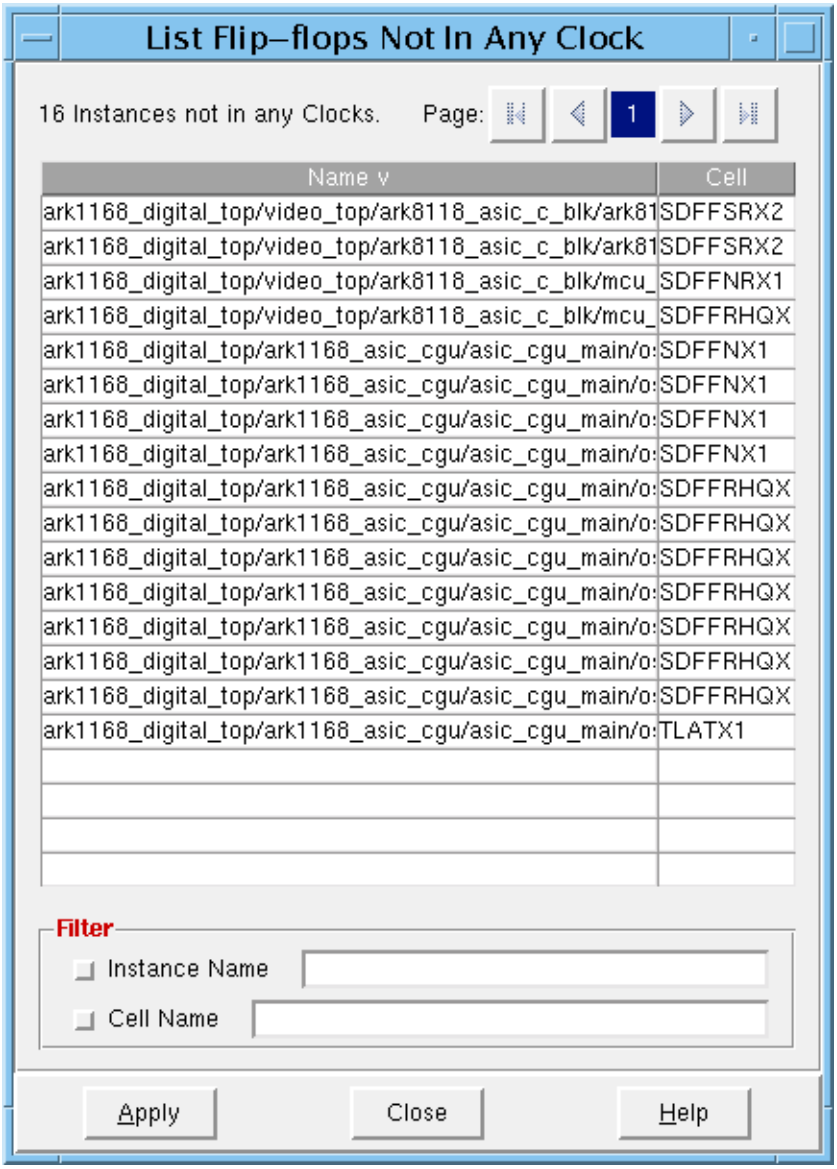
Instance	Locates an instance or instances specified by *Name Pattern*.
Cell	Locates a cell or cells specified by Name Pattern.
Name Pattern	Specifies the name or names of cells or instances to find.
Displayed Clocks	Locates the instances or cells in the displayed clocks only.

All Clocks	Locates the instances or cells in all clocks.
Highlight & Zoom To	Highlights the instances or cells and zoom-in to display them.
Highlight Only	Highlights the instances or cells.
Zoom To Only	Zooms into the instances or cells and displays them.

Clock Tree Analyst – Tool – List Flip-Flops Not In Any Clock

You can use this form to list flip-flops not belonging to any clock.

➤ From the Clock Tree Analyst Main Window, choose *List FF's Not In Clock Tree* from the *Tool* menu.



Fields and Options

Instance Name	Filters the sink list based on the instance name pattern.
Cell Name	Filters the sink list based on the cell name pattern.

Clock Tree Analyst – Find – Reconvergence

Use the Find Reconvergence form to find and display reconvergent objects.

➤ From the Clock Tree Analyst main window, choose *Find* from the *Tool* menu, and select *Reconvergence*.

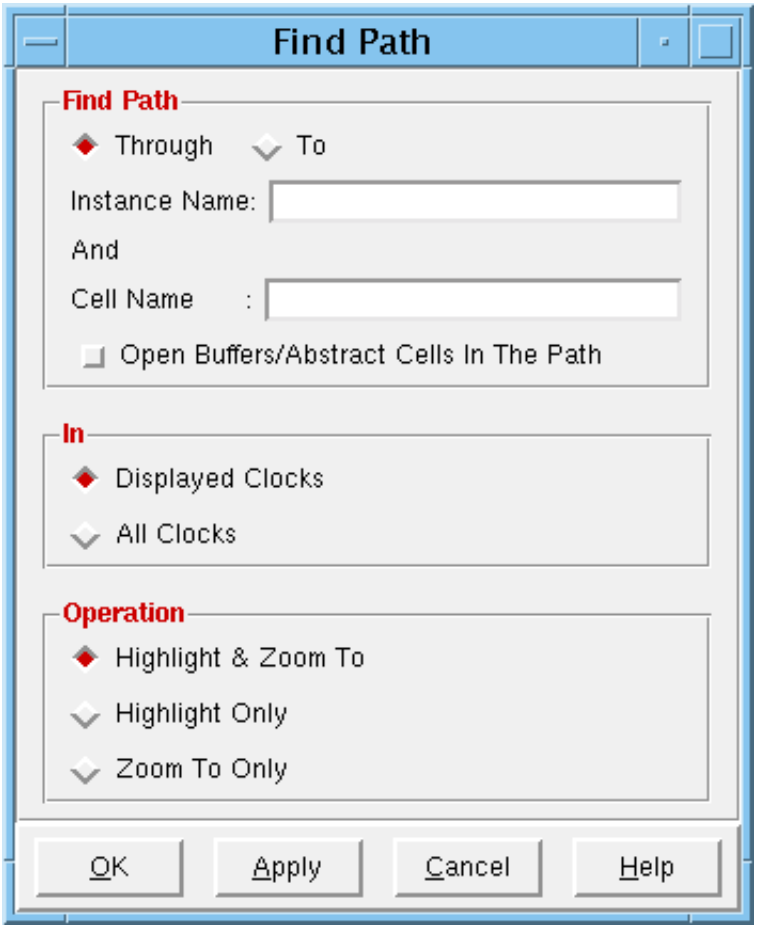
Fields and Options

Displayed Clocks	Finds reconvergence in the displayed clocks only.
All Clocks	Finds reconvergence in all clocks.
Highlight & Zoom To	Highlights the path and zooms into the reconvergence in the display. Reconvergence is shown as a dashed line.
Highlight Only	Highlights the reconvergence in the display. Reconvergence is shown as a dashed line.
Zoom To Only	Zooms into the reconvergence in the display but does not highlight it. Reconvergence is shown as a dashed line.

Clock Tree Analyst – Find – Path

Use the Find Path form to locate a path going through or to a specified instance, and display the objects between the root and a specified instance.

➤ From the Clock Tree Analyst main window, choose *Find* from the *Tool* menu, and select *Path*.



Fields and Options

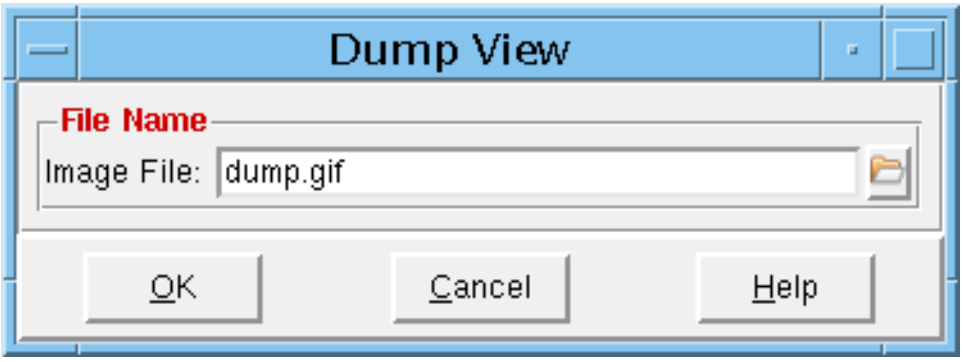
Through	Finds the path through the instance.
To	Finds the path to the instance.
Instance Name	Specifies the instance through or to which the tool must search for the path.

Cell Name	Specifies the instance's cell.
Open Buffers/Abstract Cells in the Path	
	Displays the buffers and abstracted cells in the path.
Displayed Clocks	Finds the path in the displayed clocks only.
All Clocks	Finds the path in all clocks.
Highlight & Zoom To	Highlights all the objects between the root and a specified instance and zooms into the objects in the display.
Highlight Only	Highlights the objects in the path.
Zoom To Only	Zooms into the objects in the path in the display but does not highlight them.

Clock Tree Analyst – Tool – Dump View

Use the Dump View form to write an image of the display to a file.

➤ From the Clock Tree Analyst main window, select *Dump View* from the *Tool* menu.



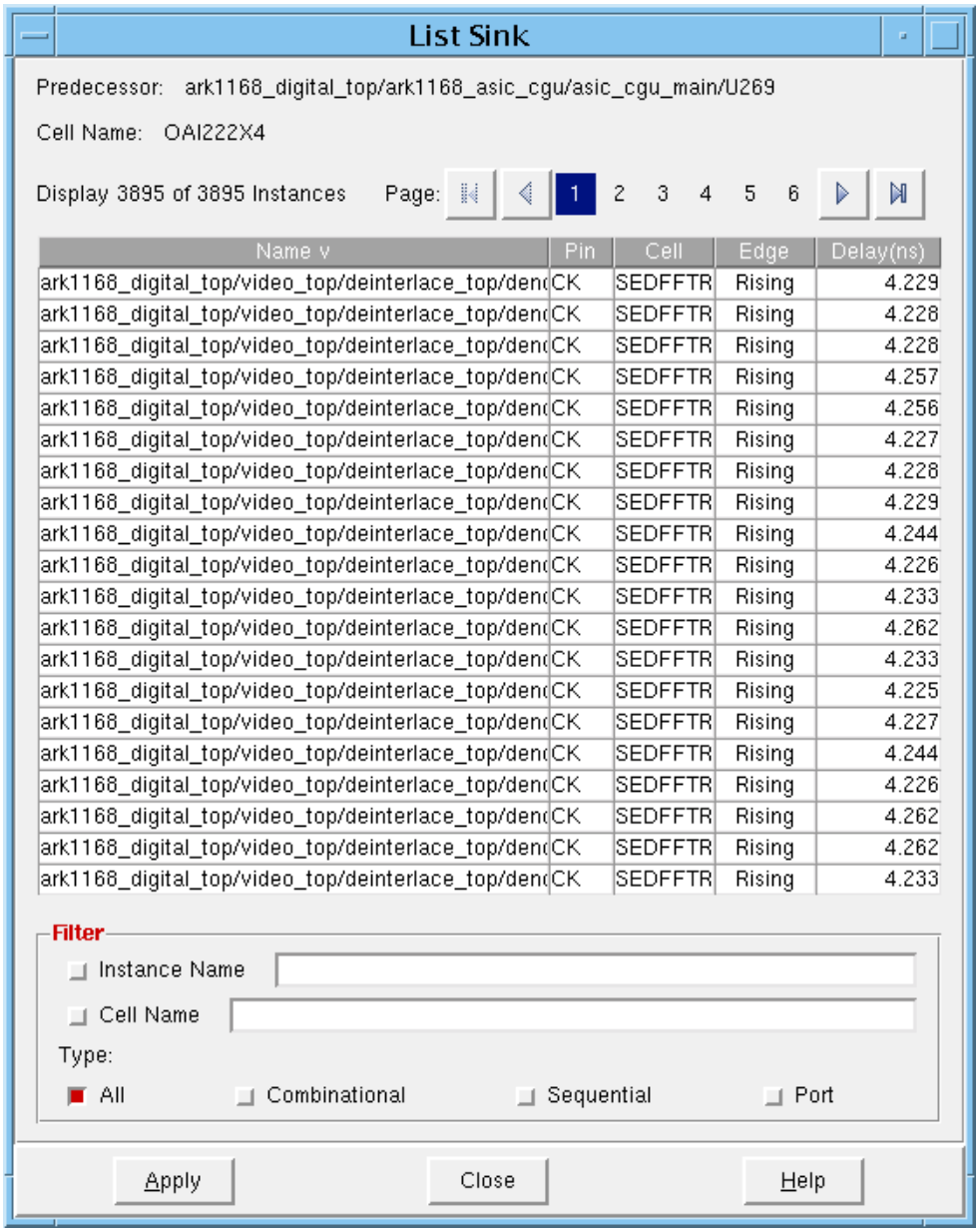
Fields and Options

Image File	Specifies the name of the file where you want to dump the display image. *Default:* `dump.gif`

Clock Tree Analyst – List Sink

Use the List Sink form to list all the leaves that are in the downstream logic from an element so that you can identify a specific leaf or leaves.

➤ From the Clock Tree Analyst display, right-click on an element and choose *List Sink*.



Fields and Options

Instance Name	Filters the sink list based on an instance name pattern.
Cell Name	Filters the sink list based on a cell name pattern.
All	Lists all types of leaves: combinational, sequential, and port.
Combinational	Lists all combinational leaves.
Sequential	Lists all sequential leaves.
Port	Lists all port leaves.

Display

The display menu provides the following forms and commands to display the clock tree after CTS, and to clear the clock tree display:

- Display Clock Tree on page 1122
- Clear Clock Tree Display on page 1125

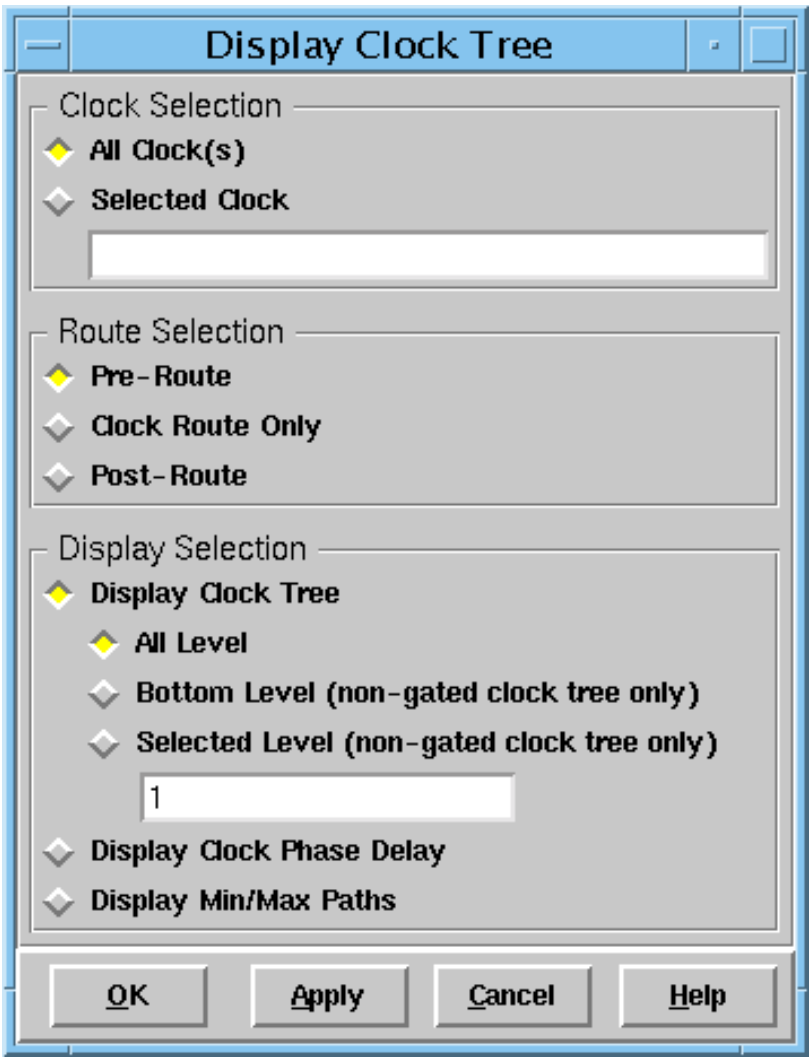
Display Clock Tree

Use the Display Clock Tree form after running CTS to display the clock tree for all clocks or for a single clock.

Important

If you want to generate a clock tree report for a design on which you have already run clock tree synthesis, and which you have restored during an Encounter session, you must load the design's clock tree specification file with the Specify Clock Tree form.

➤ Choose *Clock – Display – Display Clock Tree*.



Fields and Options

Clock Selection Determines the clock(s) to be displayed.

Choose one of the following:

All Clock(s) Displays all clocks in the clock tree specification file.

Selected Clock Displays a specific clock net.

Route Selection Selects the routing status of the clock(s) to be displayed.

Choose one of the following:

Pre-Route Displays clock tree timing analysis results that are based on a CTS Steiner tree.

Clock Route Only Displays clock tree timing analysis results that are based only on clock tree wires, even if other wires (such as signal net wires) exist in the design.

Post-Route Displays post-routing clock tree timing analysis results based on clock tree wires and signal wires on the specified clock, or on all clocks in the design if no clock is specified.

Note: CTS halts and displays a message if the design has not been routed.

Display Section Determines the kind of information to display in the Physical view.

Choose one of the following:

Display Clock Tree Displays clock tree and instances.

Choose one of the following:

All Level: Allows the display of gated and nongated clock trees in the Physical view.

Bottom Level (non-gated clock tree only): Displays the bottom level of nongated clock trees.

Selected Level (non-gated clock tree only): Displays the non-gated clock tree level specified by the user.

Display Clock Phase Delay	Displays only the selected clock tree instances' phase delay.
Display Clock Min/Max Path	Displays fly lines for the minimum (blue) and maximum (red) clock path delays.

Related Text Command

- `displayClockTree`

Clear Clock Tree Display

Use the *Clock – Display – Clear Clock Tree Display* command to clear the clock tree display.

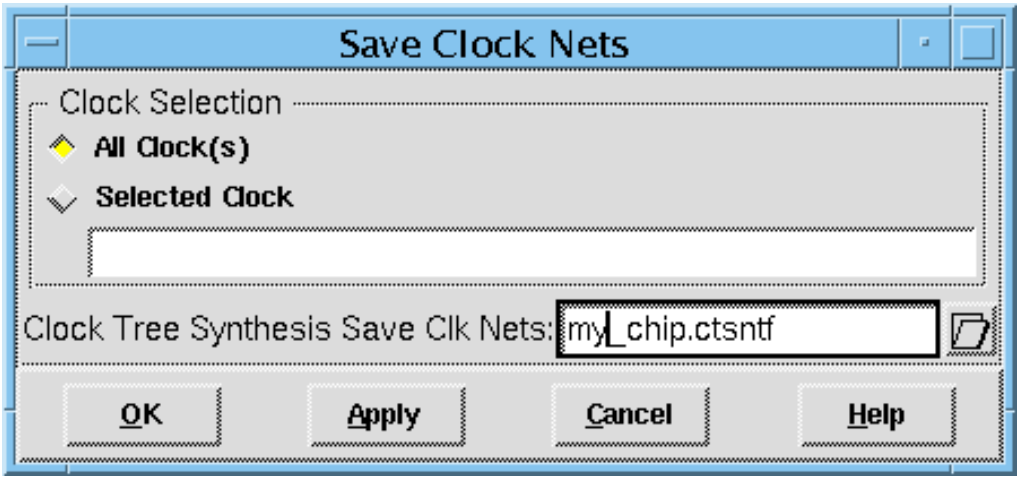
Related Text Command

- `clearClockDisplay`

Save Clock Nets

Use the Save Clock Nets form to save a clock net file that you can use for running detailed routing of the clock tree.

➤ To open the Save Clock Nets form, choose *Clock – Save Clock Nets*.



Fields and Options

Clock Selection

Specifies which clock nets to save.

Choose one of the following:

All Clock(s) Saves all clocks in the clock tree specification file.

Selected Clock Saves a specific clock net.

Clock Tree Synthesis Save Clk Nets

Specifies the filename for the report. The default report name is `top_level_cell.ctsntf`.

Related Text Command

- `saveClockNets`

Generate Clock Tree Spice

Use the Clock Tree SPICE Out form to create a SPICE netlist file (containing RC parasitics) that you can use with circuit simulation software to validate

- Skew values and insertion delay for a given clock tree
- Transition times at the inputs of clock buffers for a given clock tree

➤ Choose *Clock – Generate Clock Tree SPICE*.

Fields and Options

Clock Name	Specifies the name of the root clock's net name, the root clock fterm name, or the root clock instance term name.
cdb File	Specifies cdb files or a directory containing cdb file(s). If you specify a directory name, CTS looks for all files that end with `.cdb`, `.cdB`, or `.udn` filename extensions. The cdb file or directory provide subcircuit netlists for the logical and sequential elements in the clock tree (such as clock buffers, logical gates, and registers).

SPEF File	Specifies the SPEF file containing the RC parasitics of the clock tree. If you do not specify this parameter, CTS uses the Encounter `rcOut` command to generate the SPEF file. **Note:** If you have not extracted the parasitics for your design, CTS displays an error message.
Save SPICE Netlist To	Specifies the name of the output SPICE netlist file.

Related Text Command

- `clockSpiceOut`

Clock Mesh

The Clock Mesh menu contains the following forms and commands:

- Specify

  Opens the Edit Clock Mesh Specification form.

- Synthesize

  Opens the Synthesize Clock Mesh form.

- Delete Mesh Implementation

  Opens the Delete Clock Mesh form.

- Route Mesh

  Opens the Route Clock Mesh form.

- Trim Mesh Routes

  Opens the Trim Clock Mesh form.

- Analyze

  Refreshes timing information.

- Report

  Opens the Report Clock Mesh form.

- Display

  Opens the Display Clock Mesh form.

Edit Clock Mesh Specification

The Edit Clock Mesh Specification form can be used to view and edit the clock mesh specifications currently in memory.

You can use this form to experiment with different mesh configurations and parameters by repeatedly changing the clock mesh specification and invoking clock mesh synthesis directly from the form.

The Edit Clock Mesh Specification form contains seven pages:

- Edit Clock Mesh Specification – Route Types

  Controls routing type definitions that are common to all currently specified meshes.

- Edit Clock Mesh Specification – Constraints

  Controls the mesh environment and constraints.

- Edit Clock Mesh Specification – Scope

  Controls mesh tracing information.

- Edit Clock Mesh Specification – Chain

  Controls parameters for the top-level cascade chain.

- Edit Clock Mesh Specification – Mesh Structure

  Controls parameters for the global mesh structure.

- Edit Clock Mesh Specification – Mesh Stage

  Controls parameters for the global mesh stage.

- Edit Clock Mesh Specification – Local Tree

  Controls parameters for the mesh local tree.

Common Controls

The Edit Clock Mesh Specification form contains the following controls that can be used from any page:

- *Clock Mesh*

  Specifies which mesh of the current specification to edit.

Note: With the exception of the *Route Types* page, the data on all pages of the Edit Clock Mesh Specification form are specific to the currently selected mesh.

- *New Mesh*

  Adds a new mesh to the current specification.

  To add a new mesh:

  a. Type the name of the mesh in the text entry field.

  b. Click *New Mesh*.

  c. Fill in information for the new mesh (for example, its root pin) on the appropriate pages of the form.

  d. Click *Apply* to update the current specification.

- *OK*

  Updates the mesh specification currently in memory with the values on the form, then closes the form.

- *Apply*

  Updates the mesh specification currently in memory with the values on the form, then leaves the form open.

- *Load*

  Opens the Load Clock Mesh form.

- *Clear*

  Opens the Unspecify Clock Mesh form.

- *Synth*

  Updates the current mesh specification with the values on the form and then starts clock mesh synthesis. Clock mesh synthesis uses the specific options set with the Synthesize Clock Mesh form.

- *Save*

  Opens the Save Clock Mesh form.

- *Close*

  Closes the form without updating the mesh specification.

Related Text Commands

- `synthesizeClockMesh`

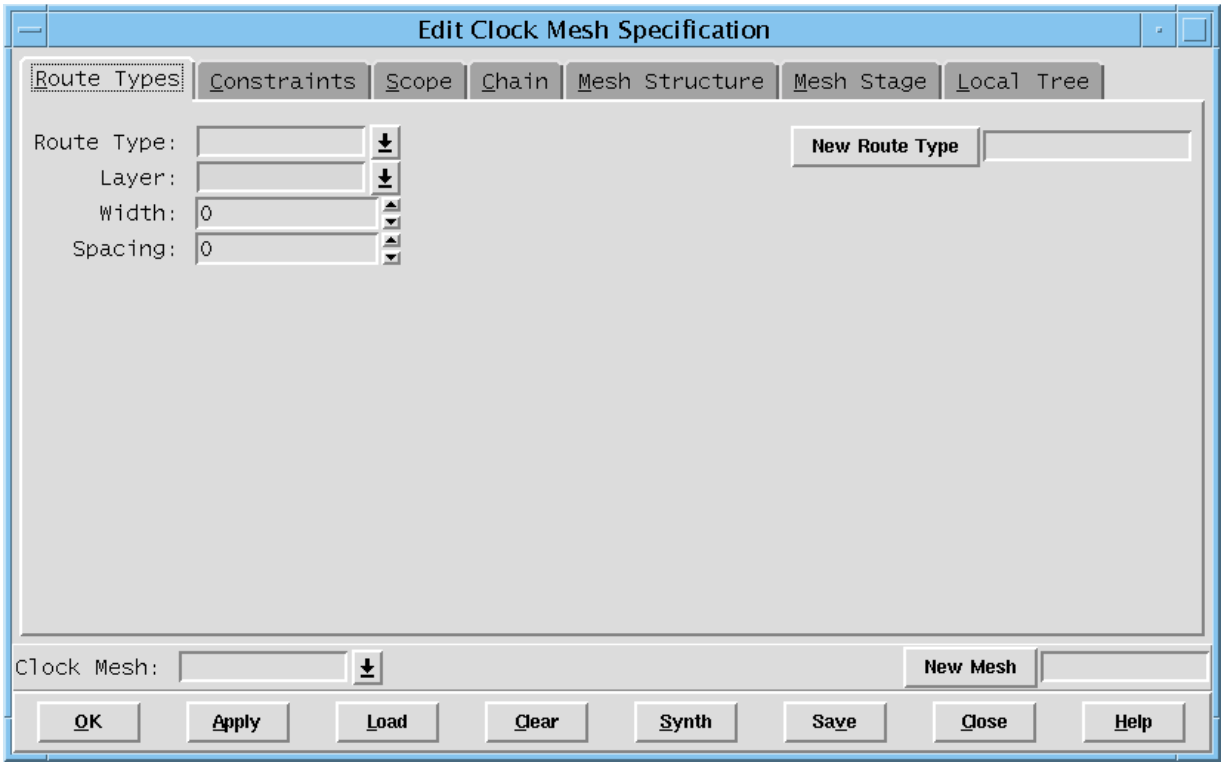
Related Topics

- Clock Mesh Specification File

Edit Clock Mesh Specification – Route Types

Use the *Route Types* page to view and edit the routing properties to be used during clock mesh implementation. These properties are referenced later in other parts of the clock mesh specification.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Route Types* tab.



Fields and Options

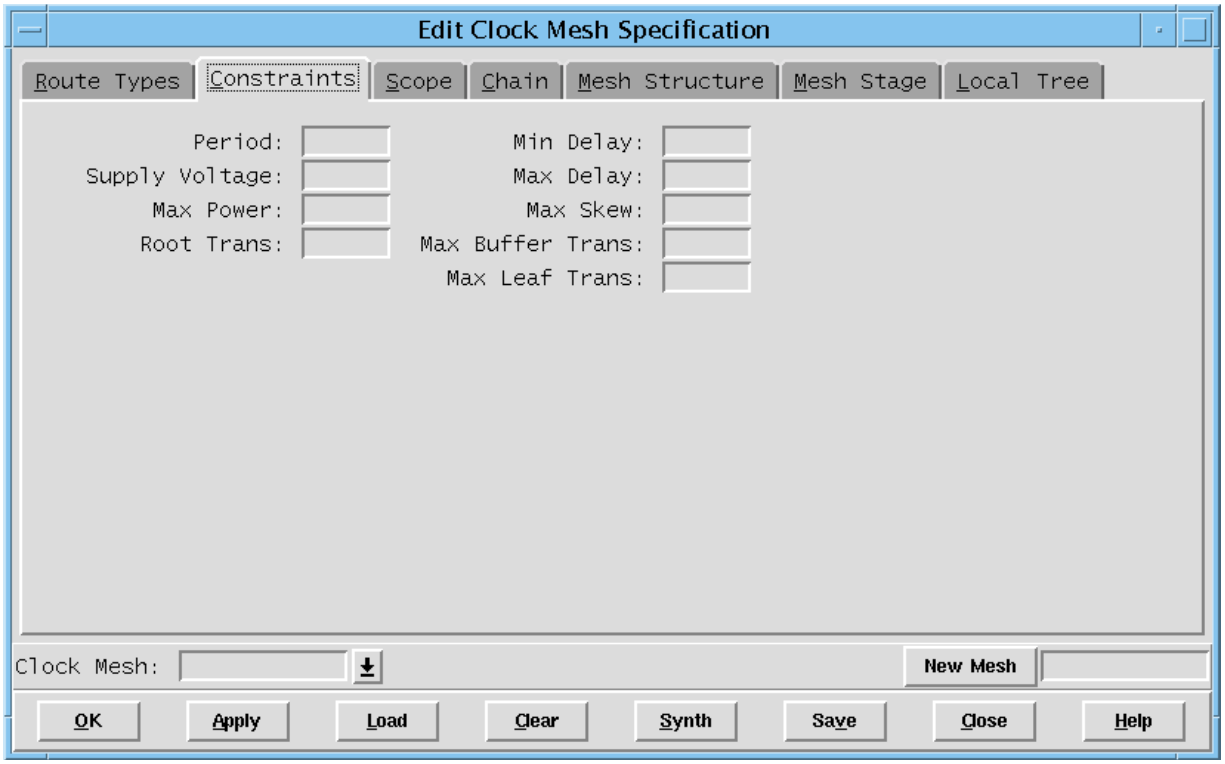
Route Type	Specifies the routing type for which you are defining routing attributes.
Layer	Specifies the metal layer to be used. The name you specify must be a layer name defined in the LEF file.
Width	Specifies the width (in microns) of the metal layer to be used. *Default:* `0`

Spacing	Specifies the spacing (in microns) to all other wires in the design. *Default:* Uses the minimum spacing values specified in the LEF file
New Route Type	Defines a new route type. **1.** Specify the new route type name. **2.** Click *New Route Type*. **3.** Specify layer, width, and spacing data on the left side of the form.

Edit Clock Mesh Specification – Constraints

Use the *Constraints* page to specify timing and power constraints for the currently selcted clock mesh.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Constraints* tab.



Fields and Options

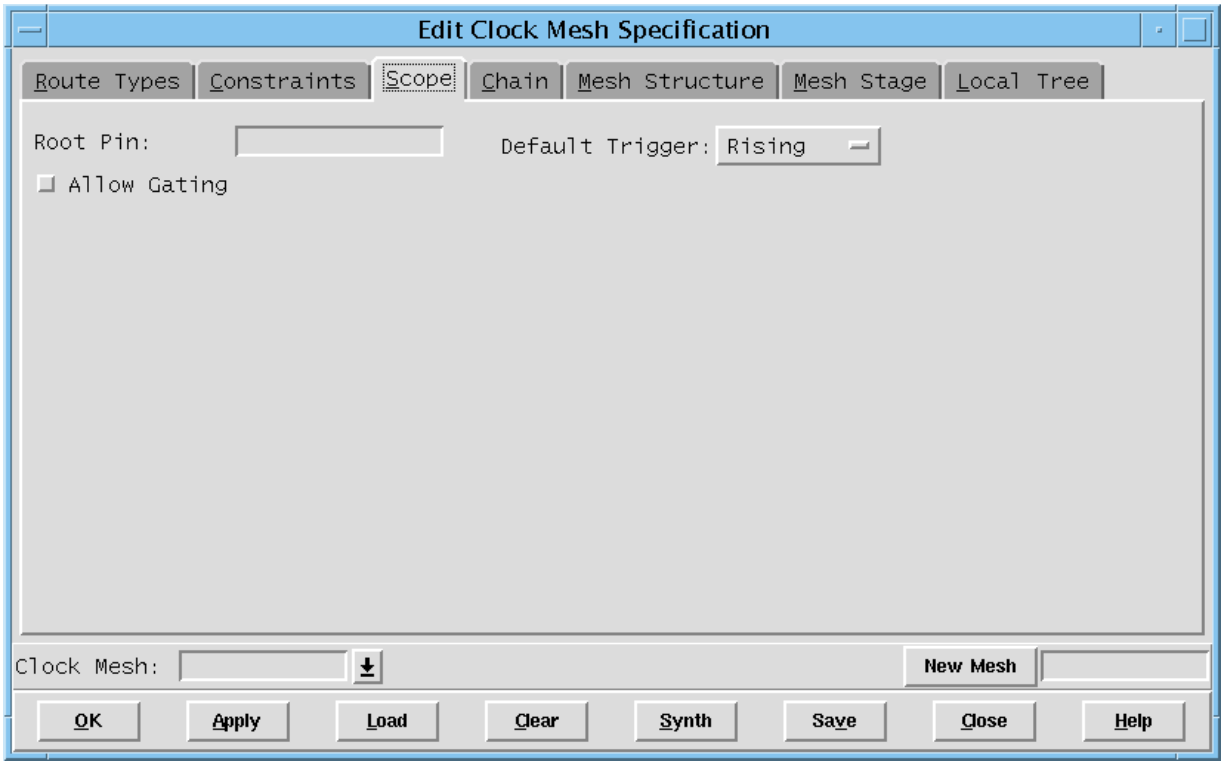
Period	Specifies the clock period (in picoseconds) for the mesh structure.
Supply Voltage	Specifies the power supply voltage for the mesh. The software uses this value when analyzing clock mesh power.
Max Power	Specifies the maximum power value (in milliwatts) for the mesh.
Root Trans	Specifies the transition time (in picoseconds) at the root pin.
Min Delay	Specifies the minimum phase delay (in picoseconds).

Max Delay	Specifies the maximum phase delay (in picoseconds).
Max Skew	Specifies the maximum skew between sink pins (in picoseconds).
Max Buffer Trans	Specifies the maximum input transition time for buffers (in picoseconds).
Max Leaf Trans	Specifies the maximum input transition time for leaf pins (in picoseconds).

Edit Clock Mesh Specification – Scope

Use the *Scope* page to specify the logical extent of the clock domain, from the root through any mesh drivers to the leaves. Scope is determined by tracing the netlist from the clock root.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Scope* tab.



Fields and Options

Root Pin	Specifies the complete name of the clock root pin from which the tracing starts.
Default Trigger	Specifies the default trigger edge value for leaves that do not have a specified trigger edge value. *Default: Rising*

Allow Gating

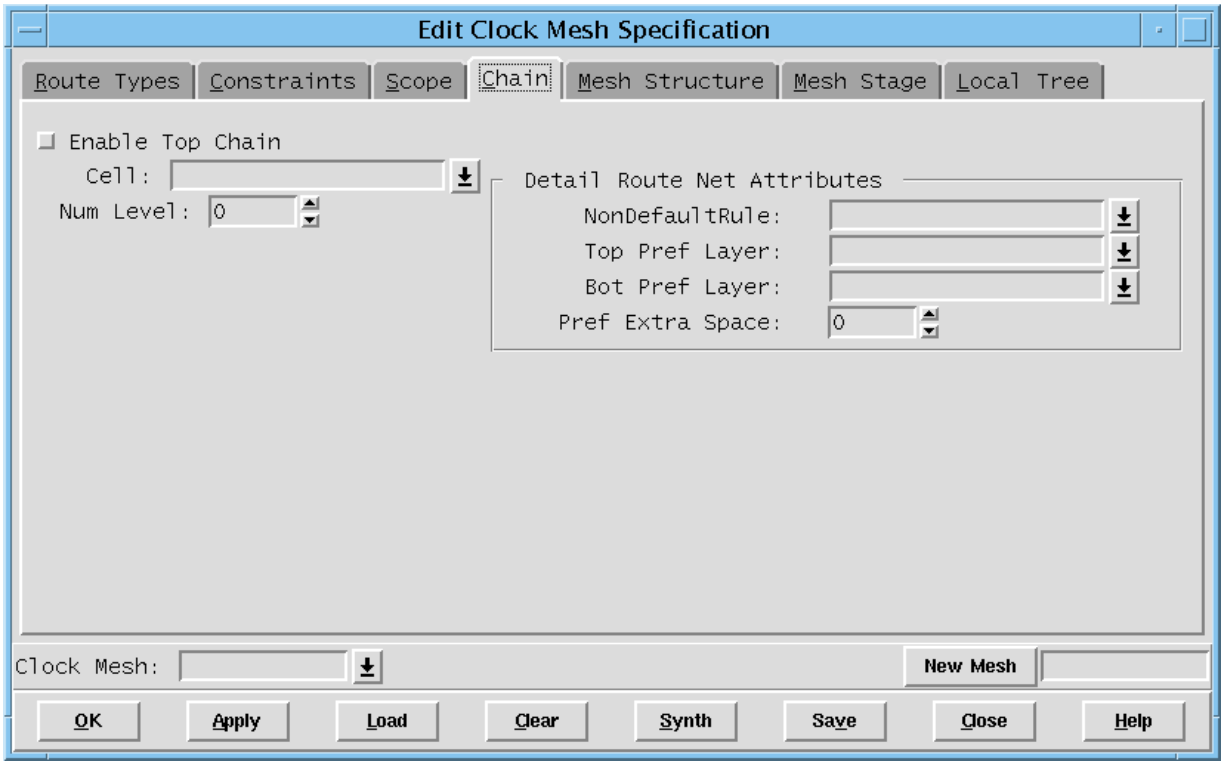
Specifies whether the clock mesh tool traces through gates. If you select this option, the software traces until it finds leaf pins. If you do not select this option, the software stops at gate inputs.

Default: Off

Edit Clock Mesh Specification – Chain

Use the *Chain* page to defines how the top chain is to be synthesized. A top-level chain is a cascaded driver chain from the mesh root to the first level of mesh pre-driver drivers.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Chain* tab.



Fields and Options

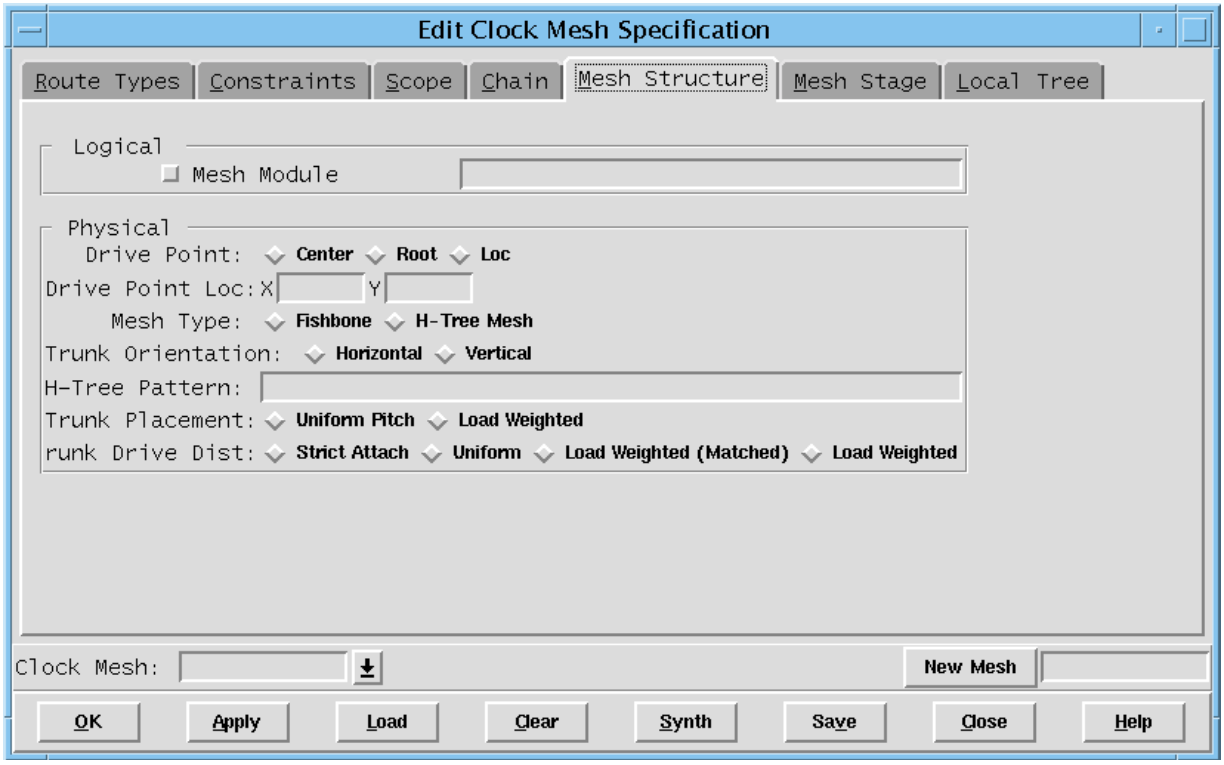
Enable Top Chain	Enables the implementation of the top chain. *Default:* Off
Cell	Specifies the type of buffer to be used for constructing the top-level chain. Only one cell type can be used for the chain.
Num Level	Specifies the number of levels in the chain structure (which is equal to the number of buffers). You must specify an even number of levels if you use an inverter for the drive cell (*Cell*).

NonDefaultRule	Specifies the LEF `NONDEFAULTRULE` statement for the router to use when routing the nets in the top-level chain. *Default:* The router uses the default routing rule.
Top Pref Layer	Specifies the top preferred metal layer to use for routing the top-level chain buffers. The name you specify must be a layer defined in the LEF file.
Bot Pref Layer	Specifies the bottom preferred metal layer to use for routing the top-level chain buffers. The name you specify must be a layer defined in the LEF file.
Pref Extra Space	Specifies the extra space to add around clock wires, when routing the nets in the top-level chain. *Default:* `0`

Edit Clock Mesh Specification – Mesh Structure

Use the *Mesh Structure* page to define overall logical and physical attributes of the global clock mesh structure.

➤ Choose *Clock – Specify*, then click the *Mesh Structure* tab.



Fields and Options

Mesh Module

Specifies whether the clock mesh tool should create a separate module for the mesh buffers, and specifies the module name to be used.

If you select this option, the software creates a module at the level of the root net. If you do not select this option, the software inserts buffers (flat) at the level of the root net.

Default: On

Drive Point

Specifies the position of the first-stage pre-drivers.

Default: *Center*

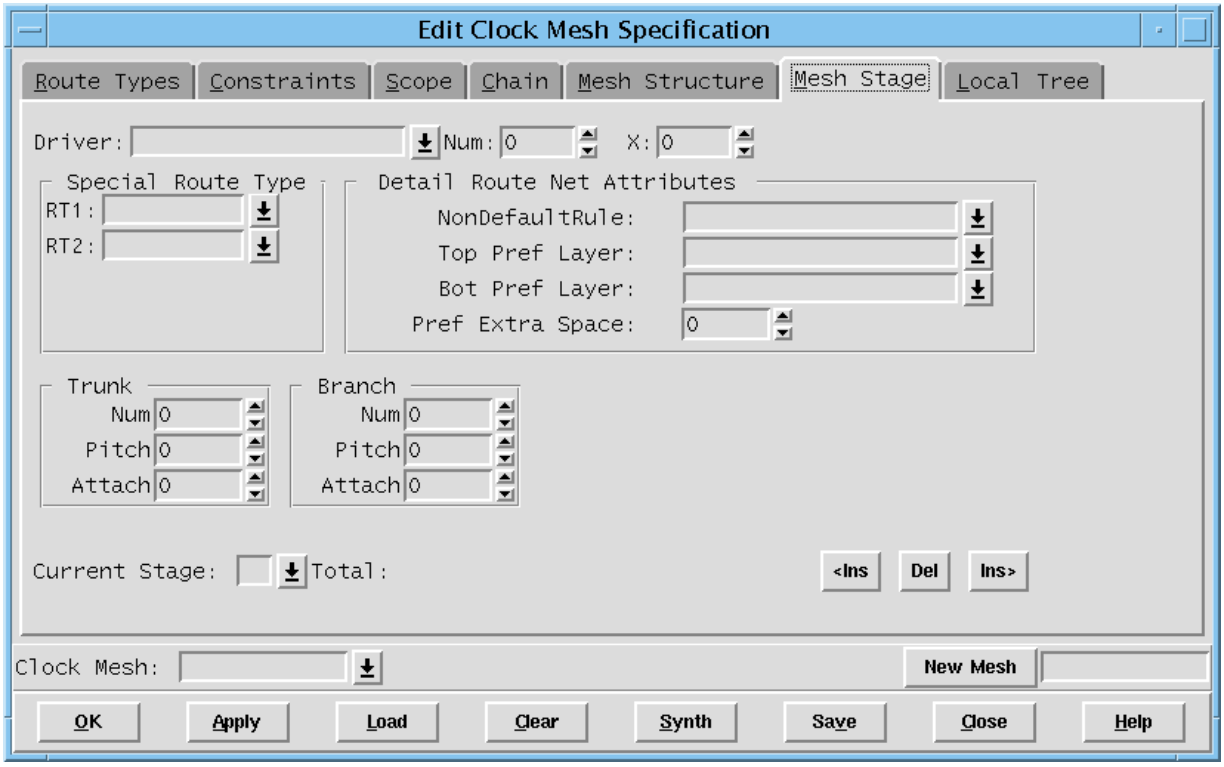
	Center	Positions the pre-drivers near the center of the clock mesh structure.
	Root	Positions the pre-drivers near the clock root pin.
	Loc	Positions the pre-drivers at the location specified with the *Drive Point Loc* option.
Drive Point Loc	Specifies the x, y coordinates of the location at which to position the pre-drivers.	
Mesh Type	Specifies the type of mesh structure to be synthesized.	
	Default: *Fishbone*	
Trunk Orientation	Specifies the trunk orientation.	
	Default: *Horizontal*	
H-Tree Pattern	Specifies the order for building horizontal (`H`) and vertical (`V`) structures for an HTree + Mesh clock mesh.	
	You can use `H` and `V` in any pattern to specify the order. Specifying an asterisk (`*`) causes the tool to repeat alternating structures. For example, specifying `H*` is equivalent to specifying `HVHV`; it is *not* equivalent to specifying `HHHH`.	
Trunk Placement	Specifies how trunks are to be placed if predefined target locations are not specified in the clock mesh specification file.	
	Uniform Pitch	Places trunks uniformly according to trunk pitch.
	Load Weighted	Places each trunk so that it drives a similar load.
Trunk Drive Dist	Specifies how buffers are placed along driving trunks in the final global mesh stage.	
	Strict Attach	Places the buffers according to the specified branch attachment period in the final global mesh stage.
	Uniform	Places the buffers in an even, uniform distribution along the trunk. .
	Load Weighted (Matched)	

	Places the drivers according to load distribution, and applies the same pattern to all trunks. The specified branch attachment period in the final global mesh stage limits how closely the buffers can be placed to each other.
Load Weighted	Places the buffers according load distribution. The specified branch attachment period in the final global mesh stage limits how closely the buffers can be placed to each other.

Edit Clock Mesh Specification – Mesh Stage

Use the *Mesh Stage* page to define stage-specific parameters for the global mesh, including driver cells, route types, and trunk and branch information.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Mesh Stage* tab.



Fields and Options

Driver	Specifies the type of driver to be used for the stage being defined.
Num	Specifies the number of drivers that should be inserted at the current stage.

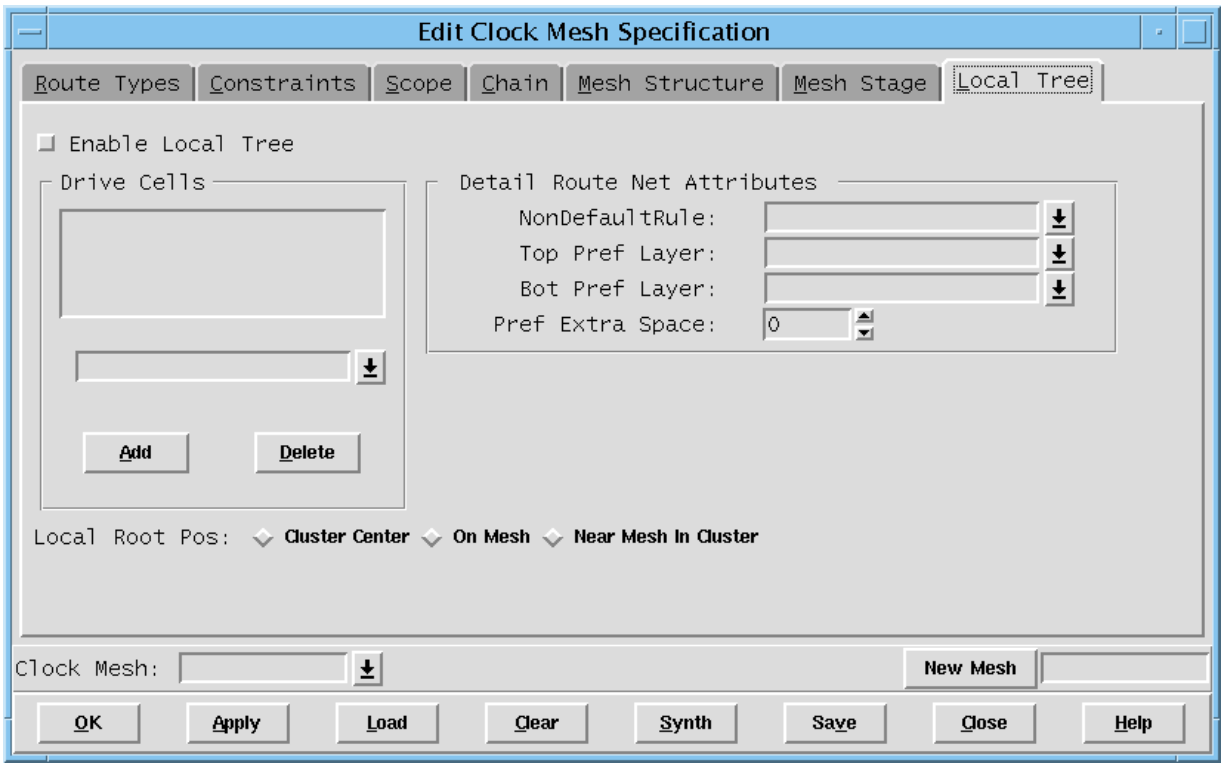
X	Specifies a grouping factor that controls the number of drivers at each node or endpoint at the current stage of an HTree clock mesh structure. If you use the X grouping factor, you can increase the drive at any given level of the tree. **Note:** This statement only can be used when you are defining an HTree + Mesh structure. *Default:* Uses a single driver at the end of each node.
RT1 RT2	Specifies the routing types to be used for the stage. Routing types are defined on the *Route Types* page.
Nondefault Rule	Specifies the LEF `NONDEFAULTRULE` statement for the router to use when routing the nets for a particular stage of the global mesh structure. *Default:* The router uses the default routing rule.
Top Pref Layer	Specifies the top preferred metal layer to use for routing for a particular stage of the global mesh structure. The name you specify must be a layer defined in the LEF file.
Bot Pref Layer	Specifies the bottom preferred metal layer to use for routing for a particular stage of the global mesh structure. The name you specify must be a layer defined in the LEF file.
Pref Extra Space	Specifies the extra space to add around clock wires, when routing the nets in the top-level chain. *Default:* `0`
Trunk Num	Specifies the number of trunks to create for a particular stage. You can specify this statement for any stage in the clock mesh structure, but it only is useful for the final construction stage. A Fishbone mesh structure can have one or two trunks (that is, you can specify single or double Fishbone mesh structures). The number of trunks for the second-to-last stage will be 1 or 3, depending on whether the mesh structure is a single of double Fishbone. For all other stages, the number of trunks is 1. For an HTree + Mesh structure, this statement is relevant only to the last stage. If you do not specify this statement for an HTree + Mesh structure, the clock mesh tool computes a suitable value automatically. If you specify a value that is less than the minimum number of trunks required to implement the structure, the clock mesh tool displays an error message.

Trunk Pitch	Specifies the pitch (in microns) for the trunk for a particular stage. **Note:** The clock mesh tool considers the *Trunk Pitch* to be a soft constraint that applies to the final mesh stage. The tool might need to adjust the specified pitch in order to meet physical constraints.
Trunk Attach	Specifies the frequency with which buffers are attached to the trunks. You must specify a number that is greater than or equal to 1.
Branch Num	Specifies the number of branches.
Branch Pitch	Specifies the pitch for the branches for a particular stage. **Note:** The clock mesh tool considers the *Branch Pitch* value to be a soft constraint that applies to the final mesh stage. The tool might need to make adjustments to the specified pitch in order to meet physical constraints.
Branch Attach	Controls the frequency with which buffers are attached to branches. You can specify a positive or negative whole number value. *Default*: If you specify *0* for this option, the clock mesh software chooses a default value automatically.
Current Stage	Specifies the stage to edit.
<Ins Del Ins>	Controls stage insertion and deletion. *<Ins* — Inserts a new stage before the current stage. *Del* — Deletes the current stage. *Ins>* — Inserts a new stage after the current stage.

Edit Clock Mesh Specification – Local Tree

Use the *Local Tree* page to define how the local tree is to be synthesized.

➤ Choose *Clock – Clock Mesh – Specify*, then click the *Local Tree* tab.



Fields and Options

Enable Local Tree	Enables the implementation of the local tree. *Default*: Off
Drive Cells	Specifies the types of drive cells to use in the local tree. Multiple drive cells can be specified. Use the *Add* and *Delete* buttons as needed to revise the list of drive cells.
NonDefaultRule	Specifies the LEF `NONDEFAULTRULE` statement for the router to use when routing the local tree. *Default:* The router uses the default routing rule.

Top Pref Layer
Specifies the top preferred metal layer to use for routing the local tree. The name you specify must be a layer defined in the LEF file.

Bot Pref Layer
Specifies the bottom preferred metal layer to use for routing the local tree. The name you specify must be a layer defined in the LEF file.

Pref Extra Space
Specifies the extra space to add around clock wires when routing the local tree.

Default: `0`

Local Root Pos
Specifies how to place the buffers.

Default: Cluster Center

Cluster Center
Places buffers at the cluster center of gravity.

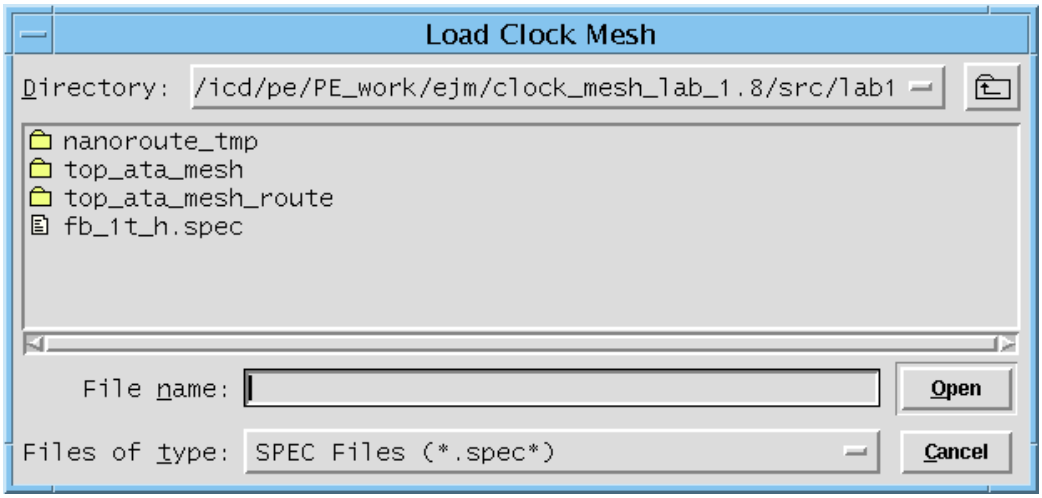
On Mesh
Places buffers on or along the nearest mesh trunk or branch. Buffer placement can extend beyond the bounding box of the cluster.

Near Mesh In Cluster
Places the buffers as close as possible to a mesh trunk or branch without going outside the bounding box of leaves driven by the local root.

Load Clock Mesh

Use the Load Clock Mesh form to choose a clock mesh specification file and load it into system memory.

➤ Click the *Load* button at the bottom of the Edit Clock Mesh Specification form.



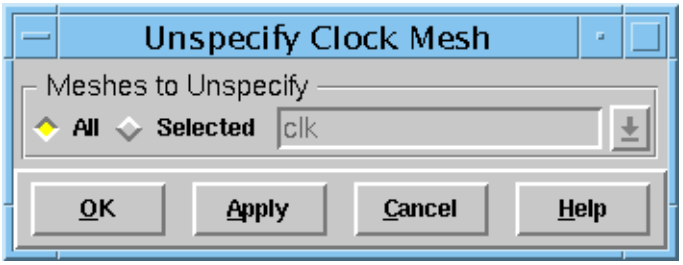
Related Text Commands

■ `specifyClockMesh`

Unspecify Clock Mesh

Use the Unspecify Clock Mesh form to remove the specification for one or more clock meshes.

➤ Click the *Clear* button at the bottom of the Edit Clock Mesh Specification form.



Fields and Options

Meshes to Unspecify

Specifies the clock meshes for which to remove mesh specification information from the system memory.

Default: All

All	Removes all mesh specification information from system memory, including cutouts and route type definitions.
Selected	Removes mesh information for the selected clock meshes.

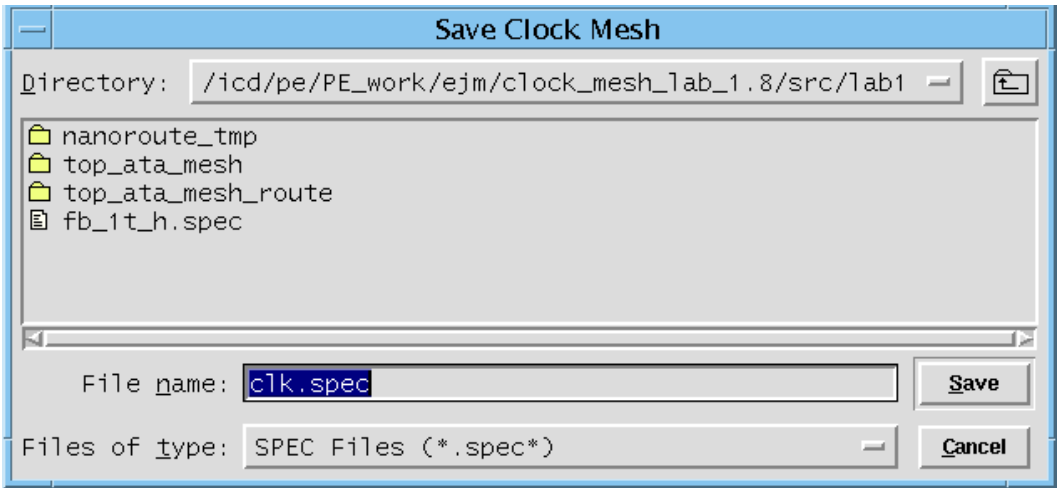
Related Text Commands

- `unspecifyClockMesh`

Save Clock Mesh

Use the Save Clock Mesh form to save the current mesh specification in a file.

➤ Click the *Save* button at the bottom of the Edit Clock Mesh Specification form.



Fields and Options

File Name	Specifies the name of the clock mesh specification file to save.

Related Text Commands

- `saveClockMeshSpec`

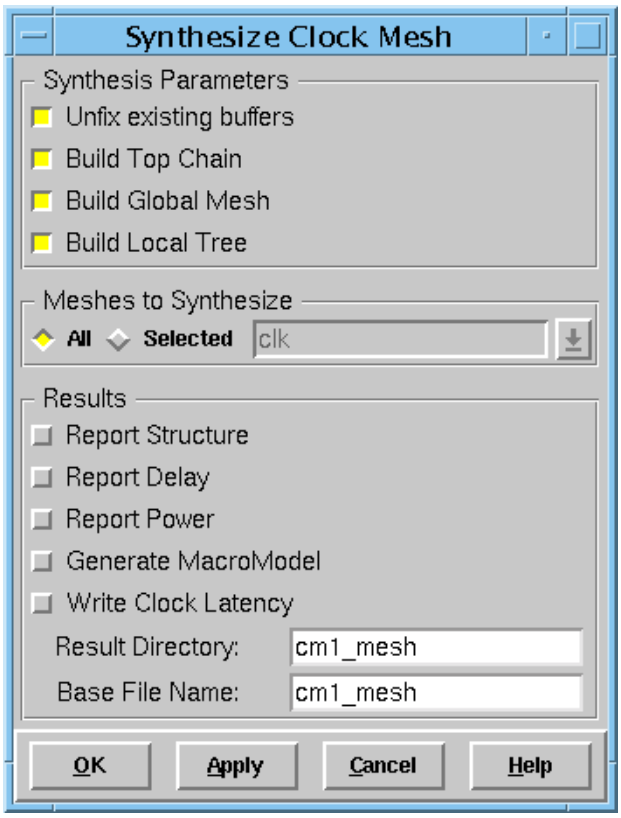
Synthesize Clock Mesh

Use the Synthesize Clock Mesh form to synthesize and generate reports for one or more clock meshes.

Important

When you click *OK* or *Apply* on this form, the software synthesizes the selected meshes. The *Synthesis Parameters* and *Meshes to Synthesize* sections of this form also control the behavior of *Synth* button on the Edit Clock Mesh Specification form.

➤ Choose *Clock – Clock Mesh – Synthesize*.



Fields and Options

Unfix existing buffers

Unfixes any fixed drivers before synthesizing the clock mesh(es).

If your design contains clock meshes that have fixed buffers and if you do not select this option, the synthesis process will fail.

Default: On

Build Top Chain

Synthesizes the top-level chain, if one is defined and enabled in the clock mesh specification file.

Default: On

Build Local Tree

Synthesizes the local trees, if they are defined and enabled in the clock mesh specification file.

Default: On

Meshes to Synthesize

Instructs the clock mesh software to synthesize the specified clock mesh(es).

Default: All

All	Synthesizes all meshes.
Selected	Synthesizes only the selected mesh.

Report Structure

Creates a level-based report of the logical clock mesh structure that includes the following information:

- Clock root pin
- Level number
- Fanout information (including number of leaf pins and gated cells)

Default: Off

Report Delay

Reports the following delay information:

- A summary table showing the delay, skew, and transition time
- A breakdown of the delay, skew, and transition data for each mesh level.

Default: Off

Report Power	Reports total and per-level power information. *Default:* Off
Generate MacroModel	Generates a file containing clock tree specification file `MacroModel` statements that can be used with clock tree synthesis (CTS). *Default:* Off
Write Clock Latency	Generates a file containing `set_clock_latency` and `set_clock_transition` statements. *Default:* Off
Result Directory	Specifies the directory in which the reports should be written.
Base File Name	Specifies the base name that the clock mesh software uses when preparing reports.

Related Text Commands

- `reportClockMesh`
- `synthesizeClockMesh`

Delete Clock Mesh

Use the Delete Clock Mesh form to remove the logical and physical implementations of one or more clock meshes.

➤ Choose *Clock – Clock Mesh – Delete Mesh Implementation*.

Fields and Options

All	Removes the logical and physical implementations for all clock meshes. *Default*: On
Selected	Removes the logical and physical implementations for the selected clock meshes. *Default:* Off

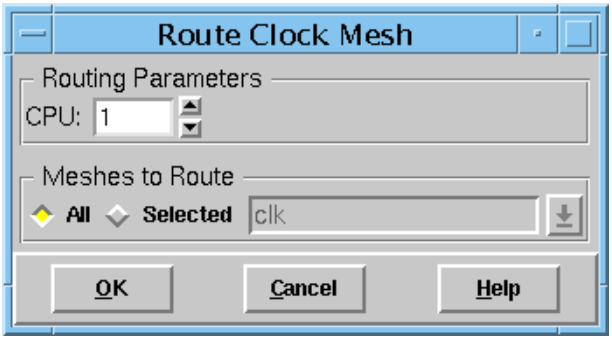
Related Text Commands

■ `deleteClockMesh`

Route Clock Mesh

Use the Route Clock Mesh form to complete the detailed routing for one or more clock meshes.

➤ To open the Route Clock Mesh form, choose *Clock – Clock Mesh – Route Mesh*.



Fields and Options

CPU	Temporarily overrides the NanoRoute router's `setNanoRouteMode -envNumberProcessor` parameter, which specifies the number of processors to use (on one workstation) for multi-threading.	
Meshes to Route	Specifies which clock meshes to route.	
	Default: All	
	All	Routes all clock meshes.
	Selected	Routes only the selected clock meshes.

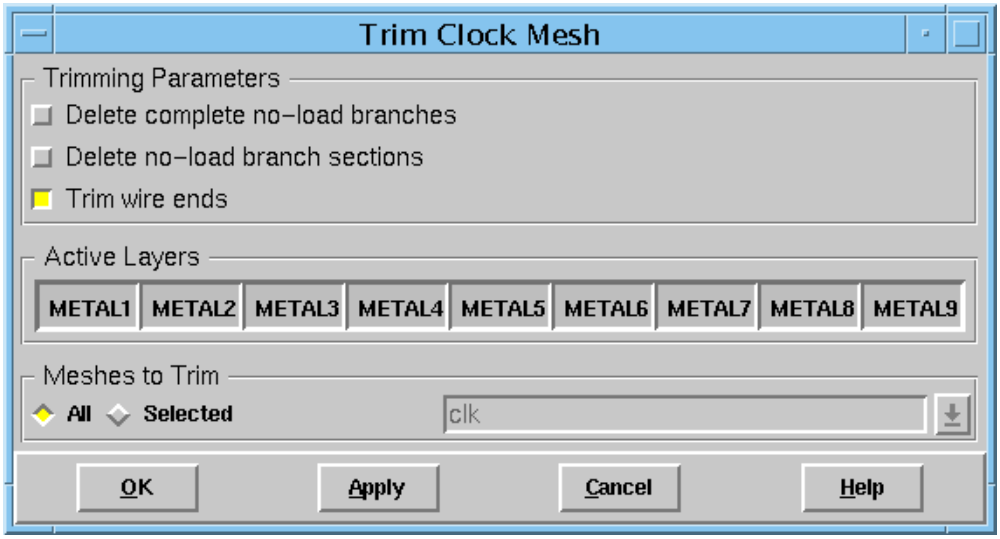
Related Text Commands

- `routeClockMesh`

Trim Clock Mesh

Use the Trim Clock Mesh form to remove unused metal from the clock mesh.

➤ Choose *Clock – Clock Mesh – Trim Mesh Routes*.



Fields and Options

Delete complete no-load branches

Removes (entire) branches if the (entire) branch does not connect to any loads.

Default: Off

Delete no-load branch sections

Removes portions of branches (sections between trunks) that do not connect to any loads.

Default: Off

Trim wire ends

Trims back trunks and branches from their endpoints to the first routing connection or via point.

Default: On

Active Layers	Limits clock mesh trimming to specific layers. Use LEF layer names with this parameter. *Default*: If you do not modify any layer settings, all layers are considered for clock mesh trimming.	
Meshes to Trim	Specifies which clock meshes to trim. *Default: All*	
	All	Trims all clock meshes.
	Selected	Trims only the selected clock meshes.

Related Text Commands

- `trimClockMesh`

Analyze

Use the *Clock – Clock Mesh – Analyze* command to refresh delay and transition times for currently loaded clock meshes.

➤ Choose *Clock – Display – Analyze*.

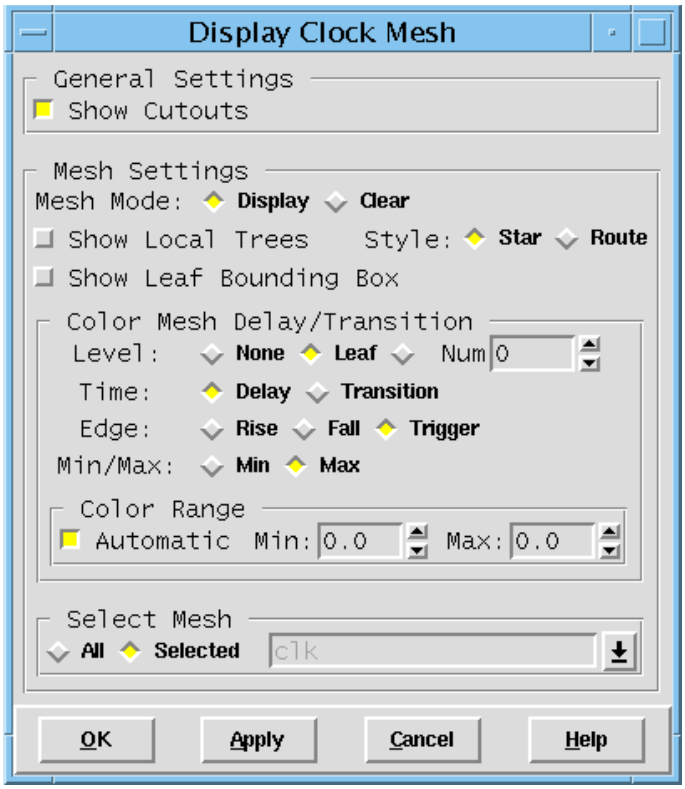
Related Text Commands

■ `analyzeClockMesh`

Report Clock Mesh

Use the Report Clock Mesh form to generate various clock mesh reports.

➤ Choose *Clock – Clock Mesh – Report*.



Fields and Options

Force Mesh Analysis

Forces the clock mesh software to reanalyze mesh timing data before preparing reports, even if the software believes that cached timing information is up to date.

This option is useful on rare occasions when the caching mechanism does not notice that timing data are invalid (for example, due to changes made by other non-clock-mesh commands).

Default: Off

Report Structure

Reports the logical clock mesh structure.

Default: Off

Report Route Connectivity

Specifies that net routing connectivity information be included in the report file or displayed in the Encounter console.

Default: Off

Report Delay

Reports the following delay information:

- A summary table showing the delay, skew, and transition time
- A breakdown of the delay, skew, and transition data for each mesh level

Default: Off

Report Power

Reports total and per-level power information.

Default: Off

Generate MacroModel

Generates a file containing clock tree specification file `MacroModel` statements that can be used with clock tree synthesis (CTS).

Default: Off

Write Clock Latency

Generates a file containing `set_clock_latency` and `set_clock_transition` statements.

Default: Off

Result Directory

Specifies the directory in which to save the reports.

Base File Name

Specifies the base name that the clock mesh software uses when preparing reports.

Meshes to Report

Specifies for which clock meshes to generate reports.

Default: All

All	Generates reports for all clock meshes.
Selected	Generates reports for the selected clock meshes.

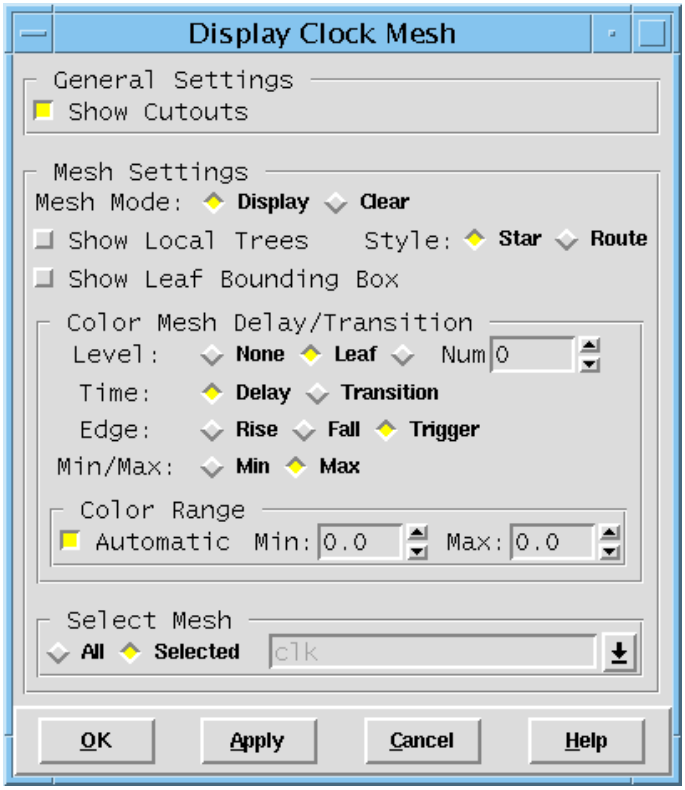
Related Text Commands

- `analyzeClockMesh`
- `reportClockMesh`

Display Clock Mesh

Use the Display Clock Mesh form to control which clock mesh data are shown in the Encounter display.

➤ Choose *Clock – Clock Mesh – Display*.



Fields and Options

Show Cutouts	Displays cutouts.	
	Default: On	
Mesh Mode	Contols the display of selected meshes.	
	Default: Display	
	Display	Displays the selected meshes.
	Clear	Clears the selected meshes from the display.

Show Local Trees

Highlights local tree clusters.

Default: Off

Style — Specifies whether to display the local tree connection flight lines (*Star*), or the route guide topology (*Route*). This feature can be useful for debugging routing guides, as well as timing.

Default: Star

Show Leaf Bounding Box

Displays the bounding boxes of clock mesh leaves.

Default: Off

Level

Specifies the display of clock mesh delay or transition times by color.

Default: *Leaf*

None — Does not display delay and transition times.

Leaf — Displays timing at the clock mesh leaf level.

Num — Displays delay or transition times by level number.

Time

Specifies by which value to display timing data by color:

Default: *Delay*

Delay — Uses delay values when displaying timing data by color.

Transition — Uses transition time values when displaying timing data by color.

Edge

Specifies by which edge to base coloring the display.

Default: *Trigger*

Rise — Colors the display based on rise delay.

Fall — Colors the display based on fall delay.

Trigger — Colors the display based on trigger delay.

Color Range

Specifies the time range display.

	Automatic	Automatically selects the time range for coloring delays or transition times to match the current range of timing values.
	Min/Max	Specifies minimum and maximum settings of the time range.
Select Mesh	Specifies which clock meshes to display.	
	Default: *All*	
	All	Displays all clock meshes.
	Selected	Displays the selected clock meshes.

Related Text Commands

- `displayClockMesh`

Mode

Use the *Clock – Clock Mesh – Mode* command to open the *Clock Mesh* page of the Mode setup form. You can use the *Clock Mesh* page to to set various global clock mesh parameters that are used for clock mesh synthesis, analysis, and optimization.

11

Route Menu

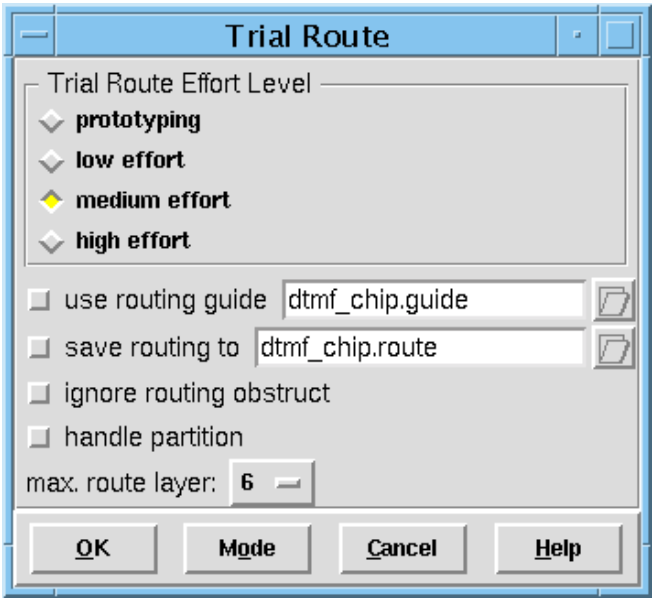
- Trial Route on page 1168
- Special Route on page 1171
- NanoRoute on page 1209
- Mixed Signal on page 1229
- Metal Fill on page 1234
- Via Fill on page 1249
- Flip Chip on page 1253
- Virtuoso CAR Interface on page 1268
- WRoute on page 1273
- Generate Routing Guide on page 1306

Trial Route

Use the Trial Route form to perform quick global and detailed routing for estimating routing-related congestion and capacitance values. Trial Route results are also used for pin assignment when you commit partitions in hierarchical designs.

Note: Trial Route does not guarantee DRC-clean routing results. Do not perform signal integrity analysis on a design that has been routed using Trial Route, because these routes are only used to estimate parasitic values for timing analysis. Route designs with the NanoRoute® router or the WRoute router, if you want to perform signal integrity analysis.

➤ Choose *Route – Trial Route*.



Trial Route Fields and Options

Trial Route Effort Level

Prototyping Runs quickly to gauge the feasibility of your netlist, but components in your design might not be routed at legal locations.

The corresponding text command parameter is `-floorplan`.

Low Effort Completes a quick routing through all congested areas. Use this option only when routing a poorly designed netlist in which a part of the design is good and needs to be analyzed.

The corresponding text command parameter is `-noDetour`.

If you use this option, the routing of the design is not be accurate because some nets might be routed through congested areas or over blockages in order to complete the routing.

Medium Effort Runs the default effort level of Trial Route. This level is used for most routing, including the final version of placement that is the input for detailed routing in a third-party tool.

High Effort Runs additional iterations for resolving difficult routing congestions.

The corresponding text command parameter is `-highEffort`.

Use Routing Guide Specifies a routing guide file to use. Routing guides help control the routing topology by dividing the design into routing regions in which Trial Route then creates wires.

The corresponding text command parameter is `-guide`.

Save Routing to Specifies a file in which to save the routing data after performing Trial Route.

The corresponding text command is `saveRoute`.

Ignore Routing Obstruct

Routes over all partitions and blocks.

The corresponding text command parameter is `-ignoreObstruct`.

Handle Partition

Routes intra-partition and global signals using the specifications of the partitions, such as area and the number of layers. Select this option to gauge the congestion at the full chip level for the chip to be partitioned.

The corresponding text command parameter is `-handlePartition`.

Note: You can use this option in flat partitioned designs to simulate channel-based routing. Do not use this option for channelless designs. For more information, see "Routing a Partitioned Design" in the *Encounter User Guide*.

Max. Route Layer

Limits routing to layers at and below the specified layer. All metal layers above the specified metal number are not routed.

Default: Top-most layer

The corresponding text command parameter is `-maxRouteLayer`.

Related Text Commands

- `trialRoute`
- `setTrialRouteMode`
- `saveRoute`

For more information, see "Route Commands" in the *Encounter Text Command Reference*.

Related Topics

For information on the following topics, see the *Encounter User Guide*:

- "Loading and Saving Route Data"
- "Analyzing Route Data"
- "Improving Route Congestion"

Special Route

The SRoute form enables you to route pins to nearby rings and stripes.

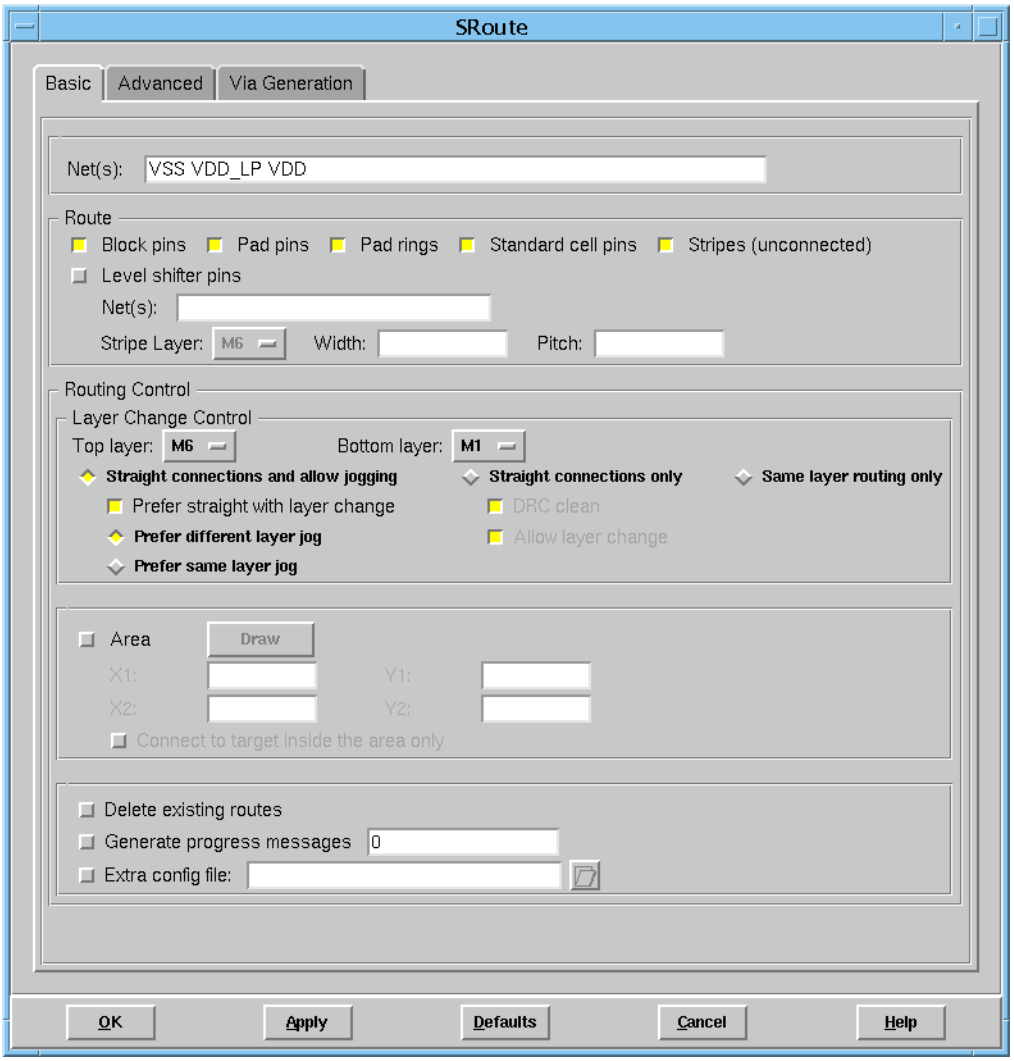
The SRoute form contains the following three pages:

- *SRoute – Basic* on page 1172
- *SRoute – Advanced* on page 1179
- *SRoute – Via Generation* on page 1203

SRoute – Basic

Use the *Basic* page of the SRoute form to limit connections to specific nets or routes.

➤ To open the Basic page of the SRoute form, choose *Route – SRoute*, then click the *Basic* tab.



SRoute – Basic Fields and Options

Nets	The nets that must be connected in the core rows, or on the blocks, pads, or stripes. Both ground and power are specified by default.

Top Layer — The top-most metal layers that the tool can use when routing power structures. Power structures on higher layers are not connected.

Bottom Layer — The top-most metal layers that the tool can use when routing power structures. Power structures on lower layers are not connected.

Route — The types of routing that the Sroute tool can perform. Sroute performs all routing types by default. Select or deselect any of the following options:

- *Block pins* — Connects the power and ground pins of the blocks to rings and stripes.
- *Pad pins* — Connects the power and ground pins of the power pads into the core power ring.

  Note: The physical port must be identified with the `CLASS CORE` statement in the LEF file so that SRoute can recognize the proper pad pins to be routed to the core.
- *Pad rings* — Creates pad rings. If you do not specify any layers, a pad ring is created on each layer that contains pad pins.
- *Standard cell pins* — Connects the power and ground pins of the standard cells along the core rows. The end connections are based on the options you set using the *Advanced* tab of this form. By default, the end connections are at the first ring or stripe outside the row.
- *Stripes (unconnected)* — Extends unconnected stripes to allow a connection to a target.

Level shifter pins — Connects voltage level shifter pins on the specified nets to the closest segment of the ring around the power domain. You must specify one or more nets in the *Net(s)* field directly below this option.

Select the following choices:

- *Stripe Layer* — Defines the stripe layer on which level-shifter pins should be connected.

  Default: If you turn this option off, the software uses the preferred layer.

Width

Specifies the width (in user units) of stripes that connect to level-shifter pins.

Default: If you turn this option off, the software uses the rail width.

Pitch

Specifies the pitch (in user units) of stripes that connect to level-shifter pins.

Default: Twice the level-shifter width plus the width value specified in *Pitch*.

Note: This option is available only if a power domain is defined. By default, this option is deselected.

Straight Connections and Allow Jogging

The Routing Control option that allows jogs during routing to avoid DRC violations. This is the default Routing Control option.

Prefer Straight with Layer Change

If selected, the route is straight, and the tool changes layers when encountering a routing obstruction. This is the default. If deselected, the tool has more flexibility in making connections by both jogging and changing layers.

Prefer Different Layer Jog

If the route must jog to avoid a DRC violation, the jog occurs on the layer that is in the preferred routing direction whenever possible. This is the default.

Prefer Same Layer Jog

If the route must jog to avoid a DRC violation, the jog occurs on the same layer whenever possible. This can result in routing in the non-preferred direction.

Straight Connections only

The Routing Control option that allows only straight connections between targets and that prevents jogs during routing.

DRC Clean
If selected, leaves a route open if a straight connection cannot reach a target without causing a DRC violation. This is the default. If deselected, the tool makes a straight connection to a target, even if the route creates a DRC violations.

Allow Layer Change
If selected, permits the route to change to another layer to avoid DRC violations. This is the default. If deselected, the tool makes only straight connections on the same layer.

Same layer routing only
The Routing Control option that permits only targets on the same layer to be connected.

Area
If selected, you can either enter coordinates in the *X1*, *X2*, *Y1*, and *Y2* fields, or click the *Draw* button to interactively select an area in the design display window. Metal fill is created only in the specified area. If deselected, the tool performs routing for the entire design area. This is the default.

Note: Selecting the *Area* option always preserves existing connections. If you select this option, the *Delete Existing Routes* option is disabled.

Connect to Target Inside the Area Only
If selected, connections from all sources within the specified area can connect only to targets that are also inside that area. If deselected, the tool makes connections from all sources within the specified area to targets both inside and outside the specified area.

Delete Existing Routes
If selected, removes existing connections when you click *Apply* or *OK*. If deselected, existing connections are left untouched each time you use the SRoute form.

Note: This option is disabled if you select the *Area* option.

Generate progress messages
If selected, allows you to see all messages displayed while power routing takes place. Specify an integer value in the associated text entry field to set the interval at which progress messages are generated. If you specify `1`, SRoute generates every progress message; if you specify `2`, SRoute generates every other progress message, and so on. If deselected or if you specify a value of `0`, routing messages do not display in the Encounter console. This is the default.

Extra Config File

(Optional) The name of an extra configuration file that contains additional commands to provide more control over the placement of metal fill in the design.

Caution

You should only use the extra configuration file if you are familiar with its use.

The following variables can be used in the extra configuration file:

- `srouteAllowObsInsideRingPin {true | false}`

  The default is `false`.

- `srouteAllowOverlapWire {true | false}`

  The default is `true`.

- `srouteAllowStripeStopAtFollowpin {true | false}`

  The default is `false`.

- `srouteAvoidOverCoreRowLayer` *`numberOfLayersToAvoid`*

  The default is `2`.

- `srouteBlockPinWidth` *`width`*

  The default is `0`.

- `srouteBlockToStripe {true | false}`

  The default is `true`.

- `srouteCorePinMergeExtent` *`width`*

  The default is `0`.

- `srouteCoreTargetWidth` *`width`*

  The default is `0`.

- `srouteCornerPinThreshold` *`aspectRatio`*

  The default is `0`.

- `srouteCornerPinThreshold` *`aspectRatio`*

  The default is `0`.

- `srouteExtendToDieBoundary` `{true | false}`

  The default is `false`.

- `srouteForbidStackVia` `{true | false}`

  The default is `false`.

- `srouteLayerWrongWayCost.`*`layerNumber costvalue`*

  `costvalue` is an integer in the range of `1` to `32`.

- srouteLayerNormalCost`.`*`layerNumber costvalue`*

  `costvalue` is an integer in the range of `1` to `32`.

- `srouteManufacturingGrid` *`gridSize`*

  The default is `1x1`.

- `srouteMaxViaArraySize` *`percent`*

  The default is `100`.

- `srouteMergeVia` `{true | false}`

  The default is `false`.

- `srouteReduceLayerChanges` *`integer`*

  The default is `0`.

- `srouteRingPinToRingPin` `{true | false}`

  The default is `false`.

- `srouteRoutePowerBarPort` `{true | false}`

  The default is `true`.

- `srouteRouteToLastPadRing` `{true | false}`

  The default is `false`.

- `srouteRouteToLastTarget` `{true | false}`

  The default is `false`.

- `srouteRouteToPadRing {true | false}`

  The default is `false`.

- `srouteStraightConnections [straight routing style (layer change, DRC clean)]`

- `srouteTimeLimit` *`seconds`*

  The default is `100`.

- `srouteTrivialRouteOnly {true | false}`

  The default is `false`.

- `srouteViaOnFeedthru {true | false}`

  The default is `false`

Related Text Commands

For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced

Use the *Advanced* page on the SRoute form to set additional options for creating pad rings and routing block pins, pad pins, and standard cell pins.

➤ To open the Advanced page of the SRoute form, choose *Route – SRoute*, then click the *Advanced* tab.

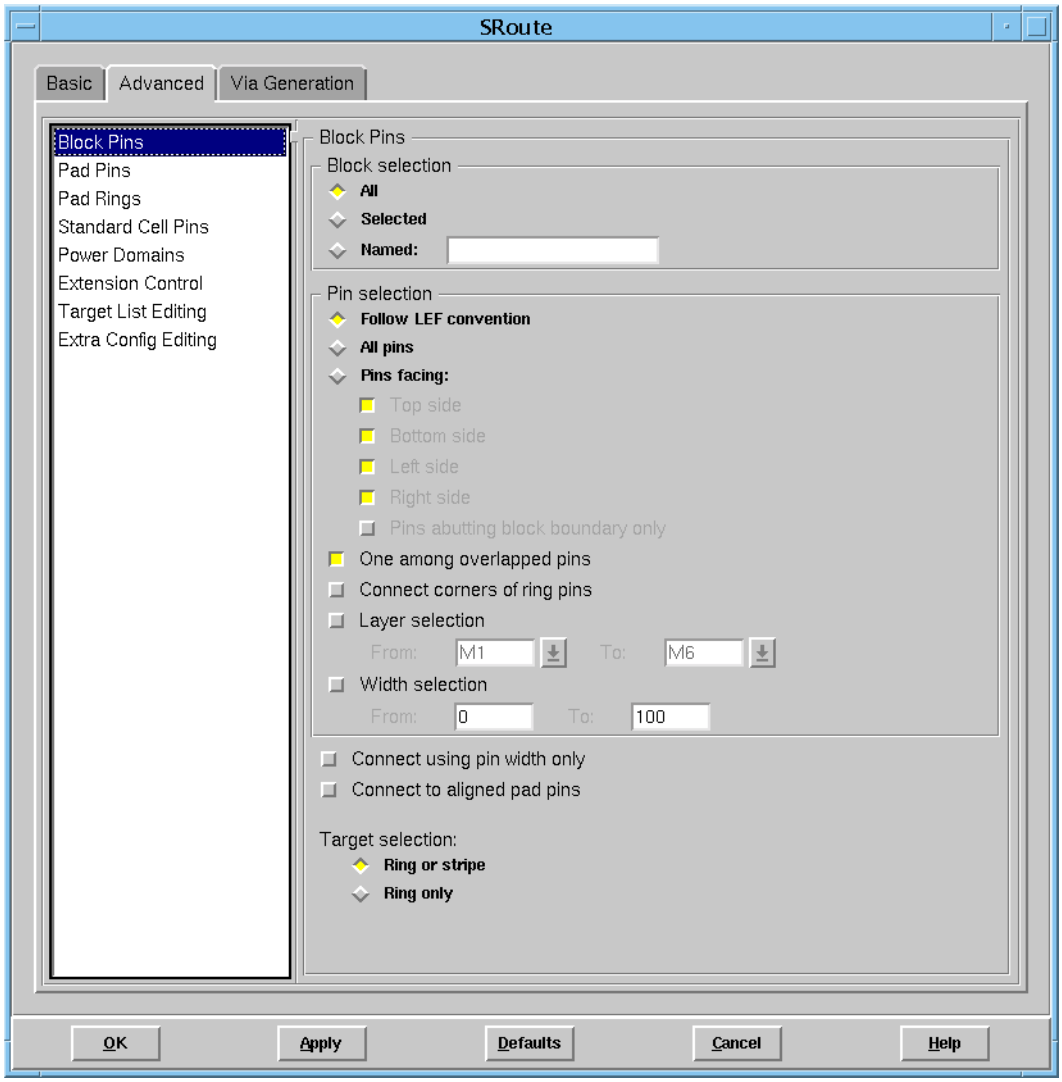
The *Advanced* page on the SRoute form contains the following seven pages:

- SRoute – Advanced – Block Pins *on page 1180*
- SRoute – Advanced – Pad Pins *on page 1184*
- SRoute – Advanced – Pad Rings *on page 1187*
- SRoute – Advanced – Standard Cell Pins *on page 1189*
- SRoute – Advanced – Power Domains *on page 1191*
- SRoute – Advanced – Extension Control *on page 1193*
- *SRoute – Advanced – Target List Editing on page 1197*
- *SRoute – Advanced – Extra Config Editing on page 1201*

SRoute – Advanced – Block Pins

Use the Block Pins page of the SRoute form to specify options for how block pins are to be connected.

➤ To open the Block Pins page of the SRoute forms, choose *Route – SRoute*, click the *Advanced* tab, then choose *Block pins* from the display list.



SRoute – Advanced – Block Pins Fields and Options

Block Selection

The blocks for which pins are to be connected. Select one of the following options:

All

Connects the power and ground pins of all blocks. This is the default.

Selected

Connects only to the blocks that you select interactively. Place the cursor on a block, and then click to select it.

Named

Connects only to blocks that you specify in the text field.

Pin Selection

The block pins that are to be connected. Select one of the following options:

Follow LEF convention

Pins are connected exactly as specified in the LEF file. For example, if the LEF file has multiple ports with one geometry connecting to each port, then one port per pin is connected.

All Pins

All pins on all ports are connected, regardless of how pins are specified in the LEF file.

Pins facing

Only boundary pins are connected. If you select this option, you can also deselect one or more of the following options to prevent the connection of boundary pins at the deselected location:

Top Side

Bottom Side

Left Side

Right Side

Pins abutting block boundary only

One Among Overlapped Pins

If selected, specifies that all pins (including those that overlap) should be routed. If deselected, if multiple pins overlap either fully or partially, only one will be routed.

Note: This parameter is effective *only* if *Pin Selection – All Pins* is selected.

Connect Corners of Ring Pins

If selected, connects the ring pins to the nearby targets by extensions at the corners, creating a total of eight possible connections per net. If deselected, the tool does not extend the ring pins at the corners. This is the default.

Note: This option is useful when internal power connections from the ring pin are modeled as obstructions.

Layer Selection

If selected, limits the layers on which block pins can be routed to the layer numbers you select in the *From* and the *To* drop-down menus. If deselected, the tool routes block pins on all layers. This is the default.

Width Selection

If selected, limits the size of block pins that can be routed to a range that you specify. Specify the minimum pin width in the *From* text entry field and a maximum pin width in the *To* text entry field. If deselected, the tool routes block pins of all widths. This is the default.

Connect using pin width only

If selected, specifies that the block wire used for a connection is to have the same width as the pin from which it connects.

If you do not specify this option, the block wire width is either the width of the target or the width of the pin, whichever is smaller. This is the default.

Connect to aligned pad pins

If selected, specifies that a pad pin can be considered a connection target for a block pin if the pad pin is aligned with the block pin.
Default: If you do not specify this option, pad pins are never considered a target for block pin connection.

Target Selection

The target to which block pins are connected during routing. Select one of the following options:

Ring or Stripe	The tool considers both rings and stripes as targets for block pin connections. This is the default.
Ring only	The tool only considers rings as targets for block pin connections. Block pins are never connected to stripes.

Related Text Commands

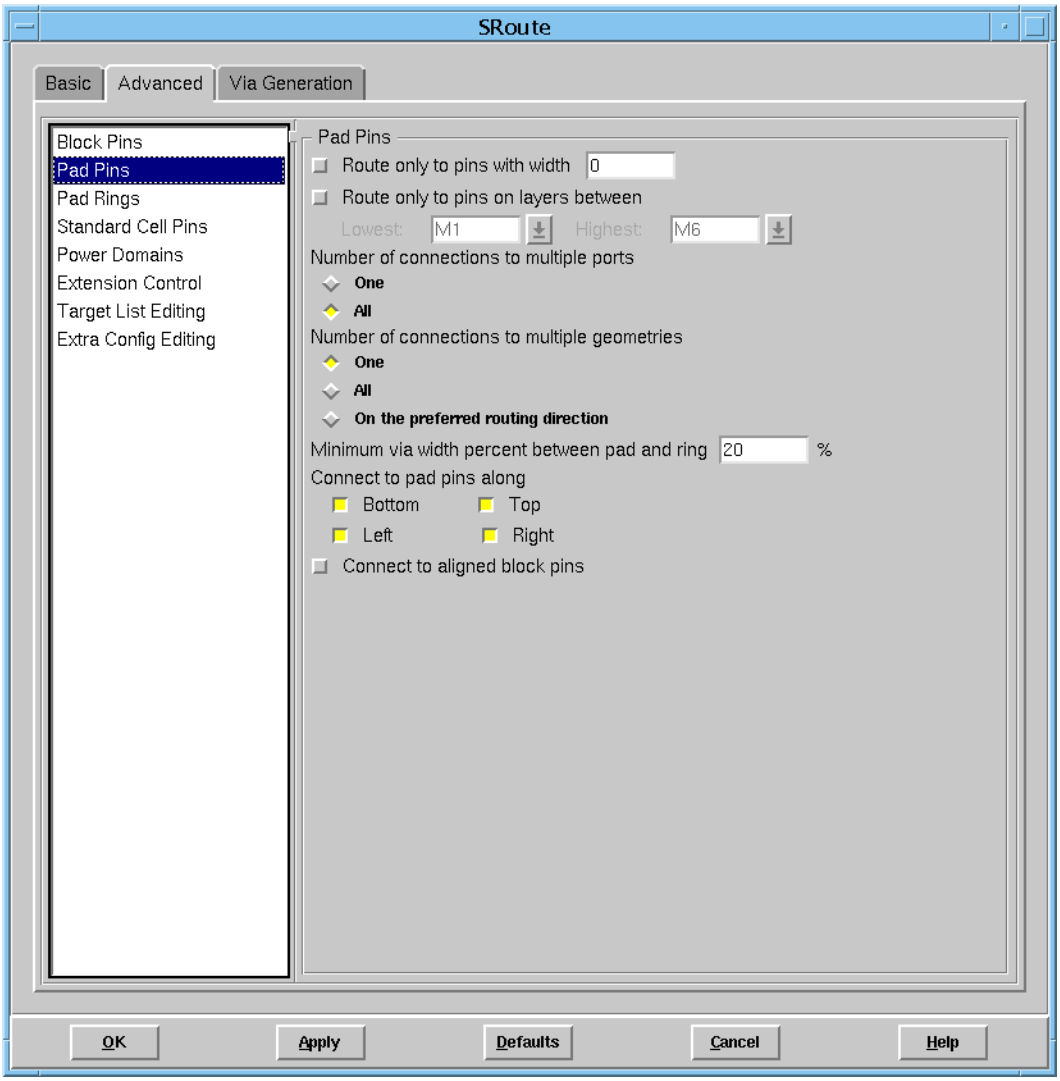
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Pad Pins

Use the Pad Pins page of the SRoute form to specify options for how pad pins are to be connected.

➤ To open the Pad Pins page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Pad Pins* from the display list.



SRoute – Advanced – Pad Pins Fields and Options

Route Only to Pins with Width

If selected, connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.

Route Only to Pins on Layers between

If selected, you can use the drop-down menus to select the lowest and highest layers permitted for a pin connection. If deselected, the tool routes pins to all layers. This is the default.

Number of connections to multiple ports

Controls the connection behavior for pins that have multiple ports defined in the LEF file. Select one of the following options:

One Connects only a single port of a block pin if multiple ports are defined in the LEF file. This is the default.

All Connects all ports defined in the LEF file.

Number of connections to multiple geometries

Controls the connection behavior for pins that have multiple geometries defined in the LEF file for each port. Select one of the following options:

One Connects to only one geometry per port. This is the default.

All Connects to all geometries defined for the port, in both the preferred and nonpreferred routing directions.

On the preferred routing direction

Connects to all geometries defined for the port that are on the preferred routing direction.

Minimum via width percent between pad and ring

(Optional) Controls the size of vias that connect the pad and the ring. Specify this value as a percentage of pad width. The default value is `20`, which prevents the generation of vias that are smaller than 20 percent of the width of the pad.

Connect to Pad Pins Along

Specifies which edges pad pins can connect to. You can prevent connections to pad pins from a particular edge by deselecting it. By default, you can connect pad pins along all edges.

Connect to Aligned Block Pins

If selected, a block pin can be considered a connection target for a pad pin if the block pin is aligned with the pad pin. If deselected, block pins are never considered a target for pad pin connection. This is the default.

Related Text Commands

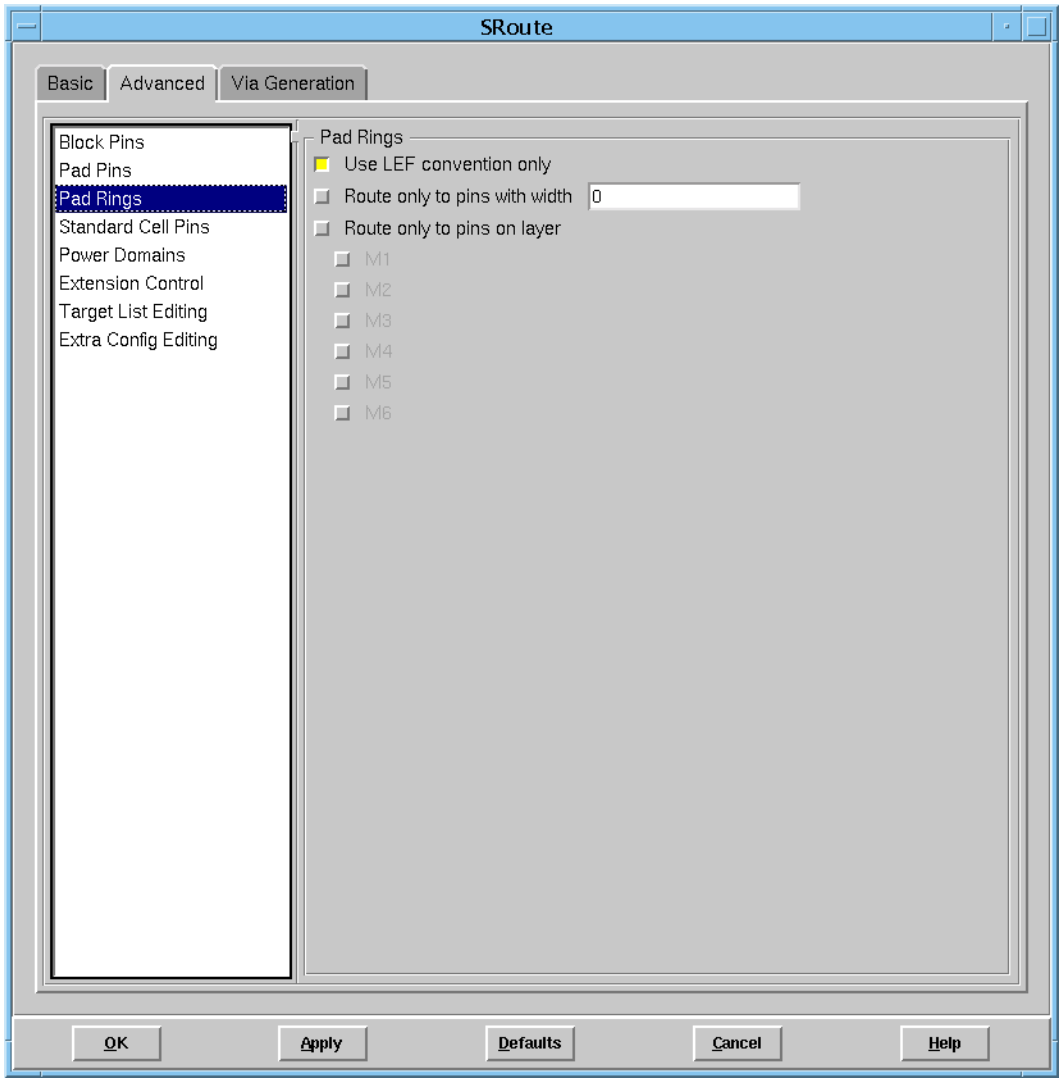
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Pad Rings

Use the Pad Rings page of the SRoute form to set limits on the pins that are connected to the pad ring.

➤ To open the Pad Rings page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Pad Rings* from the display list.



SRoute – Advanced – Pad Rings Fields and Options

Use LEF Convention Only

If selected, pad rings are routed based on what is specified in the LEF file. This is the default. If deselected, the tool chooses the pad pin connection style (`ABUTMENT` or `FEEDTHRU`) when routing pad rings, disregarding what is specified in the LEF file.

Route Only to Pins with Width

If selected, the tool connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.

Route Only to Pins on Layer

If selected, pins are connected only on the layers you select from the list. If deselected, pins on all layers are connected. This is the default.

Related Text Commands

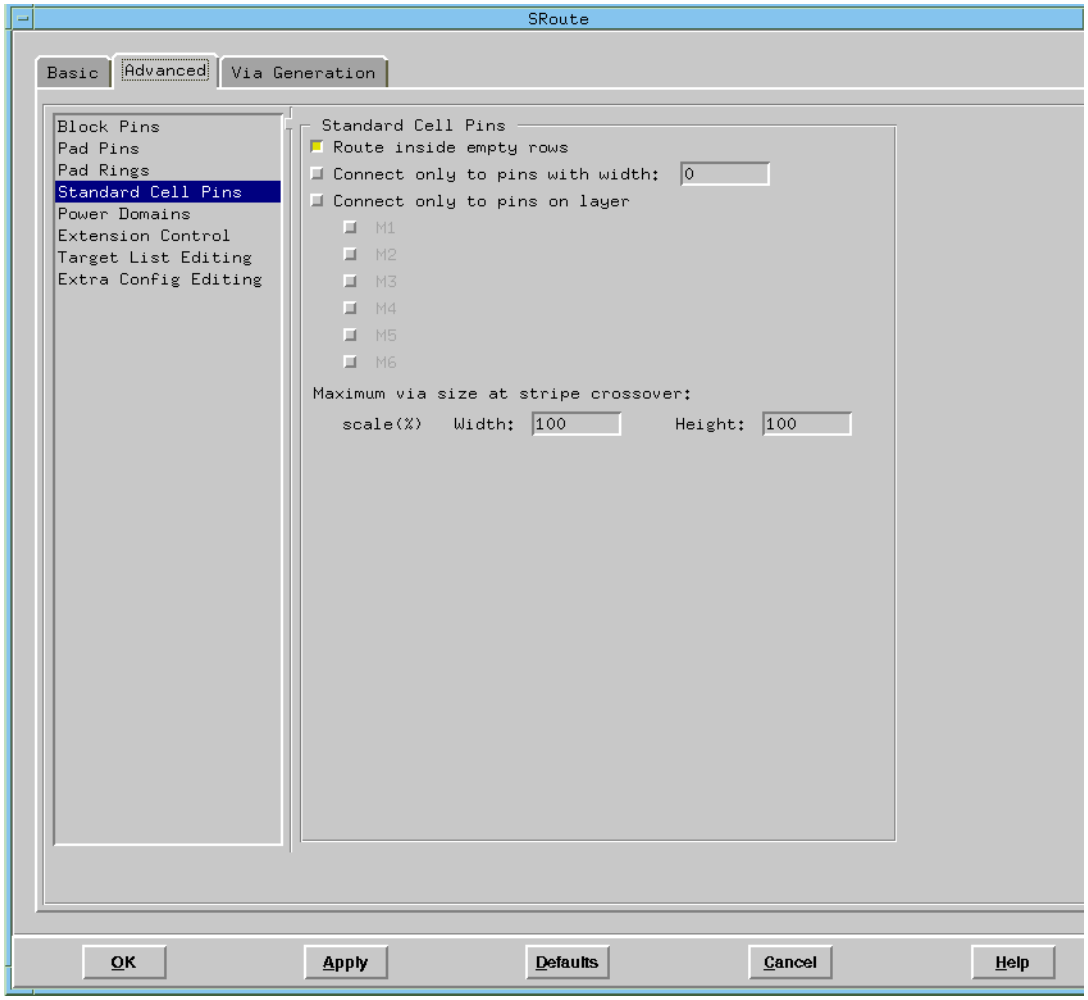
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Standard Cell Pins

Use the Standard Cell Pins page of the SRoute form to specify connectivity options for standard cell pins. (Standard cell pins are also sometimes referred to as *followpins*.)

➤ To open the Standard Cell Pins page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Standard Cell Pins* from the display list.



SRoute – Advanced – Standard Cell Pins Fields and Options

Route inside empty rows

If selected, the tool can create routes over empty rows. This is useful if you want to allow later placement or optimization that puts standard cells into the empty rows. This is the default. If deselected, routes do not go over empty rows, even if that is the shortest way to make a connection.

Connect only to pins with width

If selected, connects only pins with the width you specify in the text entry field. If deselected or if no width is specified, the tool automatically determines the width of the power pins to use. This is the default. It is generally not necessary to specify the width value.

Connect only to pins on layer

If selected, you can select one or more layers on which the tool can connect pins. If deselected, all layers are used. This is the default.

Maximum via size at stripe crossover

(Optional) Specify a *Width* and *Height* value as percentages of the width and height of the via at the top of the stack to limit the maximum size of stacked vias. Smaller vias leave room for more routing tracks on layers between the vias. The default value is `100`.

Related Text Commands

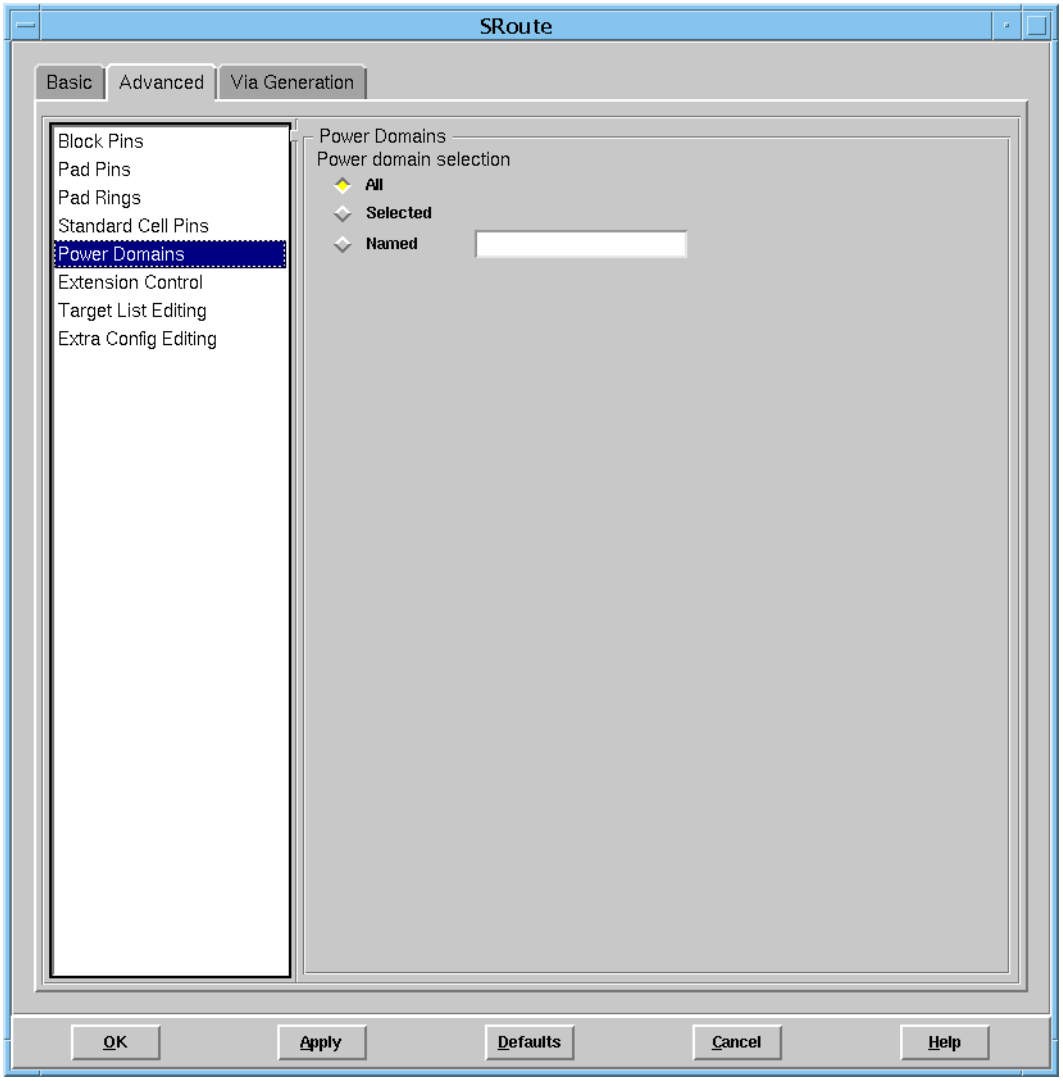
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Power Domains

Use the Power Domains page of the SRoute form to specify options for how power domains are to be connected.

➤ To open the Power Domains page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Power Domains* from the display list.



SRoute – Advanced – Power Domains Fields and Options

Power Domain Selection

Determines which power domains are connected. Select one of the following options:

All	Connects the power and ground pins of all power domains. This is the default.
Selected	Connects only to the power domains that you select interactively. Place the cursor on a block, and then click to select it.
Named	Connects only to power domains that you specify in the text field.

Related Text Commands

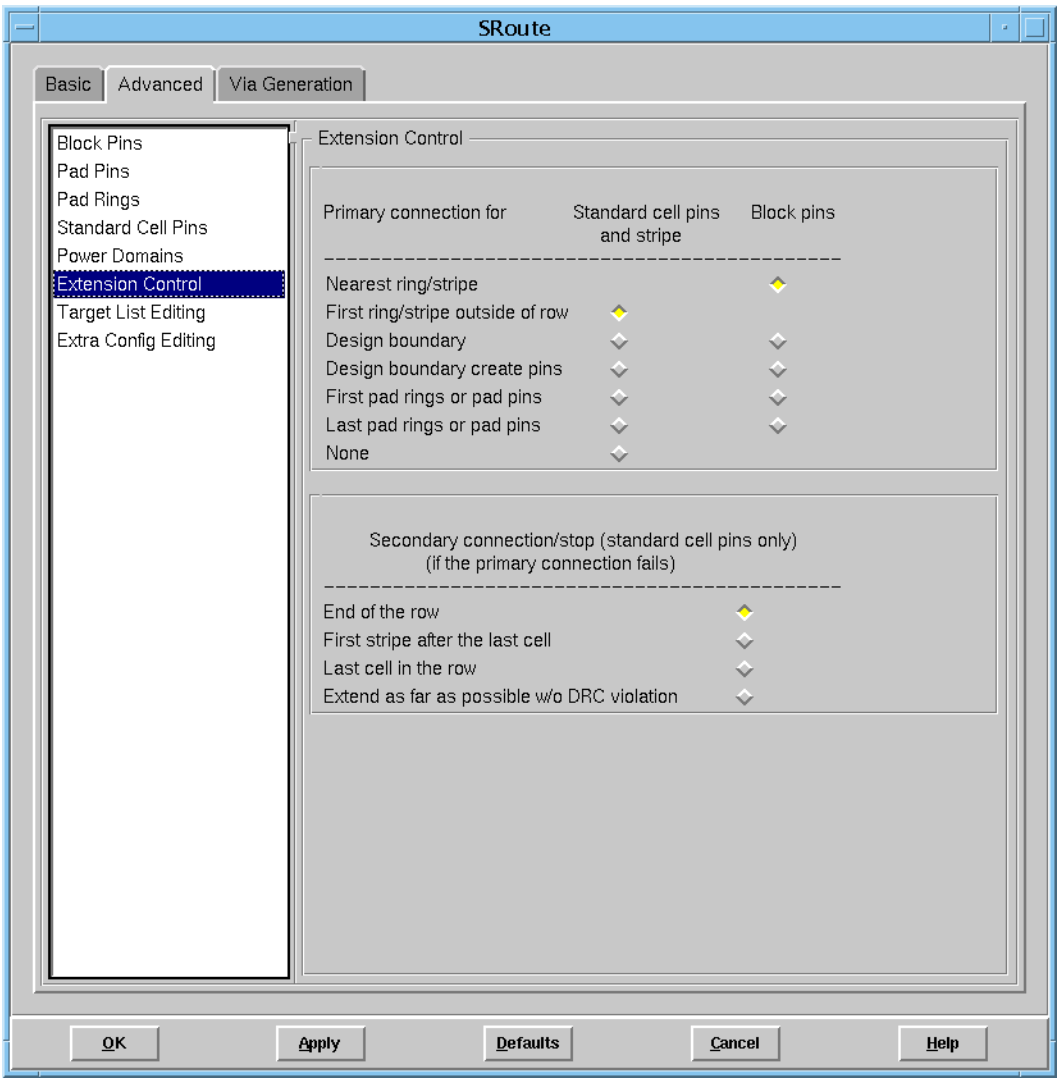
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

`sroute`

SRoute – Advanced – Extension Control

Use the Extension Control page to specify primary extension targets for block pins, standard cell pins, and unconnected stripes, as well as secondary extension targets for standard cell pins.

➤ To open the Extension Control page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Extension control* from the display list.



SRoute – Advanced – Extension Control Fields and Options

Primary connection for: Standard cell pins and stripe

Controls the behavior of the tool when extending standard cell pins and unconnected stripes. Select one of the following options:

First ring/stripe outside of row

Extends the stripe or standard cell pin to the first ring or stripe beyond the end of the row. This is the default.

Design boundary

Extends the stripe or standard cell pin to the design boundary, without creating new power pins. This option is only useful for blocks.

Design boundary and create pins

Extends the stripe or standard cell pin to the design boundary and creates new power pins along the design boundary. Any overlaps with existing I/O pins at the design boundary are flagged as violations after wire extension.

First pad rings or pad pins

Extends the stripe or standard cell pin to the first pad ring that already exists on top of the I/O pad cells.

Last pad rings or pad pins

Extends the stripe or standard cell pin to the last pad ring that already exists on top of the I/O pad cells.

None

Unconnected stripes and standard cell pins are not extended. Standard cell pins are extended to the location specified by the *Secondary Target* option.

Primary connection for: Block pins

Controls the behavior of the tool when extending block pins. Select one of the following options:

Nearest ring/stripe

Extends the block pin to the closest ring or stripe. This is the default.

Design boundary

Extends the block pin to the design boundary, without creating new power pins. This option is only useful for blocks.

Design boundary and create pins

Extends the stripe or standard cell pin to the design boundary and creates new power pins along the design boundary. Any overlaps with existing I/O pins at the design boundary are flagged as violations after wire extension.

First pad rings or pad pins

Extends the stripe or standard cell pin to the first pad ring that already exists on top of the I/O pad cells.

Last pad rings or pad pins

Extends the stripe or standard cell pin to the last pad ring that already exists on top of the I/O pad cells.

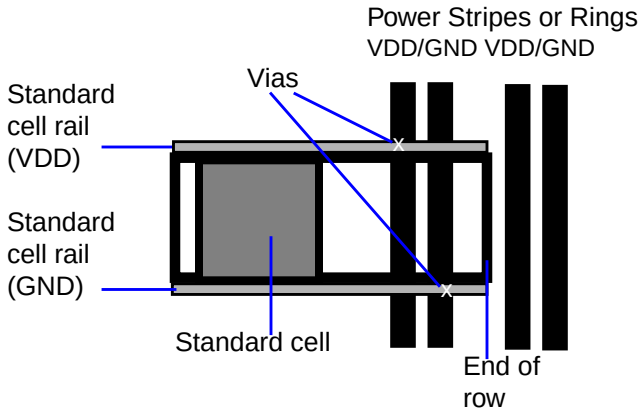
Secondary connection/stop

Specifies a secondary extension target for standard cell pins when the primary extension target is not available or would cause a DRC violation.

Note: Connections are made only if the rails are not obstructed.

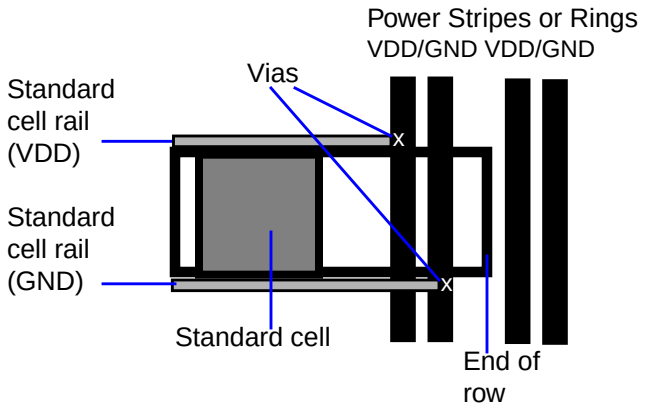
Select one of the following options:

End of the Row Extends the standard cell pin to the end of the core row, as shown in the following figure.



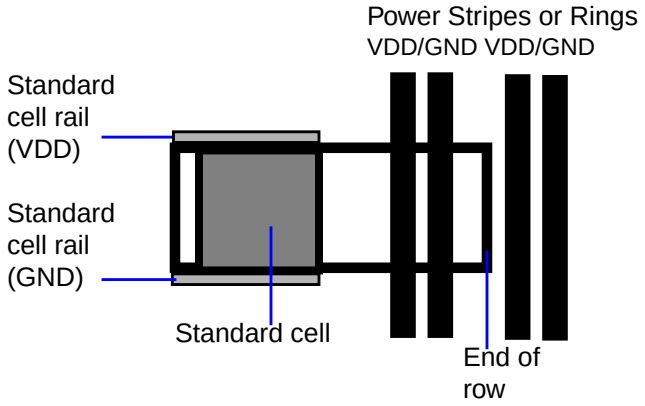
First Stripe after the last cell

Extends the standard cell pin to the first legal target after the last cell in the row, as shown in the following figure.



Last cell in the row

Extends the standard cell pin to the last standard cell in the core row, as shown in the following figure.



Extend as far as possible w/o DRC violation

Extends the standard cell pin as far as possible without creating a DRC violation.

Related Text Commands

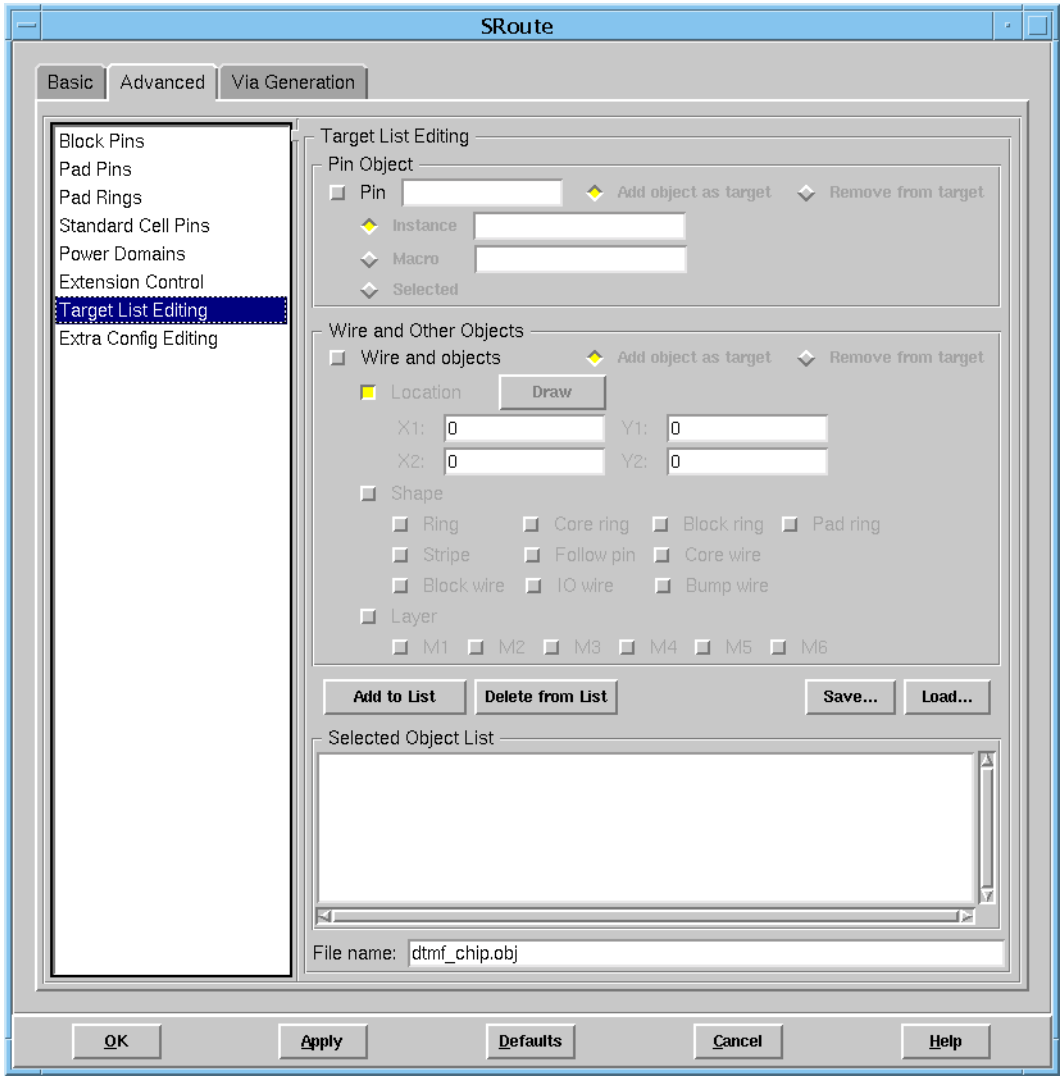
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Target List Editing

Use the Target List Editing page to specify primary extension targets for block pins, standard cell pins, and unconnected stripes, as well as secondary extension targets for standard cell pins.

➤ To open the Target List Editing page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Target List Editing* from the display list.



SRoute – Advanced – Target List Editing Fields and Options

Pin

Specifies that a pin or set of pins is to be added to or removed from the *Selected Object List*. You can specify the name of a specific pin, instance, or macro, or you can interactively select one or more pins from the design display area.

Add object as target

Adds the specified pins to the list of targets that the SRoute tool uses during routing.

Remove from target

Removes the specified pins from the list of targets that the SRoute tool uses during routing.

Instance

The instance name for the pins that are to be added or removed from the *Selected Object List*.

Macro

The name of the macro that contains the pins to be added or removed from the *Selected Object List*.

Selected

Pins that are selected interactively within the design are added or removed from the *Selected Object List*.

Wire and objects

Specifies that an object or set of objects other than pins is to be added to or removed from the *Selected Object List*.

Important

The following information applies to users who modify the existing set of valid target objects on the *Target List Editing page* (SRoute form, *Advanced* tab) and then open the *Via Generation* tab to make further changes to that set of objects: When you open the *Via Generation* tab of the SRoute form to make modifications on that tab, the via generation modifications you make apply *only* to the set of objects that you have modified on the *Target List Editing* page.

Add object as target

Adds the specified objects to the list of targets that the SRoute tool uses during routing.

Remove from target

Removes the specified objects from the list of targets that the SRoute tool uses during routing.

Location

Wires and objects within this boundary are added to or removed from the *Selected Object List*.

Draw

Click this button, then drag the mouse to interactively select a location within the design. This automatically populates the *Location* coordinate fields.

Shape

Limits the wires and objects on the *Selected Object List* to the selected shapes. If you select this option, you must specify one or more of the following shapes:

- Ring
- Stripe
- Block wire
- Core ring
- Follow pin
- IO wire
- Block ring
- Core wire
- Bump wire
- Pad ring

If you do not select this option, wires and objects of all shapes can be added to the list. This is the default.

Layer

Limits the wires and objects on the *Selected Object List* to the selected layers. If you select this option, you must specify one or more of the available layers. If you do not select this option, wires and objects on all layers can be added to the list. This is the default.

Add to List

Click this button to add the selected pins, wires, and objects to the *Selected Object List*.

Delete from List

Select an object from the *Selected Object List*, then click this button to remove that object from the list.

Save	Saves the object on the *Selected Object List* to the location specified in the *File name* field.
Load	Loads the objects in the file to the *Selected Object List*.
Selected Object List	A list that shows which pins, wires, and objects are to be considered as targets or removed from consideration as targets by the sroute software.
File name	The name of a file that contains the list of pins, wires, and objects along with information about whether they are to be considered as targets or removed from consideration as targets when the sroute software runs.

Related Text Commands

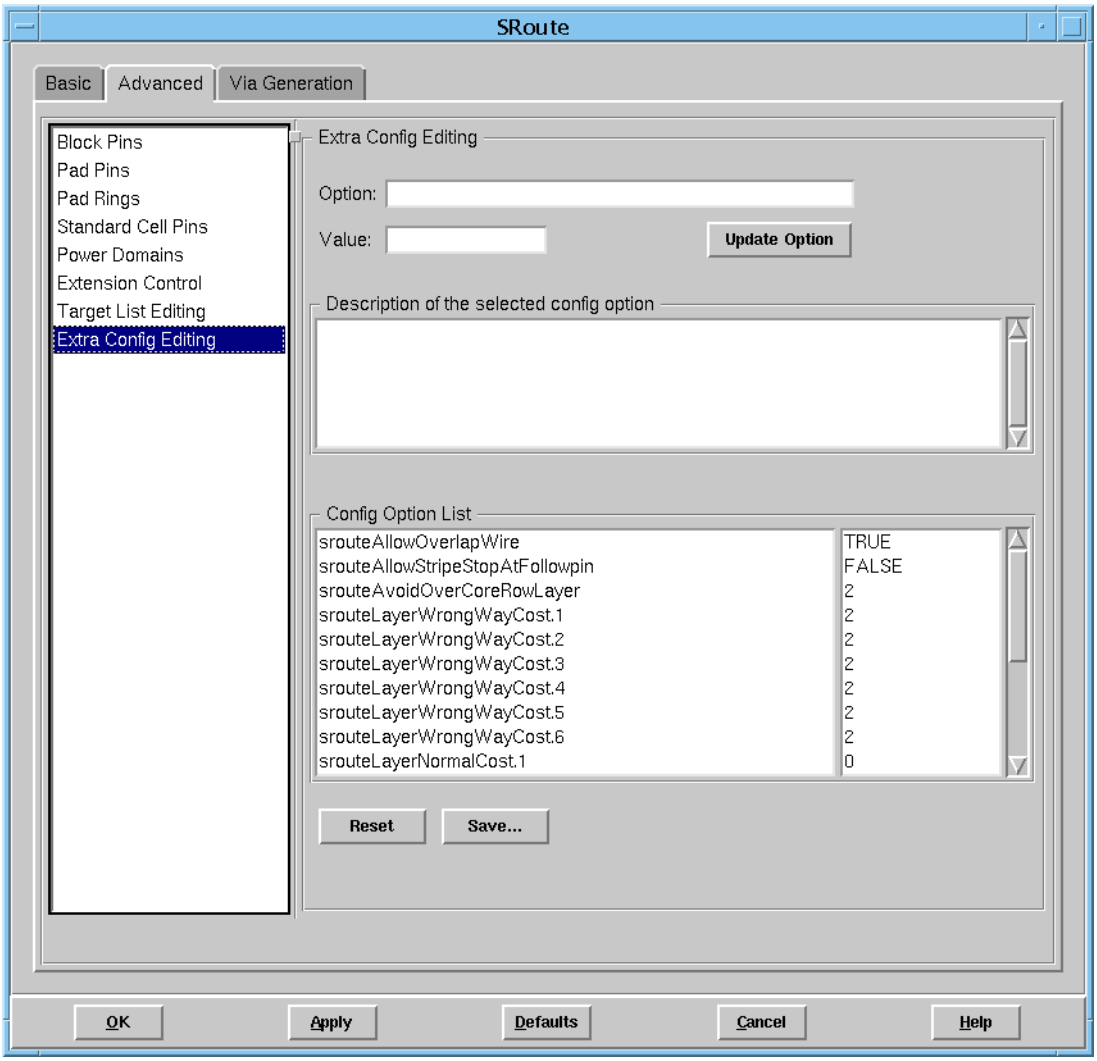
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

SRoute – Advanced – Extra Config Editing

Use the Extra Config Editing page to create a configuration file containing revised SRoute option values.

➤ To open the Extra Config Editing page of the SRoute form, choose *Route – SRoute*, click the *Advanced* tab, then choose *Extra Config Editing* from the display list.



SRoute – Advanced – Extra Config Editing Fields and Options

Option	Displays the configuration file option you select in *Config Option List*. This is a read-only field.

Value	Displays the current value for the selected SRoute option. Use this field to change the current option value.
Update Option	Updates the revised value in *Config Option List*.
Description of the selected config option	
	Displays a description of the selected option value.
Config Option List	Displays a list of the most frequently used SRoute options. Click a line in this area to display the option and its description, and to revise the selected option value.
Reset	Resets the page to the default SRoute values.
Save	Displays a form through which you can save the revised values to a new extra configuration file.
	Default: The default filename is `top_cell_name.xcf`.

SRoute – Via Generation

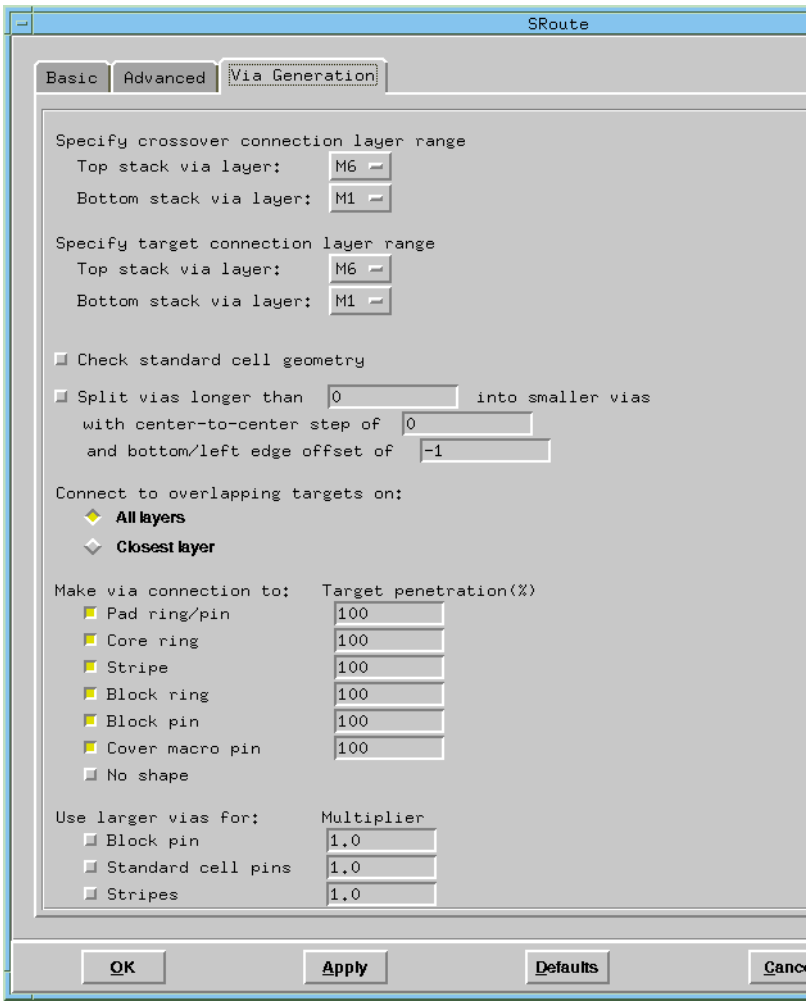
Use the Via Generation page of the SRoute form to limit the connections that vias generated by SRoute are allowed to make.

➤ To open the Via Generation page of the SRoute form, choose *Route – SRoute*, then click the *Via Generation* tab.

Important

The following information applies to users who modify the existing set of valid target objects on the *Target List Editing page* (SRoute form, *Advanced* tab) and then open the *Via Generation* tab to make further changes to that set of objects: When

you open the *Via Generation* tab of the SRoute form to make modifications on that tab, the via generation modifications you make apply *only* to the set of objects that you have modified on the *Target List Editing* page.



SRoute – Via Generation Fields and Options

Specify crossover connection layer range

The range of layers in which vias are created to connect wires that cross over the route. Vias are not created to connect wires outside this range. Select a layer from each of the following pulldown menus:

Top stack via layer

The highest layer in which vias can be stacked. The default is the top-most metal layer.

Bottom stack via layer

The lowest layer in which vias can be stacked. The default is the bottom-most metal layer.

Specify target connection layer range

The range of layers in which vias are created to connect target wires and pins. Vias are not created to connect wires or pins outside this range. Select a layer from each of the following pulldown menus:

Top stack via layer

The highest layer in which vias can be stacked. The default is the top-most metal layer.

Bottom stack via layer

Check standard cell geometry

If selected, checks the standard cell geometries in the design for any spacing violations between the power rail to power stripe vias and cell blockages to repair any DRC violations. When detected, Encounter repairs these violations by trimming the via arrays as needed. This check box is off by default.

Split vias longer than X *into smaller vias with center-to-center step of* Y *and bottom/left edge offset of* Z

Splits vias that are longer than the specified length into smaller vias that have the specified center-to-center step and bottom/left edge offset (all values in micrometers).

Default: Off

Connect to overlapping targets on

Controls the behavior of via generation when rings on multiple layers have the same coordinates. Select one of the following options:

All layers	Allows via generation between rings on all layers. This is the default.
Closest layer	Prevents the generation of vias to rings on different layers.

Make via connections to

Controls the wire shapes for which the software can generate vias. Select or deselect any of the following shapes:

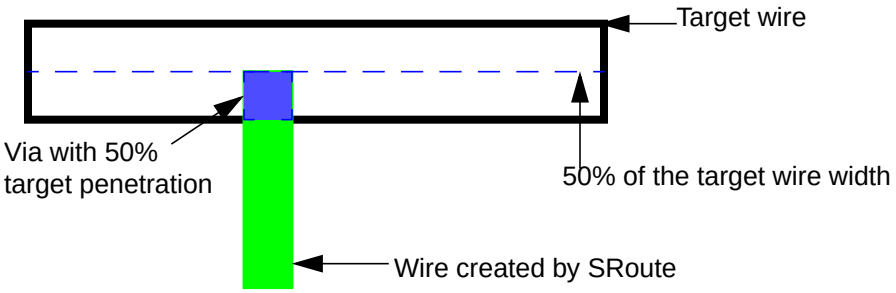
- *Pad ring/pin*
- *Core ring*
- *Stripe*
- *Block ring*
- *Block pin*
- *Cover macro pin*
- *No shape*

By default, vias can be generated on all wire shapes.

Target Penetration (%)

Specifies a smaller size for vias connecting to targets of a particular wire or pin type.

By default, if a wire or pin is a target to which a via can be connected, the via is a full-sized. If you want the via to be smaller, you can specify a value in this field for each wire type. Only a single dimension of the via will be scaled. For example, if you specify a value of 50, the via will be full-sized in one dimension (the width of the wire created by SRoute), but only half the width in the other dimension (the width of the target wire).



Use larger vias for

Increases the size of vias for wires that switch layers, which can help reduce resistance. The default for each of these options is `1.0`, which specifies that the via is a square of the same width as the wire. Select any of the following, then specify a multiplier in the text entry field:

- *Block pin*
- *Standard cell pins*
- *Stripes*

Check standard cell geometry

If selected, checks the standard cell geometries in the design for any spacing violations between the power rail to power stripe vias and cell blockages to repair any DRC violations. When detected, Encounter repairs these violations by trimming the via arrays as needed. This check box is off by default.

Related Text Commands

For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `sroute`

NanoRoute

Use the NanoRoute® forms to specify the following:

- Net attributes
- Most commonly used run-time options
- Routing type (global, detailed, or both)
- Congestion map style and options

The *NanoRoute* submenu contains the following items:

- *Specify Attribute*

  Opens the NanoRoute/Attributes form.

- *Route*

  Opens the NanoRoute form.

- *Congestion Analysis*

  Opens the Set Congestion Map Style form.

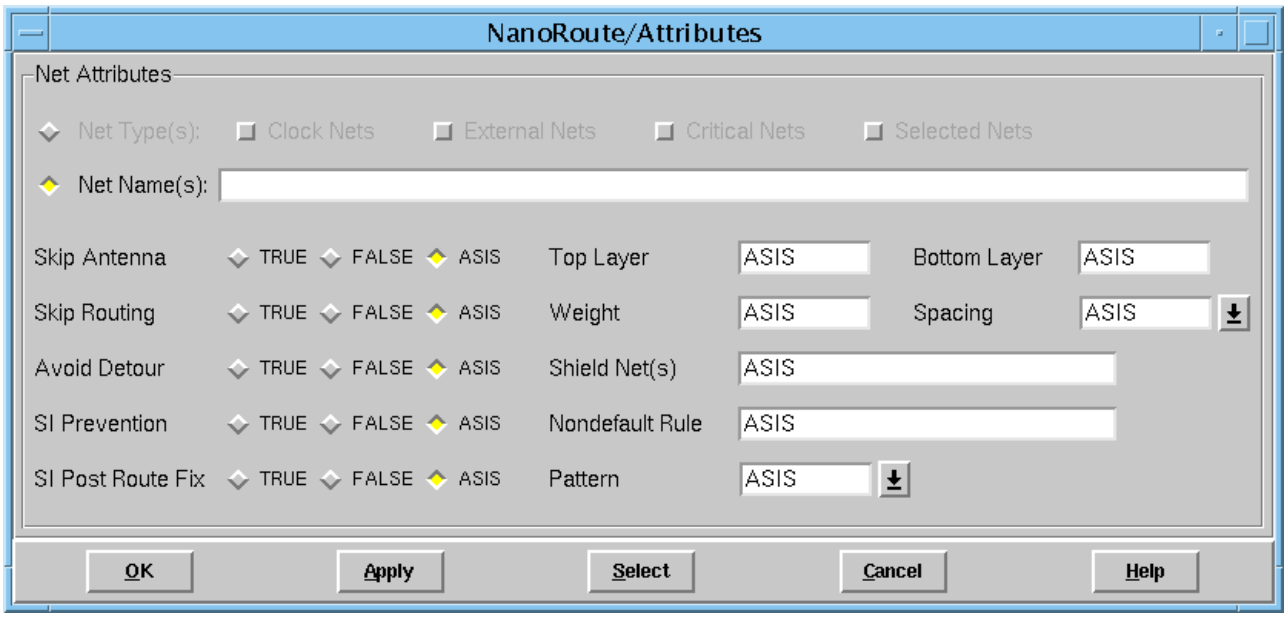
NanoRoute/Attributes

Use the NanoRoute/Attributes form to specify net attributes to use when you route your design with the NanoRoute router. Specifying net attributes is optional.

Attaching the attributes allows the router to route the nets following specific requirements. Attributes are persistent; that is, throughout the routing process, from global routing to optimization, the router honors the attributes. The attributes are saved with the Encounter database. If you save the database and exit, the attributes remain attached to the nets when you reimport the database. Attributes are not saved with the DEF file.

➤ Do one of the following:

- ❑ Choose *Route – NanoRoute/Attributes* on the menu.
- ❑ Choose *Route – NanoRoute* on the menu, and click the *Attributes* button on the NanoRoute form.



NanoRoute/Attributes Fields and Options

Note: When *ASIS* is selected for a net attribute, the router does not change the current value of the attribute in the database. To see the current value of an attribute, use the `getAttribute` text command.

Net Type(s) Specifies the net type(s). Select one or more of the following types:

Clock Nets	Specifies all clock nets.
External Nets	Specifies all nets with external pins.
Critical Nets	Specifies all timing-critical nets. If you select *Critical Nets*, you must have already run timing analysis to determine the nets that are timing critical.
Selected Nets	Sets attributes for selected nets only.

Net Name(s)

Specifies nets. You can only specify one net name. To select more than one net, you can use the asterisk (`*`) and question mark (?) wildcards in this field.

- If you select a *Net Type*, sets attributes for nets of that type only.
- If you click *Select* at the bottom of the form, selects the nets in the design display area of the Encounter® main window.

Skip Antenna

Prevents NanoRoute from repairing process antenna violations on specified nets. This attribute is useful on nets that will have antenna violations repaired at the next level of hierarchy.

Skip Routing

Prevents the NanoRoute router from routing or rerouting unrouted or partially routed nets.

When you specify this option for a net, the router treats the net as if you had marked it `+ FIXED` in the DEF file and it becomes an obstruction for other nets.

If the net is partially routed, the router does not complete the routing.

Important

The value you specify with this attribute also applies to Trial Route and the `trialXRoute` command.

Avoid Detour

Routes critical nets as short as possible. When you set this attribute, NanoRoute does not allow a net to go beyond the minimum bounding box of all of its pins.

Caution

Do not unnecessarily specify TRUE for this attribute because it adds congestion to the design.

SI Prevention

Prevents signal integrity violations by setting attributes for specified nets to avoid detours, add net weight, and add extra spacing.

Note: You can specify the *SI Prevention* attribute for a net, even if you do not run signal integrity-driven routing.

Select *True* to set the following attributes for clock nets:

- *Avoid Detour True*
- *Weight* `10`
- *Extra Spacing* `1`

Select *True* to set the following attributes for nets with external pins:

- *Avoid Detour True*
- *Weight* `5`
- *Extra Spacing* `1`

Select *True* to set the following attributes for timing-critical nets:

- *Avoid Detour True*
- *Weight* `5`
- *Extra Spacing* `1`

SI Post Route Fix

Repairs crosstalk violations after routing. If you are using a third-party tool for noise analysis, use this attribute to specify nets to target during for postroute crosstalk repair, in combination with the *Post Route SI* option on the NanoRoute form.

Top Layer

Specifies the highest layer for routing specified nets. NanoRoute might still use a layer above the specified layer if necessary to complete the routing. Use this attribute to improve timing by restricting the routing layers available for critical nets, while simultaneously routing other nets on all routing layers.
Range: `0-15`

Note: This is a soft limit. To set a hard limit, use *Top Layer* on the NanoRoute form.

Bottom Layer

Specifies the lowest routing layer. This attribute is a soft limit; that is, NanoRoute might use a layer below the specified layer if necessary to complete routing. To set a hard limit, use *Bottom Layer* on the NanoRoute form.
Range: `0-15`

Note: If the top routing layer is equal to or greater than 4 and no bottom preferred routing layer is specified for clock nets, the router automatically sets the bottom preferred routing layer for clock nets to 3, to prevent the clock nets from blocking other nets.

Weight

Specifies a relative weight for routing nets within a switch box. NanoRoute routes nets with the highest weight first, then the next highest weight, and so on.
Default: `2`

Note: A switch box is a collection of global routing cells used during detailed routing. When you specify a net weight and route a net, NanoRoute does not route the entire net according to the weight. It routes the nets in each switch box with the highest weight first, then the next highest weight, and so on.

Spacing

Gives one or more additional pitch spacing to specified nets. NanoRoute bases the spacing on the default spacing rule defined in the LEF file plus the extra pitch defined by this attribute. For example, specify `1` to give a net 1 extra pitch spacing, compared to other nets. This parameter creates a soft rule and, if the design is congested, might not give the extra space to the net. Use this attribute to space specific nets, such as clock nets, farther apart if they are very sensitive to coupling capacitance.
Range: `0-3`

Shield Net(s)

Specifies a special net to use as a shield for a critical or high-speed net. Typically, you route shielded nets before routing other nets. You can specify one or two shield nets, however, you cannot control which side is used by the special net that is routed on the same layer as the signal routing. The shield terminates near the pin. Shielding information is saved in the DEF file.

Nondefault Rule

Identifies the nondefault routing rule to use with the specified net. Use this attribute for critical nets, such as clock nets, that might need to have wider wires or wider spacing than other nets.

The router treats nondefault rule spacing as a soft attribute; that is, when routing resources are available, it honors the nondefault rule. If the area is too congested, and resources are not available, the router might not honor nondefault spacing rules. You can override this behavior by specifying `setNanoRouteMode -strictlyHonorNonDefaultRule true`.

You define nondefault routing rules in the `NONDEFAULTRULE` statement of the LEF file.

Pattern

Specifies the routing pattern. Select one of the following:

ASIS	Retains the current setting.
steiner	Routes all pins with a single steiner tree.
trunk	Routes pins to the nearest special net of the same name. Creates multiple steiner trees and connects them to the trunk.

Select

Selects nets in the design display area of the Encounter main window.

Related Topics

- Using NanoRoute Parameters

Related Text Commands

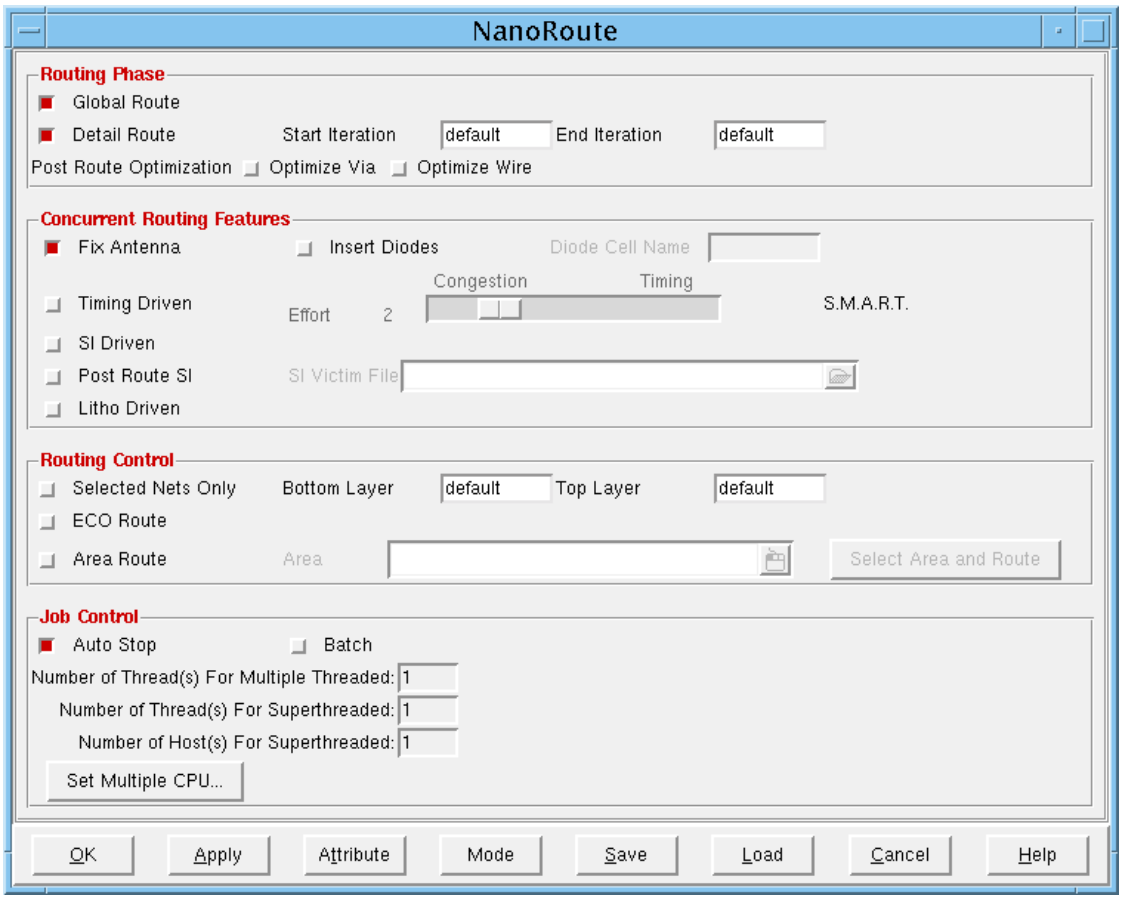
- `getAttribute`
- `setAttribute`

NanoRoute

Use the NanoRoute form to specify the most commonly used NanoRoute run-time options, and to run global and detailed routing. The NanoRoute form also provides access to the following additional forms:

- NanoRoute/Attributes on page 1210
- Mode Setup – NanoRoute on page 316
- Multiple CPU Processing on page 373

➤ Choose *Route – NanoRoute – Route*.



NanoRoute Fields and Options

Global Route

Plans the global interconnect and detailed routing for the design using the NanoRoute router, and produces a congestion map.

During global routing, the router breaks the design into rectangles called global routing cells (gcells). It connects the regular nets defined in the NETS section of the DEF file by assigning them to gcells. The goals of global routing are to distribute and minimize congestion and to minimize the number of gcells that have more nets assigned than routing resources available.

Detail Route

Uses the NanoRoute router to perform detailed routing on the entire design, on an area of the design specified, or on selected nets.

During detailed routing, the router follows the global routing plan and lays down actual wires that connect the pins to their corresponding nets. The primary goal of detailed routing is to complete the interconnect without creating shorts or spacing violations.

Note: If you have not already run detailed routing on the entire design, you cannot run detailed routing on a specified area. For more information, see "Area Route" on page 1220.

Start Iteration

Specifies the first pass in a detailed routing step. Together with *End Iteration*, divides detailed routing into intermediate steps.

End Iteration

Specifies the last pass in a detailed routing step or the beginning of postroute optimization. Together with *Start Iteration*, divides detailed routing into intermediate steps.

Note: Setting *End Iteration* to a value higher than 20 generally does not improve results.

Post Route Optimization

Replaces single-cut vias with multiple-cut vias or fat single-cut vias after postroute optimization.

Optimize Via Optimizes vias after routing.

Caution

Exercise caution with the use of this option, as the router might create violations during postroute via optimization. It runs a search and repair step after optimization if violations occur.

Optimize Wire Optimizes wires after routing.

Concurrent Routing Features

Fix Antenna Repairs process antenna violations during postroute optimization. NanoRoute repairs process antenna violations if it can do so without creating design rule violations. The router might need to make several passes before repairing all antenna violations. By default, this option is selected.

Insert Diodes Inserts and places antenna diode cells during postroute optimization if there are available placement locations for the cells. By default, NanoRoute repairs antenna violations by changing layers (also called antenna stapling or layer hopping), but it can also repair antenna violations by inserting diodes as close as possible to input gates to discharge current. By default, this option is not selected.

Diode Cell Name

Routes antenna diode cells with the specified name during postroute optimization. The antenna diode cells must have the same LEF `SITE` definition as the standard cells. If you select *Insert Diodes* and do not enter a cell name, NanoRoute searches the LEF file and inserts the first `MACRO` with `CLASS CORE ANTENNACELL` it finds with the appropriate `SITE` definition.

Timing Driven Minimizes timing violations by analyzing the timing slack for each path, the drive strengths of each cell in the library, and the maximum capacitance and maximum transition limits. During timing-driven routing, NanoRoute routes multi-pin nets to the most critical sink first, performs wire optimization by reducing resistance and coupling, and continually adjusts detouring. By default, this option is not selected.

Effort

Specifies how aggressively the router works to meet timing constraints. A higher value increases the effort toward meeting timing constraints and decreases the effort toward relieving congestion.
Range: 0 – 10

- If *Batch* is selected, this option defaults to `0`.
- If *Batch* is not selected, this option has a dynamic default setting.

S.M.A.R.T.

Abbreviation for *S*ignal integrity, *M*anufacturing *A*wareness, *R*outability, and *T*iming.

During SMART routing, the router runs both timing-driven and signal integrity-driven routing concurrently. It uses the Encounter software's extraction, delay calculation, and timing engines during detailed routing to make intelligent trade-offs between routability, timing, and crosstalk minimization.

SI Driven

Prevents or reduces crosstalk. Works in conjunction with timing-driven routing. By default, this option is not selected.

- When *Timing Driven* is selected, uses SMART routing to identify victim nets and minimize crosstalk by wire spacing, layer hopping, net ordering, and minimizing the use of long parallel wires.
- When *Timing Driven* is not selected, uses an older signal integrity engine to identify victim nets and minimize crosstalk by preventing or reducing the use of long parallel wires.

Post Route SI

After routing and signal integrity analysis, uses information from a file that contains a list of victim nets to change the routing topology, including layer assignments, spacing, and location, to prevent coupling to other nets. Specify the file with *Use SI Victim File*. Postroute signal integrity repair requires both global and detailed routing. By default, this option is not selected.

Note: This option applies to nets with the *SI Post Route Fix* attribute set to *True*.

SI Victim File Specifies a file from a crosstalk analysis tool, such as the CeltIC™ crosstalk analyzer for cell-based designs, that contains a list of nets with crosstalk problems.

Litho Driven

Avoids lithography problems during routing by avoiding certain routing patterns that might lead to the creation of lithography hotspots.

Default: Off

Routing Control

Selected Nets Only

Specifies whether NanoRoute routes all nets at once or routes selected nets only. To route critical nets as short as possible, select the critical nets and select this option. By default, this option is not selected.

When this option is selected, NanoRoute does the following:

- Removes incomplete nets unless they are marked `+ FIXED` or have a `-skip_routing` net attribute.
- Routes the remaining selected nets.

Bottom Layer

Specifies the lowest layer the router uses for global and detailed routing.

If the design has pins below the layer specified by this parameter, and if the tracks for the in-between layers are aligned to allow stacked vias to be dropped directly on top of the pins, the router uses stacked vias. However, if the tracks are not aligned, the router adds a short piece of wire before dropping a via to go to the next layer.
Default: 1

Note: To set a soft limit, use the *Bottom Layer* attribute.

Top Layer

Specifies the highest layer NanoRoute uses for global and detailed routing. This option sets a hard limit, that is, NanoRoute does not route nets above the specified layer. The default value is the number of the highest routing layer specified in the LEF `LAYER` (Routing) statement. For example, setting the value to 4 means no wires will be routed on any layer above *metal4*: The global and detailed routers will use *metal1*, *metal2*, *metal3*, and *metal4*.

Note: To set a soft limit, use the *Top Layer* attribute.

ECO Route

Specifies engineering change order (ECO) mode. During ECO mode, NanoRoute completes partial routes with added logic, while maintaining the existing wire segments as much as possible.

Note: Select *ECO Route* only if you are running both global and detailed routing.

Area Route

Repairs violations in a local area after global and detailed routing. If you move any cells after routing, you must rerun global and detailed routing before running *Area Route*. By default, this option is not selected.

Note: If you select *Area Route* and the design is not already routed, *Area Route* will route the entire design and issue a warning in the log file.

Area

Specifies the area to route.

Select Area and Route

Lets you select the routing area when you click and drag the mouse in the design display area of the Encounter main window.

Job Control

Auto Stop

Controls whether NanoRoute continues routing if there are many violations. In highly congested designs, NanoRoute stops if the number of violations is too high. If you deselect this option, NanoRoute continues routing until there is no improvement. By default, this option is selected.

Batch

Runs global and detailed routing with standalone NanoRoute from the Encounter environment. The Encounter software passes all current net attribute and option settings, and the selected set of nets, to the router. This command increases the capacity of the 32-bit routing engine.

Note: You can use *Batch* for running both global and detailed routing together; you cannot use it for global routing only or detailed routing only.

Number of Thread(s) For Multiple Threaded

Displays the maximum number of threads for multi-threaded routing. This is a view-only field.

Number of Thread(s) For Superthreaded

Displays the maximum number of threads for Superthreading. This is a view-only field.

Number of Host(s) for Superthreaded

Displays the maximum number of hosts for Superthreading. This is a view-only field.

Set Multiple CPU ... Opens the Multiple CPU Processing form. Use this form to configure multi-threading and Superthreading. For information, see "Multiple CPU Processing" on page 373.

Attribute Opens the NanoRoute/Attributes form. For information, see "NanoRoute/Attributes" on page 1210.

Mode Opens the NanoRoute page of the Mode Setup form. For information, see "Mode Setup – NanoRoute" on page 316.

Save Lets you save the router's option settings, so you can load them later. Opens the Save As form. For information, see "Design Menu" on page 107.

Load Loads a previously saved file with NanoRoute option settings. Opens the Open form. For information, see "Design Menu" on page 107.

Related Topics

- Accelerating Routing with Multi-Threading and Superthreading
- Following a Basic Routing Strategy
- Checking Congestion
- Running Timing-Driven Routing
- Routing Clocks
- Preventing and Repairing Crosstalk Problems
- Running ECO Routing
- Evaluating Violations
- Postroute Via Optimization
- Performing Shielded Routing

- Routing Wide Wires
- Repairing Process Antenna Violations
- Using a Design Flow that Includes Astro or Apollo
- Troubleshooting

Related Text Commands

- `detailRoute`
- `generateTracks`
- `getNanoRouteMode`
- `globalDetailRoute`
- `globalDetailRouteBatch`
- `globalRoute`
- `setNanoRouteMode`

Set Congestion Map Style

Use the Set Congestion Map Style form to display congestion in the design after running Trial Route or running global routing with the NanoRoute router. You can change the way congestion is displayed by selecting options on the form.

The Set Congestion Map Style form displayed depends on the type of routing that was performed.

- If you ran Trial Route, or have a Trial Routed design saved in the database, the software displays the Trial Route version of the form.
- If you ran NanoRoute global route, or have a global-routed design saved in the database, the software displays the NanoRoute version of the form.

The Set Congestion Map Style form has two pages:

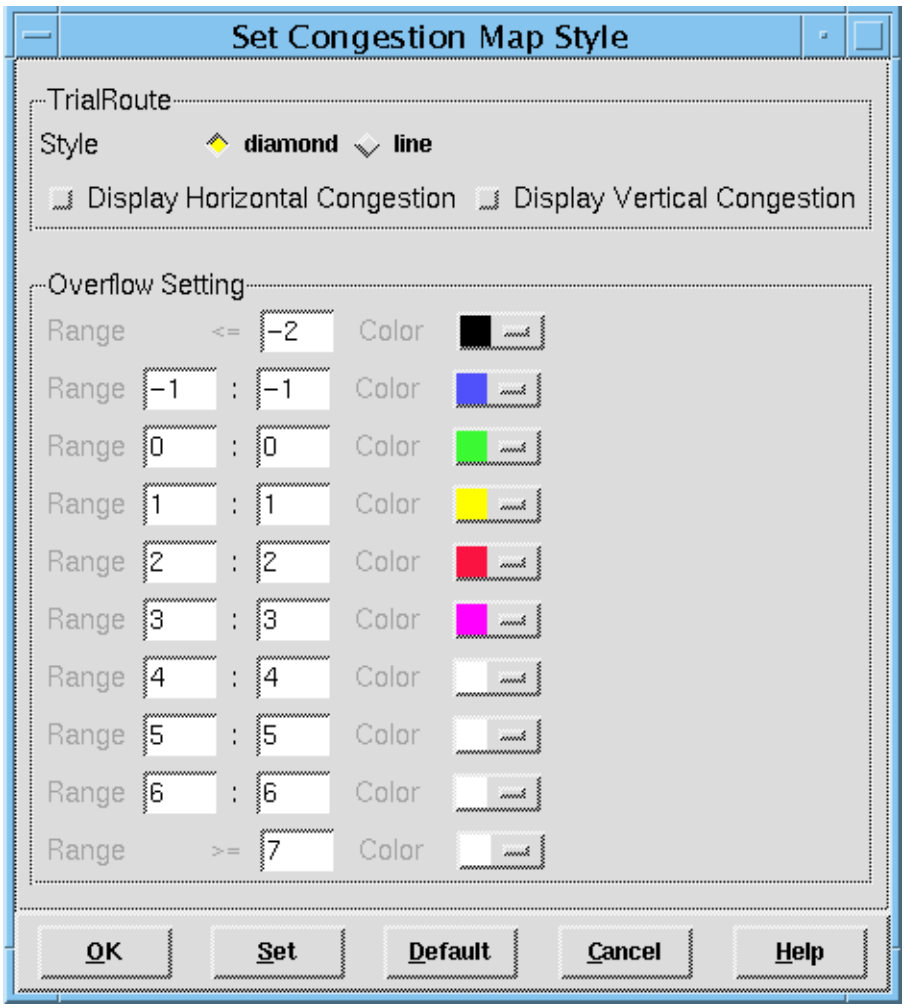
- Set Congestion Map Style – Trial Route on page 1224
- Set Congestion Map Style – NanoRoute on page 1227

Set Congestion Map Style – Trial Route

Use the Set Congestion Map Style – Trial Route form after running Trial Route to see a graphical representation of routing congestion in the design. You can display congestion information using the default Trial Route map style or the map style used by the global router.

Note: To change the display, you must click *OK* to close the form.

➤ Choose *Route – NanoRoute – Congestion Analysis*.



Set Congestion Map Style Fields and Options

Style	Specifies the display style. *Default: diamond*

diamond — Displays routing congestion using the default Trial Route map style. If you select *diamond*, you can choose whether to display horizontal congestion, vertical congestion, or both. *Overflow Setting* values do not apply.

For more information on the Trial Route map style, see "Congestion Markers in the Display" in the *Encounter User Guide*.

line — Displays routing congestion using the global router map style. If you select *line,* you can choose whether to display horizontal congestion, vertical congestion, or both. You can also specify different *Overflow Setting* values.

Display Horizontal Congestion

Displays horizontal congestion. Corresponds to the *HCongest* visibility toggle in the main Encounter window.

Display Vertical Congestion

Displays vertical congestion. Corresponds to the *VCongest* visibility toggle in the main Encounter window.

Overflow Setting

Displays different levels of congestion in the map by assigning specified colors to specified overflow values.

Overflow is the number of tracks required for routing minus the number of tracks that are available in a particular gcell. A negative number indicates that there are more tracks available than required. A positive number indicates that more tracks are required than available.

Note: This option is not enabled unless *line* is selected.

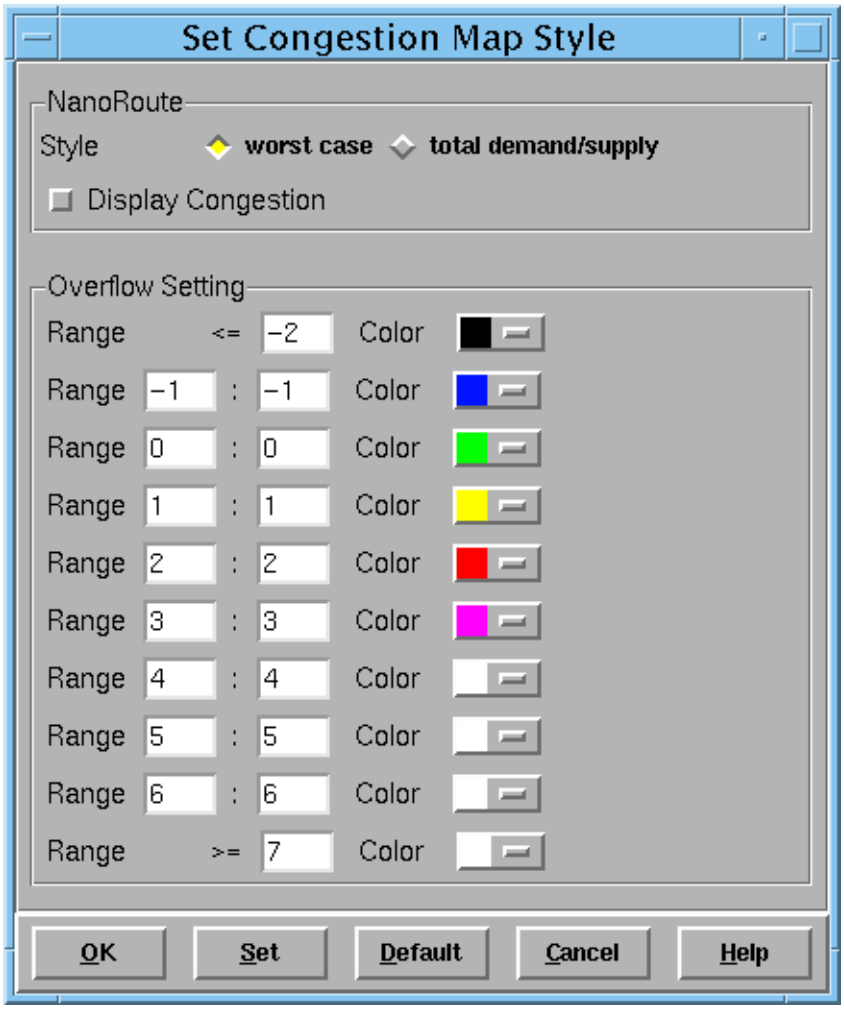
Range	Specifies one or more overflow values to be displayed with a color. You can specify a range of overflow values be displayed using the same color. For example, if you specify `-4:-1`, all areas that still have between four tracks and one track available for routing are displayed using the same color. To display only one overflow level with a color, specify the same number twice. For example, if you specify `2:2`, only areas that require two additional tracks for routing are displayed with the color.
Color	Specifies a color to assign to a *Range*.

Set Congestion Map Style – NanoRoute

Use the Set Congestion Map Style – NanoRoute form after running global routing to create a congestion map. You can select options to display congestion on all visible layers or on the most-congested visible layer only.

Note: To change the display, you must click *OK* to close the form.

➤ Choose *Route – NanoRoute – Congestion Analysis*.



Style — Specifies the display style.
Default: worst case

worst case — Bases the map on visible layer with the worst congestion.

total demand/supply

Bases the map on the total demand (tracks required to complete global routing) and supply (total tracks available for global routing) on all visible layers.

Display Congestion

Turns congestion on or off. Corresponds to the *Congestion* visibility toggle in the main Encounter window.

Overflow Setting

Displays different levels of congestion in the map by assigning specified colors to specified overflow values.

Overflow is the number of tracks required for routing minus the number of tracks that are available in a particular gcell. A negative number indicates that there are more tracks available than required. A positive number indicates that more tracks are required than available.

Range

Specifies one or more overflow values to be displayed with a color.

You can specify a range of overflow values be displayed using the same color. For example, if you specify `-4:-1`, all areas that still have between four tracks and one track available for routing are displayed using the same color.

To display only one overflow level with a color, specify the same number twice. For example, if you specify `2:2`, only areas that require two additional tracks for routing are displayed with the color.

Color

Displays the color for a *Range*.

Mixed Signal

The *Route* menu's Mixed Signal Router form enables you to route analog hard blocks and digital nets and blocks in a mixed signal design.

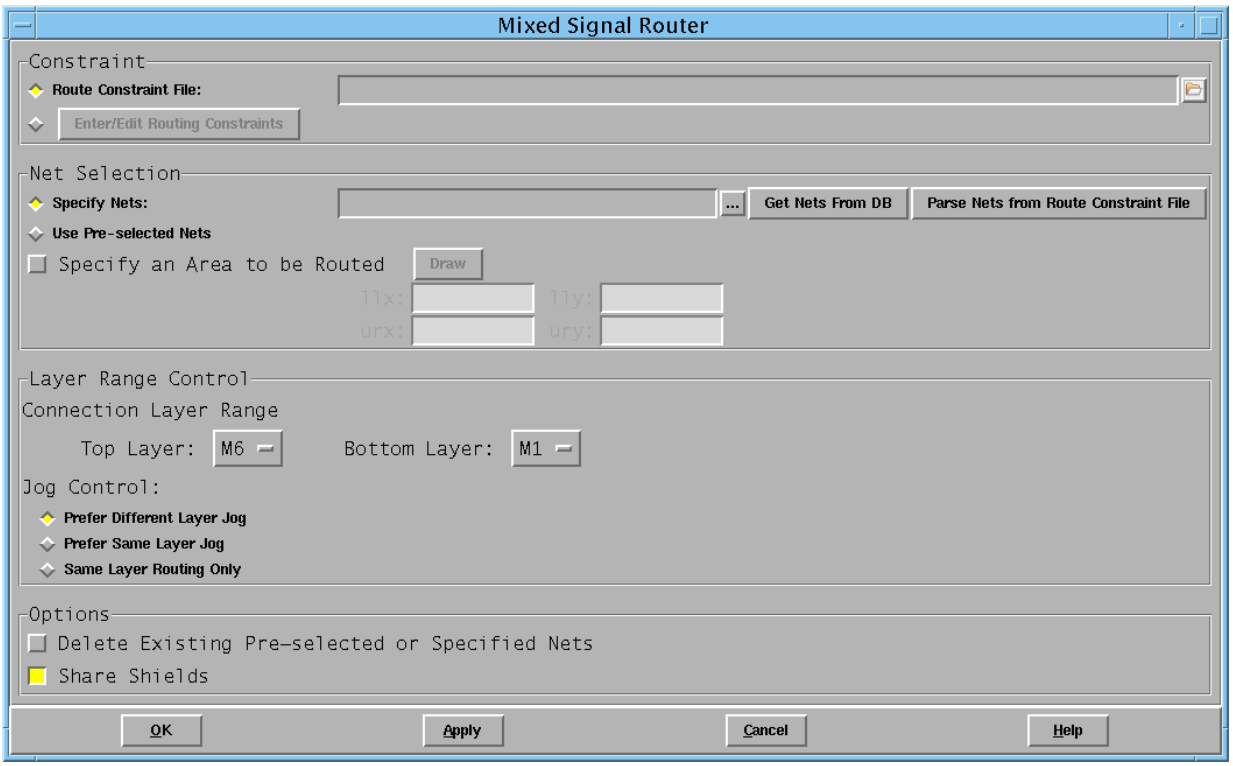
The mixed signal router honors constraints for the following types of complex routing:

- Net shielding, including coaxial shielding, in which the router shields noise-sensitive nets on the top and bottom, in addition to the right and left sides
- Matched-pair routing, in which the router attempts to create routes that are the same length, although they are not required to be topologically similar
- Differential routing, in which the router attempts to match the parasitic load on driving pins of nets
- Width and resistance

Mixed Signal Router

Use the Mixed Signal Router form to route analog hard blocks and digital nets and blocks in a mixed signal design. The mixed signal router honors the complex routing constraints you specify on the Mixed Signal Constraint Editor form.

➤ Choose *Route – Mixed Signal – Route ...*



Mixed Signal Router Fields and Options

Route Constraint File

Specifies the constraint file for the mixed signal router. The file contains the names of the nets to route and the mixed signal routing constraints.

The constraint file for the mixed signal router has a `.const` extension.

Edit/Enter Routing Constraints

Displays the Mixed Signal Constraint Editor form if *Route Constraint File* is also selected. You can edit the constraints using the constraint editor. For more information, see "Mixed Signal Constraint Editor" on page 1620.

Specify Nets:

Specifies nets to route. If you specify a constraint file, the router parses nets from the file. You do not have to specify nets one by one. You can use the *Browse* (*...*) button to edit the *Specify Nets* list.

Get Nets From DB

Populates the *Specify Nets* text box with the net names without running the router if you routed the design previously or if you entered net names using the route constraint editor.

Parse Nets From Route Constraint File

Writes nets to the database without running the router if *Route Constraint File* is selected.

Use Pre-selected Nets

Routes selected nets. When you select *Delete Existing Pre-selected or Specified Nets*, this option is also selected.

Specify an Area to be Routed

Specifies the area to route.

- If you select this option and *Use Pre-selected Nets*, all selected nets are routed and all ports that fall within the specified area are routed.
- If you select this option and *Specify Nets*, the router checks that all the specified nets fall into the specified area. It routes all the specified nets and all ports that fall within the specified area.

Connection Layer Range

Specifies the top and bottom layers to use for mixed signal routing.

- If you specify a top routing layer with the `setMaxRouteLayer` command, the form displays that value as the default value.
- If you have not set a top layer with `setMaxRouteLayer`, the form displays the topmost routing layer as the default value.

Jog Control

Specifies that jogs are allowed during routing to avoid DRC violations.
Default: Prefer Different Layer Jog

Select one of the following options:

Prefer Different Layer Jog

If a jog is necessary to avoid creating DRC a violation, changes to another layer in the preferred direction to create the jog if possible.

Prefer Same Layer Jog

If a jog is necessary to avoid creating a DRC violation, creates the jog without changing layers if possible. This can result in routing in the non-preferred direction.

Same Layer Routing Only

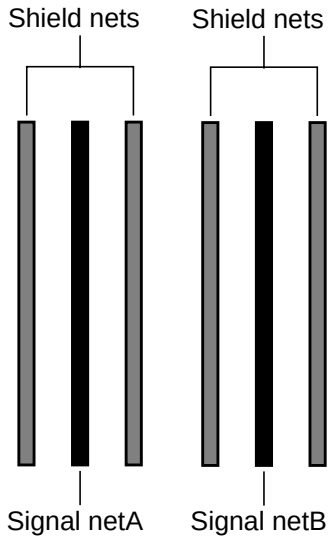
If a jog is necessary to avoid creating a DRC violation, creates the jog without changing layers. This results in routing in the non-preferred direction.

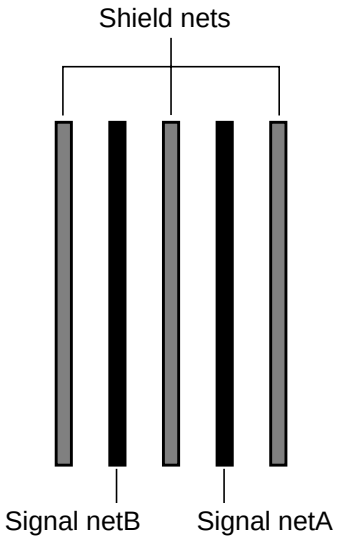
Delete Existing Pre-selected or Specified Nets

Deletes existing nets during routing. If this option is not selected, existing nets are not deleted during routing.
Default: Off

Share Shields

Specifies that the shielded nets can share a shield net when the nets are parallel. The following figures show two nets that are shielded on the right and left sides. In the figure on the left, signal netA and signal netB each has its own shield nets. In the figure on the right, signal netA and signal netB share the center shield net.
Default: On





Related Text Commands

- `routeMixedSignal`
- `setMaxRouteLayer`

Metal Fill

Use the metal fill forms to create or trim metal fill automatically, based on the constraints specified in the LEF file or the values you specify on the forms.

The *Metal Fill* submenu contains the following items:

- *Setup*

  Opens the Setup Metal Fill Options form.

- *Add*

  Opens the Add Metal Fill form.

- Trim

  Issues the `trimMetalFill` command.

Setup Metal Fill Options

Use the Setup Metal Fill Options form to set options for adding or trimming metal fill.

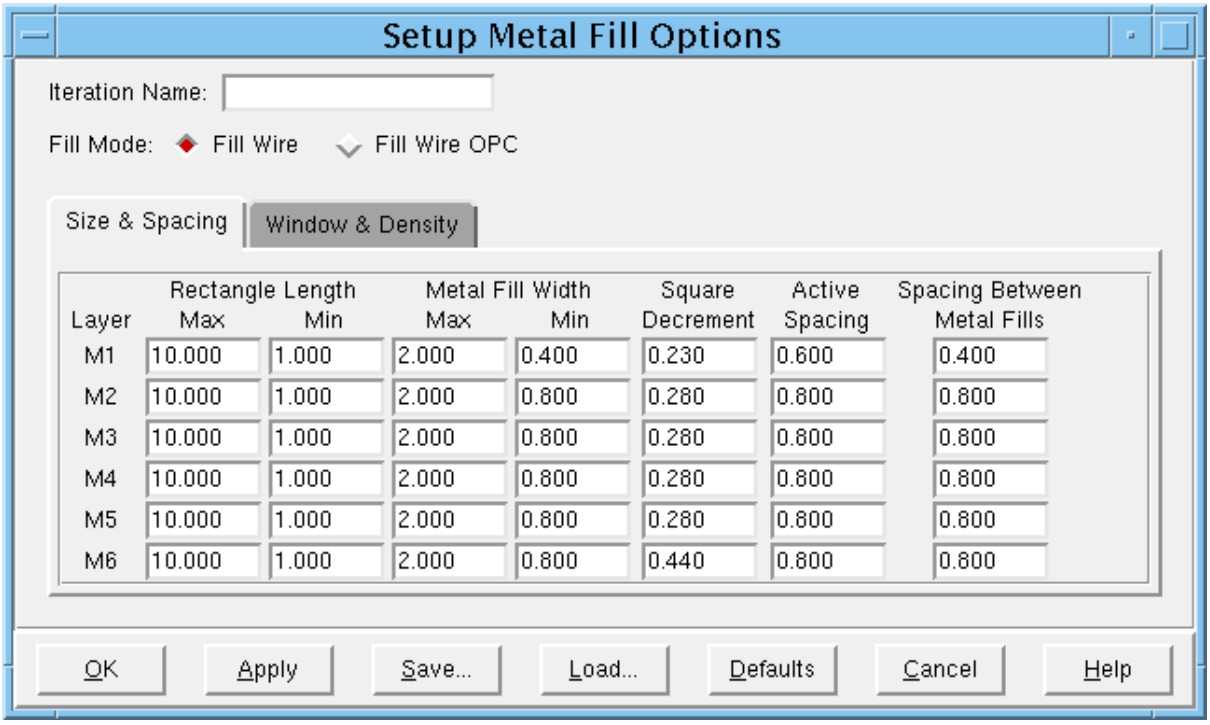
The Setup Metal Fill Options form contains the following two pages:

- Setup Metal Fill Options – Size & Spacing on page 1236
- Setup Metal Fill Options – Window & Density on page 1240

Setup Metal Fill Options – Size & Spacing

Use the *Size & Spacing* page of the Setup Metal Fill Options form to specify the size of metal fill segments.

➤ Choose *Route – Metal Fill – Setup*, then click the *Size & Spacing* tab.



Setup Metal Fill Options – Size & Spacing Fields and Options

Note: For each of the following options, you can specify different values for each layer.

Iteration Name

Specifies a name for a set of values for metal fill options that the software stores and uses when it adds metal fill.

Window size and step must be the same for all iterations of a specific layer.

Fill Mode

Specifies whether the metal fill will go through the optical proximity correction (OPC) process.
Default: Fill Wire

Fill Wire Specifies metal fill that will not go through the OPC process.

Fill Wire OPC Specifies metal fill that will go through the OPC process. This fill can be smaller than non-OPC metal fill and is governed by the same design rules as regular wires, instead of the rules that govern non-OPC metal fill.

- OPC metal fill that is floating (unconnected) is included in the Fills statement of DEF 5.7.
- OPC metal fill that is tied off (connected) is included in the Special Wiring statement of DEF 5.7.

  For more information, see the "DEF Syntax" chapter in the *LEF/DEF Language Reference*.
- The GDSII map file identifies the following object names for OPC and non-OPC metal fill: `FILL`, `FILLOPC`, `VIA`, `VIAFILL`.

  For more information, see GDSII Map File Format in the "Importing and Exporting Designs" chapter of the *Encounter User Guide*.

Rectangle Length Max Specifies the maximum length (in microns) of each metal fill segment.
Default: `10.0`

Note: Use this field only if you select the *Rectangular* shape option on the Add Metal Fill form.

Rectangle Length Min Specifies the minimum length (in microns) of each metal fill segment.
Default: `1.0`

Note: Use this field only if you select the *Rectangular* shape option on the Add Metal Fill form.

Metal Fill Width Max Specifies the maximum width (in microns) of each metal fill segment.
Default: `2.0`

Metal Fill Width Min

Specifies the minimum width (in microns) of each metal fill segment.
Default: `0.4` on thin layers (less than 0.24 microns); `0.8` on thick layers

Square Decrement

Specifies the number of microns used to decrease the size of each successively smaller segment of metal fill until the *Metal Fill Width Min* size is reached. Use this field to control the number of different sizes of metal fill in the design.

The software uses the maximum metal fill size specified unless it is impossible to fit a piece of metal fill into a particular area. The software then attempts to use successively smaller pieces of metal fill until the *Metal Fill Width Min* value is reached.

For example, if the *Metal Fill Width Max* value is `8`, the *Metal Fill Width Min* value is `4`, and the *Decrement* value is `2`, then metal fill with widths of `8`, `6`, and `4` are used. However, to give the software more flexibility, you can change the *Square Decrement* value to a smaller value. If the *Square Decrement* value is `1`, metal fill with widths of `8`, `7`, `6`, `5`, and `4` can all be used.
Default: `WIDTH` value specified in the `Layer` (Routing) statement of the LEF file

Note: Use this field only if you select the *Square* shape option on the Add Metal Fill form.

Active Spacing

Specifies the minimum distance (in microns) between a metal fill segment and any object in the design other than another metal fill segment.
Default: `FILLACTIVESPACING` value specified in the `LAYER` (Routing) statement of the LEF file. If not defined, `0.6` on thin layers (less than 0.24 microns); `0.8` on thick layers

Spacing Between Metal Fills

Specifies the minimum distance (in microns) between one metal fill segment and another metal fill segment.
Default: `0.4` on thin layers (less than 0.24 microns); `0.8` on thick layers

Related Topics

- Specifying Metal Fill Parameters

- Specifying the Active Spacing Value

Related Text Commands

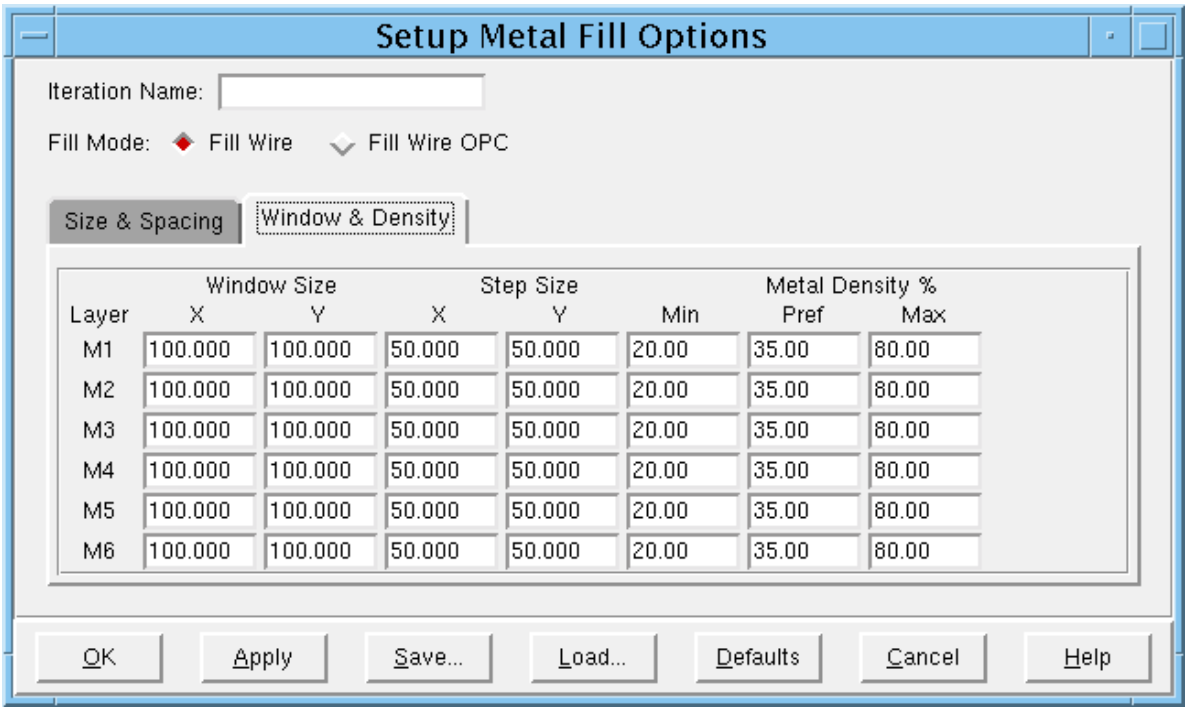
- `setMetalFill`

Setup Metal Fill Options – Window & Density

Use the *Window & Density* page of the Setup Metal Fill Options form to specify the density for the metal fill, as well as the areas in which density is checked before metal fill is added. The software examines the metal density in each window and automatically inserts metal fill to achieve preferred density.

Note: If the metal density in a window exceeds the maximum metal density allowed in the LEF file, the software issues an error message.

➤ Choose *Route – Metal Fill – Setup*, then click the *Window & Density* tab.



Setup Metal Fill Options– Window & Density Fields and Options

Note: You can specify different values for the options for each layer.

Iteration Name

Specifies a name for a set of values for metal fill parameters that the software stores and uses later, when it adds metal fill.

Window size and step must be the same for all iterations of a specific layer.

Fill Mode

Specifies the type of metal fill to add. Select one of the following types:

Fill Wire

Specifies metal fill that has not gone through the OPC process.

Fill Wire OPC

Specifies metal fill that has gone through the OPC process.

Window Size X

specifies the x dimension (width in microns) of the area used by the software to examine the metal density. The command assesses the metal density in each window, moving the window iteratively through the design.
Default: `DENSITYCHECKWINDOW` value in the `LAYER` (Routing) statement of the `LEF` file. If not defined, `100.000`.

Window Size Y

Specifies the y dimension (height in microns) of the area this command uses to examine the metal density. The command assesses the metal density in each window, moving the window iteratively through the design.
Default: `DENSITYCHECKWINDOW` value in the `LAYER` (Routing) statement of the `LEF` file. If not defined, `100.000`.

Step Size X

Specifies the x distance (width in microns) the window moves for each iteration of metal density analysis. The recommended value is half the value of the Window Size.
Default: `DENSITYCHECKSTEP` in the `LEF` file. If not defined, `50.000`.

Step Size Y

Specifies the y distance (height in microns) the window moves for each iteration of metal density analysis. The recommended value is half the value of the Window Size.
Default: `DENSITYCHECKSTEP` in the `LEF` file. If not defined, `50.000`.

Metal Density % Min

Specifies the minimum metal density allowed in the design. Changing this value overrides the value defined in the `LEF` file. The software checks for a conflict between the value you specify and the default density range defined in the `LEF` file.
Default: `MINIMUMDENSITY` value of the `LAYER` (Routing) statement of the `LEF` file. If not defined, `20.000`.

Metal Density % Pref

Specifies a percentage value for the preferred metal density for the layer. When the metal density in a window is less than the minimum metal fill density value, adds metal fill to achieve a density slightly above the preferred density if possible.

In addition, metal fill uses the prefered density value in the estimation of `MACRO` density for layers that have most of the `MACRO` covered by `OBS` shapes and for DEF `BLOCKAGES` without both `+ FILLS` and `+ PUSHDOWN`.

Metal fill uses the following scheme for the treatment of DEF blockages with `+ FILLS` or `+ PUSHDOWN`:

- DEF `BLOCKAGES` with `+ PUSHDOWN` = 100 percent density (the same as real metal segments)
- DEF `BLOCKAGES` with `+ FILLS` = 0 percent density

Cadence recommends modelling LEF `MACRO`s by using the `DENSITY` statement, with density windows that are smaller than the metal fill windows. For example, if the metal fill windows are 100 x 100, use 25 x 25 or smaller values for the density rectangles.
Default: `35.00`

Metal Density % Max

Specifies the maximum metal density allowed in the design. Changing this value overrides the value defined in the LEF file. This command checks whether the value you specify conflicts with the default density range defined in the LEF file.
Default: `MAXIMUMDENSITY` value of the `LAYER` (Routing) statement of the LEF file. If not defined, `80.000`.

Related Topics

- Specifying Metal Fill Parameters
- Specifying the Active Spacing Value

Related Text Commands

- `setMetalFill`

Add Metal Fill

Use the Add Metal Fill form to specify how to perform the following operations:

- Connect new metal fill
- Specify whether to remove or retain existing metal fill
- Select the layers on which to add metal fill
- Specify an area within the design into which to add metal fill

➤ Choose *Route – Metal Fill – Add*.

Add Metal Fill Fields and Options

Number of Hosts
Displays the number of hosts to use for distributed processing. This is a non-editable field. To change setting for distributed processing, select the *Set Multiple CPU* button.

Set Multiple CPU
Opens the Multiple CPU Processing form, where you can view or change settings for distributed processing. For more inforamtion, see "Multiple CPU Processing" on page 373.

Iteration Name List
Specifies a list of iterations (specify the names on the Setup Metal Fill form) for adding metal fill. Processes the iterations in the order listed, and stops when the preferred density is reached in any iteration.

When you add metal fill in iteration mode, it runs several times with just one invocation of `addMetalFill`, and uses the ending density from an iteration as the starting density of the next iteration. For that one invocation, the window size and step for a specific layer must be the same for all iterations.

Shape
Specifies the shape of the metal fill. Select one of the following options:

Rectangle
Creates both rectangular and square metal fill. If you select this option, you can specify maximum and minimum width and height values on the Setup Metal Fill Options – Size & Spacing page.

Square
Creates only square metal fill. If you select this option, you can specify maximum and minimum width values, as well as a decrement value on the Setup Metal Fill Options – Size & Spacing page.

Tie High/Low to net(s):
Connects metal fill to the nets specified in the text entry field. List the nets in a priority order, because the software always attempts to connect metal fill segments to the first net in the list. Metal fill segments connect to other nets in the list if a connection to the first net in the list is not possible.
Default: By default, this option is selected and the text entry field is automatically populated with the net names specified on the *Power* page of the Design Import form. If deselected, metal fill is left floating.

Connection shape

Specifies whether metal fill is connected in a *Tree* or *Mesh* shape.
Default: Tree

Tree — Connects metal fill shapes using the minimum number of via cuts. When *Tree* is selected, metal fill shapes do not carry current.

Mesh — Connects metal fill shapes to the power mesh, allowing it to carry current as part of the power and ground structure. Uses the maximum number of cuts in vias at every intersection. Increasing the number of cuts helps to reduce IR drop.

Keep unconnected metal fills:

Allows the creation of metal fill that is not connected to the nets specified by the *Tie High//low to net(s)* option. If deselected, the software does not create unconnected metal fill segments.

Note: This option is enabled when you select *Tie High/Low to net(s)*.

Square shape

Adds unconnected metal fill that has a square shape. If deselected, the software can create both rectangular and square unconnected metal fill segments. This is the default.

Note: This option is available only if you select *Tie High/Low to net(s)* and *Keep unconnected metal fills*.

Use Generated Vias Only

Specifies that only generated vias are used for metal fill connections.
Default: Off

Allow Fill on Cells

Allows the software to add metal fill into `CLASS BLOCK` and `CLASS PAD` macro cells.

Before adding the metal fill, make sure that the cells are at preferred density, because adding metal fill shapes inside the cells might lead to timing problems inside the cells.

The software can always add metal fill to `CLASS CORE SPACER` cells, but can add it to `CLASS BLOCK` and `CLASS PAD` cells only when this option is specified.
Default: Off

Delete metal fill before creating new metal fill

Removes existing metal fill from a layer before creating more metal fill on that layer.
Default: Off

Layer Selection

Specifies the metal layers for adding metal fill.

Timing Aware

Considers the impact of metal fill on timing. Minimizes cross-coupling while meeting preferred density targets when adding metal fill. Assigns costs to adding metal fill near power or ground nets (0 cost), signal nets (moderate cost), and clock nets (high cost) and minimizes costs when adding metal fill.

If the `buildTimingGraph` command has run before you add metal fill, the software adjusts the costs as a function of the slack (the worst slack has the highest cost).

Critical nets from timing analysis

Uses the Encounter common timing engine (CTE) for static timing analysis. Further divides signal nets into non-critical nets (small cost) and critical nets (moderate cost).

Slack threshold

Specifies a slack threshold for timing-critical nets during timing-driven routing with CTE. Specify a small positive value, such as 100 nanoseconds, to give yourself a margin of safety.
Default: `0.0`

Area	Restricts metal fill to the specified portion of the design. You can enter coordinates in the *X1*, *X2*, *Y1*, and *Y2* fields or click the *Draw* button and drag the mouse in the design area to populate the coordinate fields automatically. *Default:* Entire design area

Related Topics

- Specifying Metal Fill Parameters

Related Text Commands

- `addMetalFill`
- `editDelete -shapes {FILLWIRE FILLWIREOPC}`

Trim

Use the *Trim* item on the *Metal Fill* submenu to trim metal and via fill that causes DRC violations.

➤ Choose *Route – Metal Fill – Trim*.

This menu command does not have an associated GUI form.

Related Topics

- Trimming Metal Fill

Related Text Commands

- `trimMetalFill`

Via Fill

Use the Via Fill forms to create via fill automatically, based on the values you specify on the forms.

The Encounter software inserts vias into a placed and routed design to help achieve cut density within the range required by a specific manufacturing process. Unlike adding metal fill, when the software considers only the layer on which the fill is added, adding via fill requires that the software consider the metal layers above and below the cut layer.

The vias can be floating or connected to power or ground wiring.

Add via fill in the following areas immediately before adding metal fill:

- Where metal fill shapes would intersect with power or ground nets on consecutive layers if no via fill was added.
- Where metal fill shapes on consecutive layers would intersect if no via fill was added.

Tip

To reduce the need for via fill, insert multiple-cut vias with the NanoRoute® router. For information, see `setNanoRouteMode`.

The *Via Fill* submenu contains the following items:

- *Setup*

  Opens the Setup Via Fill Options form.

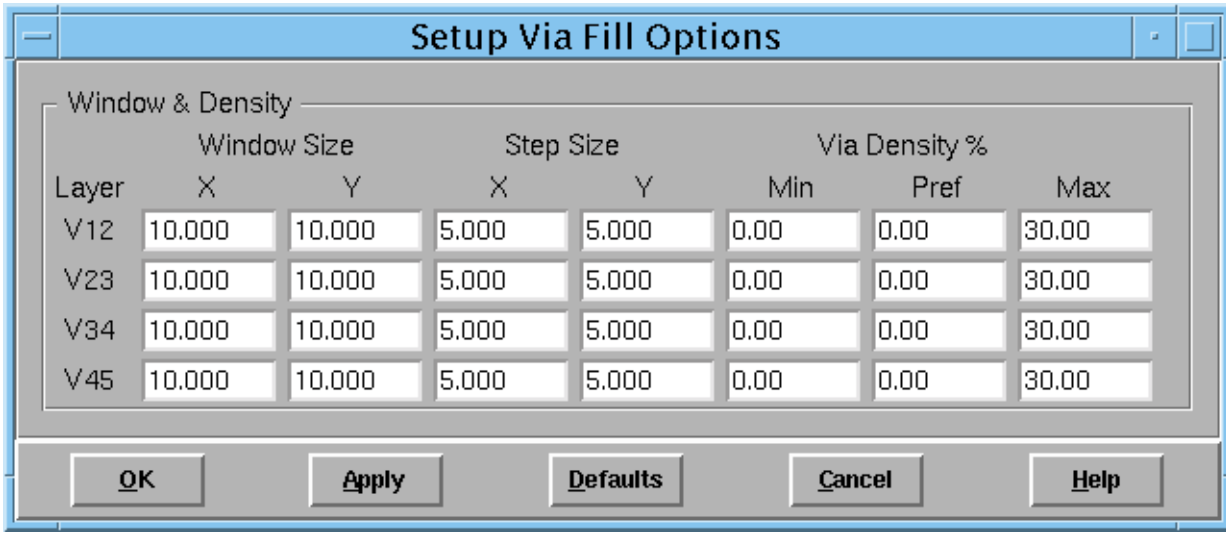
- *Add*

  Opens the Add Via Fill form.

Setup Via Fill Options

Use the Setup Metal Fill form to set options for adding or trimming via fill.

➤ Choose *Route – Via Fill – Setup*.



Setup Via Fill Fields and Options

Note: The software uses the width and spacing values on the Setup Metal Fill Options form.

Window Size	Specifies the x and y dimensions in microns of the area `setViaFill` uses to examine the cut density. The software assesses the cut density in each window, moving the window iteratively through the design. *Default:* 10 microns in each dimension	
Step Size	Specifies the x and y step distance in microns the window moves for each iteration of cut density analysis. *Default:* 5 microns in each dimension	
Via Density %	*Min*	Specifies a percentage value for the minimum cut density allowed in the design. *Default:* area of two cuts divided by 100 square microns

	Pref	Specifies a percentage value for the preferred cut density for the layer. When the cut density in a window is less than the minimum cut density value, this parameter adds via fill to achieve a density as close as possible to the preferred value. To disable the preferred density feature, specify `0`. *Default:* area of two cuts in the cut layer
	Max	Specifies a percentage value for the maximum cut density allowed. *Default:* `30%`
Layer	Specifies the cut layer to which the parameters of the `setViaFill` command apply.	

Related Text Commands

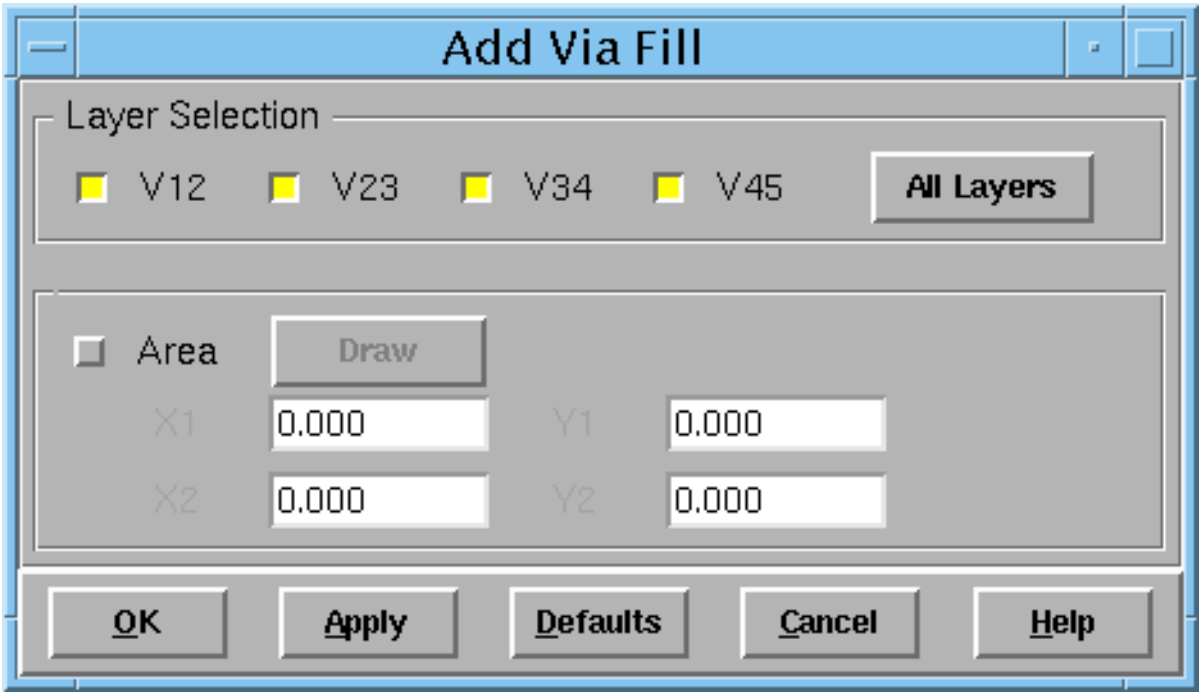
- `setViaFill`

Add Via Fill

Use the Add Via Fill form to specify where to perform the following operations:

- Layers on which to add via fill
- Area in which to add via fill

➤ Choose *Route – Via Fill – Add*.



Add Via Fill Fields and Options

Layer Selection	Specifies the cut layers where via fill is added. *Default: All Layers*
Area	Specifies a set of coordinates within which to add via fill.

Related Text Commands

- `addViaFill`

Flip Chip

The *Route* menu's Flip Chip submenu contains the Flip Chip Route form to enable you to create special route wires to power bumps and create regular route wires to signal bumps.

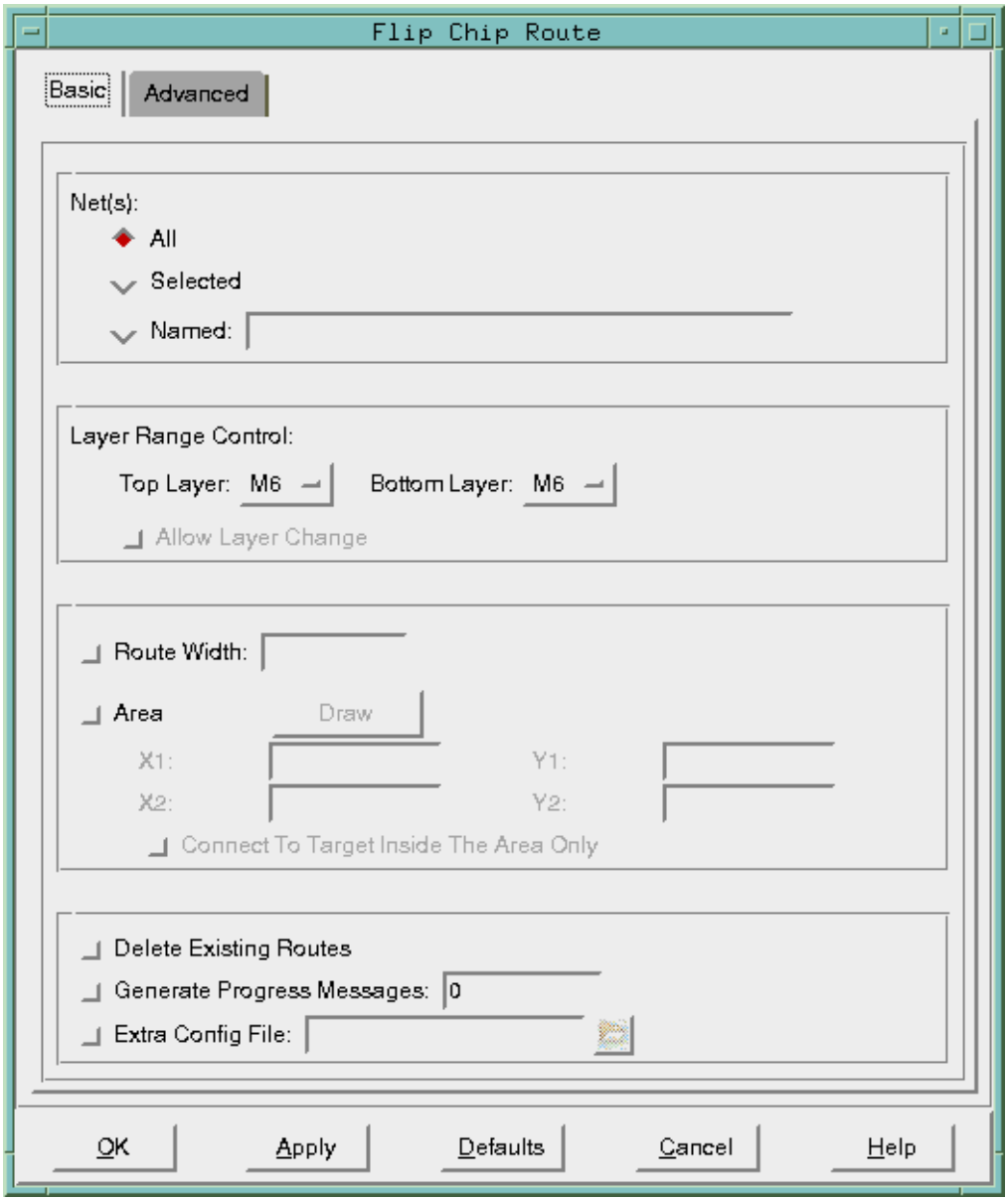
The Flip Chip Route form contains the following two pages:

- *Flip Chip Route – Basic*
- *Flip Chip Route – Advanced*

Flip Chip Route – Basic

Use the *Basic* page of the Flip Chip Route form to create special route wires to power bumps.

➤ To open the *Basic* page of the Flip Chip Route form, choose *Route – Flip Chip – Flip Chip Route,* then click the *Basic* tab.



Flip Chip Route – Basic Fields and Options

Net(s)

Specify one of the following options for which nets are to be connected to the bumps:

All	Connects to bumps belonging to all nets in the design. This is the default.
Selected	Connects to bumps belonging to the nets that you select interactively in the design display area.
Named	Connects to bumps belonging to the nets that you specify in the text entry field.

Layer Range Control

Top Layer	The top-most metal layer that the software can use when routing power bumps. Power bumps on higher layers are not connected.
Bottom Layer	The bottom-most metal layer that the software can use when routing power bumps. Power bumps on lower layers are not connected.
Allow Layer Change	If selected, the software makes only straight connections on the same layer. This is the default. If deselected, the software permits the route to change to another layer to avoid DRC violations.

Route Width

If selected, wires that connect to the bumps always use the width that you specify in the text entry field, regardless of the size of the bump or the source to which the bump connects. If deselected, the width of the route is the smaller of either the bump or the pin that is connected to the bump. This is the default.

Area

If selected, restricts routing to the specified portion of the design. You can either enter coordinates in the *X1*, *X2*, *Y1*, and *Y2* fields, or click the *Draw* button to interactively select an area in the design display window. If deselected, the software performs routing for the entire design area. This is the default.

Note: Selecting the *Area* option always preserves existing connections. If you select *Area*, the *Delete Existing Routes* option is disabled.

Connect To Target Inside The Area Only

If selected, connections from all sources within the specified area can connect only to power bumps that are also inside that area. If deselected, the software makes connections from all sources within the specified area to power bumps both inside and outside the specified area. This is the default.

Note: This option is only available if you also select the *Area* option.

Delete Existing Routes

If selected, removes existing connections when you click *Apply* or *OK*. If deselected, existing connections are left untouched each time you use the Route Flip Chip Power form. This is the default.

Note: This option is disabled if you select the *Area* option.

Generate Progress Messages

If selected, you can see all messages displayed while power routing takes place. Enter a value to specify the interval at which progress messages are generated. If you specify `1`, the software generates every progress message; if you specify `2`, the software generates every other progress message, and so on. If you do not select this option, or if you specify a value of `0`, routing messages do not display in the Encounter console. This is the default.

Extra Config File

The name of the file that contains extra configuration options.

Caution

You should only use the extra configuration file if you are familiar with its use.

The following variables can be used in the extra configuration file:

- `srouteMaxViaArraySize` *`percent`*

  The default is `100`.

- `srouteReduceLayerChanges` *`integer`*

  The default is `0`.

- `srouteStraightConnections [straight routing style (layer change, DRC clean)]`

- `srouteTimeLimit` *`seconds`*

  The default is `100`.

- `srouteTrivialRouteOnly {true | false}`

  The default is `false`.

Related Text Commands

For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `fcroute -type power`

Flip Chip Route – Advanced

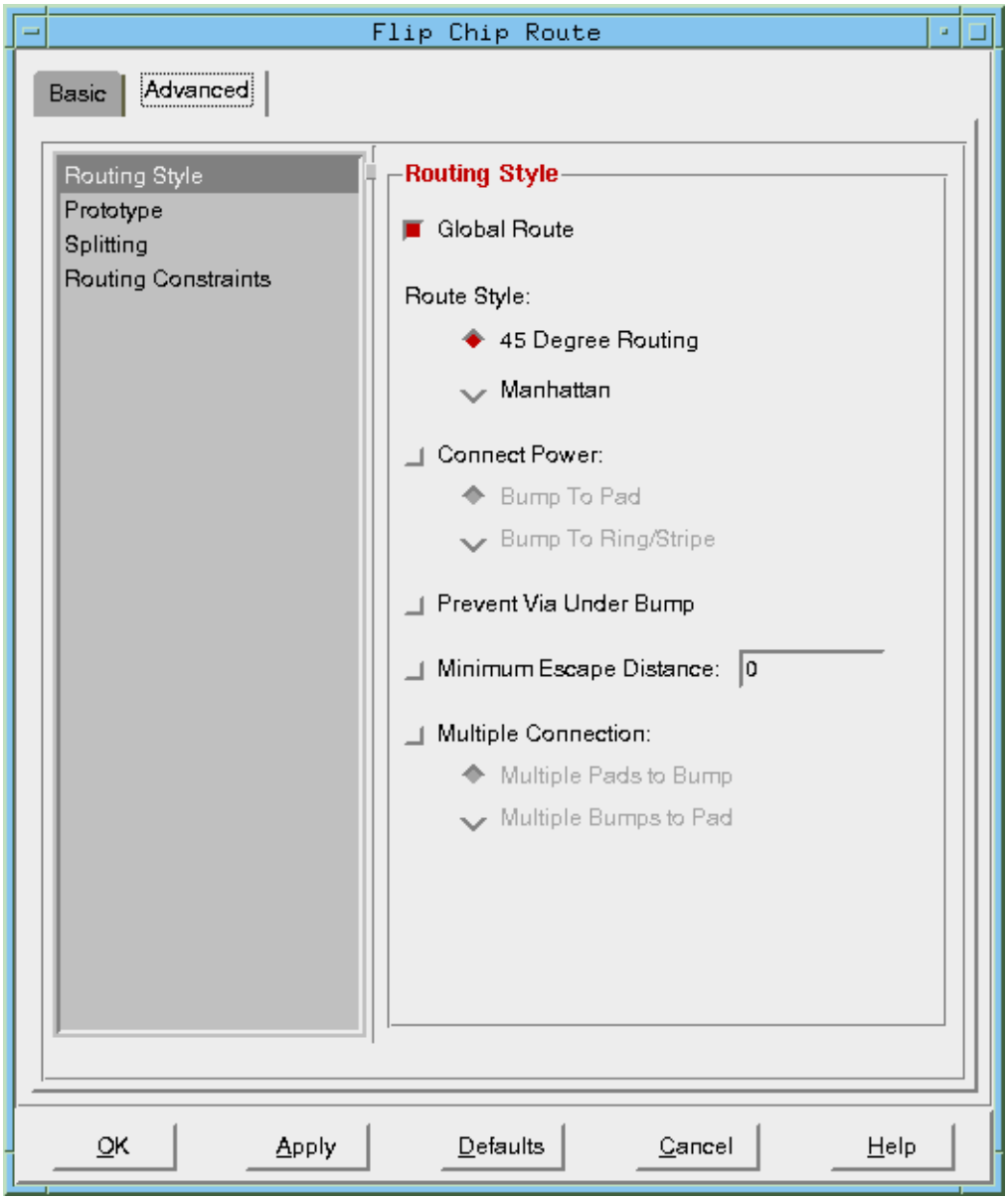
Use the *Advanced* page of the Flip Chip Route form to create regular route wires to signal bumps. The Flip Chip Route form contains the following four pages:

- *Flip Chip Route – Advanced – Routing Style*
- *Flip Chip Route – Advanced – Prototype*
- *Flip Chip Route – Advanced – Splitting*
- *Flip Chip Route – Advanced – Routing Constraints*

Flip Chip Route – Advanced – Routing Style

Use the *Advanced – Routing Style* page of the Flip Chip Route form to specify options for routing style and power connectons.

➤ To open the *Advanced – Routing Style* page of the Flip Chip Route form, choose *Route – Flip Chip – Flip Chip Route*, click the *Advanced* tab, then select *Routing Style*.



Flip Chip Route – Advanced – Routing Style Fields and Options

Global Route

Performs global routing. Plans the interconnect by breaking the routing portion of the design into rectangles called global routing cells (gcells) and assigning the signal nets to the gcells.

Route Style

Specifies the routing style options to select the type of routing for the design.

45 Degree Routing

Selects the 45-degree routing algorithm.

Manhattan

Selects orthogonal, or 90-degree, routing for the design.

Connect Power

Connects all power bumps to the I/O cell pin. It does not connect to a power or ground stripe or ring.

Bump To Pad

Connects power bumps to pads.

Bump To Ring/Stripe

Connects power bumps to rings and stripes.

Prevent Via Under Bump

Specifies that vias are generated next to the bump instead of directly on the bump.

This option is available only with `fcroute -signal`.

Default: If you do not specify this parameter, vias can be generated that connect directly to the bump.

Minimum Escape Distance

Specifies the minimum distance from the edge of the pin to the edge of the wire segment.

Multiple Connection

Multiple Pads to Bump

Enables you to route from multiple pads to one bump.

Multiple Bumps to Pad

Enables you to route from multiple bumps to one pad.

Related Text Commands

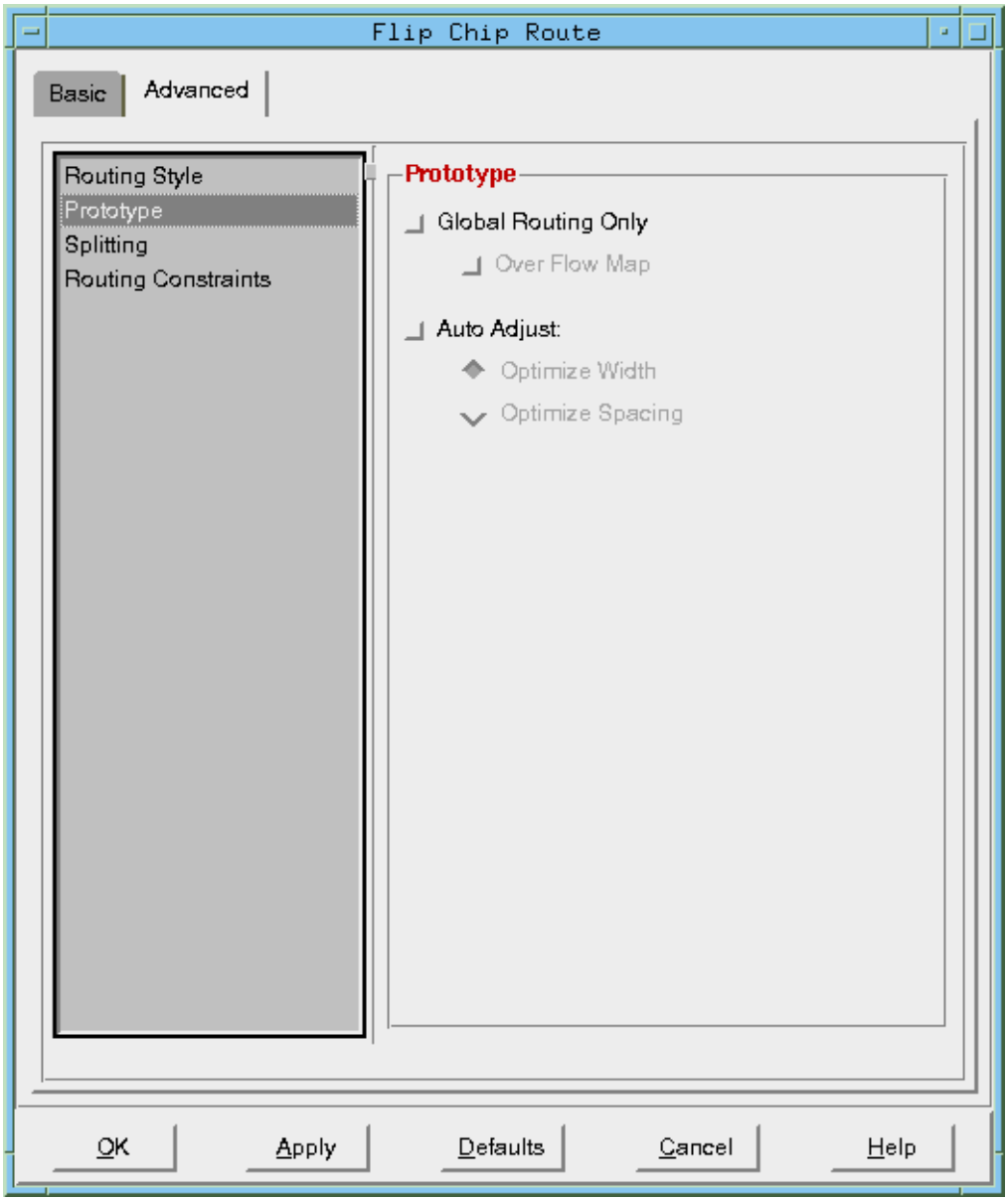
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `fcroute -type signal`

Flip Chip Route – Advanced – Prototype

Use the *Advanced – Prototype* page of the Flip Chip Route form to specify options for global routing and auto adjust.

➤ To open the *Advanced – Prototype* page of the Flip Chip Route form, choose *Route – Flip Chip – Flip Chip Route*, click the *Advanced* tab, then select *Prototype*.



Flip Chip Route – Advanced – Prototype Fields and Options

Global Routing Only

Performs global routing only. Plans the interconnect by breaking the routing portion of the design into rectangles called global routing cells (gcells) and assigning the signal nets to the gcells.

Over Flow Map

Displays the congestion map using the width and spacing parameters specified in the extra configuration file.

Auto Adjust

Optimize Width

Adjusts the width and spacing of each net in the design.

Optimize Spacing

Adjusts the spacing of each net in the design. This option uses the minimum width value of the RDL layer from the LEF file, then increases the spacing for all nets until the maximum allowable spacing is reached. The maximum allowable spacing value is written to the `encounter .log` file as: `SPACING` *`max_value`*.

Note: You do not need a constraint file as input to adjust spacing.

Related Topics

For information on the following topic, see “Power Planning and Routing” in the *Encounter Text User Guide*.

- Creating Differential Routing to Signal Bumps

Related Text Commands

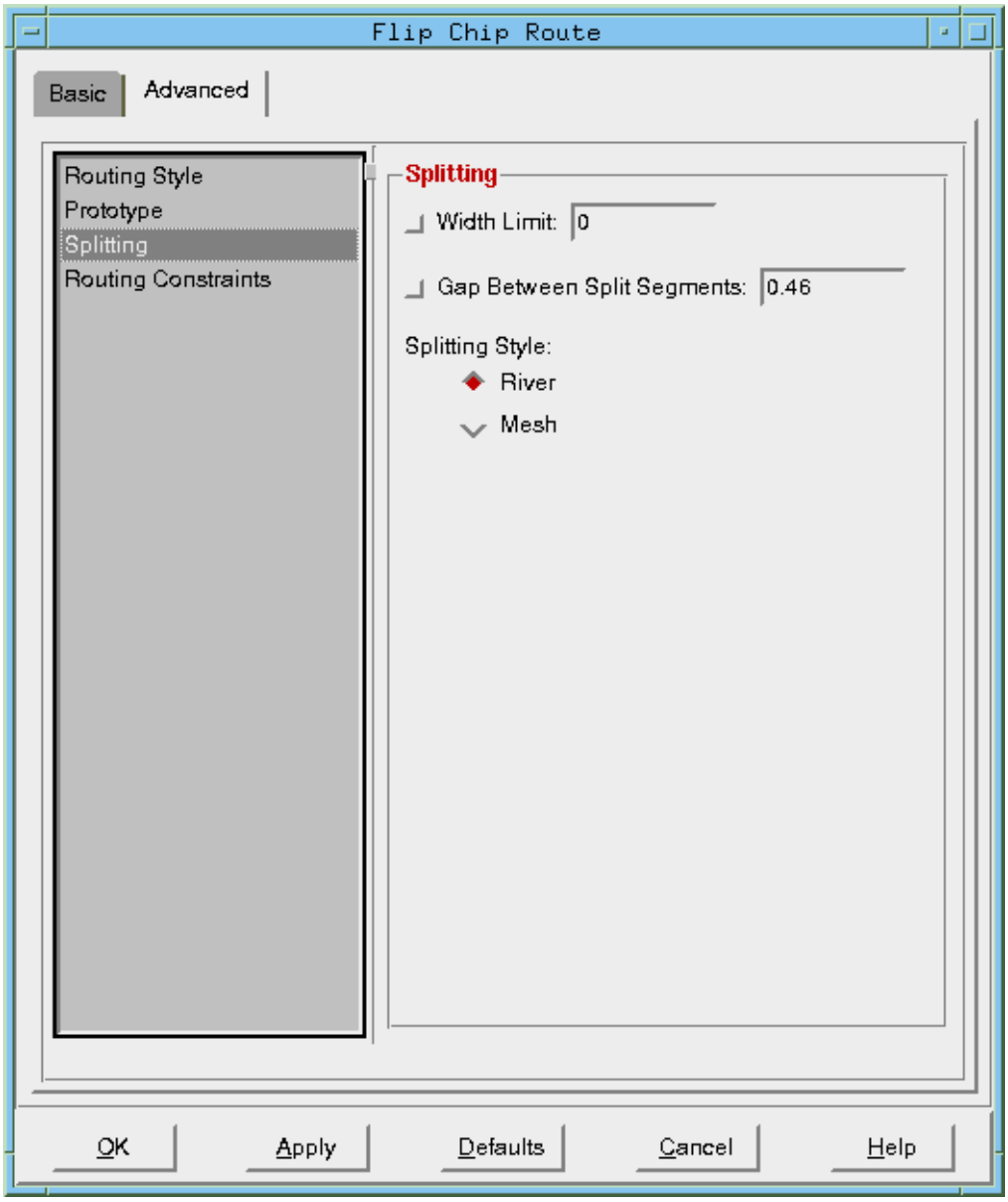
For information on the following command, see “Power Route Commands” in the *Encounter Text Command Reference*.

- `fcroute -type signal`

Flip Chip Route – Advanced – Splitting

Use the *Advanced – Splitting* page of the Flip Chip Route form to specify options for the width limit, gap between split segments, and splitting style.

➤ To open the *Advanced – Splitting* page of the Flip Chip Route form, choose *Route – Flip Chip – Flip Chip Route*, click the *Advanced* tab, then select *Splitting*.



Flip Chip Route – Advanced – Splitting Fields and Options

Width Limit

If selected, the width of each wire after the split is less than the specified limit. If deselected, the values in the LAYER statement of the LEF file determine the width of the split wires. If LAYER rules are not specified, no splitting occurs. This is the default.

Gap Between Split Segments

If selected, the distance between split wire segments must be greater than the specified value. If deselected, the distance between split wire segments is the default minimum spacing value that does not cause DRC violations.

Splitting Style

The splitting style options specify the interleaving style used for the split wires.

River

If the River style is selected, the split wires do not have an interleaving pattern. This is the default. The following illustration shows the pattern for the split wires.

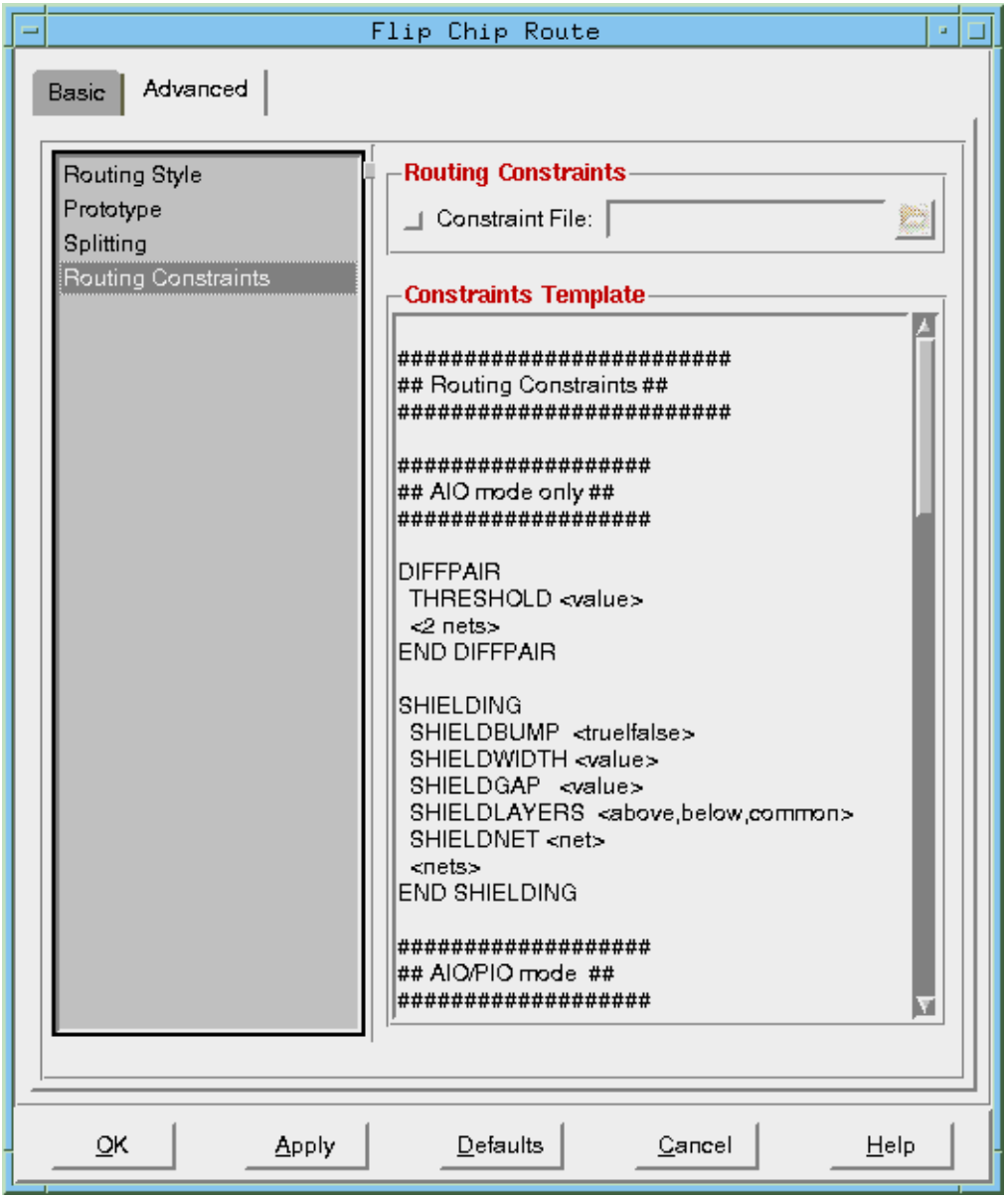
Mesh

If the mesh style is selected, the split wires interleave with one another, as shown in the following illustration:

Flip Chip Route – Advanced – Routing Constraints

Use the *Advanced – Routing Constraints* page of the Flip Chip Route form to specify options for the width limit, gap between split segments, and splitting style.

➤ To open the *Advanced – Routing Constraints* page of the Flip Chip Route form, choose *Route – Flip Chip – Flip Chip Route*, click the *Advanced* tab, then select *Routing Constraints*.



Flip Chip Route – Advanced – Routing Constraints Fields and Options

Constraint File

If selected, the specified file contains the names of the nets that are to have differential routing. If deselected and if no differential pairs are defined in the PROPERTY statement of the DEF file, differential routing is not done.

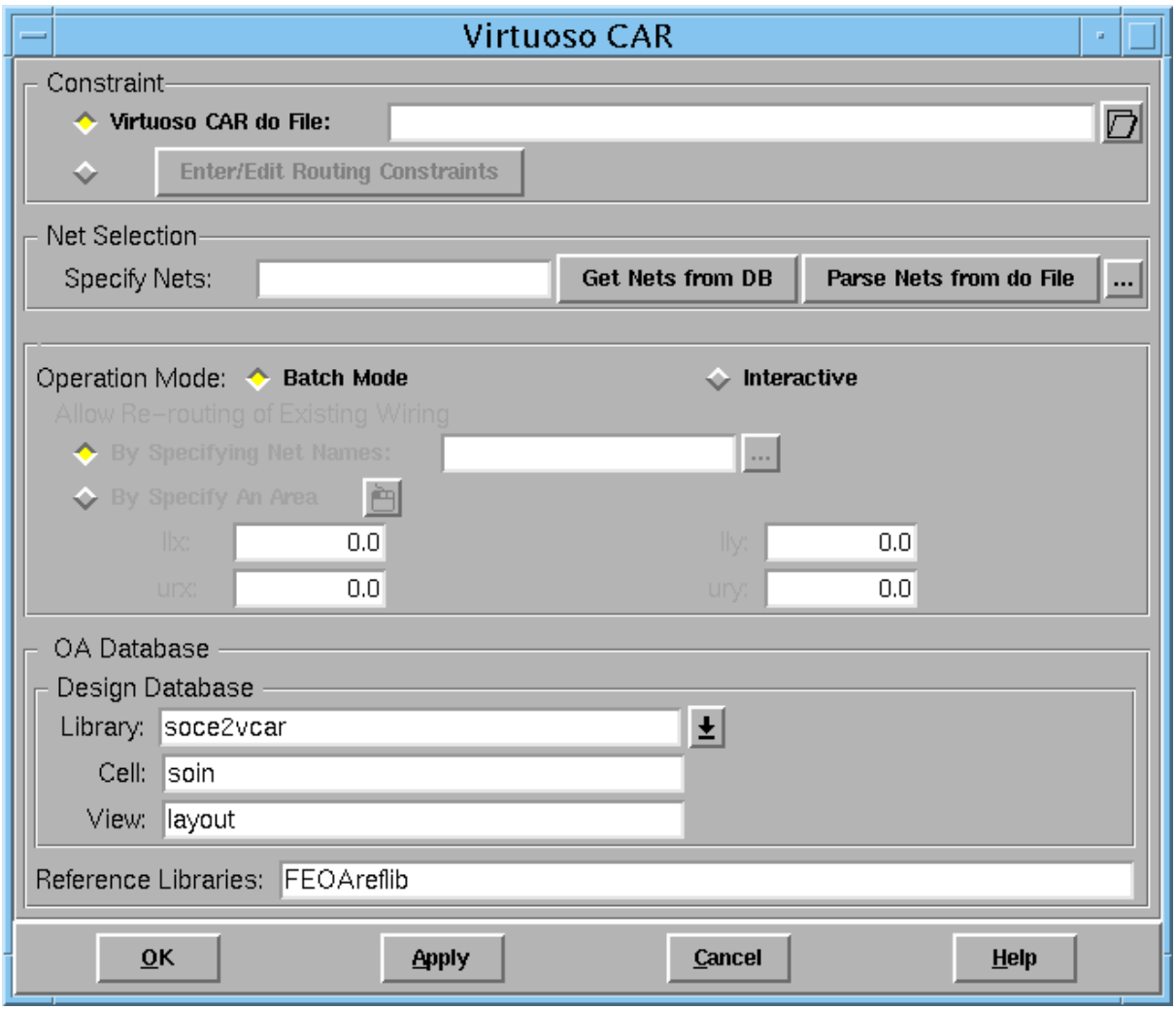
Constraints Template

Provides the list of routing constraints.

Virtuoso CAR Interface

Use the Virtuoso CAR form to place a set of nets into the Virtuoso CAR environment, where you can use the router's editing features.

➤ Choose Route – *Virtuoso CAR Interface.*



Virtuoso CAR Fields and Options

Virtuoso CAR do File:

Specifies a `.do` file for the router. If you are running in batch mode and do not specify a `.do` file, the router automatically generates a default `.do` file.

The following statements are in the default `.do` file:

```
set rotate_via off
groute 4
route 25
protect all wires
save_oa export
quit
```

If you create your own `.do` file, include the following statement before any routing commands:

```
set rotate_via off
```

If you create your own `.do` file, include the following statement after all routing commands:

```
protect all wires
```

Enter/Edit Routing Constraints

Displays the Mixed Signal Constraint Editor form.

Specify Nets:

Lists the nets to route. If you specified a `.do` file, the router can parse the nets from the file. You do not have to specify nets one by one.

Nets that are not listed are not passed to the router. Since the router does not recognize them, they cannot be selected or routed.

You can use the *Browse* (*...*) button to bring all the net names to an editing window for modification. If you specify additional nets, they are not written to the `.do` file.

Get Nets from DB

If you routed the design previously or if you entered the net names using the route constraint editor, gets nets from the database and populates the *Specify Nets* text box with the net names without running the router.

Parse Nets from do File

Writes nets to the database without running the router if the `.do` file is specified.

Operation Mode

The mode in which the router runs. Select one of the following:

Batch Mode

Performs the actions specified in the `.do` file. See Running the chip assembly router in Batch Mode for more information.

Interactive

Transfers the design from the Encounter environment into the Virtuoso CAR environment, where you can use the router editing features. This mode is asynchronous, and does not wait for the router to complete. See Running chip assembly router in Interactive Mode for more information.

Allow Re-routing of Existing Wiring

Specifies the nets that can be changed or rerouted.

By Specifying Net Names:

Lists the nets that can be changed or rerouted.

By Specifying an Area

Lets you use the mouse to select an area. Nets in the selected area can be changed or rerouted.

Design Database

Provides information to the router regarding the location of required elements. Specify the following:

Library

The design library to use. The library is created if it does not already exist.

Cell

The name of the cell to import.

View

A view name that identifies the design that you are importing.

Nets to be routed

Names of all nets to route with the chip assembly router. Nets that are not named are not passed to the chip assembly router. Since the chip assembly router does not recognize them, they cannot be selected or routed in the chip assembly router environment.

You can use bus names and wildcards in this field. For example, if the design has a bus S1[0:7], enter S1 in this field. This passes bus S1[0:7] to the chip assembly router for editing. To route nets named `clk1` and `clk2` in the chip assembly router environment, specify `cl*`.

Note: If you use the *Specify Route Area* option, the nets within the selected area are used, and you do not need to enter any net names in this field.

Caution

Do not use a wildcard to select all nets.

Although the chip assembly router provides greater routing flexibility, it has lower capacity limits than other Encounter components.

Specify Route Area

Allows you to use the mouse to select an area.

When you click the Mouse widget, the cursor changes to a cross, allowing you to drag the mouse within the design display area to indicate the portion of the design to be routed in the chip assembly router.

When you release the mouse button, the coordinates for the area automatically populate the form. Nets within the specified area are added to the list of nets available for editing in the chip assembly router.

Note: This option is only available in *Interactive* mode.

Reference Libraries

Specifies the OA reference libraries. If you specified reference libraries on the Design Import – Basic form, this field already contains those library names. You can create reference libraries using the `lef2oa` command.

Related Topics

For information on the following topics, see “Wire Editing” in the *Encounter User Guide*.

- Running the Chip Assembly Router in Batch Mode
- Running the Chip Assembly Router in Interactive Mode

Related Text Commands

- `runCCAR`

WRoute

The *Route* menu's WRoute form enables you to route placed signal and clock nets in block-and-cell designs using an area-based algorithm. You can customize the routing process by specifying basic and advanced options.

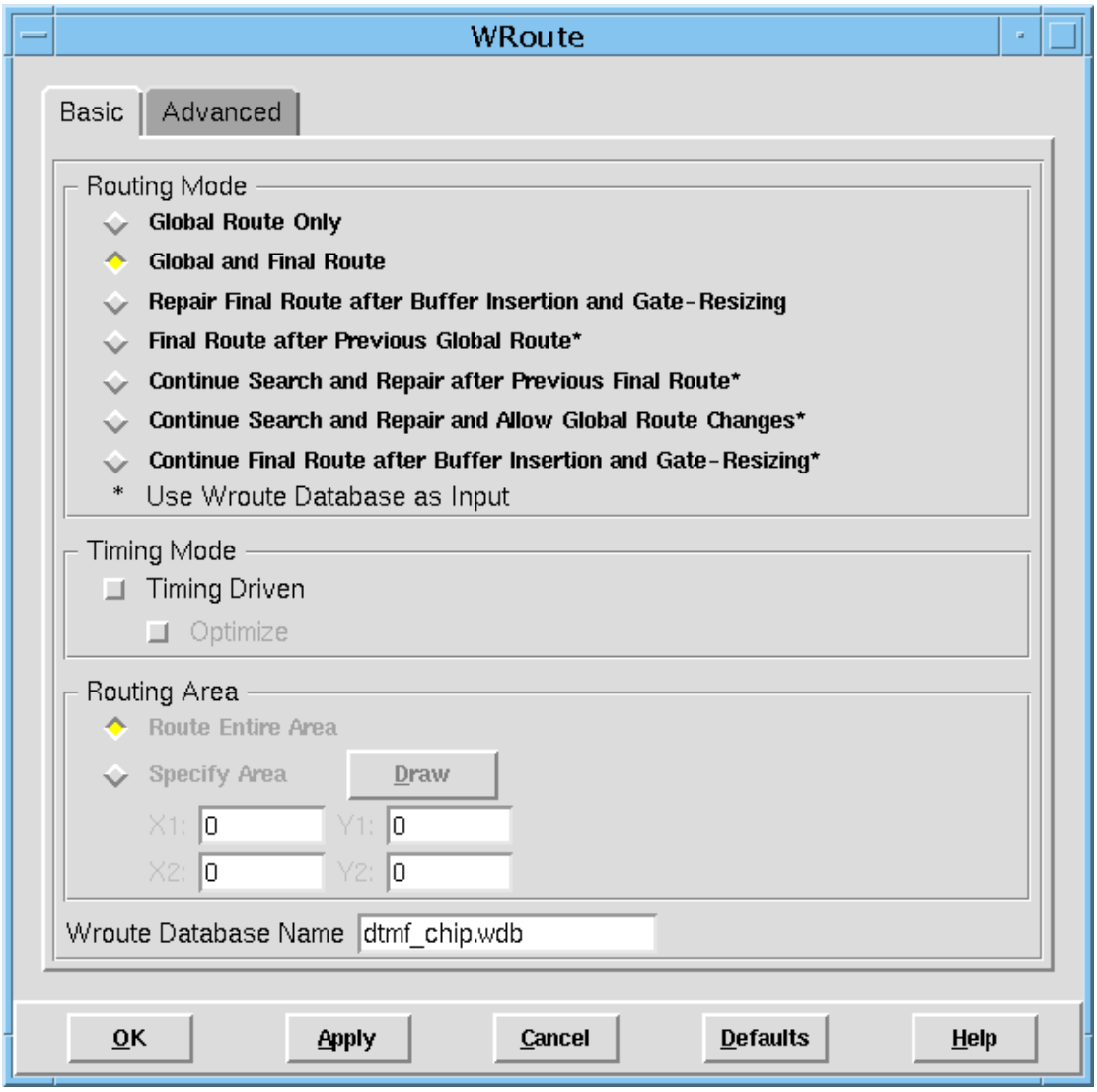
The WRoute form contains the following pages:

- WRoute – Basic on page 1274
- WRoute – Advanced on page 1280

WRoute – Basic

Use the *Basic* page of the WRoute form to specify the routing mode, the routing area, and the database to use when running any of the incremental routing options.

➤ Choose *Route – WRoute*, then click the *Basic* tab.



WRoute – Basic Fields and Options

Routing Mode

Global Route Only

Runs global routing.

During global routing, the router interconnects the regular (signal) nets defined in the NETS section of the DEF file for the design, based on the availability of routing tracks. It finds generalized pathways, without laying down actual wires, and makes iterative passes to optimize the global routing, shorten wire length, and minimize the use of vias.

Global and Final Route

Runs global and detailed routing. This is the default *Routing Mode*.

During detailed routing, the router follows the global routing plan and lays down actual wires that connect the pins to their corresponding nets. The primary goal of detailed routing is to complete all of the required interconnects without creating shorts or spacing violations. Unlike the global router, however, the detailed router is not conservative. It will create shorts or spacing violations rather than leave unconnected nets.

Detailed routing stops automatically if it exceeds the time limit you set for routing or if it cannot make further progress on routing the design.

Repair Final Route after Buffer Insertion and Gate-Resizing

Reruns both global and detailed routing during postroute optimization. Makes the router more error tolerant by allowing it to delete problematic nets, such as nets with loops and nets for which it cannot extract connectivity.

Final Route after Previous Global Route

Runs detailed routing on a database that has already had at least one global routing pass.

If you select this option, you must also specify a database name in the *Wroute Database Name* text field.

Continue Search and Repair after Previous Final Route

Runs the search-and-repair step on a previously routed database.

During search and repair, the router rips up routes with violations and reroutes them. This option does not run global routing. This option is useful when the previous detailed routing exceeded the time limit you set before removing all violations.

If you select this option, you must also specify a database name in the *Wroute Database Name* text field.

Continue Search and Repair and Allow Global Route Changes

Runs both global and detailed routing, including the search-and-repair step, on a previously routed database. This option is useful if your previous detailed route had difficulty removing all violations.

If you select this option, you must also specify a database name in the *Wroute Database Name* text field.

Continue Final Route after Buffer Insertion and Gate-Resizing

Reads the netlist and routing from the existing routed database (`.wdb`), then updates WRoute's connectivity from the data in the Encounter software, ignoring any routing in the data. The router then incrementally corrects any routing violations and routes any new nets.

This is typically used when gate-resizing buffer insertion and deletion is done during postroute repair for timing or signal integrity violations.

Note: Any routing changes done manually are lost if they were not in the original database from a previous routing run.

If you select this option, you must also specify a database name in the *Wroute Database Name* text field.

Timing Mode

Timing Driven

Performs timing-driven routing. In this mode, the router routes nets based on their timing criticality. It routes the most timing critical nets first, to achieve the shortest routes. The router considers layer RC values for routing timing critical nets.

You can choose timing-driven routing if you select either the *Global Route Only* or *Global and Final Route* options. When selected with *Global Route Only*, the Encounter software runs PKS-based global route and saves the results in the database.

When selected with *Global and Final Route*, the Encounter software runs PKS-based global route, saves the results to the database, then runs WRoute for final routing.

Note: If you perform timing-driven routing and optimization with the *Global Route Only* option, you must then run final routing (*Final Route after Previous Global Route*) to finish the route. If you decide to perform final routing in a new session in Encounter software, you must use the `restoreDesign` command (or the Restore Design form) to load the correct routing data into the design. This data can be found in the top module design file `top_tdr.enc.dat`.

Optimize

When selected with *Global Route Only*, runs PKS-based global route, PKS-based optimization, then PKS-based global route again, and saves the results in the database.

When selected with *Global and Final Route*, runs the same procedures as described above, then runs WRoute for final routing.

Routing Area

Route Entire Area

Routes the regular nets in the entire core area of the design. This is the default *Routing Area*.

Specify Area

Routes nets in the area you specify when you draw the area in the design display area or fill in the *X* and *Y* text entry boxes.

Wroute Database Name

Specifies the database to use when you run any of the incremental routing options (*Final Route after Previous Global Route, Continue Search and Repair after Previous Final Route*, *Continue Search and Repair and Allow Global Route Changes*, or *Continue Final Route after Buffer Insertion and Gate-Resizing*).

You must use the same name for the database during incremental routing as was used when the database was created.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

WRoute – Advanced

The *Advanced* page of the WRoute form enables you to specify advanced options, such as job control, net options, and pin access.

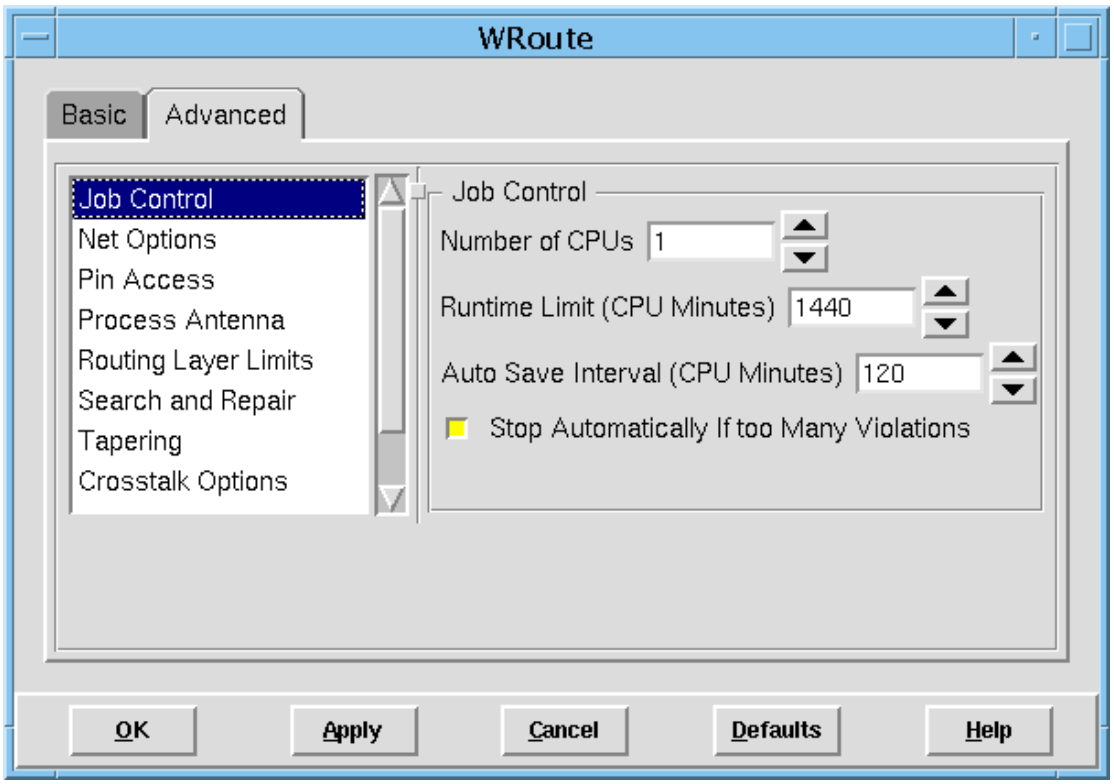
The Advanced page contains the following subpages:

- Job Control on page 1281
- Net Options on page 1283
- Pin Access on page 1286
- Process Antenna on page 1288
- Routing Layer Limits on page 1291
- Search and Repair on page 1293
- Tapering on page 1295
- Crosstalk Options on page 1297
- Route Optimization on page 1301
- Expert Options on page 1303

Job Control

Use the *Job Control* page of the WRoute form to specify the number of CPUs to use, the run-time minutes, the interval between saving the routing database, and whether to stop routing a difficult design if the router is not making progress.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Job Control*.



Job Control Fields and Options

Number of CPUs

Specifies the number of processors in a single workstation to use for multi-thread routing. WRoute can use up to 4 processors during global routing and 16 processors during detailed routing. If you enter a number greater than 16, or if you do not have the appropriate number of available Route Accelerator licenses, the router displays a warning message and resets the number of processors to the highest available number.
Default: 1

Runtime Limit (CPU Minutes)

The value of this option specifies the maximum run time for the router. This option is useful when you want to ensure that the router stops after a specified amount of time. For example, you can set a run-time limit to see whether the design is easily routable without waiting for optimization to run.
Default: `1440`

Auto Save Interval (CPU Minutes)

Specifies the interval for saving the routing data to disk.
Default: `120`

Stop Automatically If too Many Violations

Specifies that the router stops if it detects too many violations and cannot complete routing.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

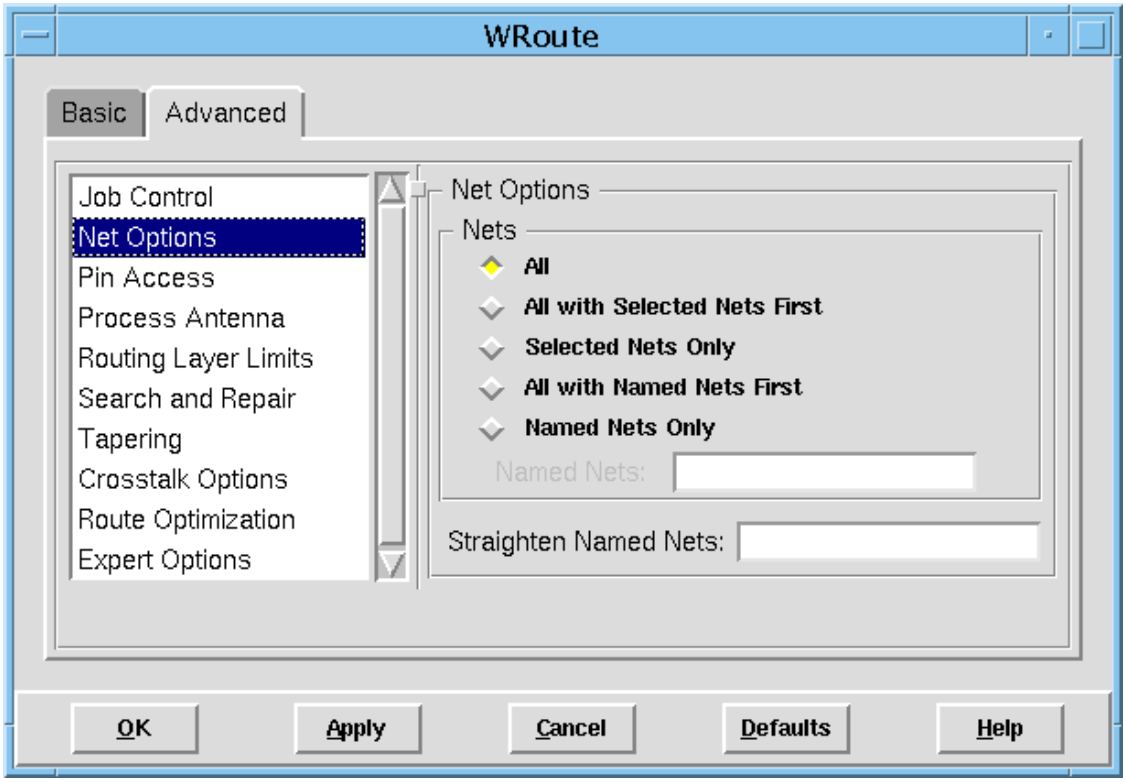
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Net Options

Use the *Net Options* page of the WRoute form to specify which nets to route and which nets to reroute as straight as possible.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Net Options*.



Net Options Fields and Options

All Routes all the regular nets in the design. This is the default.

All with Selected Nets First

Routes selected nets before routing the rest of the design and fixes the location of the routed nets so that the routing is not changed, unless you select *Allow Modification of Prerouted Nets* on the *Search and Repair* panel.

Note: To speed up routing, the router might route all nets in one detailed routing pass, even if you identify specific nets to route first. The router keeps the specified nets as straight as possible during the detailed routing pass.

Selected Nets Only Routes only the nets you select in the design display area.

All with Named Nets First

Routes the nets you specify in *Named Nets* before routing the rest of the design. Also fixes the location of the routed nets, so that the routing is not changed, unless you select *Allow Modification of Prerouted Nets* on the *Search and Repair* panel.

Named Nets Only Routes only the nets you specify in *Named Nets*.

Named Nets Specifies the nets to route. This option is only available if *All with Named Nets First* or *Named Nets Only* is selected. You can specify nets using the following methods:

~	Routes all nets *except* the specified nets.
netName	Specifies the name of a net to route.
"list_of_nets"	

Lists the DEF names of the nets to route. The list has a 4,000-character limit. Enclose the list in quotation marks. Use the following to specify multiple nets:

- `"@clock"` selects all nets marked with `+ USE CLOCK`.
- `"@subnet"` selects all nets with subnets.
- `"@rule"` selects all nets using a nondefault rule.
- `"@rule:rulename"` selects all nets using the specified nondefault rule (rulename).
- `"@shield"` selects all shielded nets.
- `"@power"` selects all nets marked with `+ USE POWER`.
- `"@ground"` selects all nets marked with `+ USE GROUND`.

"< filename" Specifies a file that contains the list of names of all the nets to route, with one name on each line. You *cannot* use regular expressions with the <.

Straighten Named Nets Deletes specified nets in a fully routed design and reroutes them as straight as possible.

Related Text Commands

- `wroute`

For more information, see "Route Commands" in the *Encounter Text Command Reference*.

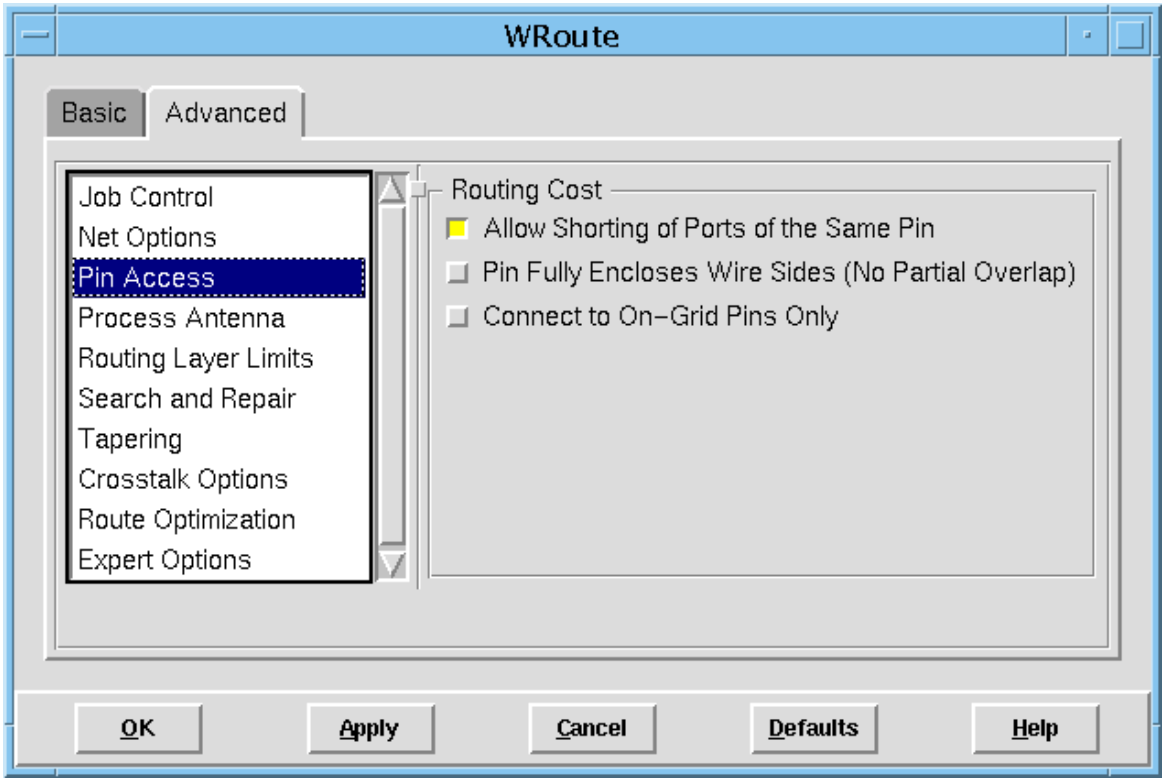
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Pin Access

Use the *Pin Access* page of the WRoute form to specify pin connection choices.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Pin Access*.



Pin Access Fields and Options

Allow Shorting of Ports of the Same Pin

Allows WRoute to short different ports of the same pin.

Pin Fully Encloses Wire Sides (No Partial Overlap)

Forces WRoute to connect to a pin if the pin encloses a wire, or connect to the center of a wire if the wire is wider than the pin.

Connect to On-Grid Pins Only

Forces WRoute to route to on-grid geometries of the port only. Select this option when all the design components are on-grid and the router will not route off-grid.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

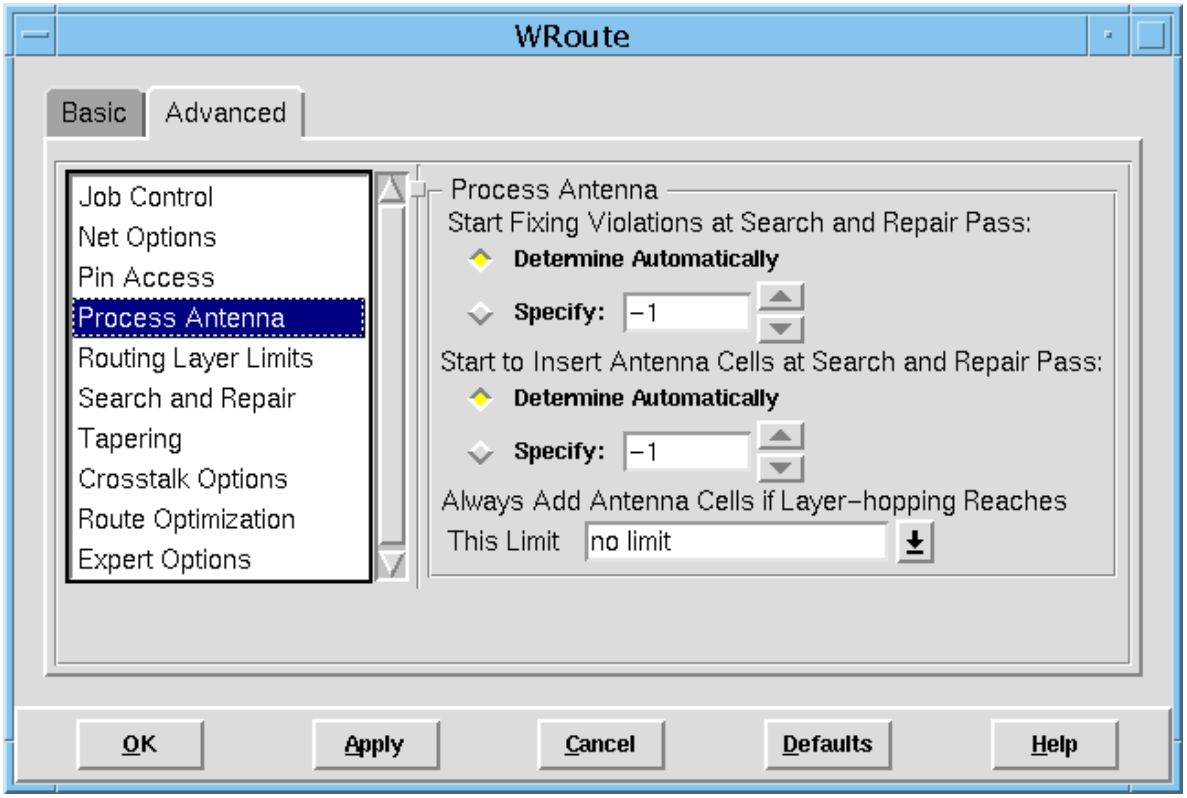
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Process Antenna

Use the *Process Antenna* page of the WRoute form to specify when and how to repair process antenna violations.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Process Antenna*.



Process Antenna Fields and Options

Start Fixing Violations at Search and Repair Pass

Determines when to start repairing process antenna violations by layer hopping.

Determine Automatically

Checks and repairs process antenna violations during search-and-repair routing by automatically shortening any wire whose area exceeds the gate/wire area ratio set in the LEF file. This option does not guarantee that the router will resolve all antenna violations. If the routing area is congested, process antenna violations can still occur, just as shorts and spacing violations can occur. By default, WRoute determines when to start repairing process antenna violations.

Specify

Enables you to specify the search-and-repair pass at which the router starts repairing process antenna violations by shortening wires.

To disable process antenna checking, specify `0`.

Start to Insert Antenna Cells at Search and Repair Pass

Determines when to start repairing process antenna violations by inserting antenna diode cells.

Determine Automatically

Adds antenna diode cells to repair process antenna violations at or after the specified search-and-repair pass. Generally, the router attempts to fix process antenna violations by shortening wires before it starts to insert antenna cells.

Specify

Enables you to specify the search-and-repair pass at which the router starts inserting antenna diode cells.

To disable antenna cell insertion, specify `0`.

Important

Do not change the setting for this option unless you want to disable the antenna check.

Always Add Antenna Cells if Layer-hopping Reaches This Limit

Ensures that WRoute adds antenna diode cells when it reaches a specified layer.

With this option, WRoute starts adding antenna diode cells if process antenna violations remain after layer hopping reaches the specified layer. Use this option to minimize congestion. For example, in a design with six or more layers, if you set the value of this option to `4`, WRoute attempts to repair antenna violations by layer hopping until it reaches *metal4*. Then it starts repairing the violations by adding antenna diode cells.

By default, this option is set to `no limit`.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

Related Topics

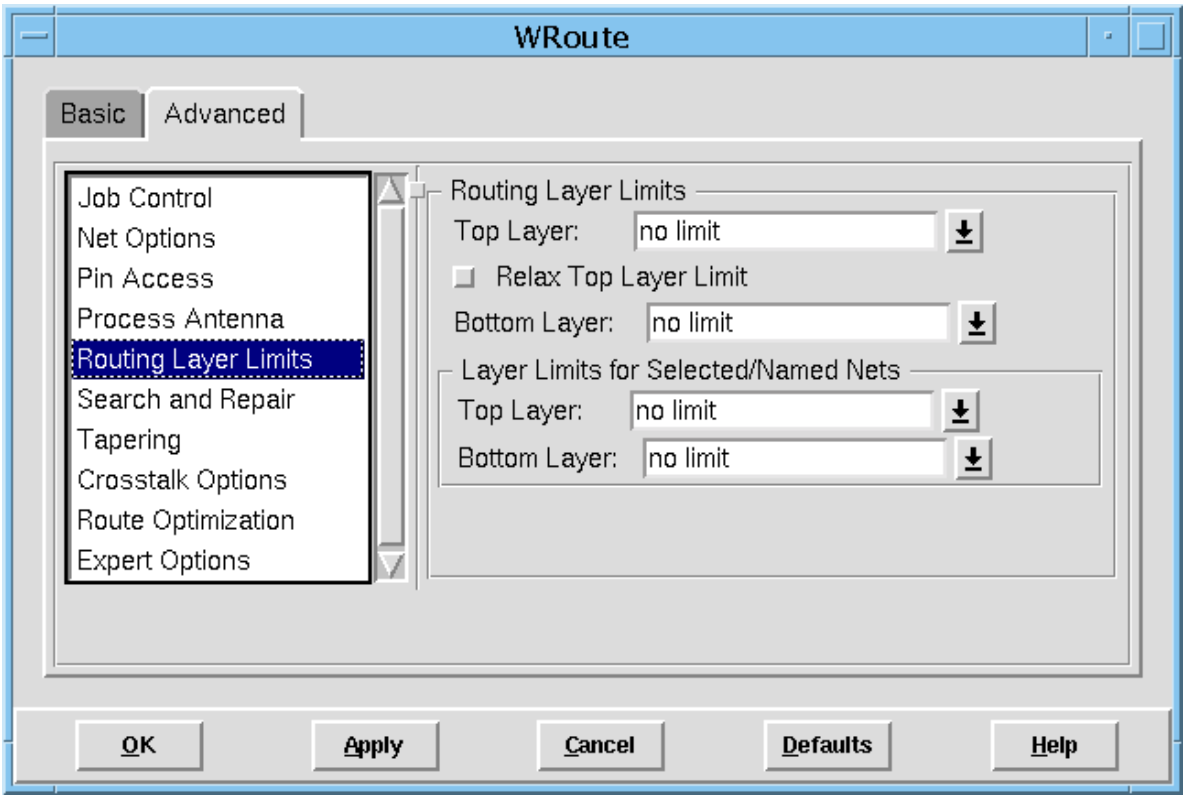
For more information on using WRoute, see the *Ultra Router Reference*.

Routing Layer Limits

Use the *Routing Layer Limits* page of the WRoute form to set layer limits on routing.

By default, WRoute does not set layer limits on routing. You can override WRoute's default behavior by setting limits for the top or bottom routing layer, or limits on routing selected nets.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Routing Layer Limits*.



Routing Layer Limits Fields and Options

Top Layer

Limits the top routing layer for all signal nets to the layer you specify. This option is useful if you want to reserve the top routing layers for power or ground or other special net routing.

Relax Top Layer Limit

Allows routing on layers higher than the one specified by *Top Layer*. When you select this option, the router might route to a layer higher than the one set by *Top Layer*, but at a high cost.

Bottom Layer Allows routing below the specified layer, but at a very high cost. Use this option to limit the wire length below the specified layer.

Layer Limits for Selected/Named Nets

Specifies layer limits for selected nets. You can specify values for the *Top Layer*, the *Bottom Layer*, or both.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

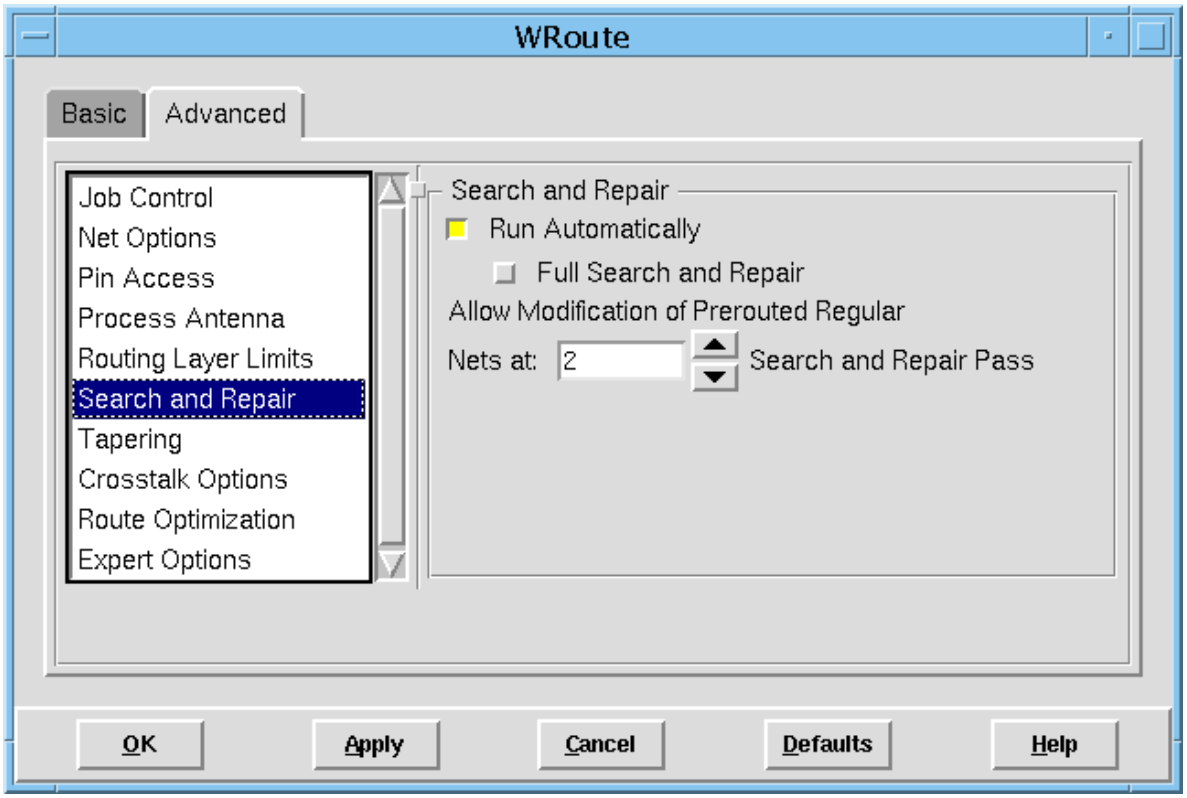
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Search and Repair

Use the *Search and Repair* page of the WRoute form to specify search-and-repair routing options.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Search and Repair*.



Search and Repair Fields and Options

Run Automatically

Runs search-and-repair routing after the initial detailed routing. During search and repair, the router creates switch boxes centered on design rule violations, then reroutes each switch box to eliminate the violation. Sometimes there are more violations after search and repair, but usually the new violations are easier to fix. Search and repair propagates shorts toward less congested parts of the design by replacing difficult shorts with others on the boundaries of switch boxes, where they are easier to resolve.
Default: On (Selected)

Full Search and Repair

Runs full search-and-repair routing. By default, WRoute runs search-and-repair routing in quick mode, by turning off certain time consuming options and limiting the number of search-and-repair passes.
Default: Off

Allow Modification of Prerouted Regular Nets at Search and Repair Pass

Specifies the search-and-repair pass at which the router can begin modifying prerouted regular nets. The router does not modify nets whose location is fixed.
Default: 2

Select this option to prevent the router from modifying preroutes unless absolutely necessary. The router might modify partially prerouted nets if required to complete the routing, but it will not modify fully prerouted nets that are marked as `FIXED`.

To fix the locations of the prerouted nets, do one of the following:

- Specify `0` for this option.
- Mark the nets `FIXED` in the `NETS` section of the DEF file.
- Put regular nets in the `SPECIALNETS` section of the DEF file. WRoute does not touch nets in the `SPECIALNETS` section.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

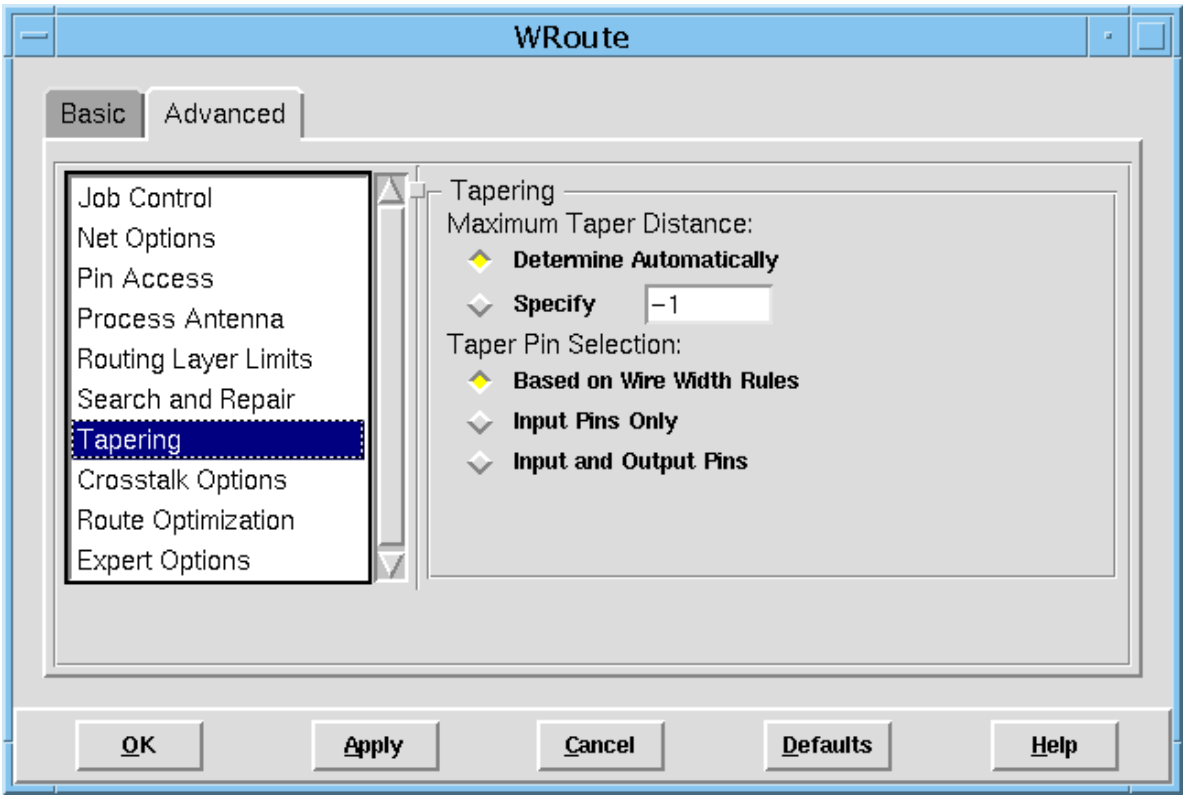
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Tapering

Use the *Tapering* page of the WRoute form to specify wire tapering options.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Tapering*.



Tapering Fields and Options

Determine Automatically

Sets the maximum tapering distance, starting from the bounding box of a pin, in microns. By default, WRoute determines the maximum taper distance automatically.

This option sets the maximum distance for tapering—it does not force the router to taper pins. Do not change the value of this option unless you want to disable automatic tapering.

Specify

Enables you to specify the maximum tapering distance. To disable tapering, specify `0`.

Based on Wire Width Rules

Tapers wires based on the nondefault spacing rules defined in the technology library. You can specify several wire widths and associate special wire spacing with the widths.

- If the spacing associated with a wide wire is the same as for a regular wire, the router assumes that the wire is widened to avoid wire self-heat effects. In this case, the router tapers wide wires at input pins. (The behavior is like *Input Pins Only*.)
- If the spacing associated with a wide wire is larger than for a regular wire, the router assumes that the wider spacing is used to control crosstalk effects. In this case, the router tapers wires at all pins where violations occur. (The behavior is like *Input and Output Pins*.)

Input Pins Only Tapers wires at input pins if violations occur. Does not taper wide wires at the output or I/O pins.

Input and Output Pins Tapers wires at all pins where violations occur.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

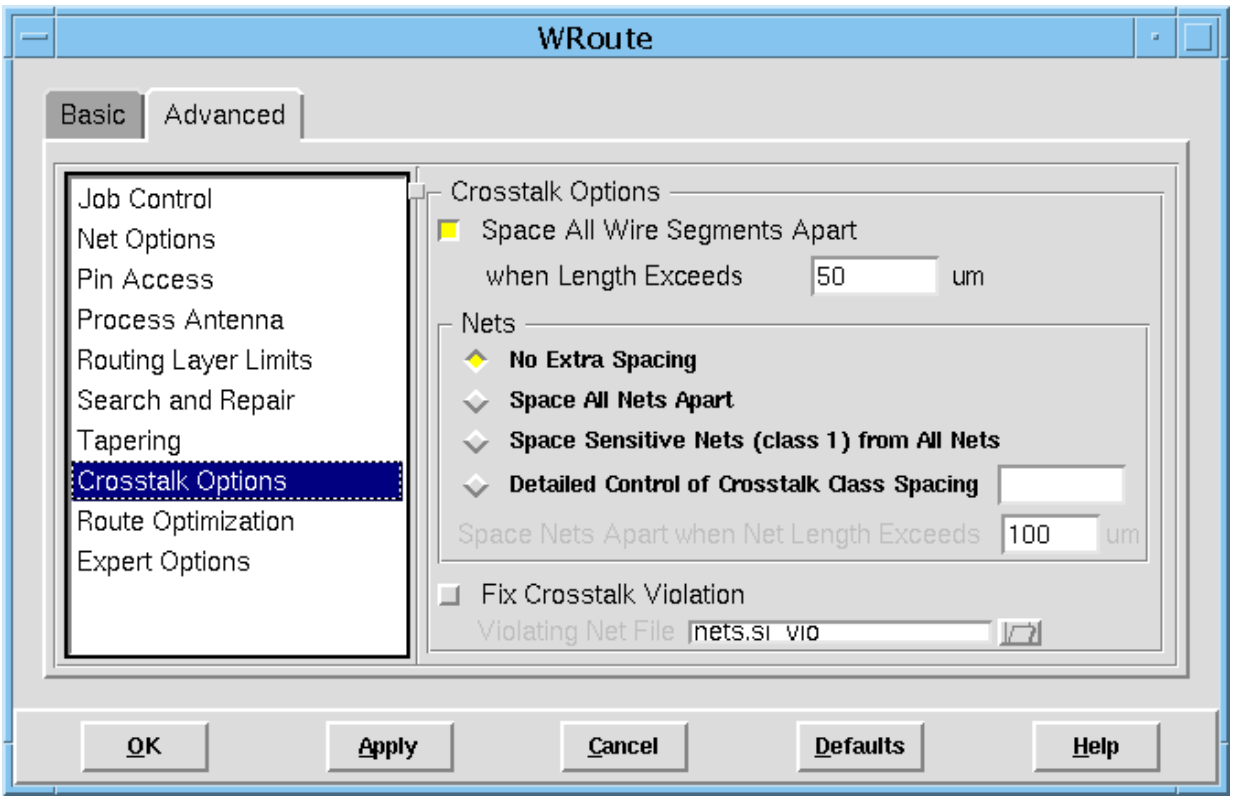
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Crosstalk Options

Use the *Crosstalk Options* page of the WRoute form to specify options for avoiding and correcting crosstalk.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Crosstalk Options*.



Crosstalk Options Fields and Options

Crosstalk Options

Space All Wire Segments Apart when Length Exceeds

Specifies the maximum allowable length, in microns, for parallel wire segments. If the router finds parallel wire segments that exceed the specified length, it attempts to space out the wires by one additional track within a global routing cell (gcell) to avoid crosstalk. If the gcell does not have enough room, the router completes the routing without the additional spacing. To disable this option, specify `0`.
Default: `50`

Nets

No Extra Spacing

Does not add extra spacing between regular nets. This is the default value for this option.

Space All Nets Apart

Minimizes crosstalk by adding spacing between all regular nets.

Space Sensitive Nets (class1) from All Nets

Minimizes crosstalk between regular nets with `+ XTALK 1` specified in the DEF file and other nets by adding spacing. Use this option to specify a set of nets that are crosstalk sensitive and give them extra spacing.

Detailed Control of Crosstalk Class Spacing

Specifies detailed interaction rules for crosstalk classes. Class interactions are symmetric. For example, if `class_a` repels `class_b`, then `class_b` repels `class_a`. Class interactions might add slight routing penalties to your design.

The rules apply to regular and special wires, but not to pins or obstructions.

Note: To use interaction rules, you must specify `+ XTALK class` as a net attribute in your DEF file. The default class for any net without a class number is `0`.

To specify a rule, type the rule into the text entry box, using the following syntax:

- `class` specifies the crosstalk class.

Note: If the class is `0` (the default), `XTALK` will not be written to the DEF file.

- `"` specifies the beginning or the end of the string that defines the class interaction rule.
- `+` specifies repulsion. This is the class interaction operator.
- `|` separates the classes.
- `,` separates class groups.

Example Rule `"1|2|3+2|3, 4+0"`

In the example,

- Nets in classes 1, 2, and 3 repel nets in classes 2 and 3.
- Nets in classes 2 and 3 repel nets in classes 1, 2, and 3.
- Nets in class 4 repel nets in class 0.
- Nets in class 0 repel nets in class 4.

Space Nets Apart when Net Length Exceeds

Specifies a wire-length threshold to apply to the class interaction rules. The default is 100 µm. This option is not available when you select *No Extra Spacing*.

- WRoute considers nets whose estimated wire length after global routing is equal to or greater than the threshold as active nets for class interaction.
- WRoute considers nets whose estimated wire length after global routing is less than the threshold as inactive nets and removes their class assignments.

Note: To use this option, you must specify `+ XTALK` *`class`* as a net attribute in your DEF file. The default class for any net without a class number is `0`.

Fix Crosstalk Violation

Repairs crosstalk violations after routing. WRoute repairs these violations by pushing adjacent routing aside.

Use this option on a fully routed database during detailed routing only. This option takes the WRoute database and the list of nets with crosstalk problems specified in the *Violating Net File* text entry box as input.

Violating Net File

Specifies a file that contains a list of nets with crosstalk problems. The list can be generated by the CeltIC™ crosstalk analyzer or another crosstalk analyzer.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

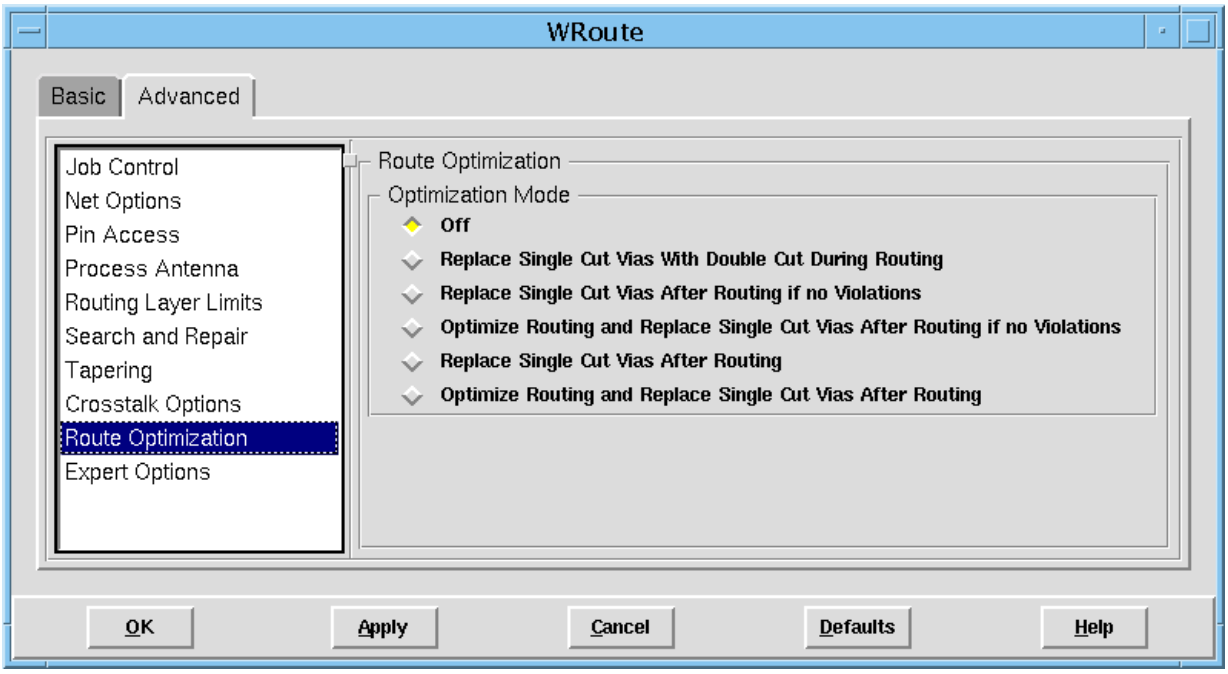
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Route Optimization

Use the *Route Optimization* page of the WRoute form to specify whether and how to minimize wire length and the number of vias.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Route Optimization*.



Route Optimization Fields and Options

Off
Does not minimize wire length and the number of vias.

Replace Single Cut Vias With Double Cut During Routing
Replaces single-cut vias with double-cut vias during both the initial and search-and-repair phases of final routing. Wroute attempts the replacement even if the design has violations.

Replace Single Cut Vias After Routing if no Violations
Replaces single-cut vias with double-cut vias after detailed routing is complete and violation free.

Optimize Routing and Replace Single Cut Vias After Routing if no Violations

Minimizes wire length and the number of vias after detailed routing is complete and violation free. During routing optimization, WRoute attempts to remove extra vias by jogging wires in the nonpreferred direction. This blocks tracks but does not cause problems because routing is already complete.

Optimizing the design takes approximately the same amount of time as the initial detailed routing pass and should decrease the wire length and number of vias by a few percent. By default, this option is not selected.

Note: If you select this option, WRoute does not attempt to repair process antenna violations until after optimization.

Important

Do not select this option if your design has design rule violations. If you do, the router does not optimize the design.

Replace Single Cut Vias After Routing

Replaces single-cut vias with double-cut vias after detailed routing is complete, even if the design has violations.

Optimize Routing and Replace Single Cut Vias After Routing

Minimizes wire length and the number of vias after detailed routing is complete, even if the design has violations.

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

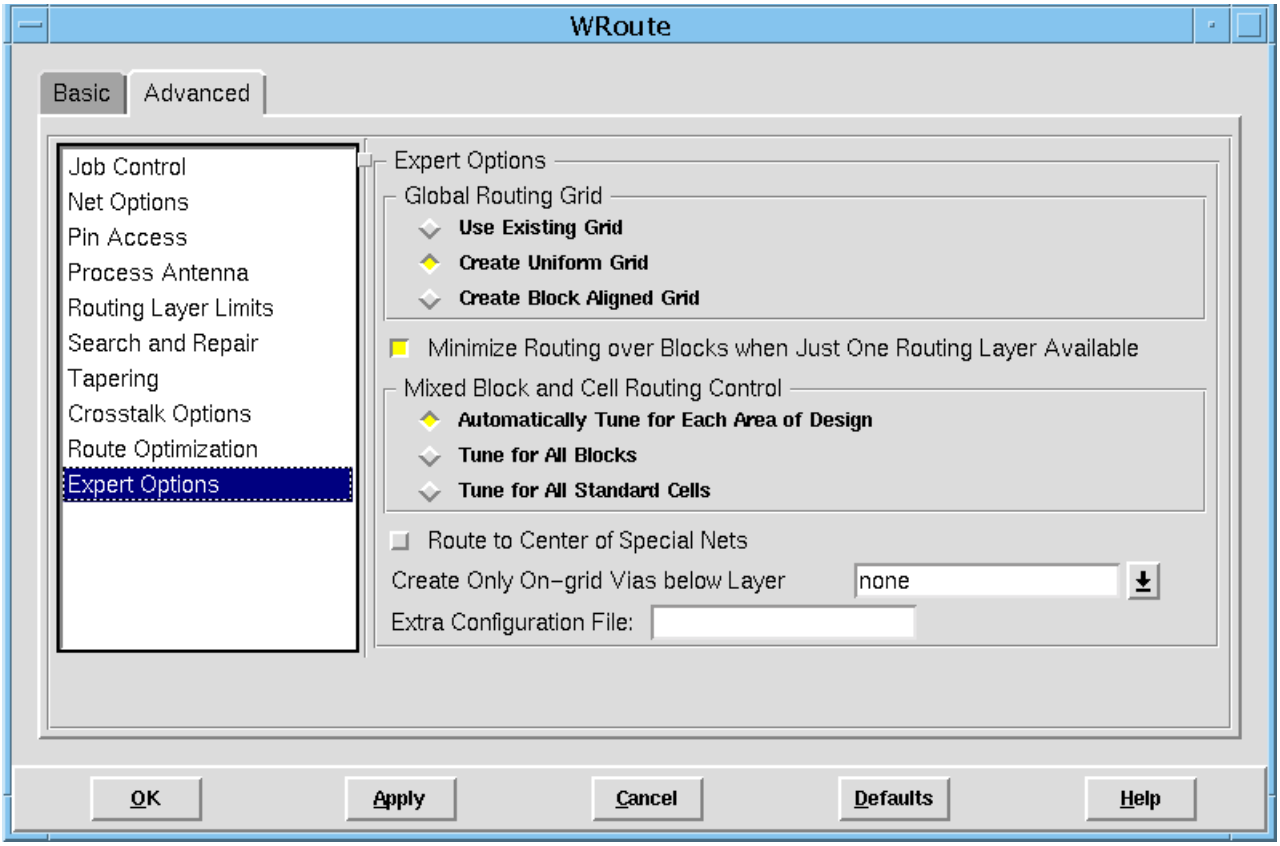
Related Topics

For more information on using WRoute, see the *Ultra Router Reference*.

Expert Options

Use the *Expert Options* page of the WRoute form to specify various advanced routing functions.

➤ Choose *Route – WRoute*, click the *Advanced* tab, and select *Expert Options*.



Expert Options Fields and Options

Global Routing Grid

Use Existing Grid

Uses the global routing grid defined in the DEF file.

Create Uniform Grid

Generates a uniform global routing grid. This is the default value for this option.

Create Block Aligned Grid

Generates a global routing grid that aligns with the channels and macro block boundaries in your design. This option improves routing quality for block-based designs because, by aligning the grids, the global router can route more effectively in empty gcells in the channel area.

Minimize Routing over Blocks when Just One Routing Layer Available

Penalizes routing over blocks. Routing on one layer increases the possibility that wires will cross. Selecting this option might help routing if your design meets the following three conditions:

1. Violations that are generated when this option is *not* selected are on top of the blocks.
2. Only one routing layer is on top of the blocks.

Routing resources are available between the blocks.

Mixed Block and Cell Routing Control

Automatically Tune for Each Area of Design

Lets the router determine when to route in chip-assembly mode, depending on the percentage of the design area that is covered by blocks, rings, or pads. This is the default value for this option.

Tune for All Blocks

Routes in chip-assembly mode only. In chip-assembly mode, the router runs an order of magnitude faster than in non-chip-assembly mode at the expense of slightly degraded routing quality.

Tune for All Standard Cells

Routes in non-chip-assembly mode only.

Route to Center of Special Nets

Forces connections to the center of wide stripes. This option forces the router to connect tie-high nets and tie-low nets to stripes, not to power or ground pins.

Create Only On-grid Vias below Layer

Permits on-grid vias below the specified routing layer. By default, no on-grid vias are permitted.

Extra Configuration File

Specifies an additional configuration file for routing. You can use the additional configuration file to set WRoute options that are not available within the Encounter software. If there is a discrepancy between an option that is set in the Encounter GUI and an option that is set in the extra configuration file, WRoute uses the value of the option in the extra configuration file

Related Text Commands

- `wroute`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

Related Topics

- For more information on using WRoute, see the *Ultra Router Reference*.

Generate Routing Guide

Generates a routing guide file to use with Trial Route. When you select *Generate Routing Guide* from the Route menu, the Routing Guide File form enables you generate a routing guide file

Routing Guide File

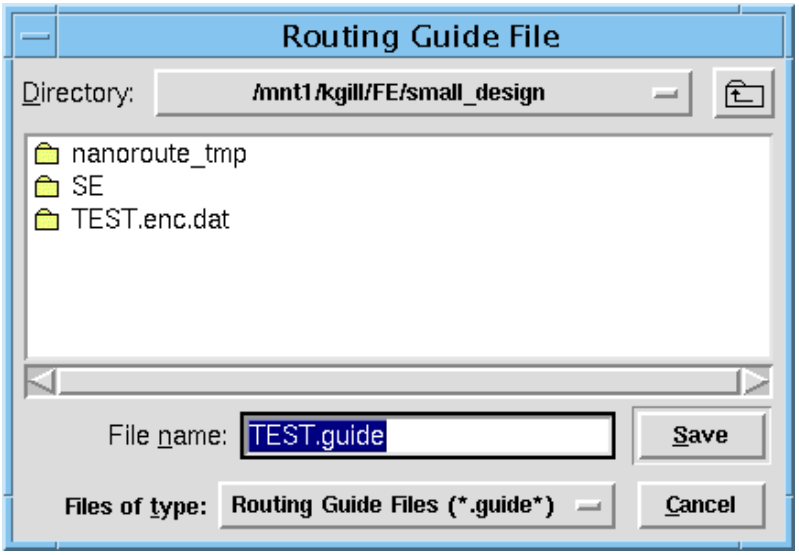
Use the Routing Guide File form to generate a routing guide file to use with Trial Route. Routing guide files help control the routing topology by creating regions in which Trial Route can create wires.

Routing guide files contain the following wire information: the coordinates of the wire ends, whether it is a horizontal or vertical wire, the width of the wire, and the layer number. The following example shows a section of a routing guide file:

```
routeGuideNet clk
wire 32.89 50 32.89 45.715 V 0.5 L 3
wire 32.89 45.715 32.89 10.045 V 0.5 L 5
wire 32.89 45.715 43.47 45.715 H 0.5 L 4
wire 32.89 10.045 7.13 10.045 H 0.5 L 4
wire 7.13 10.045 7.13 35.465 V 0.5 L 3
endRouteGuideNet
```

Note: Trial Route honors completely routed nets with wires marked `FIXED` or `COVER`

➤ Choose *Route – Generate Routing Guide*.



Routing Guide File Fields and Options

File name	Specifies a name for the routing guide file.

Related Text Commands

- `trialRoute`
- `saveRouteGuide`

For more information, see “Route Commands” in the *Encounter Text Command Reference*.

12

Timing Menu

- Analysis Condition on page 1311
- Configure MMMC on page 1327
- Load Timing Constraints on page 1330
- Cell Footprint on page 1331
  - Load on page 1332
  - Check on page 1333
- Extract RC on page 1334
- QRC Standalone Extraction on page 1336
- Analyze Timing on page 1357
- Debug Timing on page 1365
- Analyze What-If Timing on page 1436
- Optimize on page 1459
- Interactive ECO on page 1463
- Timing Library on page 1475
  - Timing Library – Check on page 1476
  - Timing Library – Report on page 1477
- Report on page 1479
  - Clock Waveform on page 1480
  - Cell Footprint on page 1482
- Calculate Delay on page 1484
- Generate on page 1485

- Capacitance Table on page 1486
- Wire-Load Model on page 1489

Analysis Condition

The Analysis Condition menu provides the options for setting the modes for extraction, timing analysis, and delay calculation.

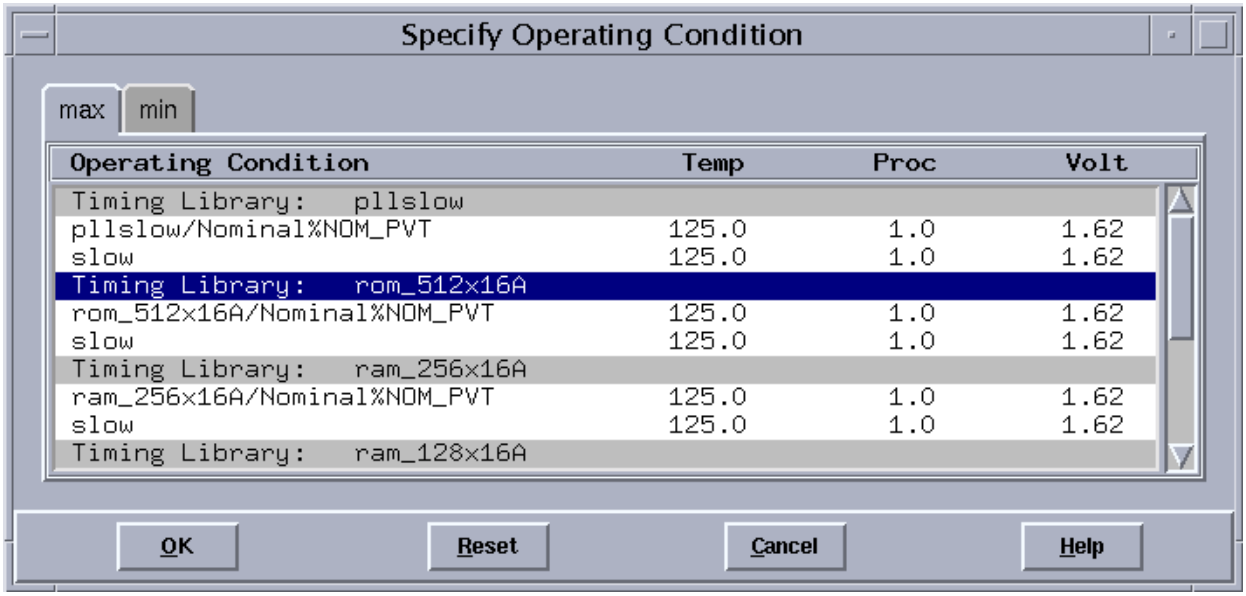
The following menu options are available:

- Specify Operating Condition on page 1312
- Specify RC Extraction Mode on page 1314
- Specify Analysis Mode on page 1318
- Set Timing Derate on page 1324
- Specify Delay Calculation Mode on page 1326

Specify Operating Condition

Use the Specify Operating Condition form to select the operating temperature, process, or voltage conditions for the design. The operating conditions are contained in the timing library, which are normally read in during design import.

➤ Choose *Timing – Specify Analysis Condition – Specify Operating Condition/PVT* and click on either the Min or Max tab to select the operating condition you want to specify.



Specify Operating Condition Fields and Options

Operating Condition	Displays the name of the operating condition. By default, the operating condition selected under the *Max* tab is used for setup analysis and the operating condition selected under the *Min* tab is used for hold analysis. When using the SignalStorm integration, it is advisable to keep the operating conditions consistent with the process corners selected for SignalStorm analysis.
Temp	Displays either the minimum or maximum temperature for the operating condition.
Proc	Displays either the minimum or maximum process parameter for the operating condition.

Volt	Displays either the minimum or maximum voltage for the operating condition.

Related Text Commands

The following text commands provide equivalent or additional functionality:

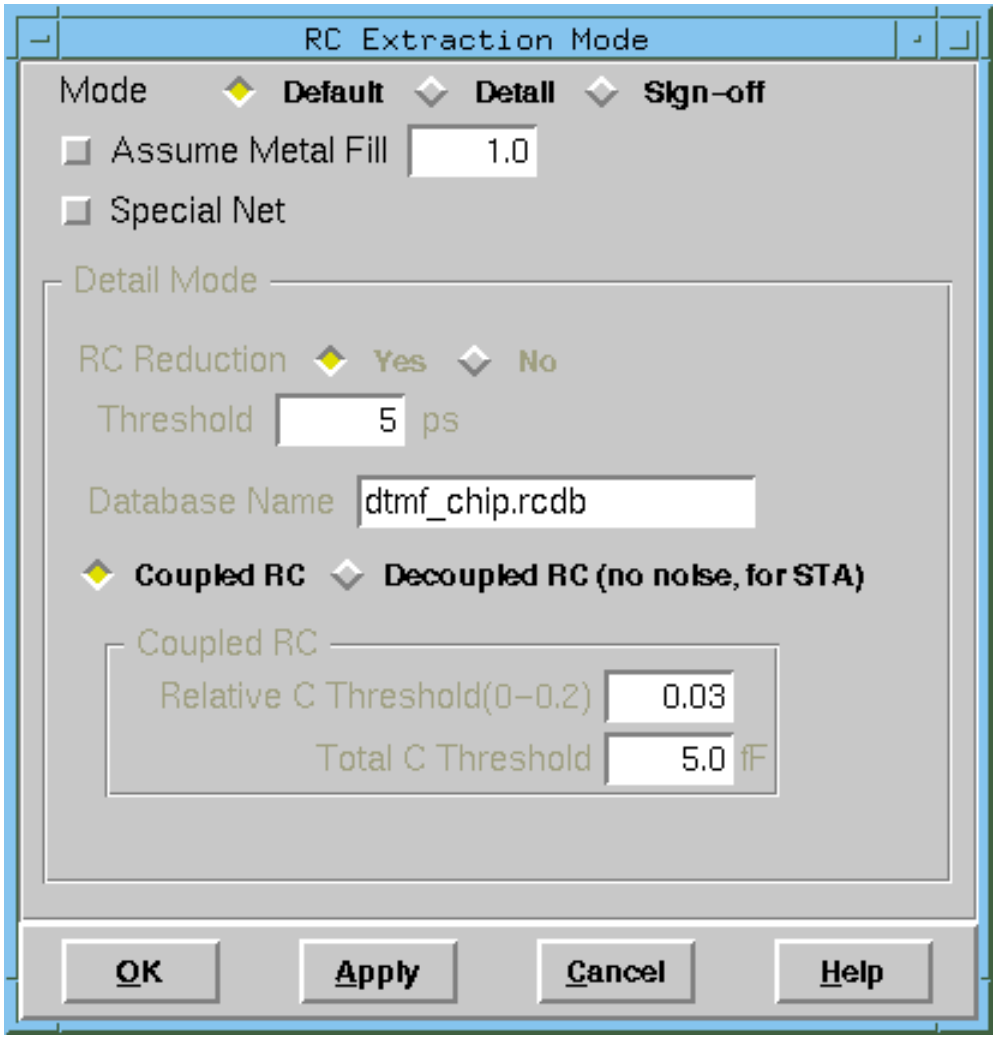
- `setOpCond`
- `setTimingLibrary`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Specify RC Extraction Mode

Use the *RC Extraction Mode* form to set the RC extract mode, to specify the threshold value (in picoseconds) used to perform RC reduction, to specify whether noise should be considered during extraction, and to specify the database output filename.

➤ Choose *Timing – Specify Analysis Condition – Specify RC Extraction Mode*.



RC Extraction Mode Fields and Options

Default — Uses default mode. Default mode should only be used during an early prototyping stage where the more detailed extraction is not needed. The coupling capacitances are not reported.

Detail — Uses detailed mode. Detailed mode is used for detailed measurement of surrounding wires where the coupling capacitances are reported.

Sign-off — Uses native full chip sign-off extraction mode. Full chip sign-off extraction supports the sign-off timing and SI optimization flow.

Assume Metal Fill — With this option, extraction assumes metal fill as follows:

- Where net-to-net spacing is at the specified minimum, the cross-coupling capacitance will be extracted and reported.
- Where there is no wire within the minimum spacing, a capacitance to ground will mimic minimum-spaced metal fill in that location.

Assume Metal Fill can have the following scale values:

- `0`: Assume no metal fill.
- `1`: Assume full metal fill at minimum spacing distance.
- *x*: Capacitance value is calculated once with full metal fill and once without metal fill. The user-specified scale value (decimal value between `0 and 1`) determines the interpolation point between the two calculated values. For example, `.5`

  Note: If no scale value is specified, the default value of `1` is used.

Special Net — Extracts special nets including nets that are a combination of signals and special wires.
Default: Special nets will not be extracted.

The following options are only available in detailed mode:

RC Reduction — Lowers the number of resistance and capacitance values stored for each path, thereby reducing the size of the parasitics database and parasitics output file when requested later in the flow. Select *No* if you do not want any RC reduction.

Threshold — Simplifying the RC structure through the reduction algorithm will slightly influence the timing response through the equivalent RC network. The timing response will not be off more than the user-specified value in picoseconds. For designs operating at a lower frequency, you can increase the default threshold value to further enhance the performance without impacting the timing. The default value is `5` ps.

Database Name — Specifies the RC database output filename.The RC database is used to store the RC network, and is used as the source for the parasitics output file generation in the `extractRC` command.

Coupled RC — Extracts the coupled resistance and capacitance network in each wire and between adjacent wires. You must enter threshold data for the capacitance values (*Coupled RC* panel). Use coupled for SI analysis.

Decoupled RC — Extracts the resistance and capacitance network of just the wires themselves. The coupling capacitances between nets are grounded. Use decoupled for STA.

The following information is required when you select *Coupled RC* in the *Coupled RC* panel.

Relative C Threshold (0-0.2)

The coupling between net A and B is recorded when it is higher than the specified fraction of the total capacitance of net A and B. The default value is `0.03` (3%).

Total C Threshold (fF) — If the total capacitance of a net is smaller than this value, the Encounter® software will ground any coupling capacitance for this net. The default value is `5` fF.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setExtractRCMode`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “RC Extraction” in the *Encounter User Guide*:

- Native RC Extraction

Specify Analysis Mode

Use the Specify Analysis Mode form to set the global analysis modes for timing analysis.

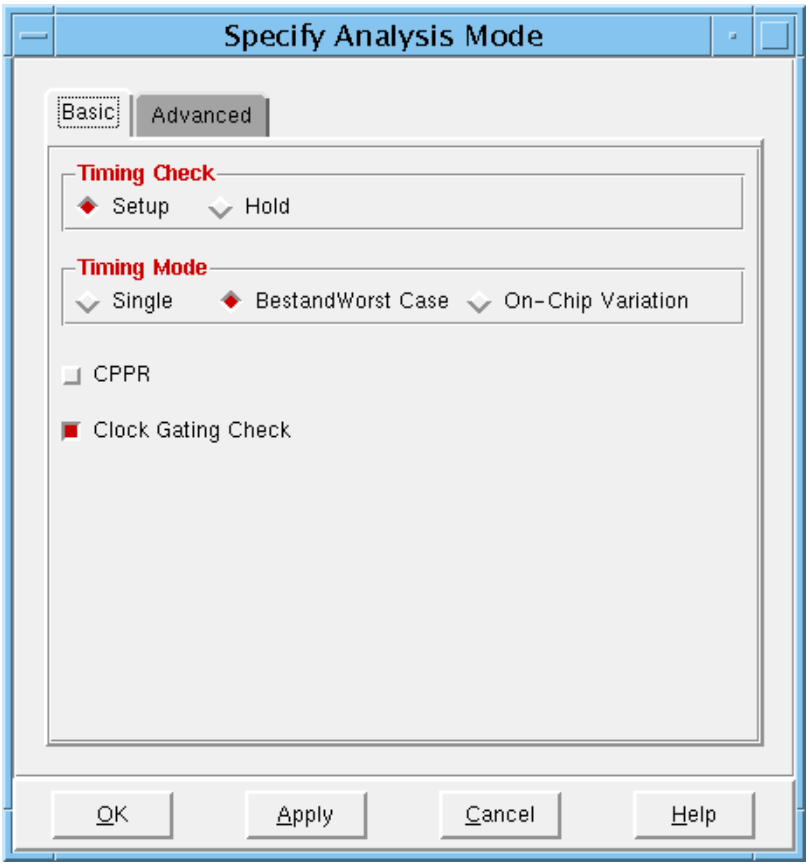
The Specify Analysis Mode form contains the following pages:

- Specify Analysis Mode – Basic on page 1319
- Specify Analysis Mode – Advanced on page 1321

Specify Analysis Mode – Basic

Use the *Basic* page of the Specify Analysis Mode form to specify setup or hold check, and timing analysis mode.

➤ Choose *Timing – Specify Analysis Condition – Specify Analysis Mode*.



Specify Analysis Mode – Basic Fields and Options

Setup	Specifies to check setup violation only.
Hold	Specifies to check hold violations only.
Single	Sets the timing analysis mode to single. In the single analysis mode, the software scales the delay values based on one operating condition. For more information, see "Single Timing Analysis Mode," in the *Encounter User Guide*.

BestandWorst Case	Sets the timing analysis mode to best case worst case. In the best case worst case analysis mode, the software checks the design for two extreme operating conditions. The software uses the maximum delays for all paths during setup checks and minimum delays for all paths during hold checks. For more information, see "Best-Case Worst-Case (BC-WC) Timing Analysis Mode," in the *Encounter User Guide*.
On-Chip Variation	Sets the timing analysis mode to on-chip variation. In the on-chip variation analysis mode, the software calculates the delay for one path based on maximum operating condition while calculating the delay for another path based on minimum operating condition for setup or hold checks. For more information, see "On-Chip Variation (OCV) Timing Analysis Mode," in the *Encounter User Guide*.
CPPR	Set the timing analysis mode to consider clock reconvergence pessimism.
Clock Gating Check	Reports the gating checks.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setAnalysisMode`

For more information, see "Timing Commands" in the *Encounter Text Command Reference*.

Related Topics

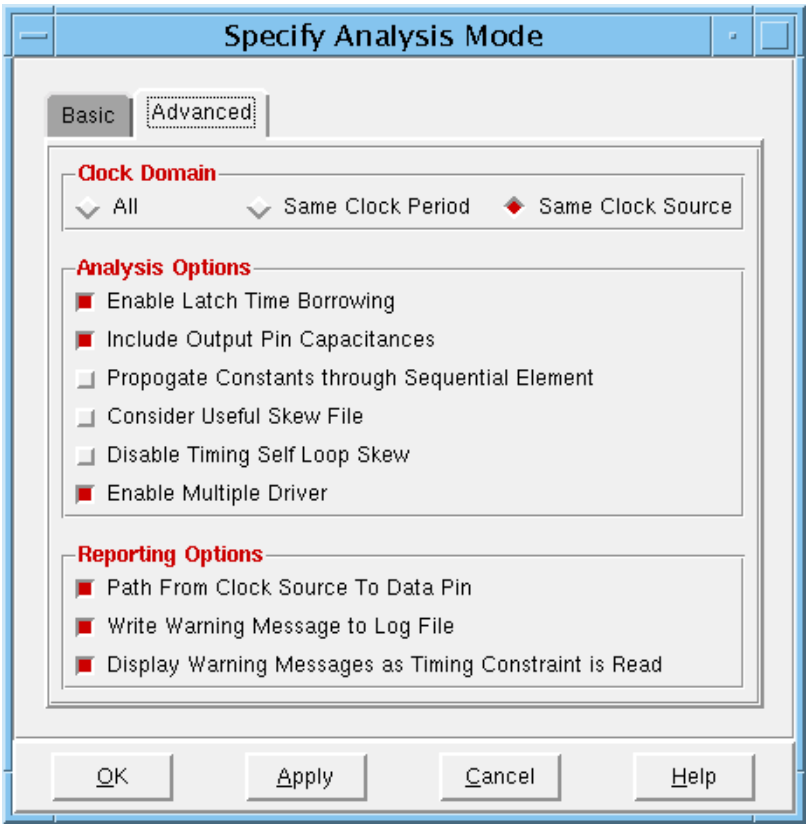
For information on the following topics, see "Timing Analysis" in the *Encounter User Guide*.

- Specifying Timing Analysis Modes

Specify Analysis Mode – Advanced

Use the *Advanced* page of the Specify Analysis Mode form to specify additional parameters for timing analysis checks.

➤ Choose *Timing – Specify Analysis Condition – Specify Analysis Mode*, and click the *Advanced* tab.



Specify Analysis Mode – Advanced Fields and Options

Clock Domain

Note: The *Clock Domain* options are obsolete.

All

Analyzes all the domains, including cross-clock domains.

Same Clock Period

Analyzes domains for which the source and destination clocks have the same period.

Same Clock Source

Analyzes domains containing paths with the same source and destination clocks.

Enable Latch Time Borrowing

Specifies whether to consider time borrowing during timing analysis. Time borrowing is the amount of time borrowed by a previous logic.

Include Output Pin Capacitance

Includes the output pin capacitance when calculating delay values.

If you do not select this option, the Encounter software excludes only the pin capacitance of the driver for which you are calculating the delay.

Propagate Constants through Sequential Element

Sets the constants to be propagated while building the timing graph. The software reads the constants from the timing constraints file or the netlist.

Default: Disables the propagation of the constants and does not use the constants from the SDC file.

Consider Useful Skew File

Considers clock skew while performing timing analysis.

Disable Timing Self Loop Skew

Disables the consideration of clock skew due to clock uncertainty for a path starting and ending at the same register. If the clock skew is considered, the timing for such paths is pessimistic.

Enable Multiple Driver

Enables the multiple-driver support for reporting.

Path From Clock Source To Data Pin

Specifies whether to report the path from the clock source to the D input pin of a register path.

Write Warning Message to Log File

Writes warning messages to the log file.

Display Warning Messages as Timing Constraint is Read

Displays warning messages as the timing constraints file is read.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setAnalysisMode`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

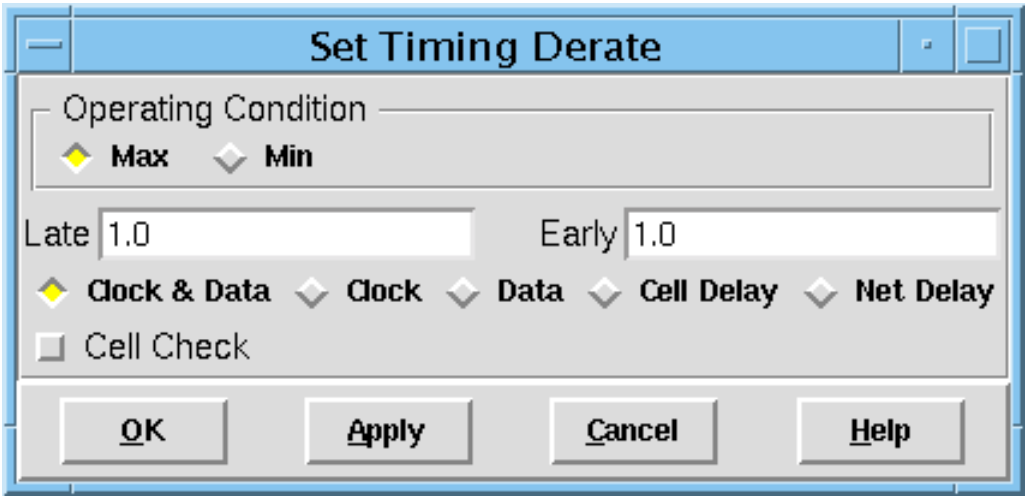
For information on the following topics, see “Timing Analysis” in the *Encounter User Guide*.

- Specifying Timing Analysis Modes

Set Timing Derate

Use the Set Timing Derate form to set the scaling or derating factors for early and late paths in the current design. The timing scaling factors affect the delay values generated in the timing reports. You can set scaling factors for data paths, clock paths, minimum and maximum operating conditions.

➤ Choose *Timing – Specify Analysis Condition – Set Timing Derate.*



Set Timing Derate Fields and Options

Max	Applies the derating factor to the maximum operating condition.
Min	Applies the derating factor to the minimum operating condition.
Late	Specifies the derating factor for late paths. *Default:* `1.0`
Early	Specifies the derating factor for early paths. *Default:* `1.0`
Clock & Data	Applies the derating factors to both clock and data paths.
Clock	Applies the derating factors to clock paths only.
Data	Applies the derating factors to data paths only.

Cell Delay	Specifies scaling on cell delays. If neither the *Cell Delay* nor the *Net Delay* option is specified, the specified scaling factor applies to both types of delays.
Net Delay	Specifies scaling on net delays.
Cell Check	Specifies scaling on timing checks. Select this option with the *Min* option to specify scaling on hold arcs and with the *Max* option to specify scaling on setup arcs.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setTimingDerate`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

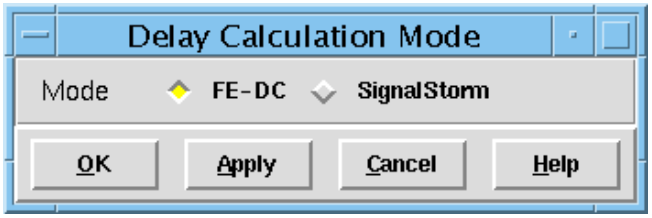
For information on the following topics, see “Timing Analysis” in the *Encounter User Guide*.

- Specifying Timing Analysis Modes

Specify Delay Calculation Mode

Use the Delay Calculation Mode form to select which delay calculation engine to use for delay calculation and SDF generation.

➤ Choose *Timing – Specify Analysis Condition – Specify Delay Calculation Mode.*



Delay Calculation Mode Fields and Options

FE-DC	Sets the delay calculation algorithm to Encounter. This is the default mode.
SignalStorm	Sets the delay calculation algorithm to SignalStorm.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setDelayCalMode`

For more information, see “Delay Calculation Commands” in the *Encounter Text Command Reference*.

Related Topics

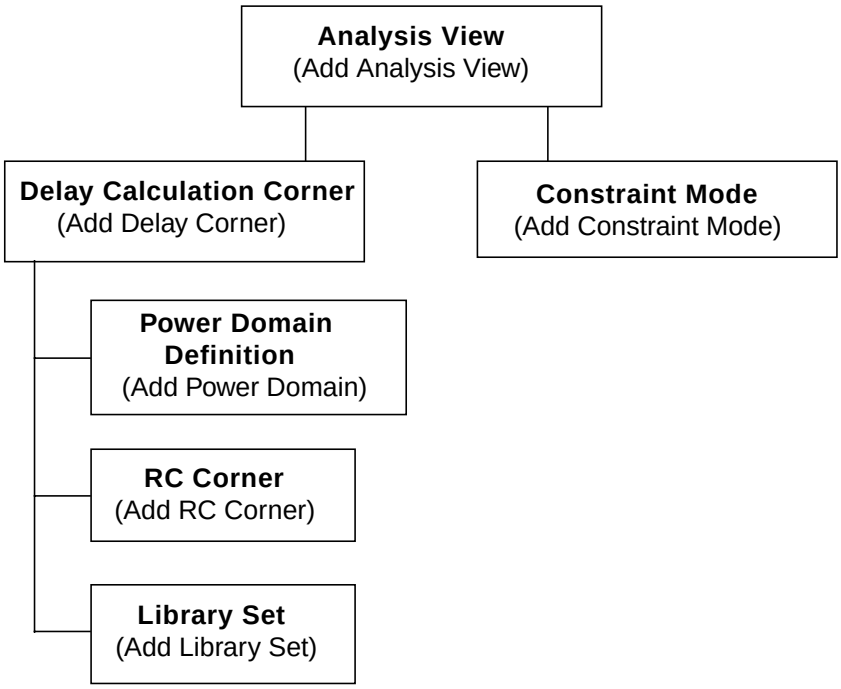
For information on the following topics, see “Calculating Delay” in the *Encounter User Guide*.

- Delay Calculation Modes and Related Controls
- Choosing A Delay Calculation Engine

Configure MMMC

Use the MMMC Browser to hierarchically create the view configurations necessary for multi-mode multi-corner analysis. Each top-level set of information is called an analysis view, and is composed of a delay calculation corner and a constraint mode. The active analysis views defined in the software represent the different design variations that will be analyzed.

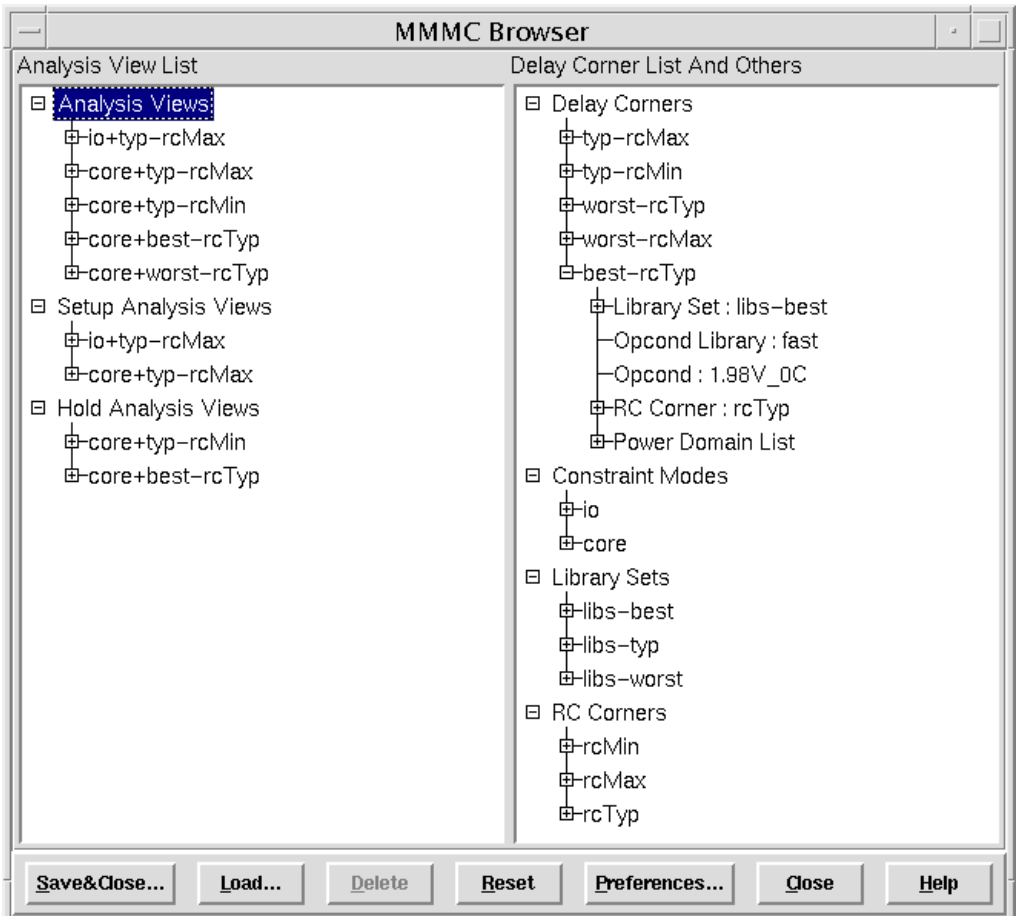
Figure 12-1 Hierarchical Analysis View Configuration



Note: You can access the MMMC Browser from the *Design Import* form, and from the *Timing* menu. Use the MMMC Browser accessed from the *Design Import* form to create a new multi-mode multi-corner configuration for the design. Use the MMMC Browser accessed from the *Timing* menu to add new objects and control analysis views to the existing multi-mode multi-corner configuration that is in memory for the design.

The configurations that you create are stored as Tcl commands in a view definition file that can then be loaded into the design.

➤ Choose *Timing – Configure MMMC*.



You can access the following forms from the MMMC Browser by double clicking on the generic object or view name:

- Add RC Corner on page 146
- Add Constraint Mode on page 149
- Add Delay Corner on page 151
- Add Power Domain on page 156
- Add Analysis View on page 160
- Add Hold Analysis View on page 162
- Add Setup Analysis View on page 164
- MMMC Preferences on page 166

You also can access the following editing forms from the MMMC Browser by double clicking on a specific object name.

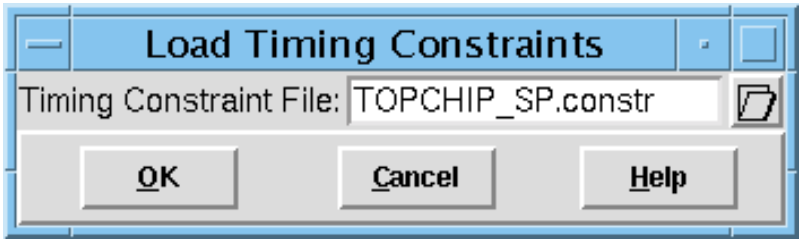
- Edit Library Set on page 169
- Edit RC Corner on page 173
- Edit Constraint Mode on page 176
- Edit Delay Corner on page 178
- Edit Power Domain on page 181

Note: The editing forms are available only before the multi-mode multi-corner view definition file is loaded into the database. After the software processes the file, the objects can no longer be edited; however, you can still control the selection of active analysis views.

Load Timing Constraints

Use the Load Timing Constraints form to load or reload a timing constraints file into Encounter any time after importing the design. The timing constraints file can be in any format including PrimeTime (PT) and Synopsys Design Constraints (SDC).

➤ Choose *Timing – Load Timing Constraint*.



Load Timing Constraint Fields and Options

Timing Constraint File	Specifies the name of the Timing Constraint file. You can click the file folder icon to choose from a list of files. The default filename is `TopCellName.constr`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `loadTimingCon`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see, “Timing Analysis” in the *Encounter User Guide*.

- Constraints Quick Reference

Cell Footprint

The Cell Footprint menu provides commands to load new cell footprint information, and examine the timing library for missing footprint functions or timing information:

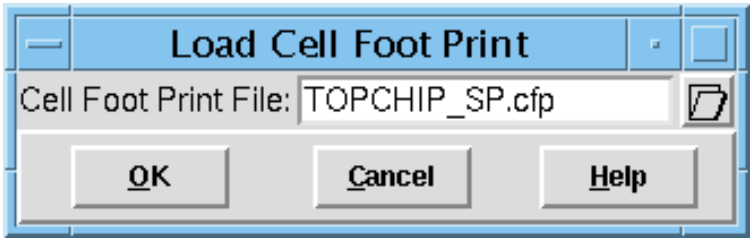
- Load on page 1332
- Check on page 1333

Load

Use the Load Cell Foot Print form to load new cell footprint information or change cell footprint information at any time after importing the design.

➤ Choose *Timing – Cell Footprint – Load*.

Note: If you previously loaded a configuration file, you do not need to load the cell footprint information explicitly.



Load Timing Constraint Fields and Options

Cell Foot Print File

Specifies the name of the Cell Foot Print file. You can click the file folder icon to choose from a list of files. The default filename is `TopCellName.cfp`. The footprint file format is as follows:

```
Library:library_name
cell_name  footprint_name
cell_name  footprint_name
```

Related Text Commands

The following text command provides equivalent or additional functionality:

- `loadFootPrint`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Check

The *Check* menu command examines the timing library for missing footprint functions or timing information. Use this command after importing the design or after loading a footprint file.

➤ Choose *Timing – Cell Footprint – Check*.

Related Text Commands

The following text command provides equivalent or additional functionality:

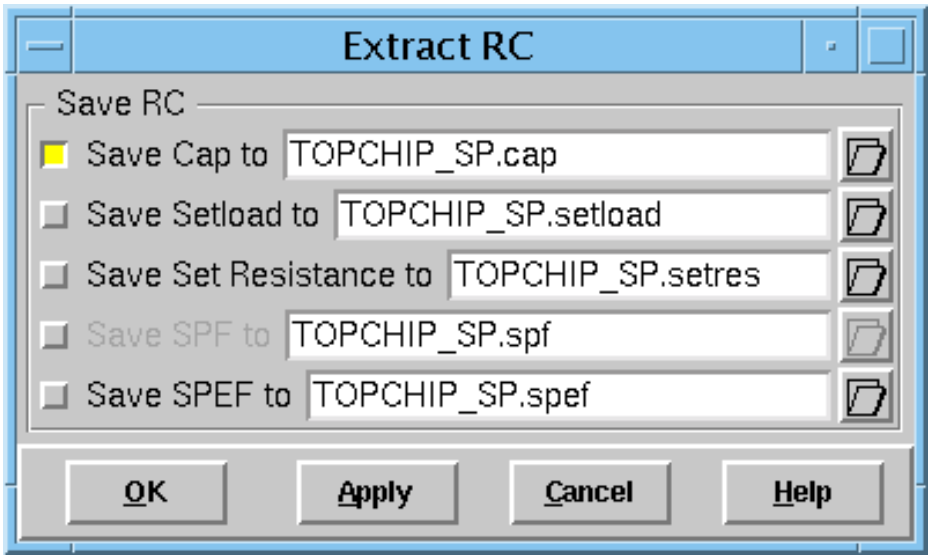
■ `checkFootPrint`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Extract RC

Use the Extract RC form to run RC extraction.

➤ Choose *Timing – Extract RC*.



Extract RC Fields and Options

Save Cap to	Specifies the name of the file in which the extracted capacitance values are stored. **Note:** This option applies only to the default mode.
Save Setload to	Specifies the name of the Synopsys `set_load` formatted file in which the value of lump sum capacitance on nets is stored.
Save Set Resistance to	Specifies the name of the Synopsys `set_resistance` formatted file in which the resistance value on nets is stored.
Save SPF to	Specifies the name of the Standard Parasitic Format file. **Note:** This option is not available in Detail RC extraction mode.
Save SPEF to	Specifies the name of the Standard Parasitic Exchange Format file.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `extractRC`
- `rcOut`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “RC Extraction” in the *Encounter User Guide*:

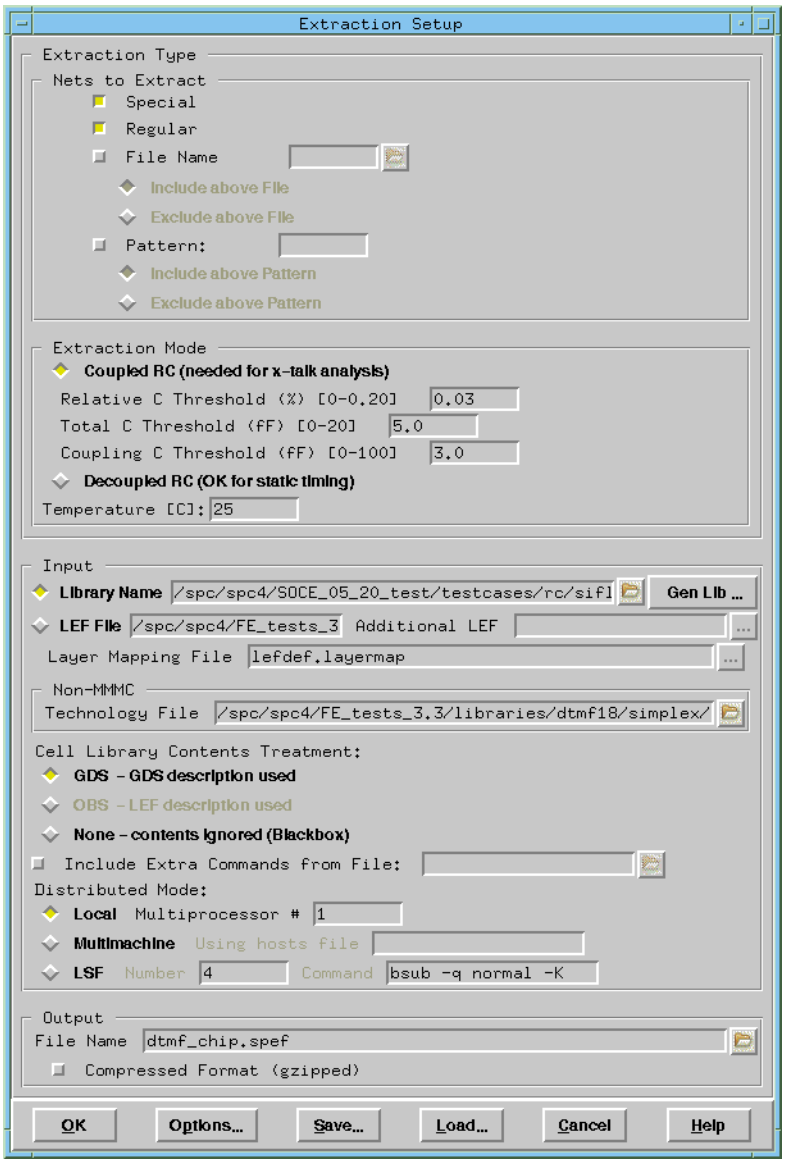
- Native RC Extraction

QRC Standalone Extraction

Note: QRC standalone extraction replaces Fire & Ice QX extraction in this release. If you are running Encounter with the QRC binaries in your search path, this form is listed in the *Timing* menu. If not, the *Fire & Ice Extract RC* form is listed in the *Timing* menu.

Use the Extraction Setup form to define extraction options and run sign-off RC extraction using QRC standalone extraction.

➤ Choose *Timing – QRC Standalone Extraction*.



Extraction Setup Fields and Options

Special

Extracts all special nets, such as power nets and clock nets. Any net that is listed in the `DEF SPECIALNETS` section of the DEF file is considered a special net. Mixed nets, which are listed partially in the `DEF SPECIALNETS` section and partially in the `DEF NETS` section, are also considered special nets.

Regular

Extracts all nets that are not special, or mixed nets.

File Name

Specifies the name of the file that lists the nets to consider. You specify one net name per line in this file. Select one of the following options:

Include above File

Specifies that the nets listed in the file to be included in extraction.

Exclude above File

Specifies that the nets listed in the file to be excluded from extraction.

Pattern

Selects all nets whose names contain one of the patterns specified. The patterns use the DEF regular expression syntax:

`*` Matches any sequence of zero or more characters.

`%` Matches any single character.

`-` Matches the whole sequence of characters up to and including the next period (`.`). If there is no period in the string, it matches to the end of the string.

Select one of the following options:

Include above Pattern

Specifies that the nets that match the listed patterns to be included in extraction.

Exclude above Pattern

Specifies that the nets that match the listed patterns to be excluded in extraction.

Coupled RC

Extracts the coupled resistance and capacitance network. Enter data for the following capacitance values:

Relative C Threshold (%)

The coupling between net A and B is recorded when it is higher than the specified fraction of the smaller of the total capacitance of net A and B.

Default: `0.03` (3%)

Range: 0-0.20

Total C Threshold (fF)

Specifies that if the total capacitance of a net is larger than this value, QRC records the net's coupling capacitance.

Default: `5.0` fF

Range: 0-20

Coupling C Threshold (fF)

Sets a fixed threshold value that determines when the extractor lumps a net's coupling capacitance to ground. Supports native sign-off extraction (`-coupled` only).

Default: 3 femtoFarads

Decoupled RC

Extracts the decoupled resistance and capacitance network. In this case, the coupling capacitances between nets are grounded.

Temperature [C]

Specifies the operating temperature for derating resistance based on the temperature coefficient defined in the technology file.

Library Name

Specifies the name of the cell library file. You can either specify an existing library file name, or click *Gen Lib* to generate a library file. For detailed information on using the *Gen Lib* option, see "Library Generation" on page 1347.

LEF File

Specifies the LEF files that contain the standard cells and macros. You must use this field in conjunction with the *Layer Mapping File* field to map the LEF data to the QRC technology file. This supports the direct LEF flow.

Additional LEF

Specifies an additional LEF file.

Layer Mapping File

Specifies the layer mapping file used to map the LEF data to the QRC technology file. Use this field in conjunction with the *LEF File* field to support the direct LEF flow.

Technology File

Specifies the name of the QRC technology file.

Note: The QRC technology file is required as input only when the software is not in multi-mode multi-corner mode (MMMC). When the software is in MMMC mode, the software automatically detects the QRC technology file.

Cell Library Contents Treatment

Performs a capacitance extraction, which recognizes the effects of the cells on the interconnect. The source of the gray data can be one of the following:

GDS

Indicates that the source of the gray data is the GDS data type from the GDS cell library.

OBS

Indicates that the source of the gray data is the obstruction data type from the LEF cell library.

None

Performs blackbox extraction that ignores the effects of the cells on the interconnect.

Include Extra Commands from File

Specifies the name of the file that contains additional commands for QRC standalone sign-off extraction. For more information on additional options that you can specify, see the *Fire & Ice QX Gate-Level Extraction* manual.

Distributed Mode

Supports distributed processing mode for QRC standalone sign-off extraction. Distributed processing mode improves run time performance by enabling you to run extraction jobs on multiple machines over the network.

Local, Multiprocessor #

When using a local machine with multiple processors, you can run multiprocessor mode by specifying the number of processors (2 to 4) that are available for the extraction jobs.

Default: 2

Multimachine, Using hosts file

Runs extraction jobs on multiple machines over the network. You must specify the machine names (hosts) to use this option.

LSF, Number, Command

Specifies the number of remote host machines and the protocol command that will be used to assign the extraction jobs for distributed processing. The protocol command assigns the extraction jobs to a specified number of machines over the network. Machines are chosen based on their current work load and availability.

The `bsub` command is used for the LSF protocol and the `gridsub` command is used for the Grid Matrix System protocol.

Default: "`bsub -q normal -K`" (LSF)

File Name Specifies the name of the output file.

Compressed Format (gzipped)

Compresses the output file using the gzip format.

Options Specifies the advanced setup options. For more information on the advanced setup options, see "Extraction Advanced Setup Options" on page 1343.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runQRC`

For more information, see “RC Extraction Commands” in the *Encounter Text Command Reference*.

Related Topics

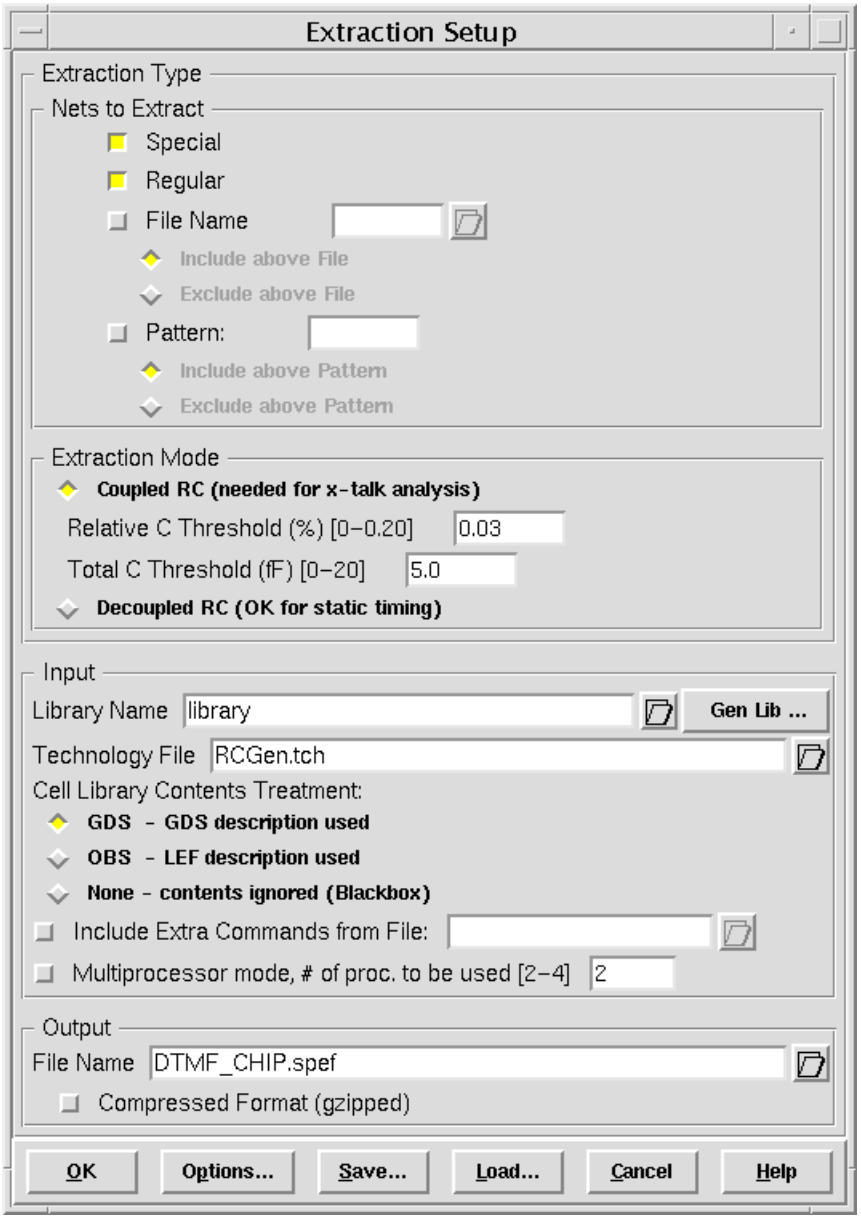
For information on the following topics, see “RC Extraction” in the *Encounter User Guide*:

- Sign-Off Extraction Using QRC
- Correlating Native Extraction With Sign-Off Extraction

Fire & Ice Extract RC

Note: The Fire & Ice QX extraction engine is obsolete and will be removed in the next major release of the software. Use the QRC Standalone Extraction engine instead.

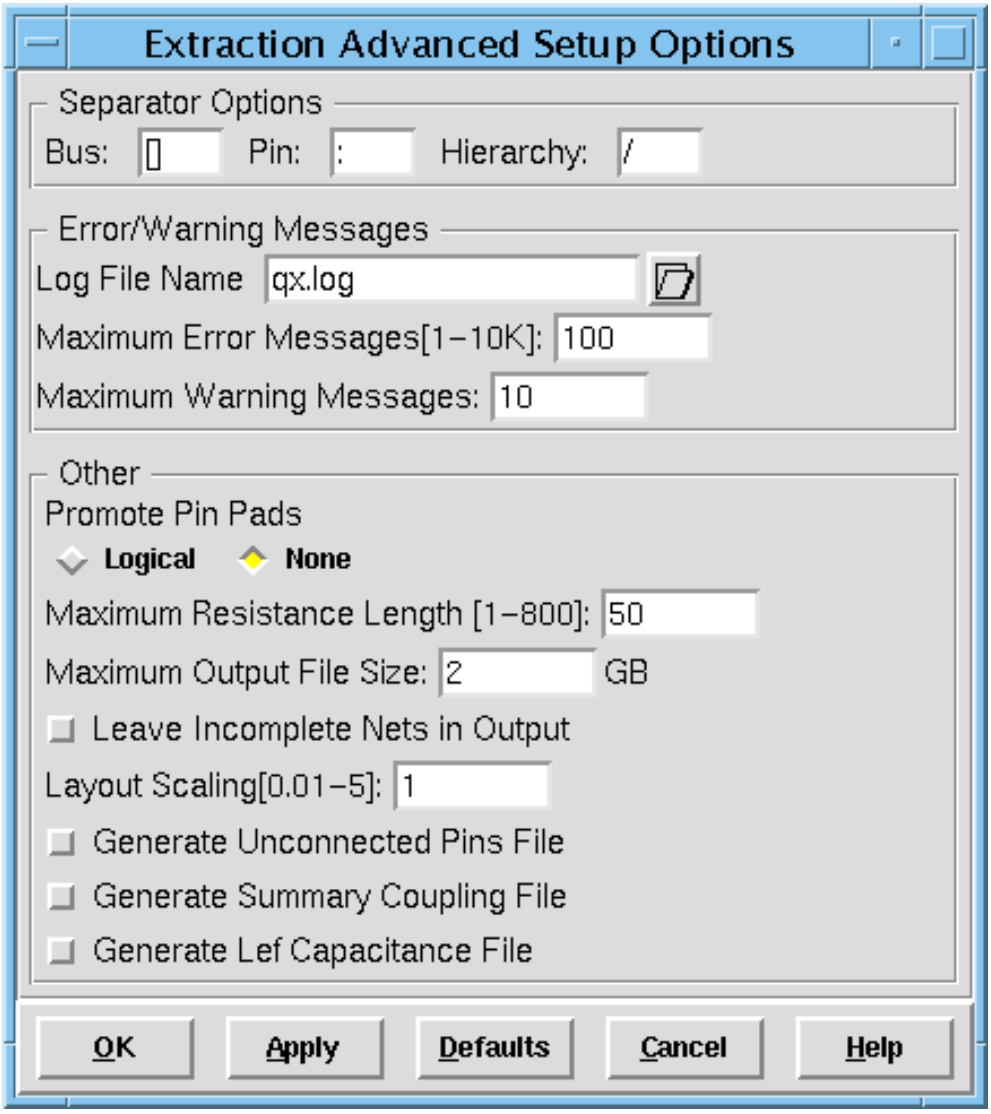
Use the Extraction Setup form to define extraction options and run sign-off RC extraction using Fire & Ice QX. See QRC Standalone Extraction for field descriptions.



Extraction Advanced Setup Options

Use the Extraction Advanced Setup Options form to specify advanced options.

➤ Choose *Timing – QRC Standalone Extraction – Options*.



Extraction Advanced Setup Fields and Options

Log File Name

Specifies the name of the log file generated by the extractor.

Maximum Error Messages

Sets the maximum number of error messages issued by the extractor during a session. The default value is `100`.

Maximum Warning Messages

Sets the maximum number of warning messages issued by the extractor during a session. The default value is `10`. The tool suppresses any warnings generated after the maximum number has been reached.

Promote Pin Pads

Determines what parasitic data to extract for the top-level logical pin connected to a pad pin by a net with no routing. Specify any one of the following:

Logical

The tool constructs the logical resistance and capacitance network for the connection between the top-level logical pin and the pad pin, but sets the parasitic data to zero.

None

The tool ignores the top-level pin and extracts no parasitic data.

Maximum Resistance Length

Sets the maximum length for a resistor. Smaller values increase the accuracy of the distributed RC database, decrease capacity, and increase run times. Specify a value between 10 to 800 µm. The default value is `50`.

Maximum Output File Size

Specifies the desired maximum size of output files, in bytes. This value is used to split large DSPF and SPEF files into several smaller files to accommodate file-size constraints of downstream tools.

Leave Incomplete Nets in Output

Includes open nets in the output DSPF or SPEF file.

Layout Scaling

Specifies a scaling factor for all layout dimensions in the design. Use this when the design has been sized by a scaling factor. This QRC parameter is equivalent to the Encounter Shrink Factor specified during design import.
Default: `1`

Generate Unconnected Pins File

Produces a file called *`designname`*`.uncon` containing a list of pins that are logically connected but not physically connected in the design.

Generate Summary Coupling File

Writes out the following types of capacitance:

- The lumped coupling capacitance between two nets (net-to-net coupling capacitance). This information is written to the *`designname`*`.n2nccap` file.
- The total capacitance of each net. This information is written to the *`designname`*`.totcap` file.
- The total capacitance of two nets plus the total coupling capacitance between them. This information is written to the *`designname`*`.capratio` file.

Note: These files are not created when decoupled RC Mode is selected.

Generate Lef Capacitance File

Outputs area capacitance per area and peripheral capacitance per edge for each conductor layer in LEF format, which can be used by physical design tools. The default name of the LEF capacitance file is *`designname`*`.lef`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runQRC`

For more information, see “RC Extraction Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topics, see “RC Extraction” in the *Encounter User Guide*:

- Sign-Off Extraction Using QRC
- Correlating Native Extraction With Sign-Off Extraction

Library Generation

Use the *Gen Lib* option in Extraction Setup form to open the Library Generation form. This form takes LEF, GDSII, or a combination of LEF and GDSII as input and creates a binary view of the cell contents within the cell library database. The default name of the file generated is `library.cl`.

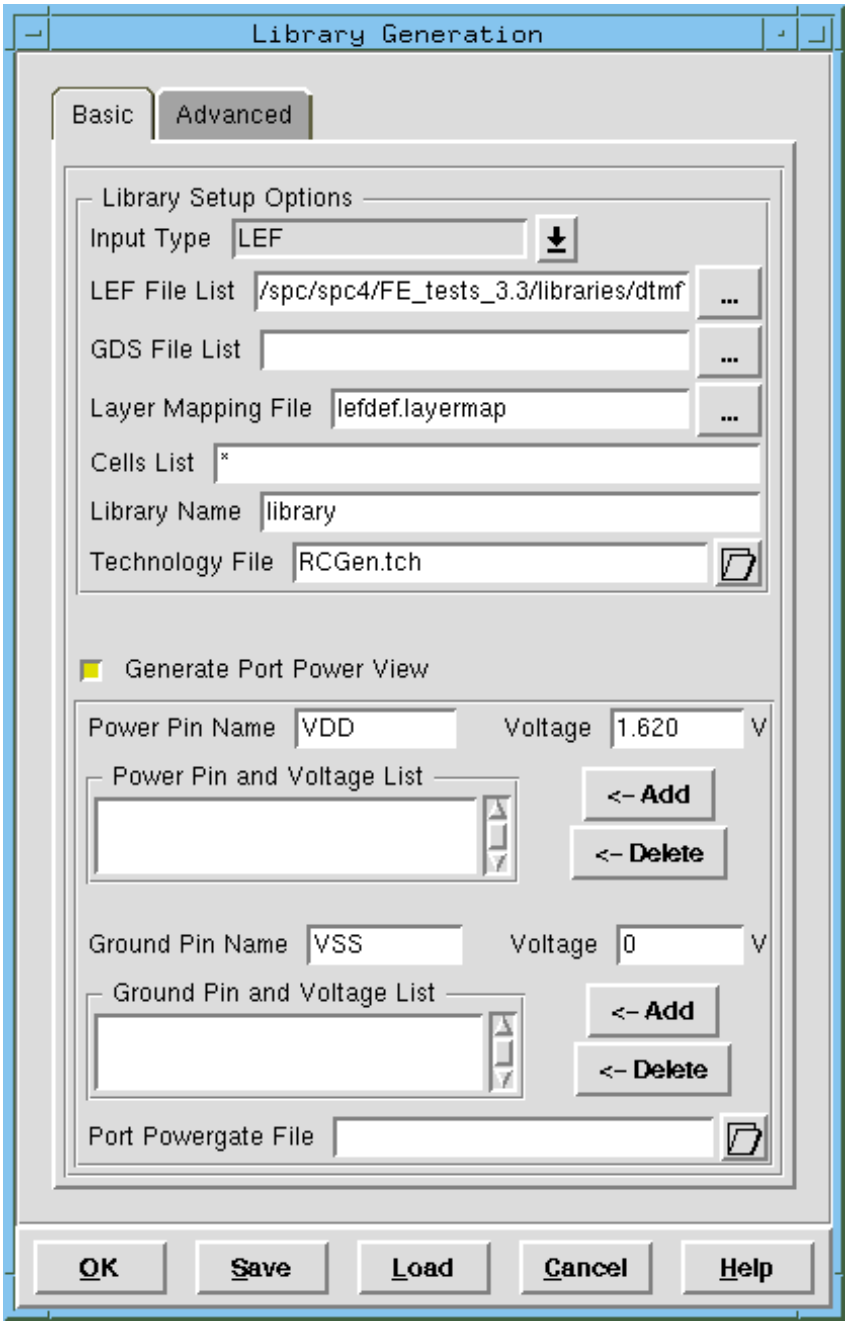
The Library Generation form contains the following pages:

- Library Generation – Basic on page 1348
- Library Generation – Advanced on page 1353

Library Generation – Basic

Use the *Basic* page of the Library Generation form to set up basic library files and options.

➤ Choose *Timing — QRC Standalone Extraction– Gen Lib* and click the *Basic* tab.



Library Generation – Basic Fields and Options

Input Type

Specifies input type. Select one of the following:

LEF — Specifies a Library Exchange Format (LEF) file containing library information for a class of designs. Library data includes layer, via, placement site type, and macro cell definitions.

GDS — Specifies an annotated GDSII input file.

LEF&GDS — Specifies mixed LEF/GDS input.

LEF File List

Specifies the LEF file(s). Separate multiple filenames with spaces. Clicking the button to the right of this field opens the LEF Files form for easier manageability of multiple files.

Note: Fire & Ice processes multiple LEF files in the order in which you enter them. Therefore, list incremental files that depend on predefined data after the files that define the data. Specify the technology LEF file first.

GDS File List

Specifies the GDS file(s). Separate multiple filenames with spaces. Clicking the button to the right of this field opens the GDS Files form for easier manageability of multiple files.

Layer Mapping File

Specifies the name of the file that maps between the layer name used in the ICT file and one of the following:

- The associated layer's GDSII layer and data type numbers
- The associated layer's LEF/DEF layer name

Use this option for layers that are not diffusion, local interconnect, metal, poly, via, or well layers. You can use this option multiple times for each layer name to assign a different GDSII layer number or LEF/DEF layer name to a cell library layer. Specify LEF/DEF and GDSII layers in separate commands.

For an example of the format of the layer mapping file, see "Sample Layer Mapping File" in *Encounter Text Command Reference*.

Cells List

Specifies the cells that the software will process. Use an asterisk (*) to represent all cells (the default).

Library Name

Specifies the name of the output cell library file.

Technology File

Specifies the IceCaps technology file. The technology file contains interconnect models used to extract the interconnect parasitic capacitance and resistance.

Generate Port Power View

Enables you to specify values for generating a port power grid view. This view contains power port information that provides the current loading to the power grid networks in VoltageStorm. Using this view is like running in blackbox mode. This view is typically used for standard cells or blocks that will not effect power consumption of your circuit. The equivalent VoltageStorm variable is `generate_port_powerview`.

Note: This step is required for VoltageStorm, but is optional for Fire & Ice Extract.

Power Pin Name and Voltage List

Populates the Power Pin and voltage list. Specify this value for each power pin name to be included.

Ground Pin Name and Voltage List

Populates the Ground Pin and Voltage List. Repeat this step for each ground pin name to be included.
The equivalent VoltageStorm variable is `generic_ground_names`.

Port Powergate File

Specifies a file that contains all the information that the library generation software needs to create a port power gate view. This includes the names of the power gate cells, the names of the pins in the power gate cells, the on-resistance of the power gate, and the saturation current of the power gate. The library generation software translates the VoltageStorm `port_power_gate` command to create the port power gate view. The port power gate file consists of the following syntax:

```
port_power_gate cell cellname supply
unswitched_pin_name switched switched_pin_name ron
r_value idsat idsat_value ileak ileak_value
```

where:

- `cell` *`cellname`* specifies the name of the cell.
- `supply` *`unswitched_pin_name`* specifies the name of the unswitched power pin. This is the pin that the leakage current is attached to if the power gate is in the off state.
- `switched` *`switched_pin_name`* specifies the name of the switched power pin.
- `ron` *`r_value`* specifies the on-resistance value in ohms.
- `idsat` *`idsat_value`* specifies the value of the saturation current in milliamps.
- `ileak` *`ileak_value`* specifies the leakage current in milliamps.

For information on how to perform power gate steady-state analysis, see the *Power Gating* chapter in the *VoltageStorm Cell-Level Rail Analysis User Guide.*

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runLibGen`

For more information, see “RC Extraction Commands” in the *Encounter Text Command Reference*.

Related Topics

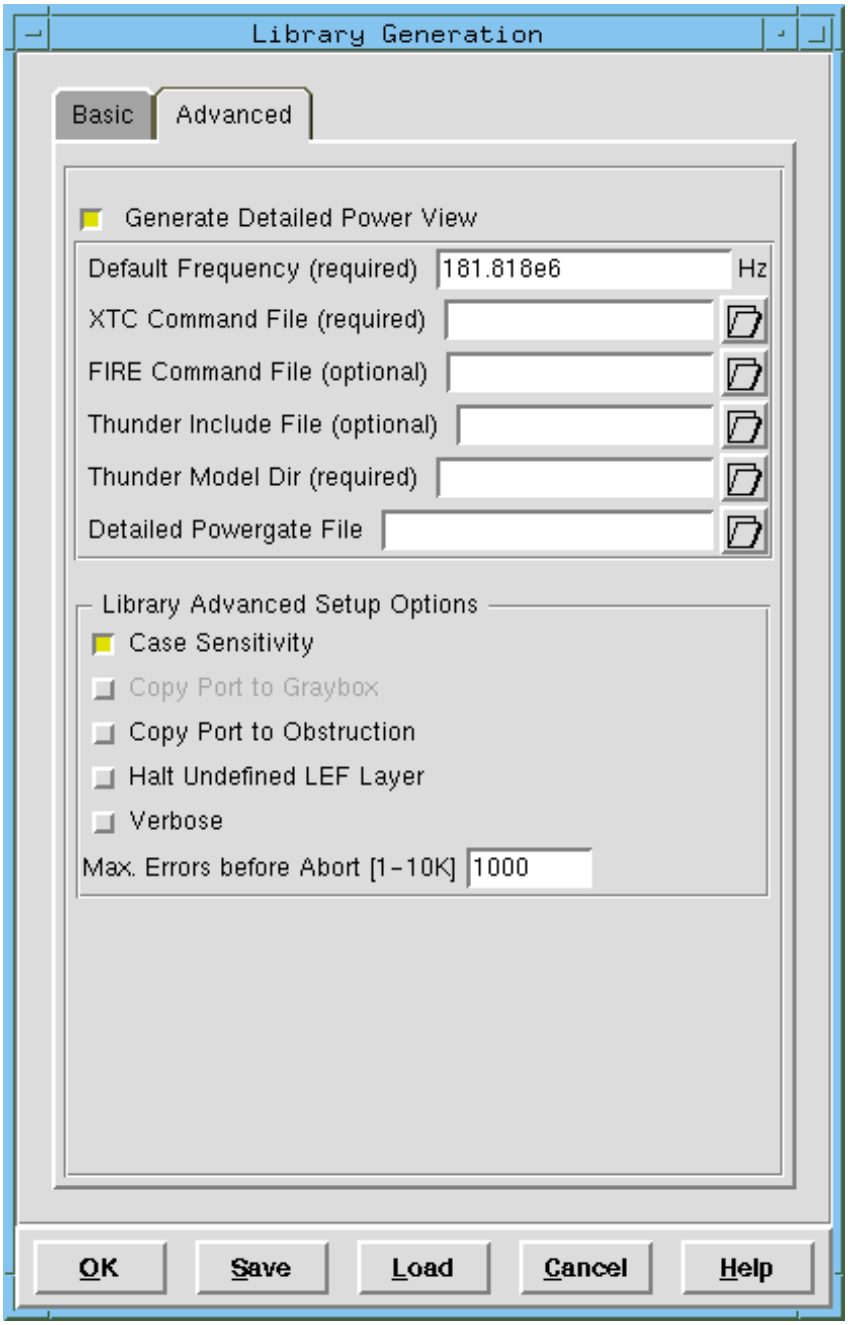
For information on the following topic, see “RC Extraction” in the *Encounter User Guide*:

- Sign-Off Extraction Using QRC

Library Generation – Advanced

Use the *Advanced* page of the Library Generation form to set up advanced library options.

➤ Choose *Timing — QRC Standalone Extraction — Gen Lib* and click the *Advanced* tab.



Library Generation – Advanced Fields and Options

Generate Detailed Power View

Enables you to specify values for generating a detailed power view. This is a detailed electrical model of the internal power routing of a cell or macro extracted from GDS data. It contains power port information that provides the current loading to the power grid networks.

The equivalent VoltageStorm variable is `generate_detailed_powerview`. For more information on detailed view generation, see the *VoltageStorm Hierarchical PGS Manual.*

Note: You must have GDS and LEF files available to generate a detailed power view.

Default Frequency (required)

This is the default operating frequency for blocks. This option is required for generating detailed power grid views for power analysis, using the Accura technology. The equivalent VoltageStorm variable is `default_frequency`.

XTC Command File (required)

This file specifies how devices are formed and how they are connected. The equivalent VoltageStorm variable is `gds_extractor_command_file`.

FIRE Command File (optional)

This specifies the name of the fire command file that contains information about the cells in the design and is used for resistance extraction. The equivalent VoltageStorm variable is `fire_command_file`.

Thunder Include File (optional)

This specifies the name of a thunder file to include SPICE netlist details for a cell. The equivalent VoltageStorm variable is `circuit_include_file`.

Thunder Model Dir (required)

This directory specifies the location of the Thunder model tables that are used to generate the current data for the cells in the library. The equivalent VoltageStorm variable is `thunder_model_table_directory`.

Detailed Powergate File

Specifies a list of power-gating cells to perform power gate steady-state analysis. Power-gating cells contain large transistors which can be turned off when the cell is not being used. The library generation software translates the VoltageStorm `detailed_power_gate` command to calculate the saturation current, leakage current, and resistance value of each power-gating cell to generate the detailed power gate view. The detailed power gate file consists of the following syntax:

```
detailed_power_gate cell cellname supply
supply_net_name switched switched_net_name
```

where:

- `cell` *`cellname`* specifies the name of the cell.
- `supply` *`supply_net_name`* specifies the name of the supply net.
- `switched` *`switched_net_name`* specifies the name of the switched power net.

For information on how to perform power gate steady-state analysis, see the *Power Gating* chapter in the *VoltageStorm Cell-Level Rail Analysis User Guide.*

Case Sensitivity

Determines whether the software interprets the data in the LEF file as case-sensitive or case-insensitive.

Copy Port to Graybox

Copies the port and feedthrough geometries from the GDS data into the graybox view used for parasitic extraction.

Copy Port to Obstruction

Copies the port and feedthrough geometries from the LEF file into the obstruction view used for parasitic extraction.

Halt Undefined LEF Layer

Aborts processing if the software encounters a LEF layer that was not defined in the layer map in the command file.

Verbose Controls the amount of information written to the log file.

Max. Errors before Abort [1-10K]

Specifies the maximum number of errors to report before exiting the tool.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `runLibGen`

For more information, see “RC Extraction Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “RC Extraction” in the *Encounter User Guide*:

- Sign-Off Extraction Using QRC

Analyze Timing

Use the Timing Analysis form to build the timing graph for the design and generate a slack report and a detailed timing violation report. Load both the Timing Library and the timing constraints file (`dc_shell` or PrimeTime) during design import.

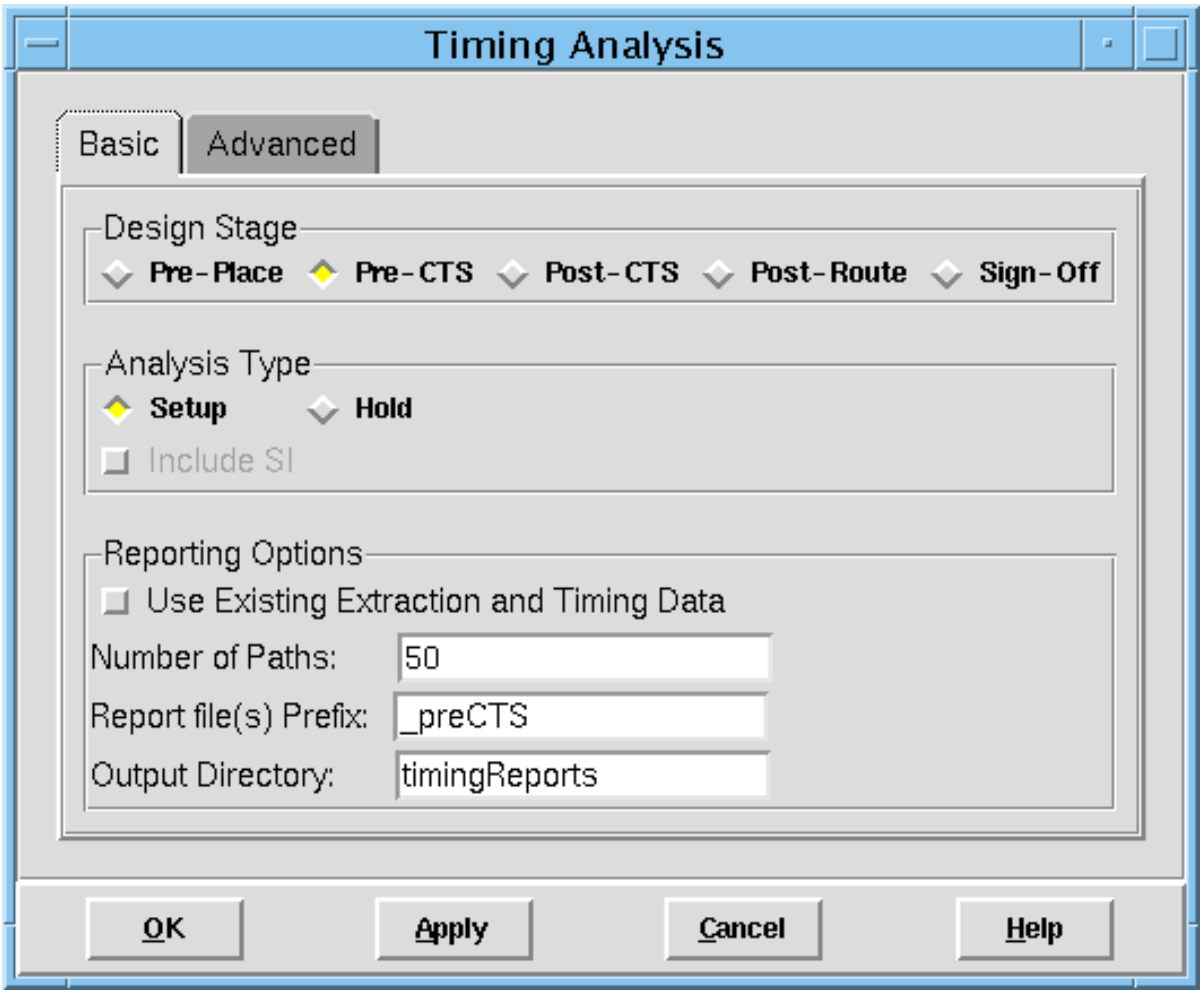
The Timing Analysis form contains the following pages:

- Timing Analysis – Basic on page 1358
- Timing Analysis – Advanced on page 1361

Timing Analysis – Basic

Use the *Basic* page of the Timing Analysis form to set up reporting options.

➤ Choose *Timing – Timing Analysis* and click the *Basic* tab.



Timing Analysis – Basic Fields and Options

Pre-Place	Generates timing reports before the design is placed. In this mode, the software ignores the net load while building the timing graph and runs FE timing analysis for generating timing reports. The DRV report files are not generated in this mode. The *Pre-Place* option sets the `setAnalysisMode` to `-clkSrcPath false` and `-clockPropagation forcedIdeal`.
Pre-CTS	Generates timing reports for a design before the clock tree has been created. By default, in this mode the software runs trialRoute, native default extraction, and FE timing analysis for generating timing reports. The *Pre-CTS* option sets the `setAnalysisMode` to `-clkSrcPath false` and `-clockPropagation forcedIdeal`.
Post-CTS	Generates timing reports for a design whose clock tree has been created. By default, in this mode the software runs trialRoute, native default extraction, and FE timing analysis for generating timing reports. The *Post-CTS* option sets the `setAnalysisMode` to `-clkSrcPath true` and `-clockPropagation sdcControl`.
Post-Route	Generates timing reports for a design whose routing is complete. By default, in this mode the software runs native detailed extraction, and FE timing analysis for generating timing reports. The *Post-Route* option sets the `setAnalysisMode` to `-clkSrcPath true` and `-clockPropagation sdcControl`.
Sign-Off	Generates timing reports for sign-off timing analysis. By default, in this mode the software runs QRC standalone extraction. **Note:** To use this parameter, you must ensure that the Encounter configuration file contains data for QRC standalone extraction.
Setup	Reports setup violation only.
Hold	Reports hold violation only.
	Default: Reports setup violations.

Include SI

Runs CeltIC and generates glitch violation report and incremental SDF for timing analysis. You can use this parameter with the *Post-Route* and *Sign-Off* options only.

Note: To use this parameter, you must ensure that the Encounter configuration file contains data for CeltIC™ crosstalk analyzer.

Use Existing Extraction and Timing Data

Specifies the use of existing extraction and timing analysis data. When you select this option, the software does not run extraction and timing analysis. The timing analysis data must match the stage of the design that you have specified using the *Pre-Place*, *Pre-CTS*, *Post-CTS*, *Post-Route*, or *Sign-Off* options.

Number of Paths

Specifies the number of paths to report in the detailed path violations.

Default: `50`

Report file(s) Prefix

Specifies a prefix for the timing report file names.

Default: `DesignName_DesignStage`

Output Directory

Specifies the name of the output directory that contains all the generated reports.

Default: `timingReports`

Related Text Commands

The following text commands provide equivalent or additional functionality:

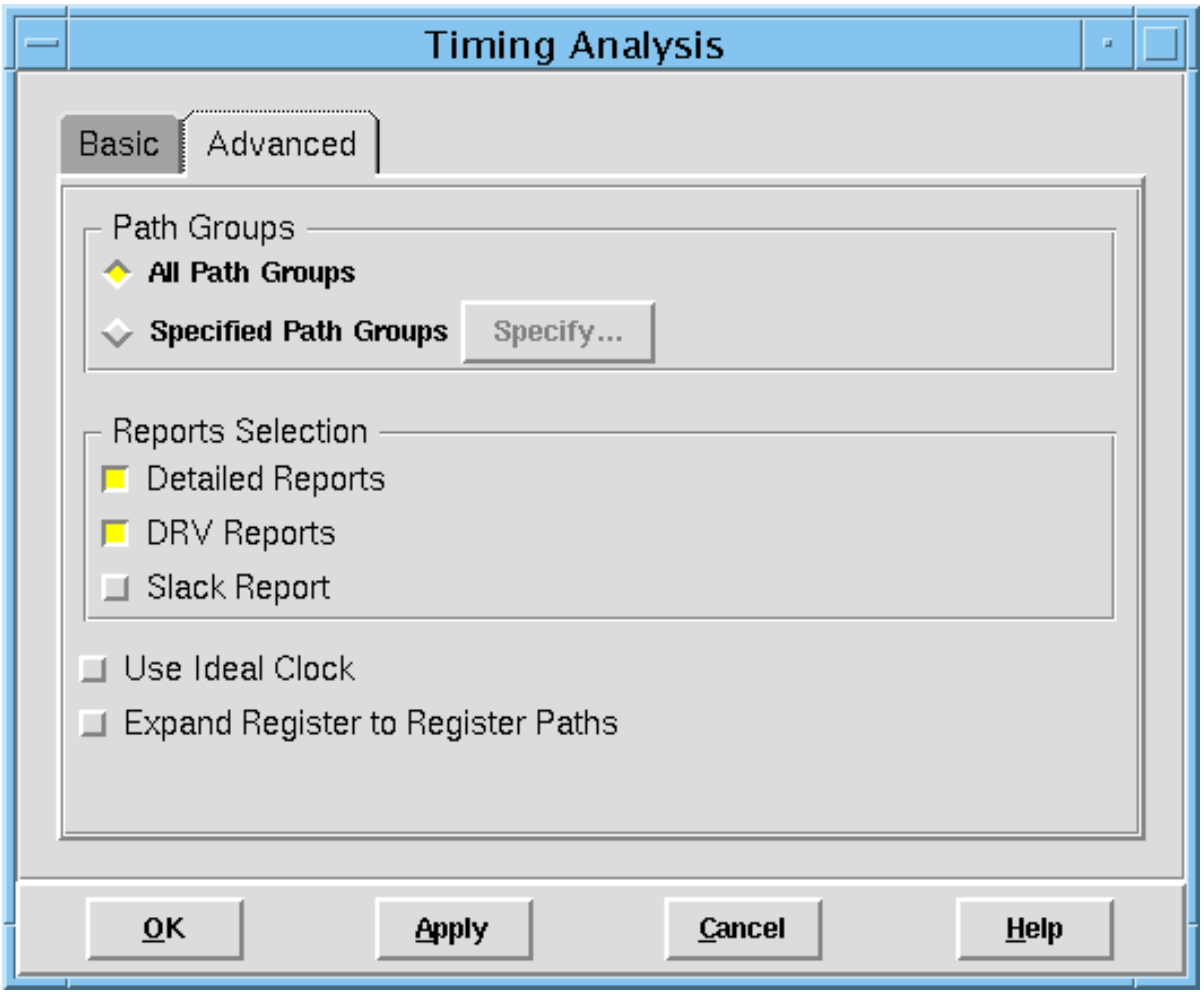
- `timeDesign`

For more information, see “Timing Analysis Commands” in the *Encounter Text Command Reference*.

Timing Analysis – Advanced

Use the *Advanced* page of the Timing Analysis form to set up the path groups along with advanced reporting options.

➤ Choose *Timing – Timing Analysis* and click the *Advanced* tab.



Timing Analysis – Advanced Fields and Options

All Path Groups Reports all path groups.

Specified Path Groups Reports selected path groups. To specify the path groups, click on the *Specify* button. This opens the Specify Path Groups form. For more information, see "Specify Path Groups" on page 1363.

Detailed Reports Generates detailed path reports.

DRV Reports Generate design rule violation (DRV) reports only.

Slack Reports Generate slack reports only.

Use Ideal Clock Performs ideal clock analysis irrespective of the design stage.

Default: The software performs propagated clock analysis with the *Post-CTS* and *Post-Route* options. The software performs ideal clock analysis with the *Pre-Place* and *Pre-CTS* options.

Expand Register to Register Paths

Specifies that the register to register path groups are divided into the following detailed path groups for generating reports:

- Flop to flop
- Macro to flop
- Flop to macro
- Macro to macro

Related Text Commands

The following text commands provide equivalent or additional functionality:

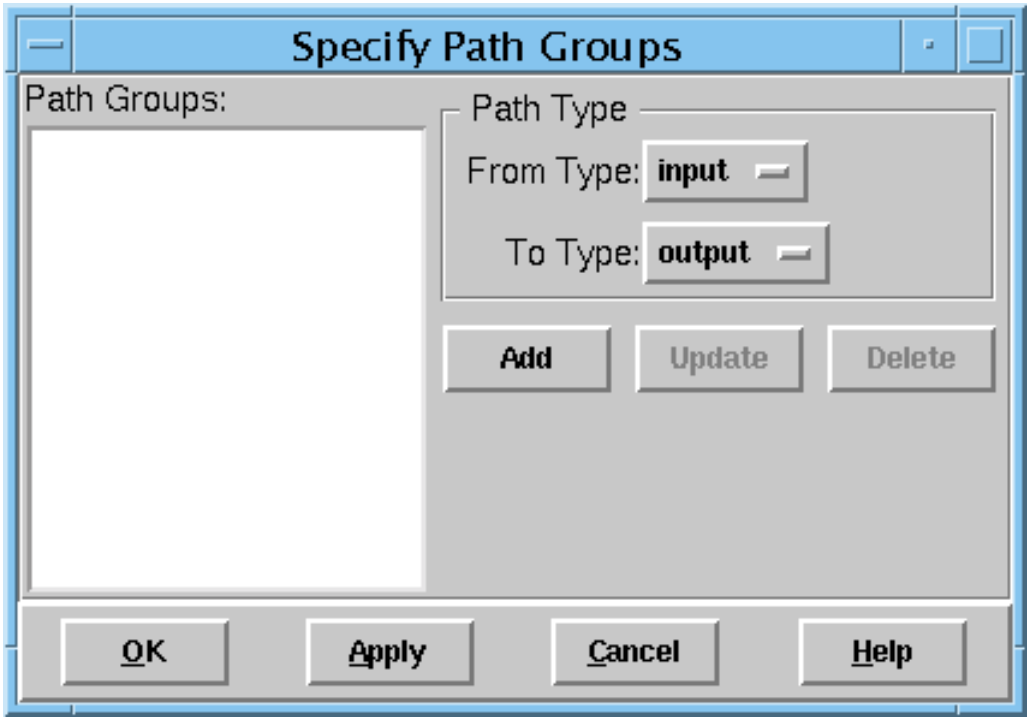
- `timeDesign`

For more information, see "Timing Analysis Commands" in the *Encounter Text Command Reference*.

Specify Path Groups

Use the Specify Path Groups form to specify the combination of path groups to be reported after timing analysis.

➤ Choose *Timing – Timing Analysis – Advanced – Specify*.



Specify Path Groups Fields and Options

From Type

Specifies the origin of the path to report. Choose from the following options:

- *input*
- *register*
- *macro*
- *flopOrLatch*
- *clkSrc*
- *moduleIOCstr*
- *noModuleIOCstr*
- *all*

Default: input

To Type

Specifies the end point of the path to report. Choose from the following options:

- *output*
- *register*
- *macro*
- *flopOrLatch*
- *moduleIOCstr*
- *noModuleIOCstr*
- *all*

Default: output

Add

Adds a path type to the *Path Groups* list. You must first specify *From Type* and *To Type*. The software reports the path groups on this list.

Debug Timing

The Global Timing Debug menu provides options for debugging the timing results. The timing debug feature provides easy cross-probing between the Timing Debug forms and Encounter design display area.

Encounter provides different timing debug features depending on the timing mode that you have selected.

- To generate a timing report, choose *Timing – Timing Debug* on the Encounter Timing menu and use the following form:
  - Timing Debug – Timing Debug Preferences on page 1387

  The following form displays the results generated:
  - Timing Debug – Browser on page 1368

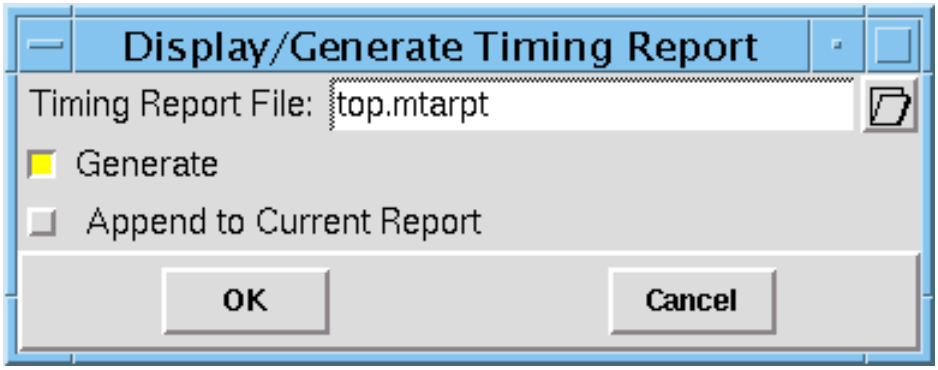
  The following form is displayed when you right-click on any path in the Timing Debug Browser:
  - Timing Debug on page 1371
- To edit table columns, right-click on any path in the Timing Debug Browser:
  - Timing Debug – Edit Table Column on page 1377
- To load global timing debug preferences, use the following form:
  - Timing Debug – Edit Table Columns – Load GTD Preferences File on page 1380

Display/Generate Timing Report

Use the Display/Generate Timing Report form to specify the violation report to be read in for debugging timing results. Alternatively you can choose to generate the violation report using the Generate option in this form.

Note: The violation report that you specify in this form has a special machine readable format. Use the `report_timing -machine_readable` command or `timeDesign -timingDebugReport` command to generate the machine readable violation report. If you want to generate a text-format report, generate a machine-readable report using this form, the run `write_text_timing_report`.

➤ Choose *Timing – Debug Timing*.



Display/Generate Timing Report Fields and Options

Timing Report File	Specify a filename, or click the file folder icon to choose a file.
Generate	Generates a violation report file in machine readable format. *Default:* `top.mtarpt`
Append to Current Report	Appends the specified report to the report that you have already loaded in a timing debug session. This feature is useful to collate reports from several views into one timing debug session.

Related Text Commands

The following text command provides equivalent or additional functionality:

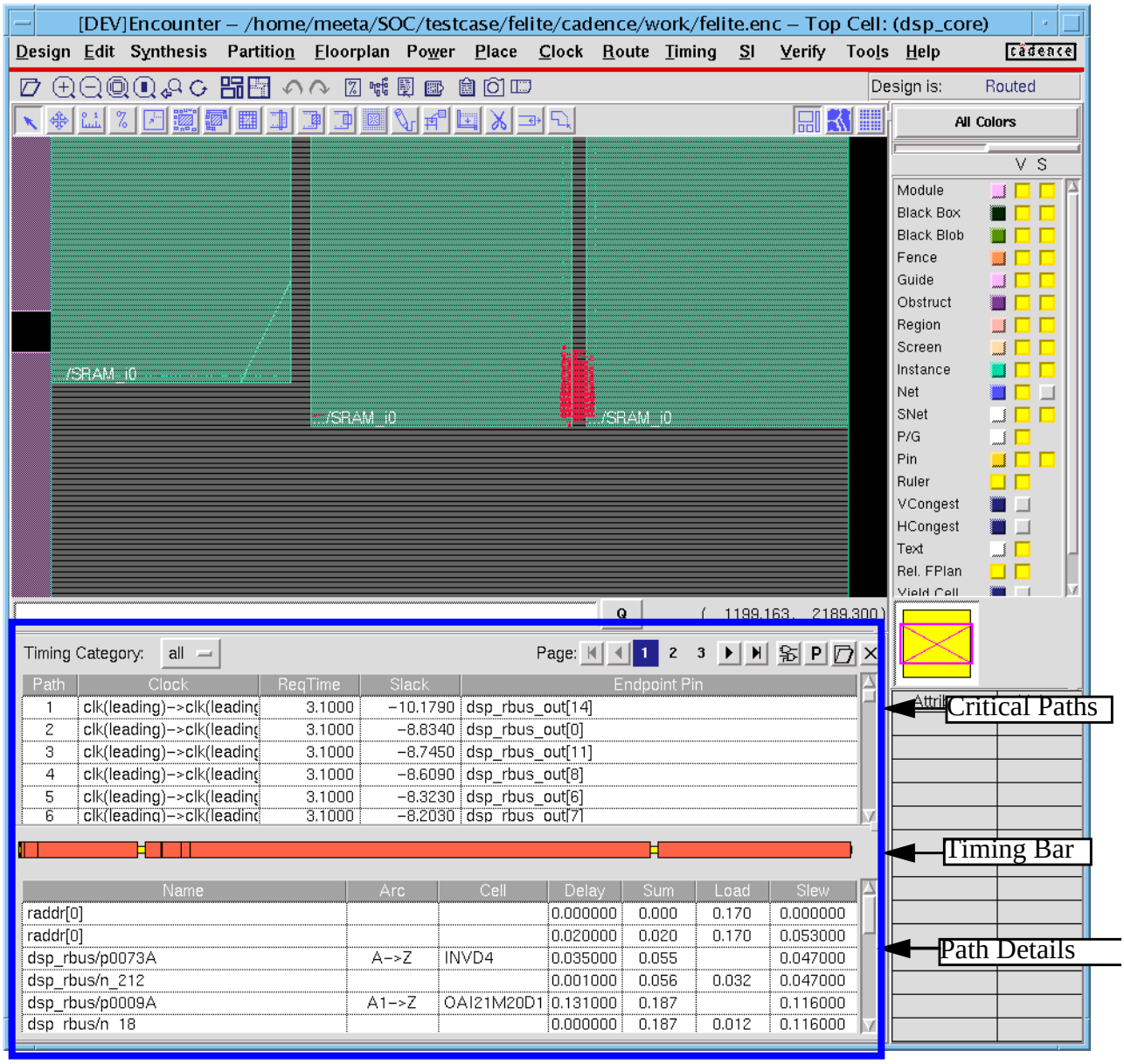
- `load_timing_debug_report`

For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Timing Debug – Browser

Use the browser window to display the violation and slack information that you generate during timing analysis.

➤ Choose *Timing – Debug Timing.*



The browser window consists of following three panes:

- *Critical Paths*

  Displays critical paths in the violation reports. You can select a path in this window to highlight it in the design display area and display the details in the *Detailed Paths* pane. For more information on cross-probing, see "Debugging Timing Results" in *Encounter User Guide*.

- *Timing Bar*

  Displays the instance and net bars. The size of the bar indicates the delay associated with that element. Moving the cursor on these elements displays the details of instances or nets. You can click on a single element to highlight it in the design display area. You can select each element consecutively to trace the entire path in the design display area.

  You can colorize the instances displayed in the timing bar based on the number of times the instances appear in violating paths. See "Timing Debug Preferences - Bottleneck Analysis" on page 1392.

  Note: Clear the highlights (*Edit – Clear Highlight – Clear All*) and selections (*Edit – Deselect All*) before using this feature.

  Right-click on the *Timing Bar* to display the following options:

Fit	Displays the bars for the entire path.
Zoom In	Displays more details about a bar.
Zoom Out	Displays more bars in the set area.
Preference	Displays the Timing Debug Preference form. Use this form to specify the statistics for the histogram and number of pages to be displayed in the Timing Debug form. You can also set the color of the various elements in the Timing Debug forms. The Timing Debug Preference form has the following option: *Show Schematic View*

Select this option to display the schematic. The Schematic Viewer displays the RTL-level or gate-level schematic view of the critical path that you select in the Timing Debug - Browser window.

To display the schematic, select this option, and double-click on the critical path in the Timing Debug - Browser window.

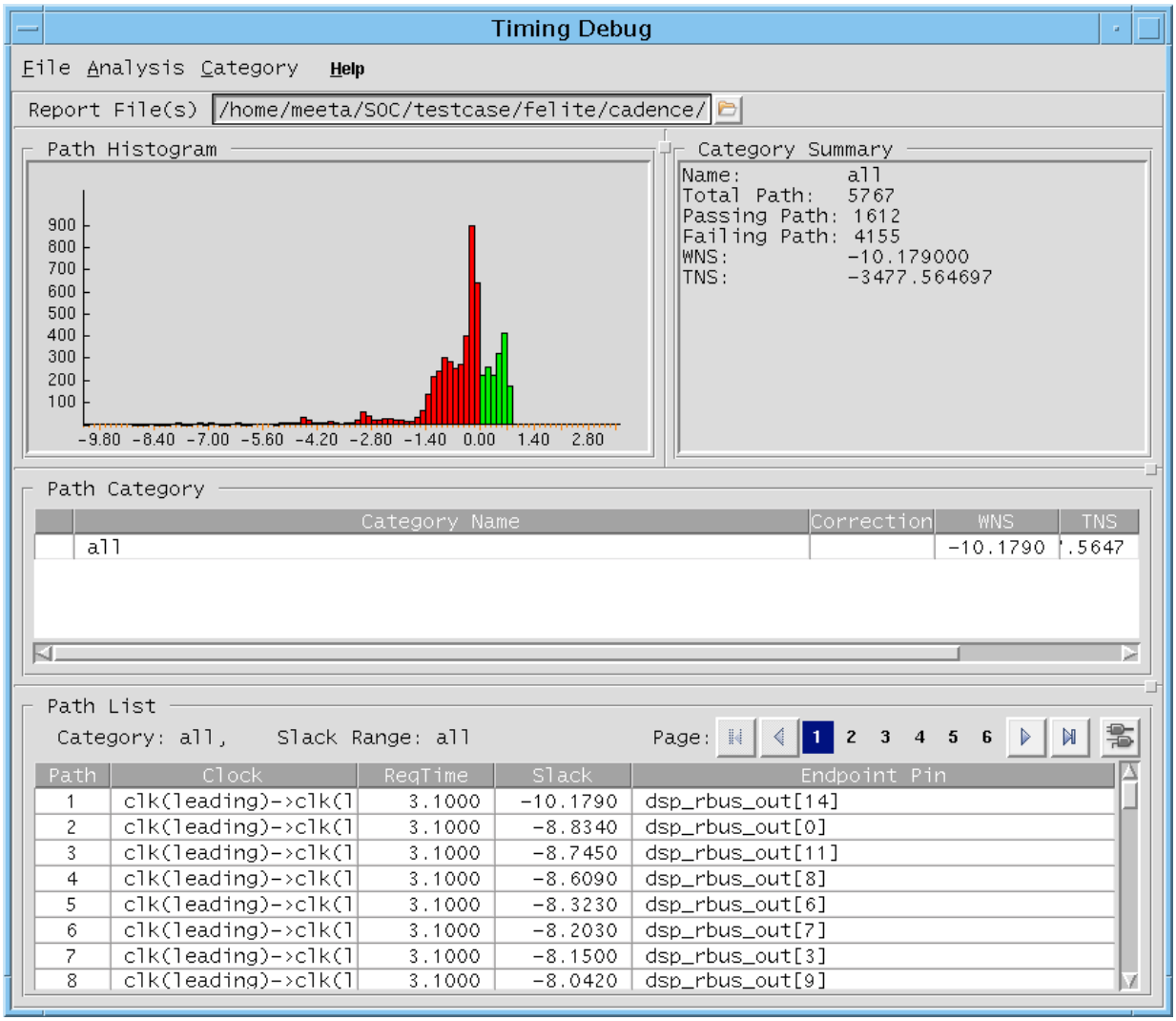
- *Path Details*

  Displays the details of the critical paths that you select in the *Critical Paths* pane. You can click on a single detail to display it in the design display area.

Timing Debug

Use the Timing Debug form to display the violation information, categories defined to group violation types, graphical display of violations, and category summary.

➤ Choose *Timing – Debug Timing.*



Timing Debug Fields and Options

File

Provides the following menu options:

Load report File

Displays the Display/Generate Timing Report form. Select or specify the name of the report file to be displayed in the Timing Debug window. For more information, see "Timing Debug – Timing Debug Preferences" on page 1387.

Preferences

Displays the Timing Debug Preferences form. For more information on the Timing Debug Preferences form, see "Timing Debug – Timing Debug Preferences" on page 1387.

Close

Closes the Timing Debug window.

Analysis

Displays menu options to create standard categories for timing debug. Following options are displayed:

Path Group Analysis

Displays Path Analysis form. Use this form to create standard path categories according to basic path groups. For more information, see "Path Analysis (Path Groups)" on page 1398.

Clock Analysis

Displays Path Analysis form. Use this form to create categories according to launch clocks - capture clock combinations.

For more information, see "Path Analysis (Clock Analysis)" on page 1400.

Hierarchical Analysis

Displays the Path Analysis form. Use this form to create categories according to the hierarchical characteristics of the paths. The software uses the floorplan file to extract information for guides, fences or Macros.

For more information, see "Path Analysis (Hierarchical Analysis)" on page 1402.

View Analysis

Displays the Path Analysis form. Use this form to create categories according to the views that were defined for multi-mode multi-corner analysis.

For more information, see "Path Analysis (View Analysis)" on page 1404.

Critical False Path

Displays the path analysis form. Use this form to create a category containing paths identified as false during the false path analysis by Conformal Constraint Designer (ccd).

Note: ccd should be in the command search path to access this menu.

Bottleneck Analysis

Displays the Path Analysis form. Use this form to create categories according to the bottleneck analysis of the critical paths.

For more information, see "Path Analysis (Bottleneck Analysis)" on page 1406.

Hierarchical AnalysisViewer

Displays the Hierarchical Analysis Viewer form.

Category

Displays menu options for creating and managing categories. Following options are displayed:

Create

Displays the Create Category form. Use this form to specify definitions for categories as per your design requirements.

For more information, see "Create Path Category" on page 1414.

Save

Saves the category definitions in a file. You can use this file to load a set of predefined categories into a new timing debug session.

Load

Loads the category definition file.

Path Histogram

Displays the end point histogram. The failing endpoints are displayed in red and the passing endpoints are displayed in green color.

Right-click on the histogram to display the following options:

Fit

Displays the entire histogram in Path Histogram area.

Zoom

Displays smaller or larger area of the histogram in greater or lesser detail.

Pan

Displays areas to the top, bottom, left or right of the displayed histogram.

Preference

Displays the Timing Debug Preferences form. Use this form to specify the statistics for the histogram and number of pages of report to be displayed in the form.

For more information on the Timing Debug Preferences form, see "Timing Debug – Timing Debug Preferences" on page 1387.

Category Summary

Displays the summary of a single selected category. To select a category, double-click on the category name in the *Path Category* field.

Path Category

Displays the category information. The columns in this field include, name of the category, worst negative slack (WNS), total negative slack (TNS), and number of failing paths. Right click on the category name to display the following options:

List Paths (Category Name)

Displays the detailed path information in the *Path List* field.

Add Category to Histogram

Displays the selected category as histogram. The added category is displayed in a different color. Use this option to identify paths grouped under a specific category.

Hide Category in Histogram

Removes the category from the histogram, but does not delete it. Hidden categories are indicated with the letter “H” to the left of the category name.

Set Category Slack Correction

Displays the Set Category Slack Correction form. Use this form to specify the estimated slack correction for the selected category of paths.

For more information, see “Manual Slack Correction of Categories” in the *Encounter User Guide*.

Edit Category Displays the Create Path Category form. Use this form to change category definition as per your requirements. For more information, see Create Category form.

Delete Category

Deletes the selected category.

Delete All Category

Deletes all categories that you have created.

Change Category Color

Displays Color Category Name form. Use this form to specify the color to be used in the Path Histogram for the selected category.

Copy Cell Copies the name of the category in the Path Category table. Use this feature to copy and paste the text from Path Category to Create Category form.

Edit Table Column

Displays the Edit Table Column form. Use this form to customize columns in the *Timing Debug* and *Timing Path Analyzer* windows.

Path List

Displays the list of paths (endpoint and slack) in the selected category. Double-click on a path to display the Timing Path Analyzer form. Use this form for detailed analysis of a single path. For more information on Timing Path Analyzer form, see "Timing Path Analyzer" on page 1420.

When you load multiple debug reports in a single timing debug session, the paths are displayed in different colors corresponding to the report file they are coming from. You can move the cursor over a path to display the name of the report file.

Displays the schematic view of the selected path.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_basic_path_group`
- `analyze_paths_by_bottleneck`
- `analyze_paths_by_clock_domain`
- `analyze_paths_by_critical_false_path`
- `analyze_paths_by_hierarchy`
- `analyze_paths_by_view`
- `create_path_category`
- `delete_path_category`
- `load_path_categories`
- `load_timing_debug_report`
- `save_path_categories`

For more information, see "Timing Debug Commands" in the *Encounter Text Command Reference*.

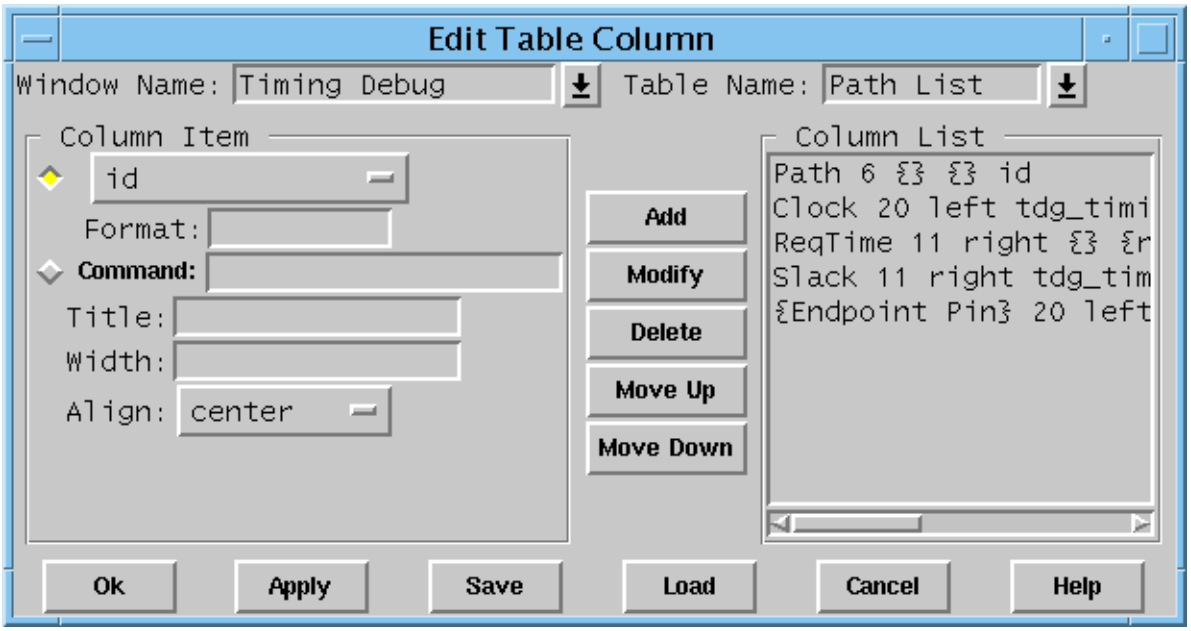
Timing Debug – Edit Table Column

Use the *Edit Table Column* form to customize columns in the *Timing Debug* and *Timing Path Analyzer* windows.

1. Open the *Timing Debug* or *Timing Path Browser* form, then right-click on a path.

   A drop-down menu is displayed.

2. Select *Edit Table Column*.



Edit Table Column Fields and Options

Window Name	Specifies the name of the window that contains the table column you want to edit. Choose from Encounter, Timing Debug, or Timing Path Analyzer.
Column Item	Specifies the type of information to include in the column. Choose from *delay*, *name*, *incr_delay*, *arrival*, *required*, *stolen*, *type*, *arc*, *cell*, *slew*, *fedge*, *tedge*, *constraint*, *load*, *pin,* or *fanout.*
Format	Specifies a table format. For example, specify `%.3f` if you only want to display three decimal digits.

Command

Specifies the procedure you want to use to determine the information you want to include in the column. In the procedure, you must pass the instance as a parameter. You must source the file containing procedure before specifying the procedure here.

For example:

```
# Combine fedge (from edge) and tedge (to edge)
#information into a single field

proc my_get_edge {id var} {
     upvar #0 $var p
     if {p(type) == "inst"} {
        return “$p(fedge) -> $p(tedge)"
     } elseif {$p(type) == "port" } {
        return $p(fedge)
     } else {
        return ""
     }
}
```

Title Specifies the column title.

Width Specifies the column width.

Align Specifies the alignment of the column. Choose from *center*, *left*, *right*, and *leftright*.

Table Name

Choose the table whose columns you want to modify:

- For the Timing Path Analyzer window choose *Data Path*, *Capture Clock*, or *Launch Clock*.
- For the Timing Debug window, choose *Path Category* or *Path List*.
- For the Encounter window, choose *Data Path*, or *Path List*.

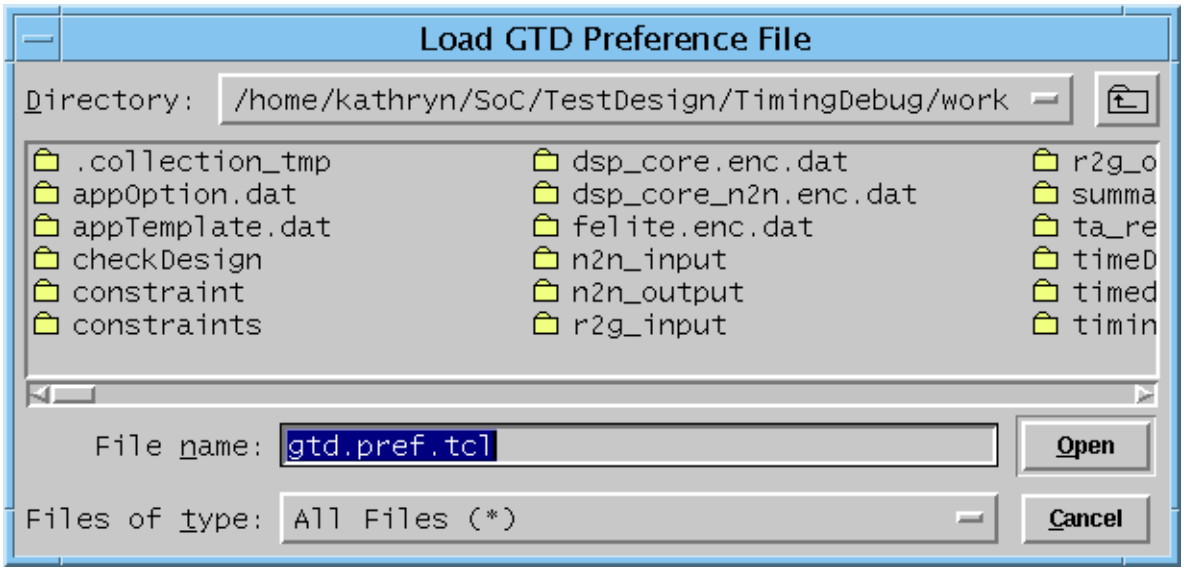
Column List	Lists the columns in the order in which they appear in the table, left to right. Each entry has the following information: ■ Column title (for example, Name, Arc, Delay) ■ The width of the column ■ The alignment of text in column (center, left, right, leftright) ■ Procedure, if any ■ The existing value from the path information
Add	Adds a column to the column list.
Modify	Let you modify characteristics. Click on a column in the column list. Edit the information, then click modify.
Delete	Deletes a column from the column list.
Move Up	Moves a column up in the column list. This effectively moves a column to the left in the table.
Move Down	Moves a column down in the column list. This effectively moves a column to the right table.
Load	Opens the GTD Preferences form.

Timing Debug – Edit Table Columns – Load GTD Preferences File

Use the *Load GTD Preferences* form to load a tcl command file to use for editing table columns.

1. On the *Timing Debug* or *Timing Path Browser* form, then right-click on a path.
2. Select *Edit Table Column*.

   The *Edit Table Column* form is displayed.
3. Click *Load*.



Timing Debug – Edit Table Columns – Load GTD Preferences File Fields and Options

File name	Specifies the file to load.

Timing Debug – File

The Timing Debug – File lets you choose the following forms:

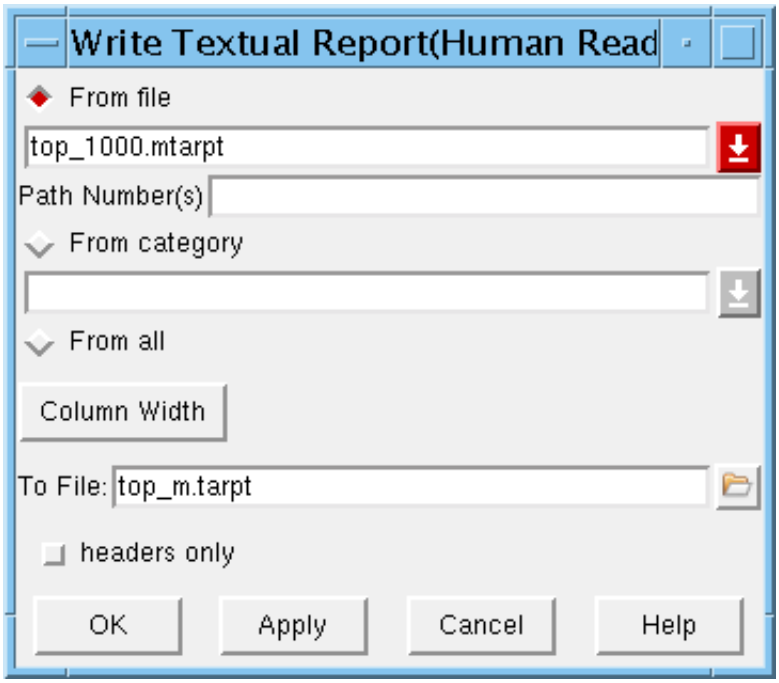
- Timing Debug – File – Write Text Report on page 1382
- Timing Debug – File – Column Width Table on page 1384
- Timing Debug – File – Write Category Report File on page 1386
- Timing Debug – Timing Debug Preferences on page 1387

Timing Debug – File – Write Text Report

Use the Write Text Report form to write a text file containing information about paths that have been loaded from a `.mtarpt` file from Timing Debug with the *Display/Generate Timing Report* form.

Note: The generated report cannot be read back into the timing debug environment.

➤ Choose *Write Text Report* on the *File* menu of the Timing Debug report form.



Timing Debug – Write Textual Report File Fields and Options

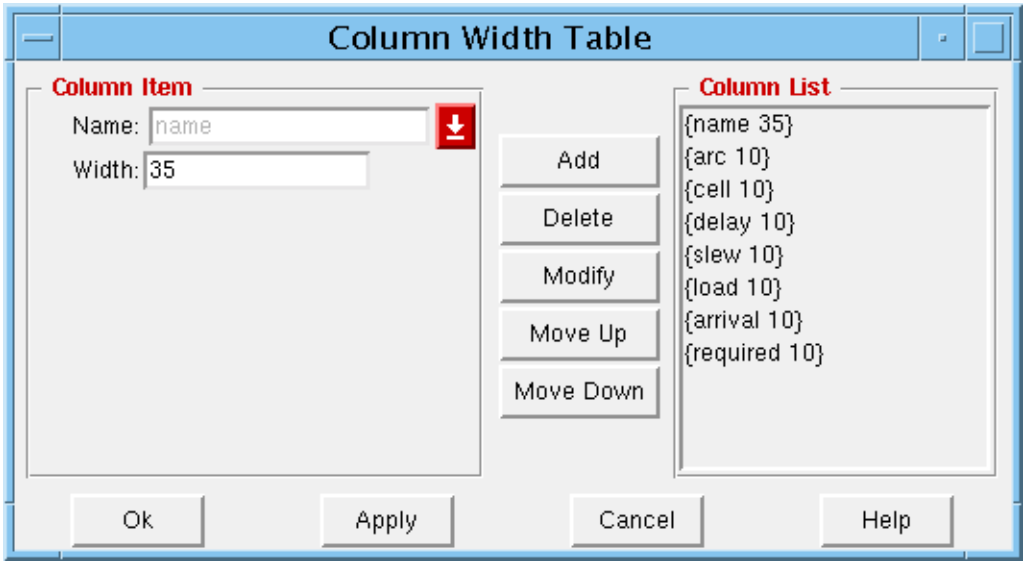
From file	Specifies the name of the `.mtarpt` file to read and convert to a text file. You cannot specify this parameter if you specify *From category*.
Path Number(s)	Writes a single number or path range separated by blank space " "or a comma ",". A path range is two numbers separated by a minus "-" sign. You can use this parameter only if a single file is specified or loaded.
From category	Specifies the category of paths to write to the text file.

From all	Writes all categories to the report file.
Column Width	Displays the Column Width Table form.
To File	Specifies the name of the text output file.
headers only	Writes the file header only. Use this parameter if you do not need a detailed table.

Timing Debug – File – Column Width Table

Use the Column Width Table form to change the width of the columns in the file created by the Write Textual Report form, and to specify the order in which you want to columns to appear.

➤ Choose *Write Text Report* from the *File* menu on the Timing Debug form, then click on the *Column Width* button.



Write Text Report – Column Width Table Fields and Options

Name	Specifies the name of the column to add, modify, or move in the column list.
Width	Specifies the width of the column.
Column List	Specifies a list of columns to create in the report generated by the Write Textual Report form.
Add	Adds a column to the column list.
Delete	Deletes a column from the column list.
Modify	Enables you to modify the width of a selected column.
Move Up	Moves the selected column up one position in the column list.

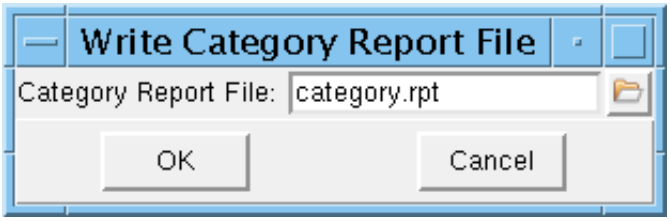
Move Down	Moves the selected column down one position in the column list.

Timing Debug – File – Write Category Report File

Use the Write Category Report File form to write a text file containing the following information:

- Category name
- Total number of paths
- Number of passing paths
- Number of failing paths
- Worst negative slack
- Total negative slack
- TNS

➤ Choose *File – Write Category Summary* on the Timing Debug form.



Timing Debug – Write Category Report Fields and Options

Category Report File	Specifies the name of the category output file. *Default*: `category.rpt`

Timing Debug – Timing Debug Preferences

The Timing Debug Preferences form enables you to set general display settings and colors for various elements.

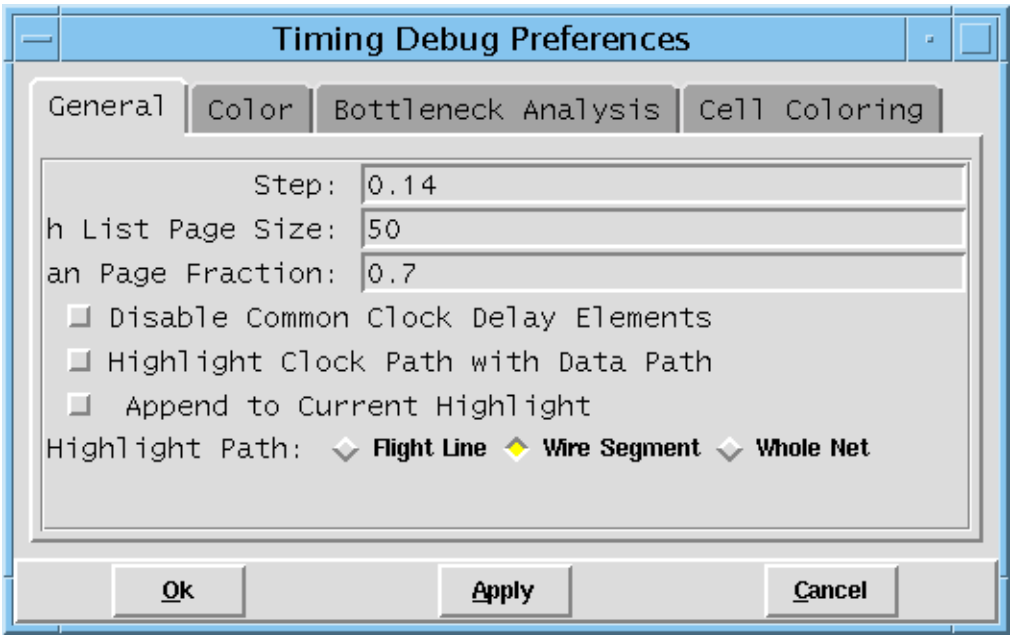
The Timing Debug Preferences form contains the following pages:

- Timing Debug Preferences - General on page 1388
- Timing Debug Preferences - Color on page 1390
- Timing Debug Preferences - Color – Set Color on page 1391
- Timing Debug Preferences - Bottleneck Analysis on page 1392
- Timing Debug Preferences - Set Color on page 1394
- Timing Debug Preferences - Cell Coloring on page 1395

Timing Debug Preferences - General

Use the *General* page of the Timing Debug Preferences form to specify the statistics for the histogram, number of pages of report to be displayed in the form, and highlighting options.

➤ Choose *Timing – Debug Timing - File - Preferences.*



Timing Debug Preferences Fields and Options

Step	Specifies the step size for the histogram.
Path List Page Size	Specifies number of pages of report to be displayed in the form.
Pan Page Fraction	Specifies the amount by which the histogram will be moved when you pan-in using the right-click options in the *Path Histogram* field in the Timing Debug window.
Disable Common Clock Delay Elements	Disables paths common to launch and capture clock in the *Data Delay* field of the *Timing Path Analyzer* form.
Highlight Clock Path with Data Path	Highlights clocks paths along with the data paths in the Design Display Area. By default, only data paths are highlighted.

Append to Current Highlight

Appends highlights to currently highlighted path.

Highlight Path

Specifies the preference for highlighting various paths. The color code used to highlight path is as follows:

Red: Launch clock path

Green: Paths specific to capture clock

White: Data path

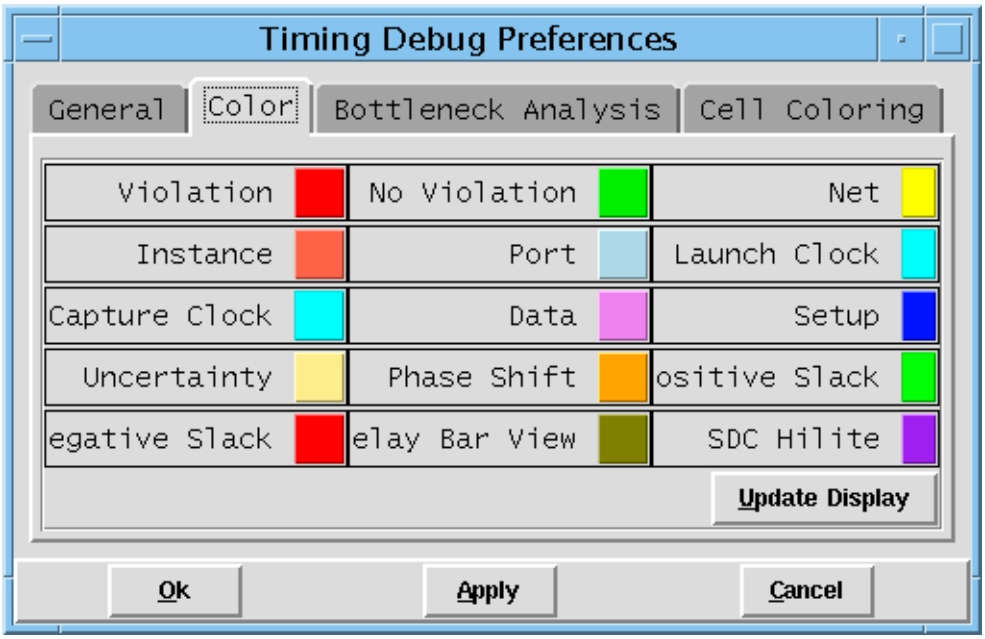
Choose from one of the following options:

Flight Line	Creates highlighted lines between the pins of the path.
Wire Segment	Highlights the wire segment.
Whole Net	Highlights all segments of the routing. The thickness of the highlight represents if the routing is part of the wire segments of the path (thicker) or if it is outside (thinner).

Timing Debug Preferences - Color

Use the *Color* page of the Timing Debug Preferences form to specify the colors for the slack calculation bar elements in the Timing Path Analyzer form.

➤ Choose *Timing – Debug Timing - File - Preferences*, and click on the *Color* tab.



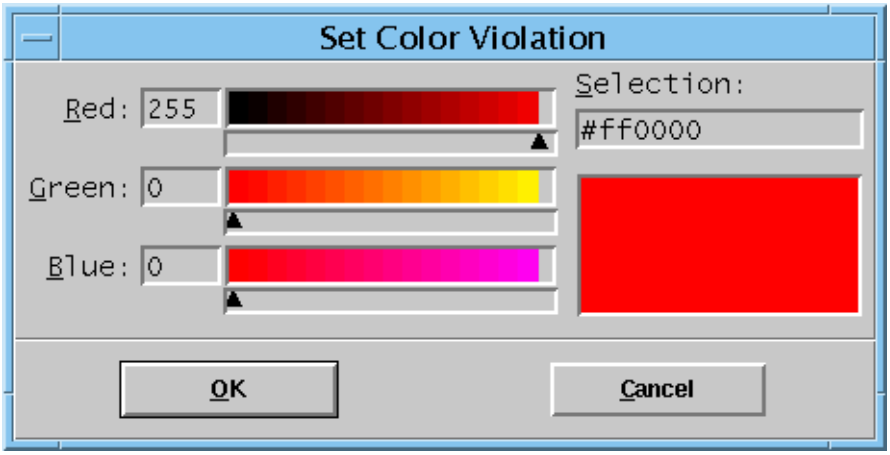
Timing Debug Preferences - Color Fields and Options

Elements	Displays the element name and the corresponding color that is used in the Slack Calculation field of the Timing Path Analyzer form. Click on a color square to display the *Set Color <Element>* form, which enables you to customize a color.
Update Display	Immediately applies the color selections to the display.
Apply	Stores the selected color information

Timing Debug Preferences - Color – Set Color

Use the *Set Color <Element Name>* form lets you customize the colors displayed on the Timing *Debug Preferences – Color* page.

➤ Choose *Timing – Debug Timing - File - Preferences*, click on the *Color* tab, then click on any colored square.



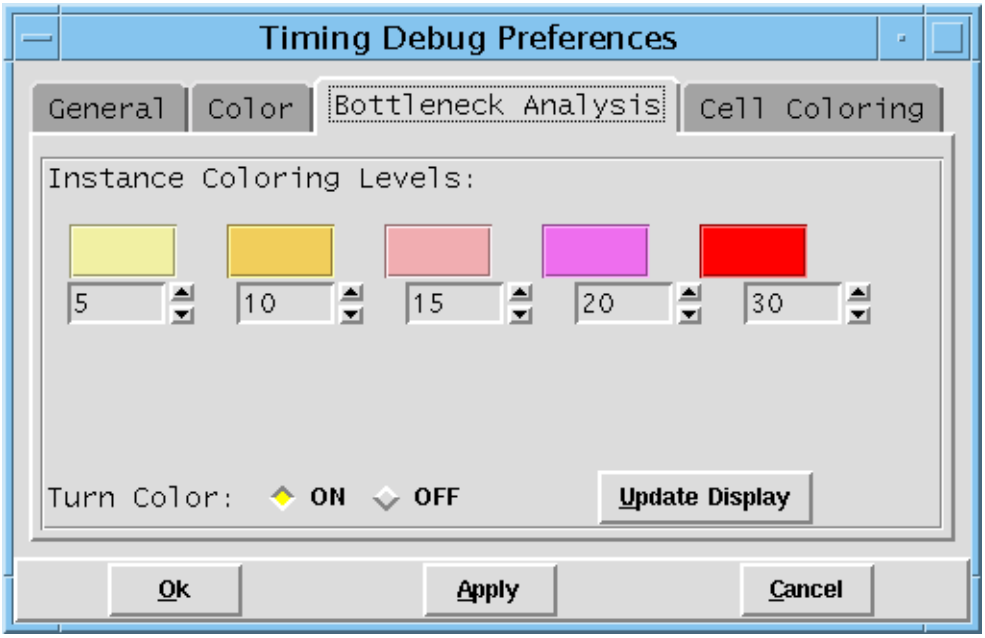
Timing Debug Preferences - Color - Set Color Violation Fields and Options

Elements	Sliders let you set the hue for the red, green, and blue colors comprising your custom color.

Timing Debug Preferences - Bottleneck Analysis

Use the *Bottleneck* page of the Timing Debug Preferences form to colorize cells based on the occurrences of violating paths.

➤ Choose *Timing – Debug Timing - File - Preferences*, and click on the *Bottleneck Analysis* tab.



Timing Debug Preferences - Bottleneck Analysis Fields and Options

Instance Coloring Levels

Specifies color corresponding to the number of times an instance can appear in the violating path. In the delay bar in on the Timing Path Analyzer GUI, the tool colorizes cells accordingly.

In this example, cells appearing in greater than five and 10 violating paths will be colored yellow. Cells appearing in between 10 and 15 times will be colored orange. Cells appearing in between 15 and 20 times will be colored pink. Cells appearing in between 20 and 30 times will be colored fuchsia and cells appearing more than 30 or more times will be colored red.

Turn Color	Specifies how the tool colorizes the instances.	
	ON	Displays the colors you selected.
	OFF	Uses the default colors.
Update Display	Immediately applies the color selections to the display.	
Apply	Stores the selected color information	

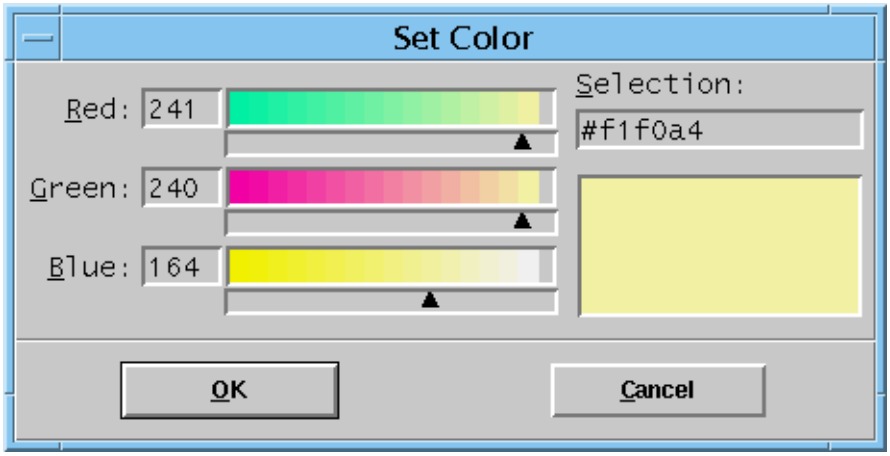
Timing Debug Preferences - Set Color

Use the *Set Color* form to set custom colors for the *Bottleneck Analysis* and *Cell Coloring* form.

➤ Choose *Timing – Debug Timing - File - Preferences*, click on the *Bottleneck Analysis* tab, then click on a color.

or

➤ Choose *Timing – Debug Timing File – Preferences*, click on the *Cell Coloring* tab, then click on a color.



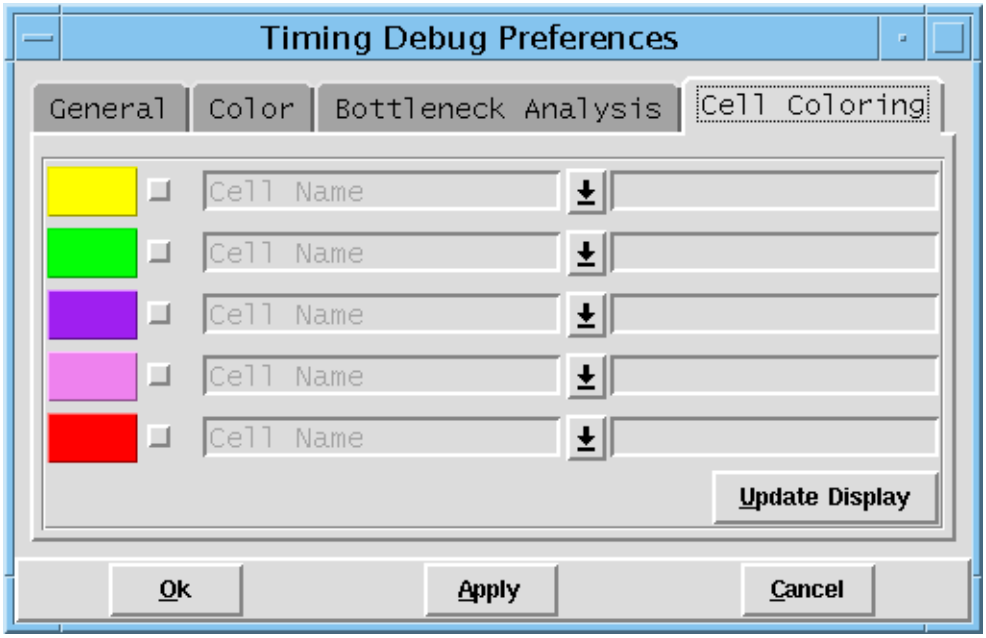
Timing Preferences – Set Color Fields and Options

Elements	Sliders let you set the hue for the red, green, and blue colors comprising your custom color.

Timing Debug Preferences - Cell Coloring

Use the *Cell Coloring* page of the Timing Debug Preferences form to choose colors for specific cells in the delay bar. Color precedence is top to bottom in this form. If you set coloring in a session, the software saves the settings and restores them in the next session.

➤ Choose *Timing – Debug Timing - File - Preferences*, and click on the *Cell Coloring* tab.



Timing Debug Preferences - Cell Coloring Fields and Options

Color elements	Shows the available colors. To customize colors, click on the color. The *Set Color* form is displayed.
Check Box Elements	Indicates whether you want to apply the color to the specified cells.

Cell Name Selection Elements

For each color, you can choose to provide one of the following

- Cell name
- Instance
- Procedure that you have defined.

The procedure is invoked with the full instance name as the argument. You must source the file containing the procedure before you use this feature. For an example, see "Cell Coloring."

Name Elements

Lets you enter the cell names or procedure name. You can use wildcards when you specify cells, for example: `INV*`, `BUF*`, `DLY*`, `HVT*`.

Timing Debug – Analysis

The Timing Debug – Analysis menu provide the following forms for timing path analysis:

- Path Analysis (Path Groups) on page 1398
- Path Analysis (Clock Analysis) on page 1400
- Path Analysis (Hierarchical Analysis) on page 1402
- Path Analysis (View Analysis) on page 1404
- Path Analysis (Bottleneck Analysis) on page 1406
- Path Analysis (DRV Analysis) on page 1408
- Path Analysis (False Path Analysis) on page 1410

The menu also provides the following analysis view form:

- Hierarchical Analysis Viewer on page 1412

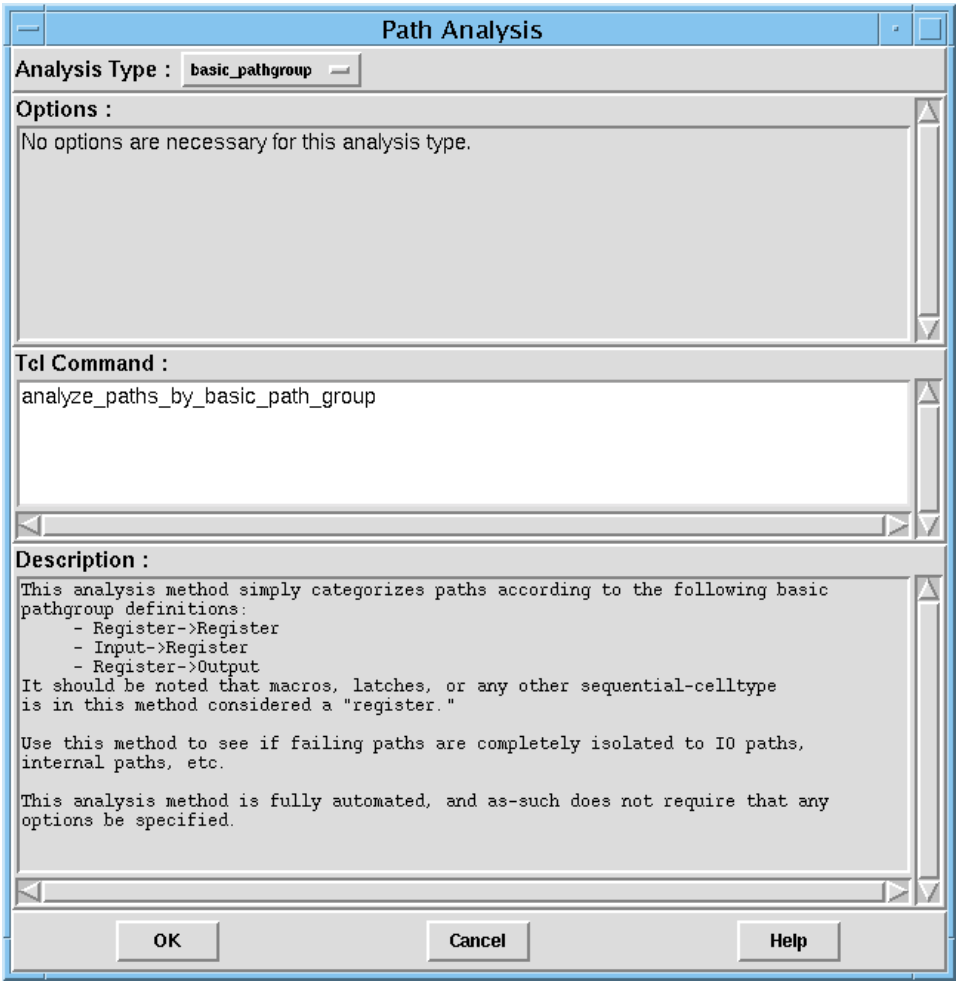
Path Analysis (Path Groups)

Use the Path Analysis form to create standard path categories according to basic path groups. The basic path groups are:

- Register to register
- Input to register
- Register to output
- Input to Output

Registers can be macros, latches, or sequential-celltypes.

➤ Choose *Timing – Debug Timing - Analysis - Path Group Analysis.*



Path Analysis (Path Groups) Fields and Options

Options	There are no additional options for this analysis.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_basic_path_group`

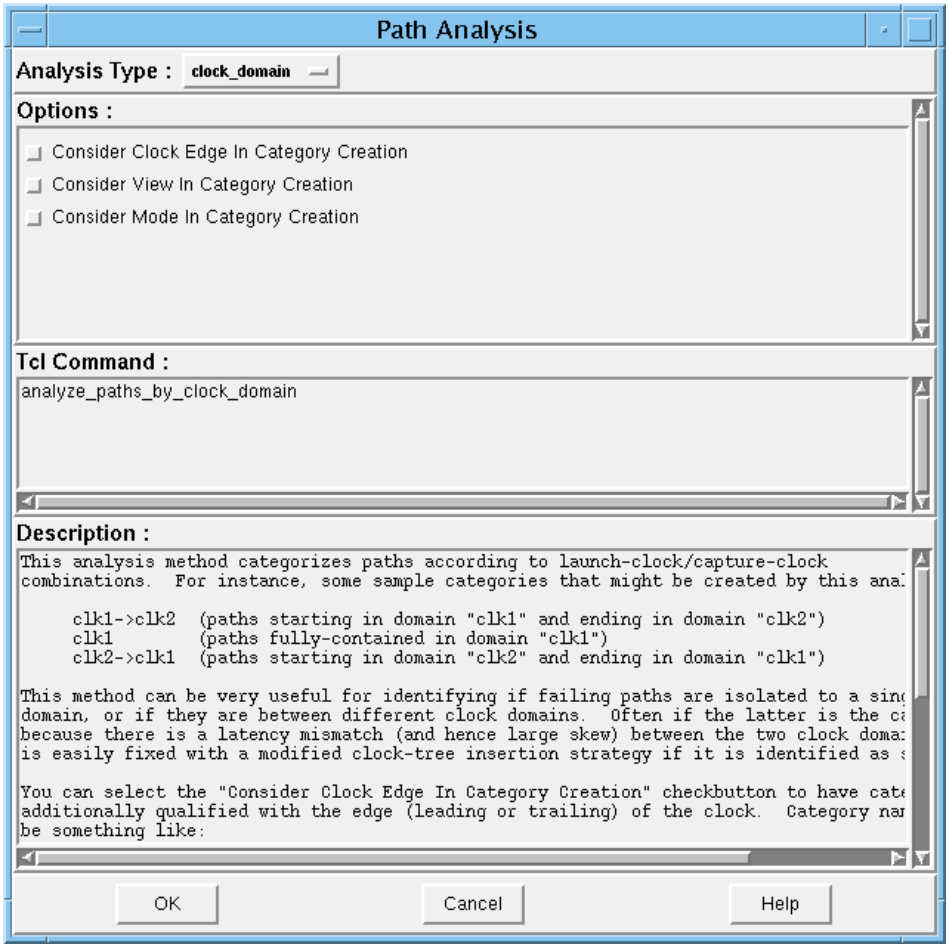
For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Path Analysis (Clock Analysis)

Use the Path Analysis form to create categories according to launch clock–capture clock combinations. Following categories are created:

- Paths with clock fully contained in a single domain, clk1.
- Paths with clocks starting one clock domain and ending at another, clk1->clk2.

➤ Choose *Timing – Debug Timing - Analysis - Clock Analysis.*



Path Analysis (Clock Analysis) Fields and Options

Consider Clock Edge in Category creation (Optional)

Considers leading or trailing edge of the clock while defining categories.

Consider View in Category Creation

Considers views while defining categories. The paths are sorted according to the clock(s) and the view, for example: Clock1<View1> Clock1<View2> ...

Consider Mode in Category Creation

Considers modes while defining categories. The mode is retrieved from the view definition loaded into the design, then the paths are sorted according to the clocks and the mode, for example: Clock1<Mode1> Clock1<Mode2>...

Tcl Command Displays the name of the text command that you can specify instead of using the GUI.

Description Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_clock_domain`

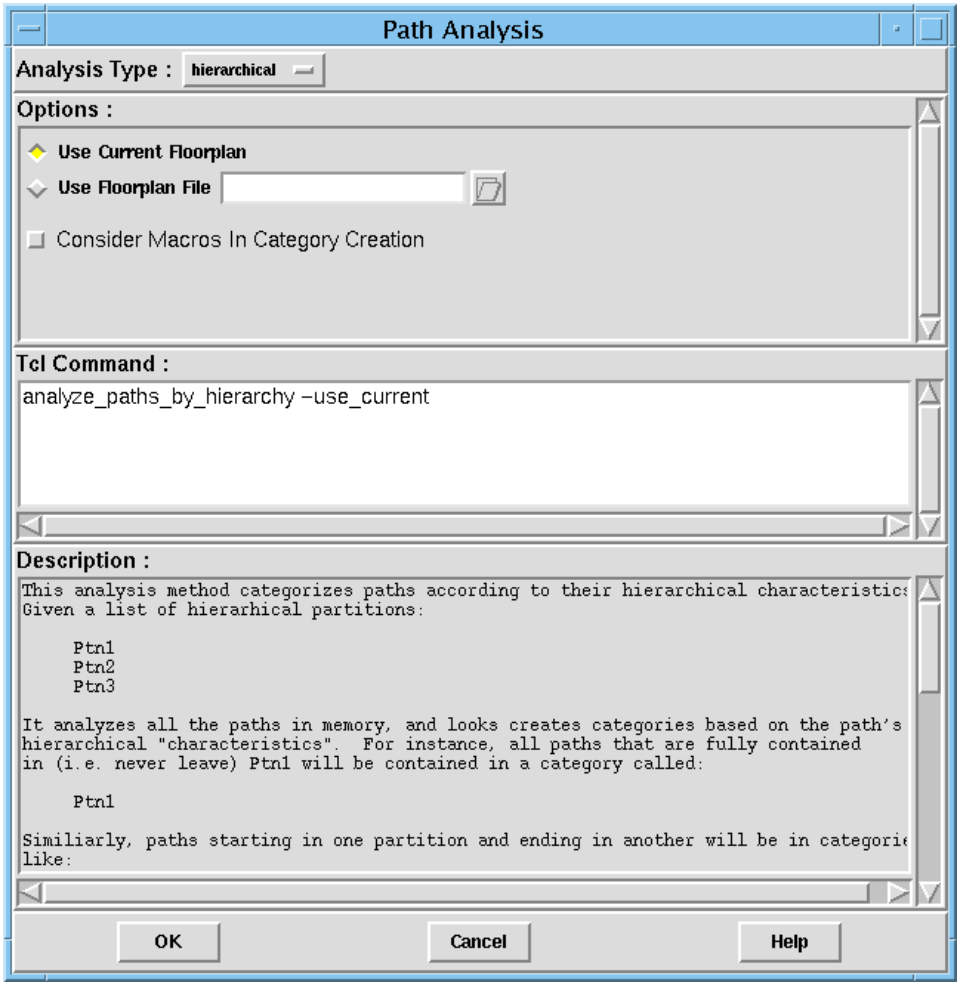
For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Path Analysis (Hierarchical Analysis)

Use the Path Analysis form to create categories according to the hierarchical characteristics of the paths. The software uses the floorplan file to extract information for guides, fences or Macros. Following categories are created:

- All paths fully contained in a single partition, Ptn1.
- Paths starting in one partition and ending in another partition, Ptn1->Ptn2.
- Paths spanning several partitions, Ptn1->Ptn2->Ptn3.
- Top-level inputs to partitions, INPUT->Ptn1.
- Paths from partitions to top-level outputs, Ptn1->OUTPUT.

➤ Choose *Timing – Debug Timing - Analysis - Hierarchical Analysis.*



Path Analysis (Hierarchical Analysis) Fields and Options

Use Current Floorplan	Uses the current floorplan for hierarchical analysis.
Use Floorplan File	Specify the name of the floorplanning file to be used for extracting the object information.
Consider Macros In Category Creation	
	Considers macros in addition to guides and fences for creating categories. By default, macros are not considered.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze paths by hierarchy`

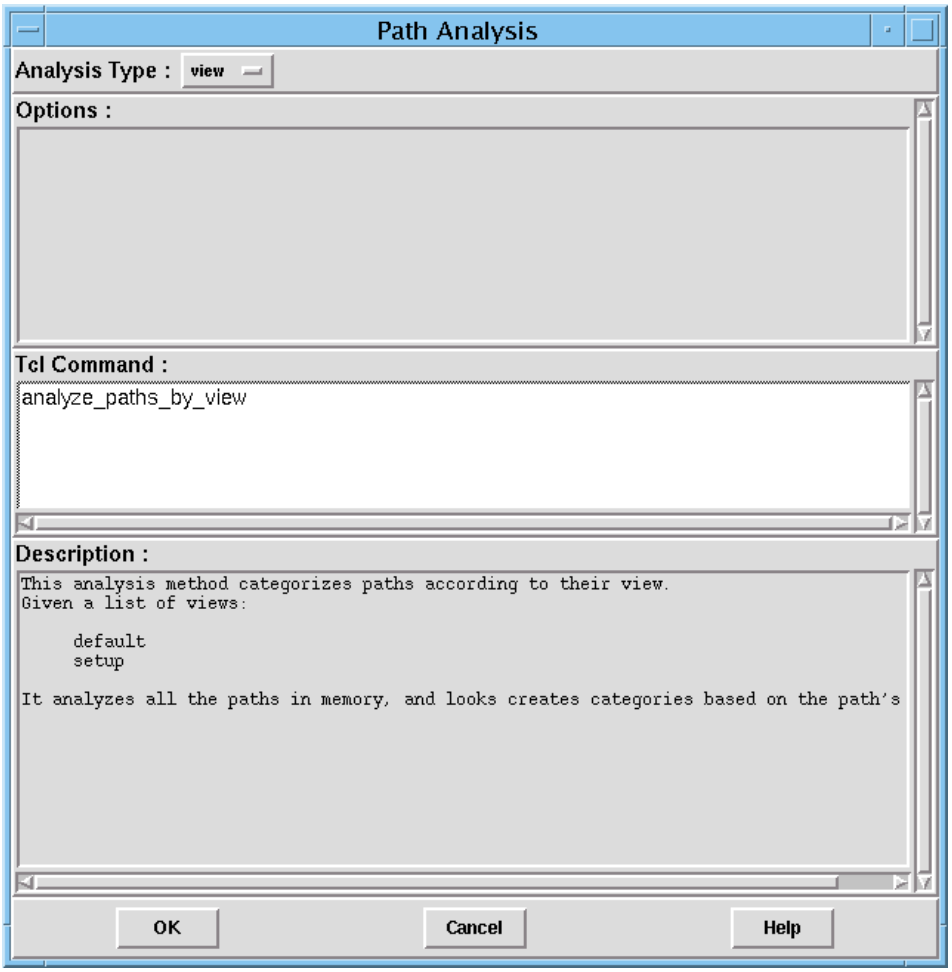
For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Path Analysis (View Analysis)

Use the Path Analysis form to create categories according to the view that each path is related to. You can analyze the impact of each view on the performance using this category.

Note: In a single report (report containing all views together) each endpoint is reported once. On the other hand, when you load several reports that were generated for different views, each endpoint may appear in each report with a different slack value.

➤ Choose *Timing – Debug Timing - Analysis - View Analysis.*



Path Analysis (View Analysis) Fields and Options

Options	There are no additional options for this analysis.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `analyze_paths_by_view`

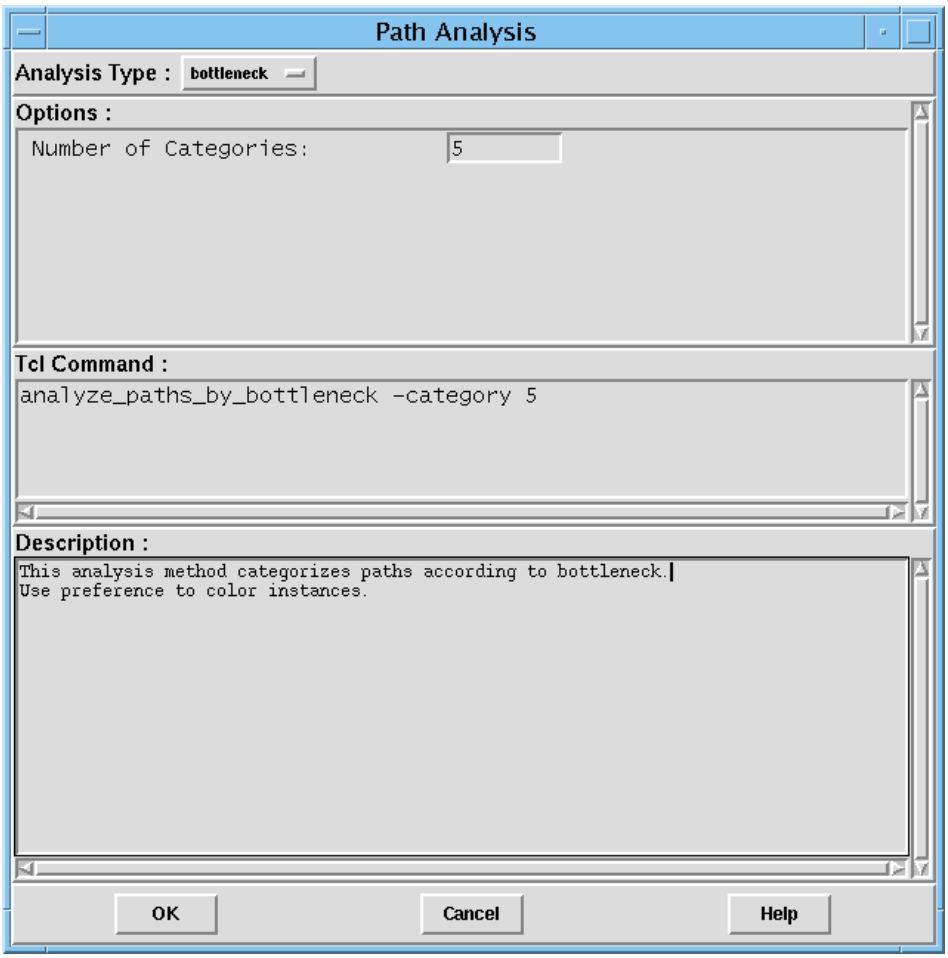
For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Path Analysis (Bottleneck Analysis)

Use the Path Analysis form to create categories according to the bottleneck analysis of the critical paths. Bottleneck Analysis detects the instances that are often involved in the critical paths in the design. Any change in timing for these instances impacts multiple critical paths in the design. Therefore you can use this information to change your design (floorplan, placement, constraints etc.) around these instances. The bottleneck analysis computes the number of occurrences that an instance appears in the paths that you display in the Timing Debug window, and provides the following output:

- Colors most used instance based on number of occurrences.
- Creates *N* number of path categories for the instances with the highest number of occurrences. *N* is the number you specify in the Path Analysis form.

➤ Choose *Timing – Debug Timing - Analysis - Bottleneck Analysis.*



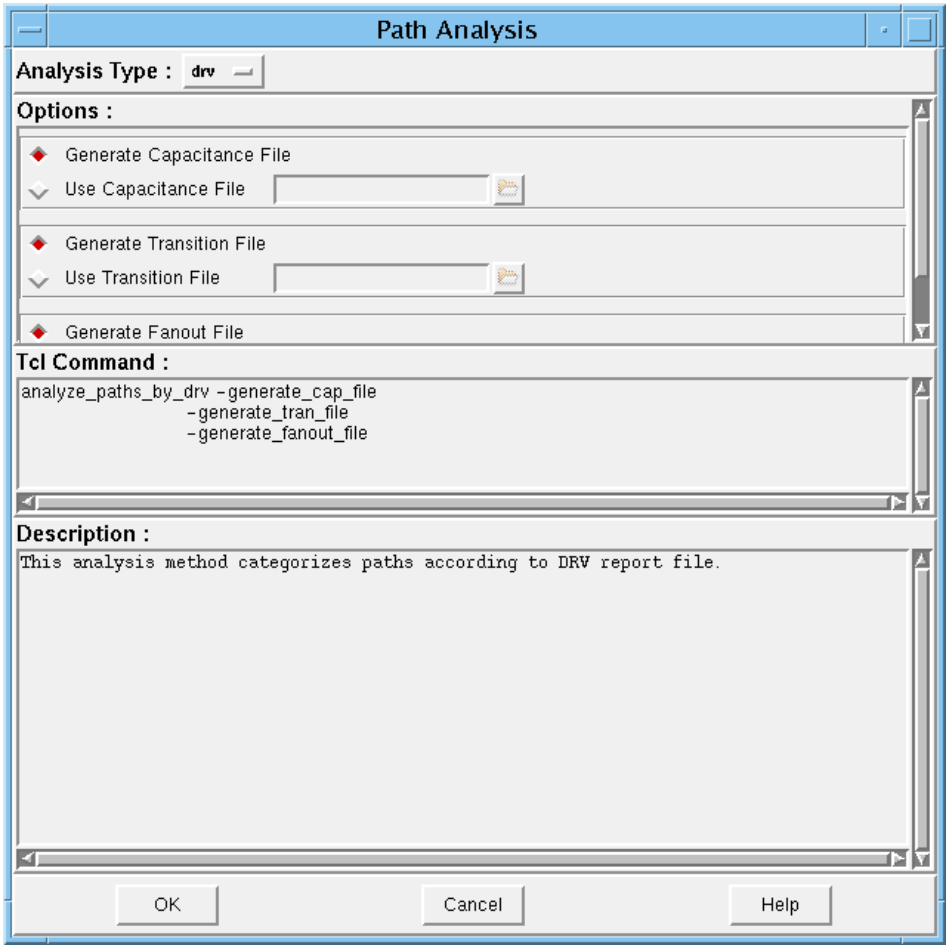
Path Analysis (Bottleneck Analysis) Fields and Options

Number of Categories	Specifies the number of categories to be created for most occurring instances. To specify the number of instances to be grouped in one category and related colors, use the Timing Debug preferences form. For more information on the Timing Debug Preferences form, see "Timing Debug – Timing Debug Preferences" on page 1387.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Path Analysis (DRV Analysis)

Use the Path Analysis form to read or generate a report containing max transition, max capacitance, and max fanout violations. Paths that are affected by the selected DRV type are grouped into a category.

➤ Choose *Timing – Debug Timing - Analysis - drv.*



Path Analysis (drv) Fields and Options

Generate Capacitance File

Generates a file containing a list of paths containing max capacitance violations.

Use Capacitance File

Reads a file containing a list of paths containing max capacitance violations.

Generate Transition File

Generates a file containing a list of paths containing max transition violations.

Use Transition File

Reads a file containing a list of paths containing max transition violations.

Generate Fanout File

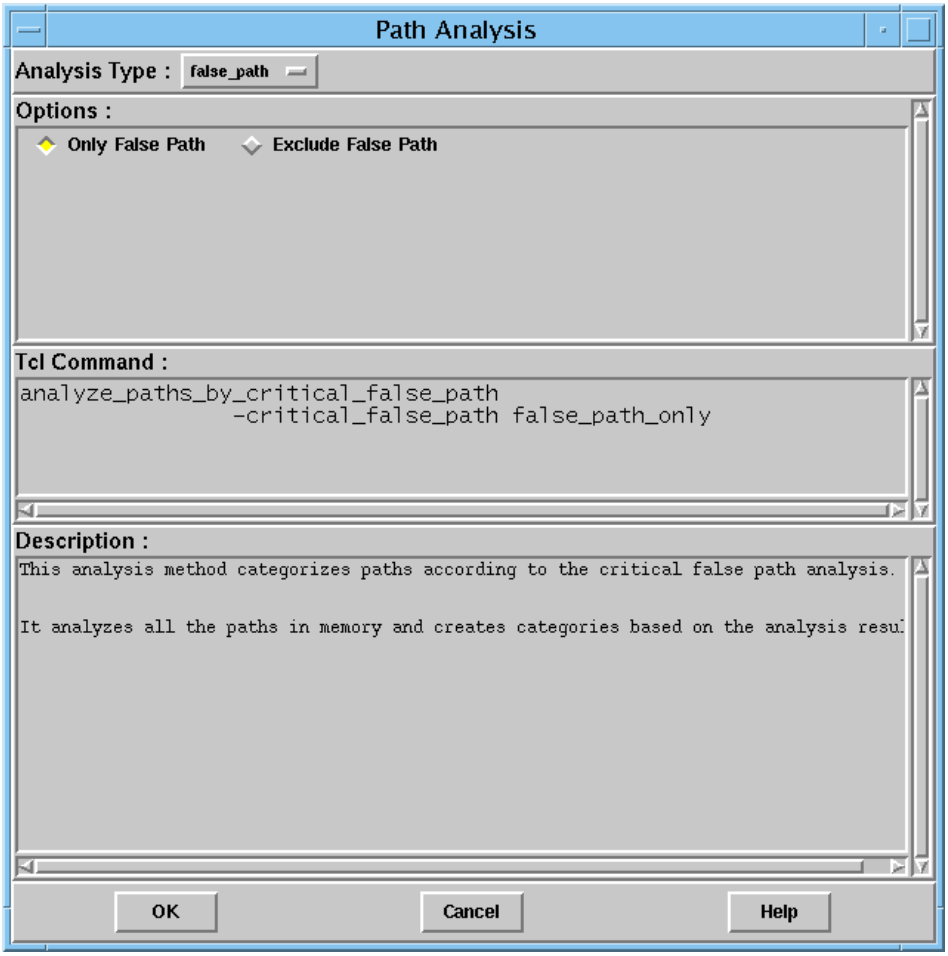
Generates a file containing a list of paths containing max fanout violations.

Use Fanout File Reads a file containing a list of paths containing max fanout violations.

Path Analysis (False Path Analysis)

Use the Path Analysis form to determine whether the reported paths are real critical paths. The analysis is performed by the Conformal Constraint Designer (CCD). As a result of this analysis, the tool creates a category in the *Global Timing Debug* window that contains either the violating paths only, or violating paths except for false paths.

➤ Choose *Timing – Debug Timing - Analysis - Path Analysis.*



Path Analysis (False Path Analysis) Fields and Options

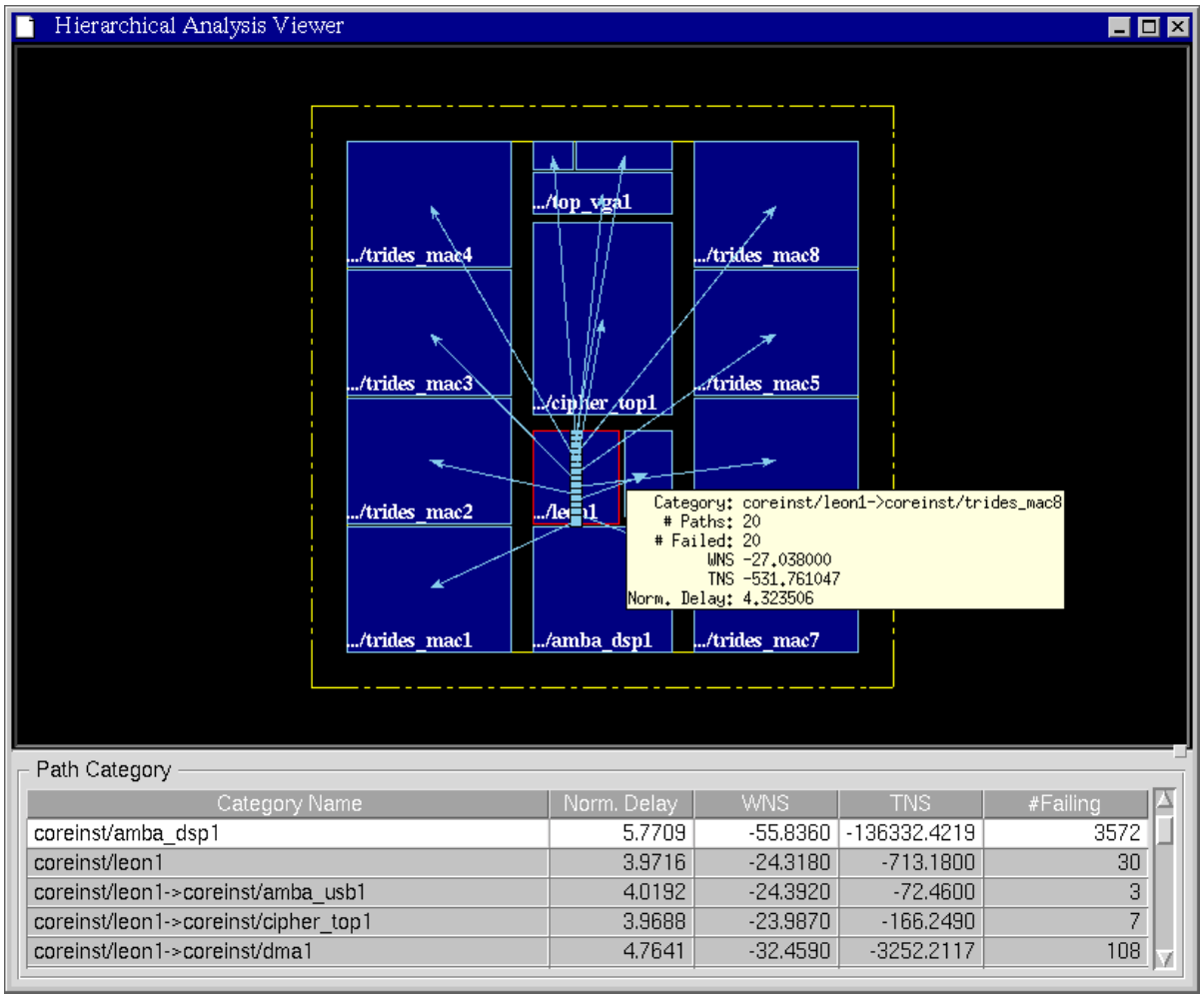
Only False Path	Creates a category containing violating false paths only.
Exclude False Path	Creates a category containing all paths other than false paths.
Tcl Command	Displays the name of the text command that you can specify instead of using the GUI.
Description	Displays the details of the categories that are created when you select the OK button.

Hierarchical Analysis Viewer

Use the Hierarchical Analysis Viewer form to view the results from hierarchical analysis that is done when you create the hierarchical paths category.

For more information on creating the hierarchical paths category, see "Path Analysis (Hierarchical Analysis)" on page 1402.

➤ Choose *Timing – Debug Timing - Analysis - Hierarchical Analysis Viewer.*



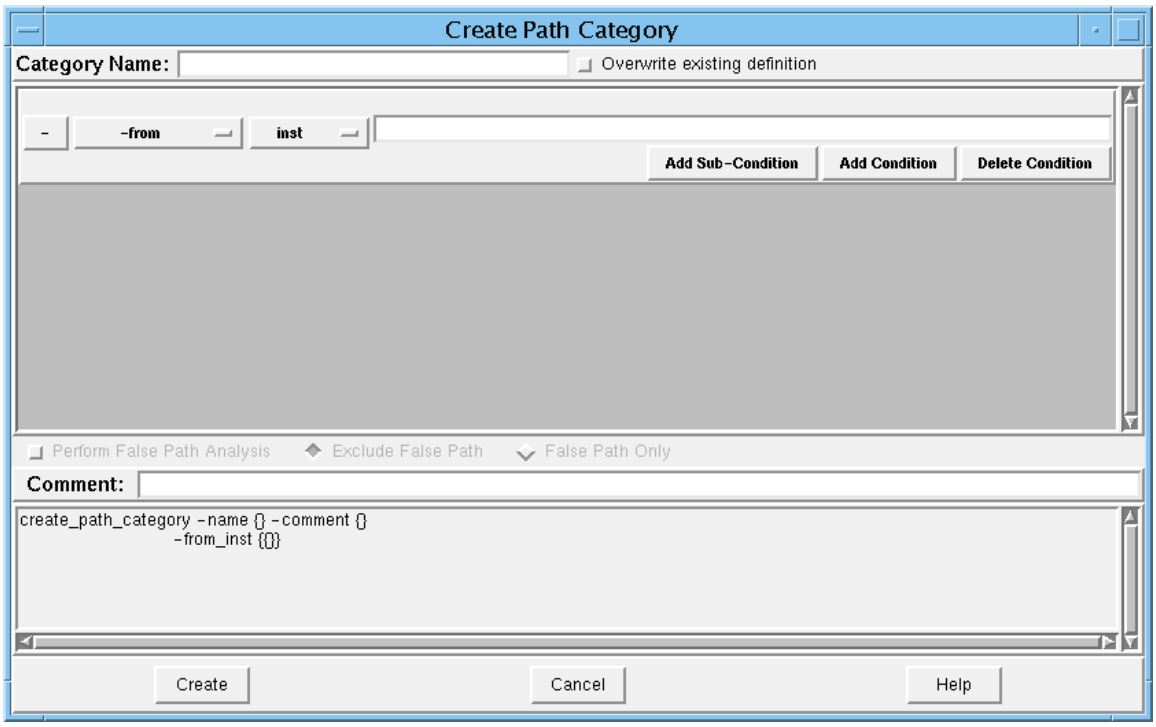
Hierarchical Analysis Viewer Fields and Options

FloorPlan Display Area	Displays the timing connectivity between floorplan modules or partitions.
Path Category	Displays the paths that are grouped in the hierarchical path category.

Create Path Category

Use the Create Path Category form to define the categories as per your design requirements. You can use the Timing Path Analyzer form to analyze the critical paths and identify possible problems with the design. You can then use the Create Path Category form to define a category or categories to group all paths with same problem.

➤ Choose *Timing – Debug Timing - Category - Create Category.*



Create Path Category Fields and Options

Category Name

Specify the name of the category.

Note: The values that you specify in this form are reflected as Tcl command in the display area at the bottom of the form.

Overwrite existing definition

Overwrites any predefined category with the same name in your category list.

Definition

Define category using the pull down menu options beginning with *-from* and *inst*.

Choose from the following options:

-from

-not_from

-through

-not_through

-to

-not_to

Choose from the following options:

- *inst*
- *pin*
- *cell*
- *clock*
- *port*

For example, you can choose *-from cell XYZ*.

-slack

-uncertainty

-skew

-launch_latency

-capture_latency

Choose from the following options:

- `==`
- `!=`
- `>`
- `<`
- `>=`
- `<=`

For example, you can choose *-uncertainty* `>= 0.4`.

-check_type

Choose from the following options:

- *Setup Check*
- *Hold Check*
- *Clock Gating Setup Check*
- *Library Clock Gating Setup Check*
- *Clock Gating Hold Check*
- *Library Clock Gating Hold Check*
- *External Delay Assertion*
- *Latch Borrowed Time Check*
- *PulseWidth Check*
- *ClockPeriod Check*
- *Recovery Check*
- *Removal Check*

-number_of

Specify number of instances with required operator. Optionally you can choose from the following options:

- *of_name*
- *not_of_name*
- *of_celltype*
- *not_of_celltype*

For example, you can specify *-number_of insts of_name* `INST1` *!=* `4`.

-delay_of

Specify the value for one of the following options:

- *any_inst*
- *any_net*
- *every_inst*
- *every_net*

For instances, you can optionally choose from the following options:

- *of_name*
- *not_of_name*
- *of_celltype*
- *not_of_celltype*

For example, you can specify *-delay_of any_inst of_name* `INST1 = 0.5`.

For nets, you can optionally choose from the following option:

- *of_name*
- *not_of_name*

For example, you can specify *-delay_of any_net of_name* `clk = 0.1`.

	-total_delay_of	Specify the value for one of the following options: path insts nets For instances, you can optionally choose from the following options: ■ *of_name* ■ *not_of_name* ■ *of_celltype* ■ *not_of_celltype* For example, you can specify *-total_delay_of inst of_name* `INST1 = 0.5`. For nets, you can optionally choose from the following options: ■ *of_name* ■ *not_of_name* For example, you can specify *-total_delay_of net of_name* `clk = 0.1`.
	-view	Specify the name of the view. The paths related to the specified view are grouped under this category.
	-file	Specify the name of the file that contains definitions for creating categories.
Add Sub-Condition	Adds a row for definition an OR sub-condition for the named category.	
Add Condition	Adds a row for definition an AND sub-condition for the named category.	
Delete Condition	Deletes defined condition.	
Comment	Allows you to enter any comment to associate with the condition.	

Related Text Commands

The following text command provides equivalent or additional functionality:

- `create_path_category`

For more information, see “Timing Debug Commands” in the *Encounter Text Command Reference*.

Timing Path Analyzer

Use the Timing Path Analyzer form to analyze a single path in detail. The various elements in the form help in identifying possible issues related to a particular path.

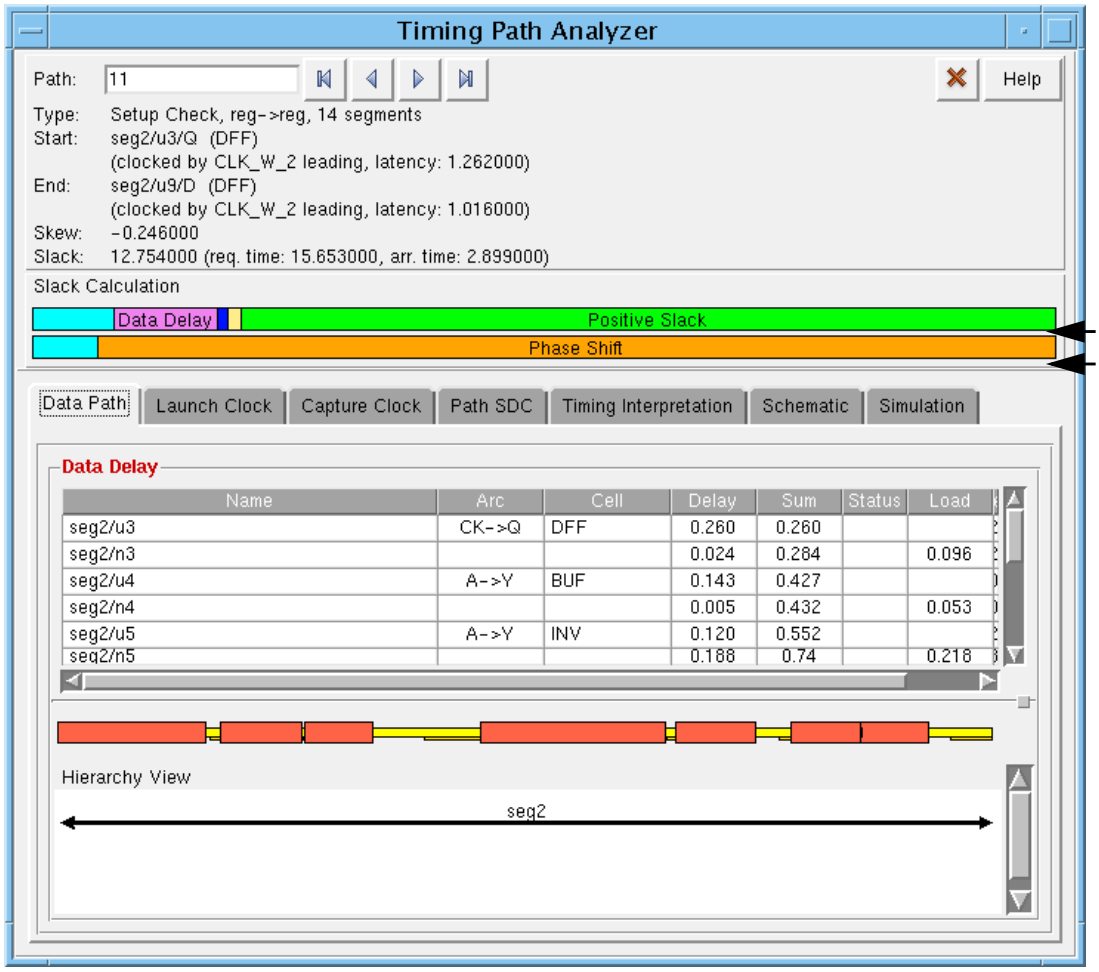
The Timing Path Analyzer form has the following five tabs:

- Timing Path Analyzer - Data Path on page 1421
- Timing Path Analyzer - Launch Clock on page 1423
- Timing Path Analyzer - Capture Clock on page 1425
- Timing Path Analyzer - Path SDC on page 1427
- Timing Path Analyzer – Timing Interpretation on page 1429
- Edit Timing Interpretation on page 1432
- Timing Path Analyzer - Schematics on page 1435

Timing Path Analyzer - Data Path

Use the Timing Path Analyzer - Data Path form to identify issues related to a path using slack calculation bars, timing bar, and hierarchy view.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.



Timing Path Analyzer - Data Path Fields and Options

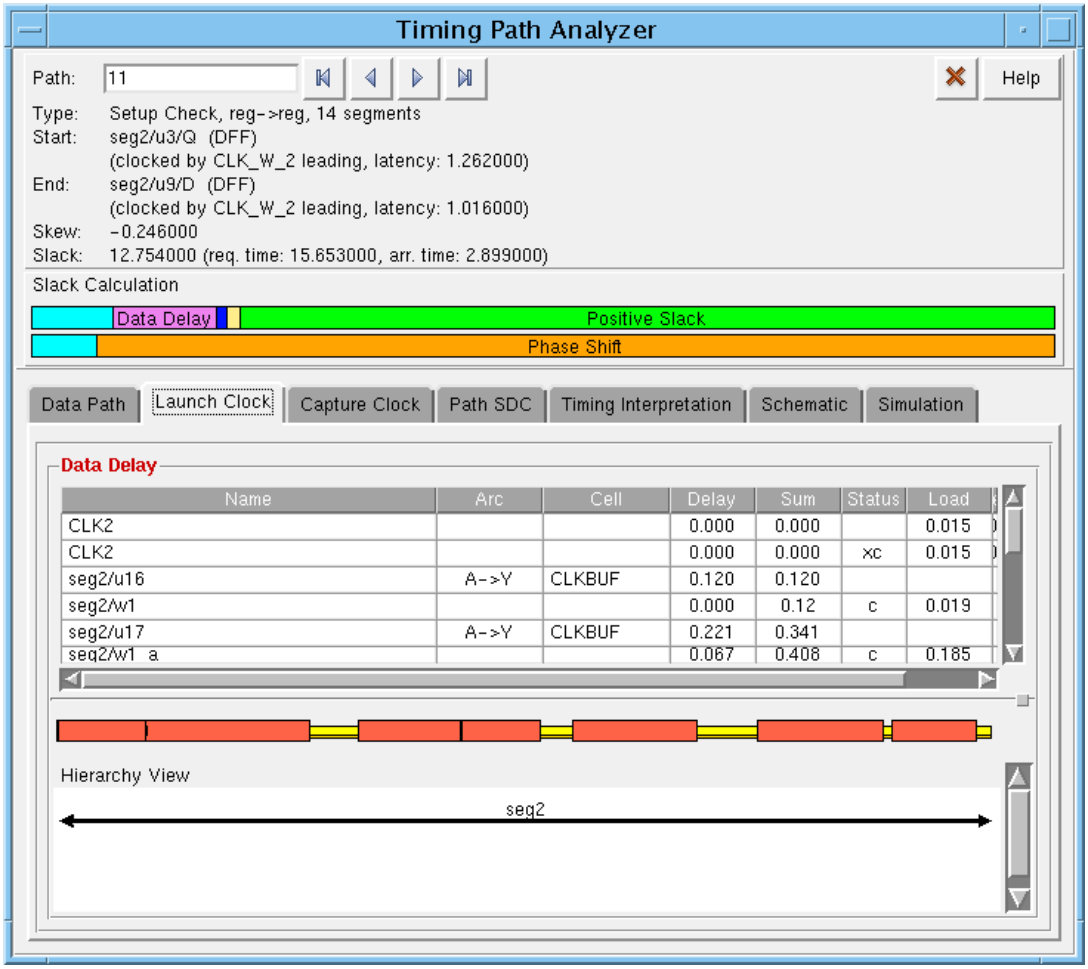
Path	Specifies the number of path as listed in the Timing Debug window.
Type	Displays the type of selected path.

Start	Displays the starting point of the path.
End	Displays the ending point of the path.
Skew	Displays the skew of the path.
Slack	Displays the slack of the path.
Slack Calculation	Displays path arrival time and required time calculations in color bars. The top bar displays the arrival time and the bottom bar displays the required time calculation. For example, arrival time can be represented as consisting of data delay (In pink), Setup time (in blue), and uncertainty (in yellow). You can inspect various aspects of calculation to identify possible problem(s) associated with a path. You can move you cursor over the color bars to display the values associated with each bar element. Use this feature to identify issues related to clock skew, latency balancing or large clock uncertainties.
Data Delay	Displays the details of the selected path in the violation reports. You can click on a single element to display it in the design display area. You can select each element consecutively to trace the entire path in the design display area.
Timing Bar	Displays the instance and net delays. The size of the bar indicates the delay associated with that element. Moving the cursor on these elements displays the details of instances or nets. The instance delays are represented in red and the net delays are represented in yellow color. Use this feature to identify issues related to large instance or net delays, repeater chains, paths with large number of buffers, and large macro delays.
Hierarchy View	Displays a path's traversal of logical hierarchy on a time-axis. This is useful for identifying issues related to inter-partition paths or paths that go through a partition.
	Closes the form.

Timing Path Analyzer - Launch Clock

Use the Timing Path Analyzer - Launch Clock form to identify issues related to a path using the launch clock details. The Launch Clock form displays the details of a complete launch clock path.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Launch Clock* tab in the Timing Path Analyzer form.



Timing Path Analyzer - Launch Clock Fields and Options

Data Delay

Displays the details of the launch clock of the selected path. You can click on a single item in the table to highlight the clock in the design display area.

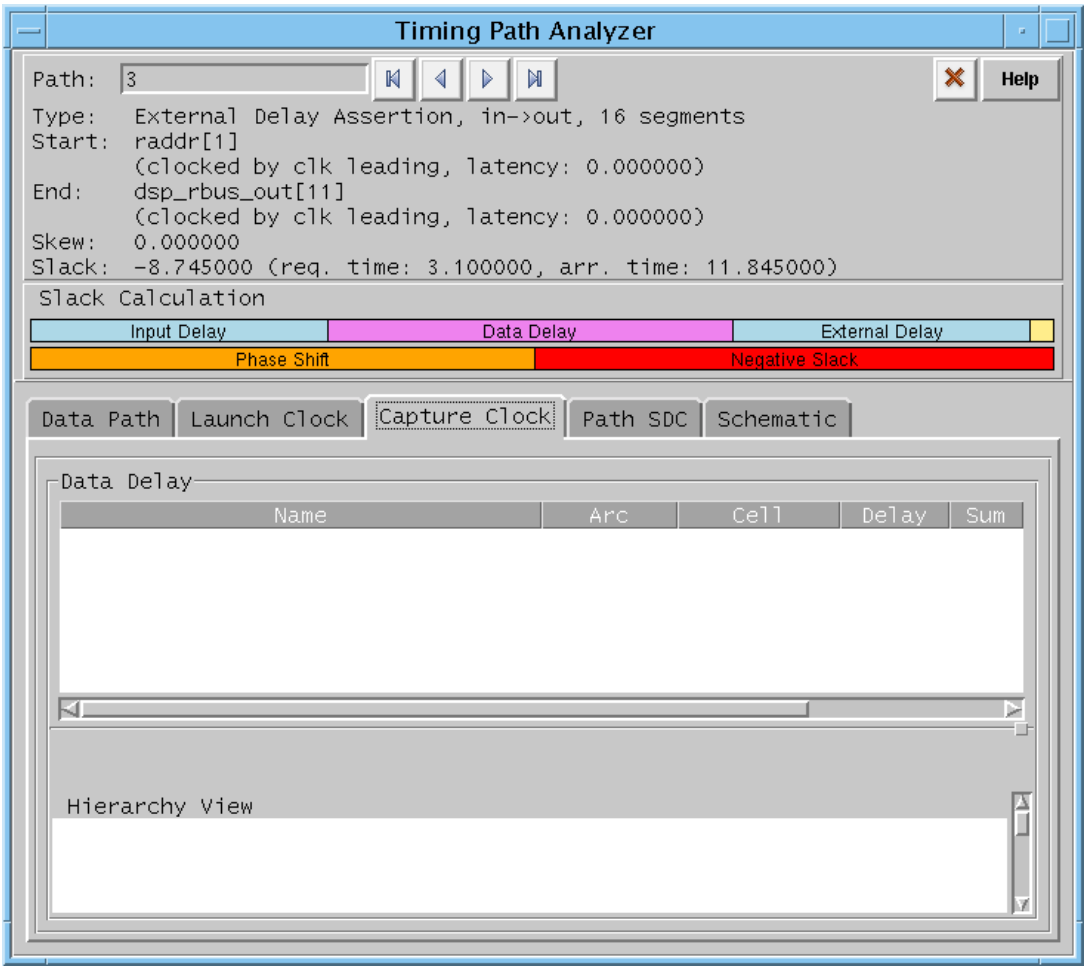
The *Timing Bar* and *Hierarchy View* display the characteristics of the launch clock path.

Closes the form.

Timing Path Analyzer - Capture Clock

Use the Timing Path Analyzer - Capture Clock form to identify issues related to a path using the capture clock details. The Capture Clock form displays the details of a complete capture clock path.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Capture Clock* tab in the Timing Path Analyzer form.



Timing Path Analyzer - Capture Clock Fields and Options

Data Delay

Displays the details of the capture clock of the selected path. You can click on a single item in the table to highlight the clock in the design display area.

The *Timing Bar* and *Hierarchy View* display the characteristics of the capture clock path.

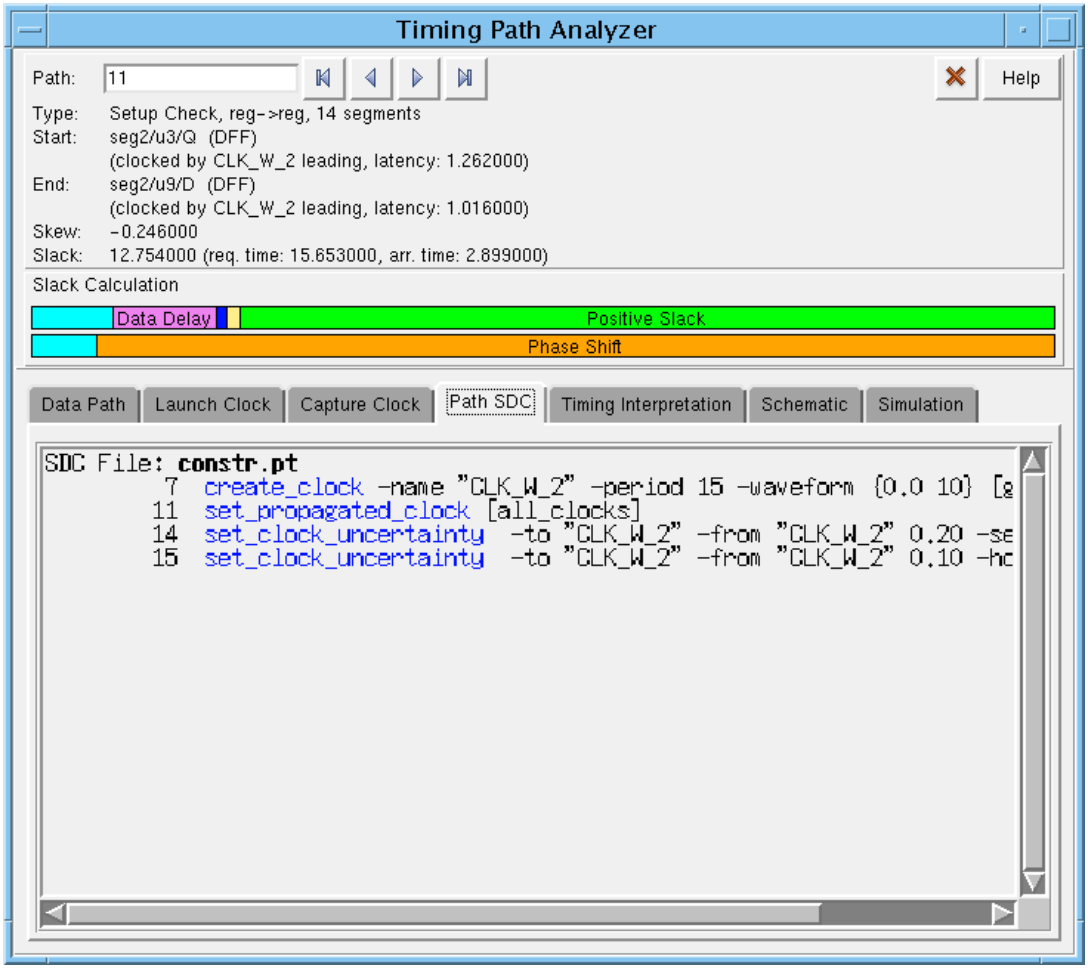
Closes the form.

Timing Path Analyzer - Path SDC

Use the Timing Path Analyzer - Path SDC form to identify issues related to the SDC constraints associated with the selected path.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Path SDC* tab in the Timing Path Analyzer form.

T



Timing Path Analyzer - Path SDC Fields and Options

SDC File

Displays the list of SDC constraints associated with the selected path. The list contains the name of the SDC file, the line number that indicates the position of the constraint in the SDC file, and the constraint definition.

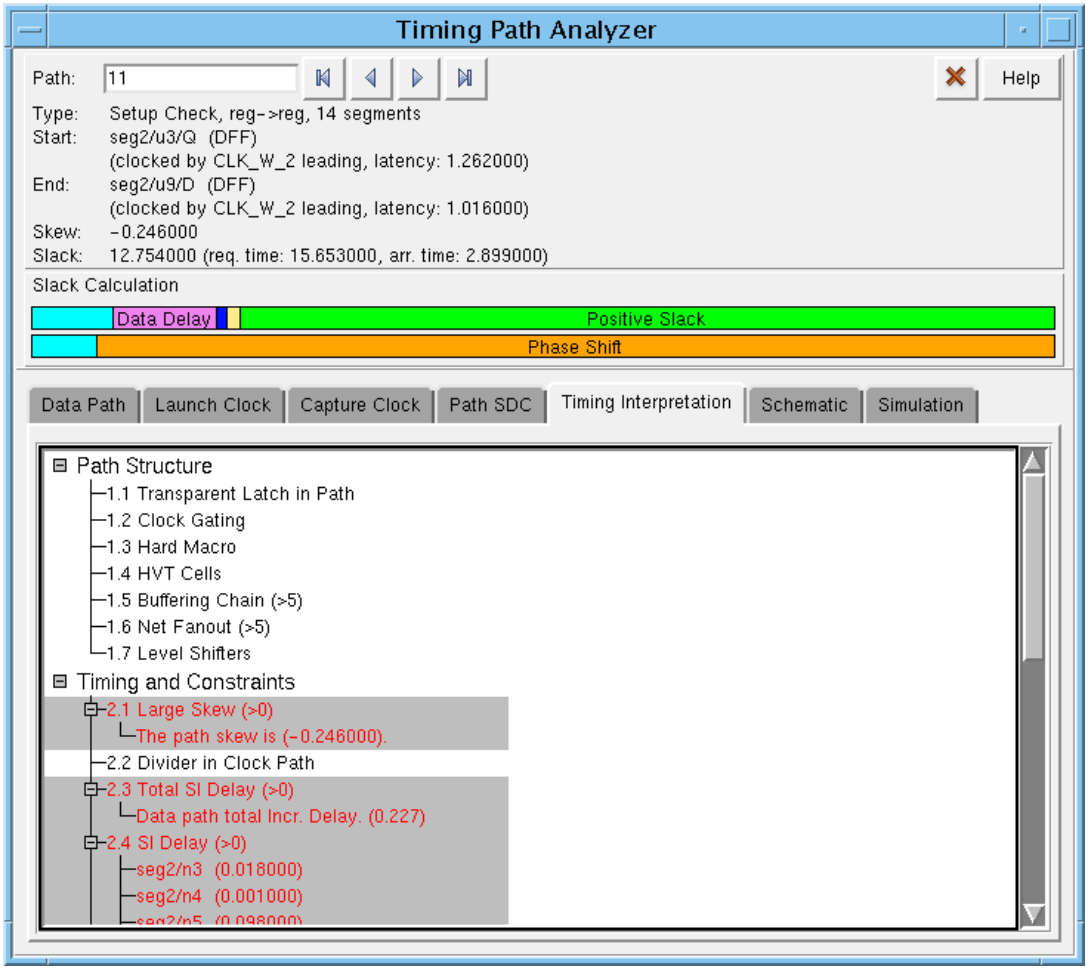
Use this from to identify issues related to the constraint definition for a path.

Closes the form.

Timing Path Analyzer – Timing Interpretation

Use the Timing Path Analyzer – Timing Interpretation form to identify the possible sources of timing problems associated with a selected path. Potential problems are highlighted in red.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose the *Timing Interpretation* tab in the Timing Path Analyzer form.



Timing Path Analyzer - Timing Interpretation Fields and Options

Path Structure

Shows the presence of structures that could cause timing issues in the path:

- *Transparent Latch in Path*
- *Clock Gating*
- *Hard Macros*
- *HVT Cells*
- *Buffering Chain*
- *Net Fanout*
- *Level Shifters*

Timing and Constraints

Shows values that exceed preset limits for timing and constraints:

- *Large Skew*
- *Total SI Delay*
- *SI Delay*
- *External Delay*

Floorplan

Shows the presence of the following floorplan elements that could be source of problems in the timing path:

- *Fixed Cells*
- *Multiple Power Domains*

Also shows violations for preset limits for the distances:

- *Distance from Start to End*
- *Distance Repeater*
- *Distance Buffer Tree*
- *Detour*

DRVs

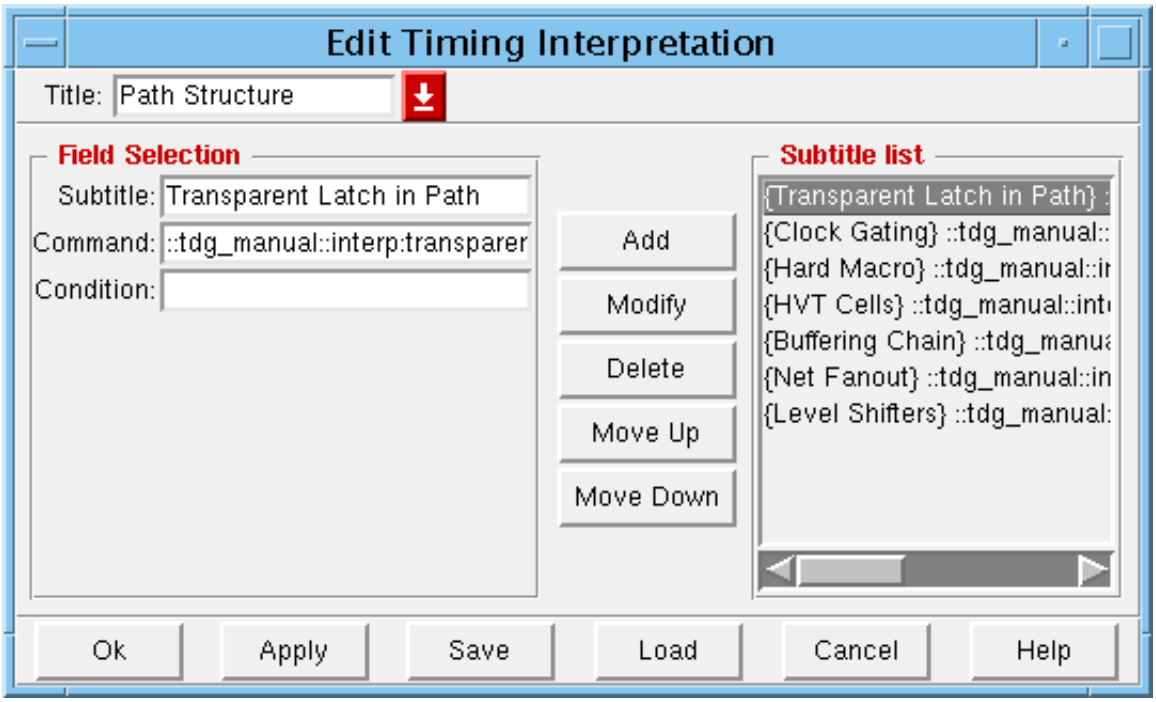
Shows max_tran, max_cap, and max_fanout values exceeding the preset limits:

- *Max Transition*
- *Max Capacitance*
- *Max Fanout*

Edit Timing Interpretation

Use the Edit Timing Interpretation form to change the type of information displayed on the Timing Interpretation table of the Timing Path Analyzer.

1. To open the Edit Timing Interpretation form, open the Timing Path Analyzer form.
2. Click on the Timing Interpretation tab.
3. Right-click on any element in the table and select *Edit Timing Interpretation*.



Timing Path Analyzer – Edit Timing Interpretation Fields and Options

Title

Specifies the title of the path element:

- Path Structure
- Timing and Constraints
- Floorplan
- DRV: Work after DRV

Subtitle

Specifies the name of the subtitle to modify.

For Path Structure:

- Transparent Latch in Path
- Clock Gating
- Hard Macro
- HVT Cells
- Buffering Chain
- Net Fanout
- Level Shifters

For Timing and Constraints:

- Large Skew
- Divider in Clock Path
- Total SI Delay
- SI Delay
- External Delay

For Floorplan:

- Fixed Cells
- Distance from Start to End
- Distance Repeater Chain
- Distance Buffer Tree
- Detour
- Multi Power Domains

For DRV: Word after DRV Analysis

- Max Transition
- Max Capacitance
- Max Fanout

Command

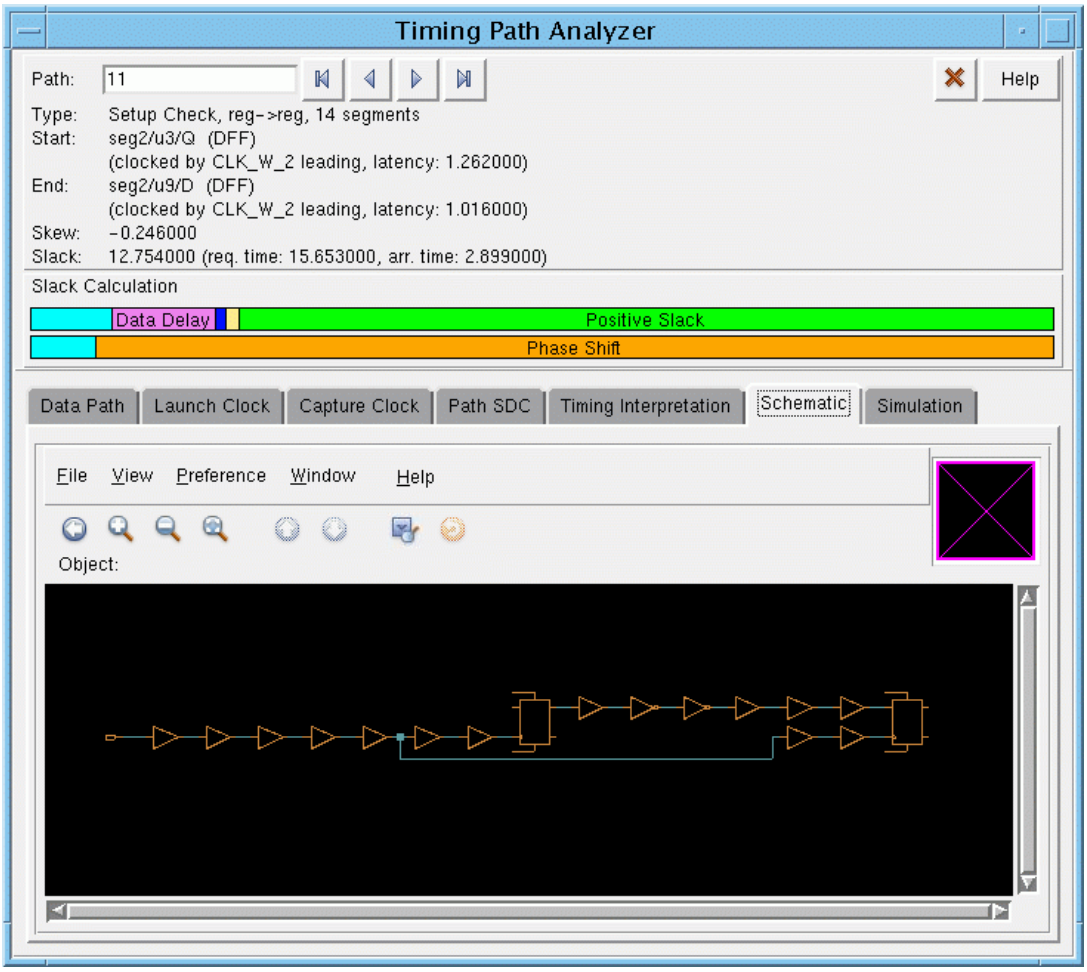
Specifies a procedure to create the subtitle.

Condition	Specifies a condition value.
Subtitle list	Displays a subtitle you selected, or lets you specify the name of the subtitle you would like to add.
Add	Adds the subtitle to the Subtitle list an subtitle that you added or changed in the Field Selection pane.
Modify	Modifies the selected subtitle.
Delete	Deletes the subtitle.
Move Up	Moves the subtitle up the list of subtitles in the Timing Interpretation table.
Move Down	Moves the subtitle down the list of subtitles in the Timing Interpretation table.

Timing Path Analyzer - Schematics

Use the Timing Path Analyzer - Schematics form to display the schematic view of the selected path.

1. Choose *Timing – Debug Timing.*
2. Double-click on a path in the *Path List* in the Timing Debug window.
3. Choose *Schematics* tab in the Timing Path Analyzer form.



Timing Path Analyzer - Schematics Fields and Options

For more information about fields and options, see "Schematics" in the Tools Menu chapter.

Analyze What-If Timing

Use the Black Box/Blob What-if Timing Analysis form to view details of blackboxes and blackblobs, and perform what-if analysis of the blackboxes or blackblobs.

The Black Box What-if Timing Analysis form contains the following two pages:

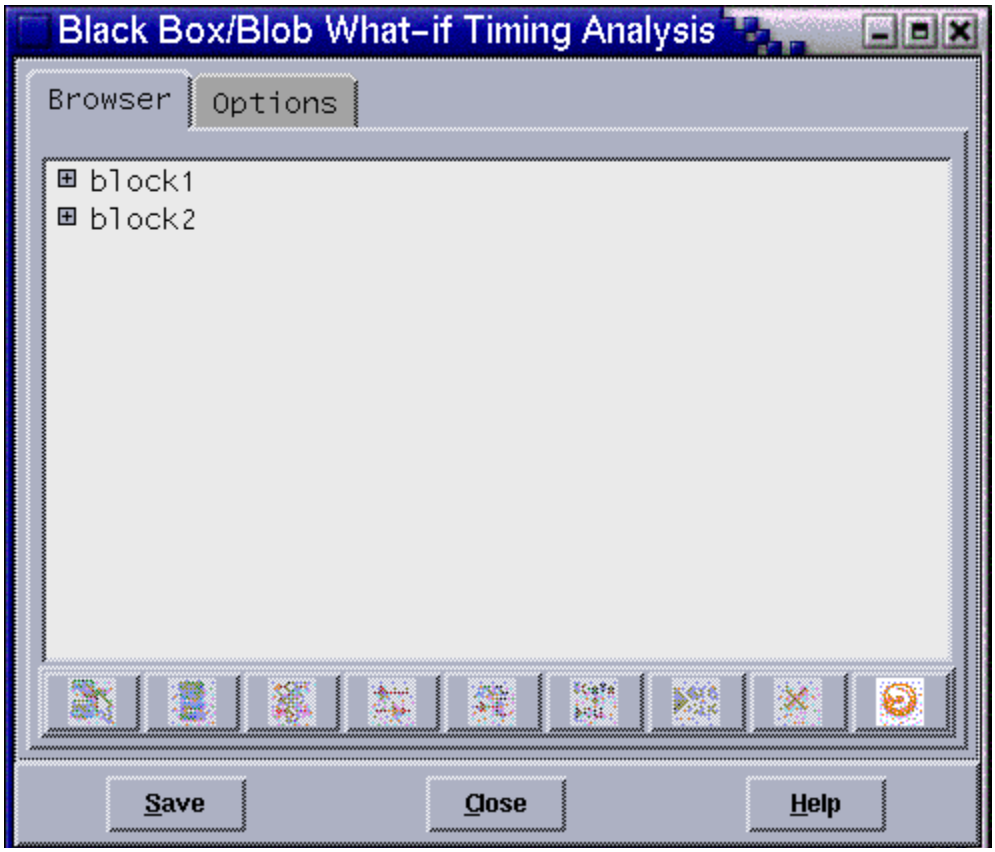
- Black Box/Blob What-If Timing Analysis – Browser on page 1437
- Black Box What-If Timing Analysis – Options on page 1451

Black Box/Blob What-If Timing Analysis – Browser

Use the *Browser* page of the Black Box What-If Timing Analysis form to navigate through the blackbox or pin specifications. The *Browser* page makes it easier to interactively display and set various values related to blackboxes.

The browser displays the blackboxes and blackblobs used in the design. The input and output ports of the blackbox or blackblob are grouped under input and output of a block. The browser also displays the timing arcs for each pin and the What-if information. The clock pins are displayed in the color blue.

➤ Choose *Timing – What-If Timing Analysis* and click on the *Browser* tab.



Black Box/Blob What-If Timing Analysis Fields and Options

Find — Allows you to view timing information for a specific blackbox, blackblob or pin. The text field supports the use of wildcard entries. You can use an asterisk (*) with regular characters to list the matching object names.

Show selected Black Boxes/Blobs—Displays the selected blackboxes and/or blackblobs in the Black Box/Blob What-if Timing Analysis window.

Show all Black Boxes/Blobs—Displays all blackboxes or blackblobs in the Black Box/Blob What-if Timing Analysis window.

Set/Create timing arcs—Opens the Create Timing Arc form. This button is activated when you select a pin name. For more information, see "Create Timing Arcs" on page 1440.

If the timing arc is already defined for a pin, clicking on the *Set/Create timing arcs* widget displays the Set Timing Arc form. For detailed information on the Set Timing Arc form, see "Set Timing Arc" on page 1442.

Set output driver—Opens the Set Output Driver form. This button is activated when you select an output pin. For more information, see "Set Output Driver" on page 1444.

Set clock latency—Opens the Set Clock Latency form. This button is activated when you select a clock pin. For more information, see "Set Clock Latency" on page 1446.

Set black box/blob clock port—Opens the Set Black Box/Blob Clock Port form. This button is activated when you select an input pin. For more information, see "Set Black Box Clock Port" on page 1448.

Generate internal clock—Creates an internal pin and defines a generated clock on the pin. For more information, see "Create Internal Generated Clock" on page 1449.

Delete timing arcs—Deletes selected timing arcs.

Refresh browser—Refreshes the Browser display.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `createWhatIfInternalGeneratedClock`
- `deleteWhatIfTimingAssertions`
- `saveWhatIfTimingAssertions`
- `setWhatIfClockLatency`
- `setWhatIfCombDelay`
- `setWhatIfDriveType`
- `setWhatIfSeqDelay`
- `setWhatIfTimingCheck`

For more information, see “What-If Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

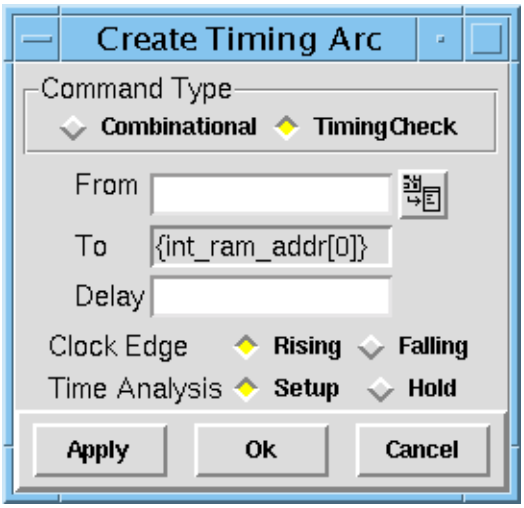
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- Performing What-If Timing Analysis

Create Timing Arcs

Use the Create Timing Arc form to create timing arcs for the pins.

➤ Choose *Timing – What-If Timing Analysis* and then click on the *Set/Create timing arcs* widget on the Black Box Timing Analysis form.



Create Timing Arc Fields and Options

Combinational

Sets the delay for purely combinatorial paths from input ports to the output ports. In the intrinsic timing model mode, the delay corresponds to the delay from the input port to the input of the driver. In the normalized timing model mode, the delay corresponds to the delay from the input port to the output port including the driver delay. If you do not specify the drive type on the output port, a constant timing table is created. In a constant timing table, delay is constant. It does not vary with respect to input slew and output capacitance.

When you select this option, the Create Timing Arc form is expanded to display options for specifying the delay value.

Timing Check	Sets the delay from the clock input port to the data input port. The delay value contains the clock latency. To create a new timing check arc which does not already exist in the timing model, the clock port that you specify in this command must be already referenced as a clock pin in the timing model. When you select this option, the Create Timing Arc form is expanded to display options for specifying the delay value.
From	Specify the name of the clock input port. If you do not specify this parameter, the delay is set for all input and bidirectional clock ports.
To	Specify the name of the data input port.
Delay	Specify the delay value.
Clock Edge	Select the *Clock Edge* as *Rising* or *Falling*. These options specify the transition on the clock input relevant to the sequential delay arc definition.
Time Analysis	Select the *Timing Analysis* as *Setup* or *Hold*. These options specify the setup or hold time for the timing check.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `setWhatIfSeqDelay`
- `setWhatIfCombDelay`
- `setWhatIfTimingCheck`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

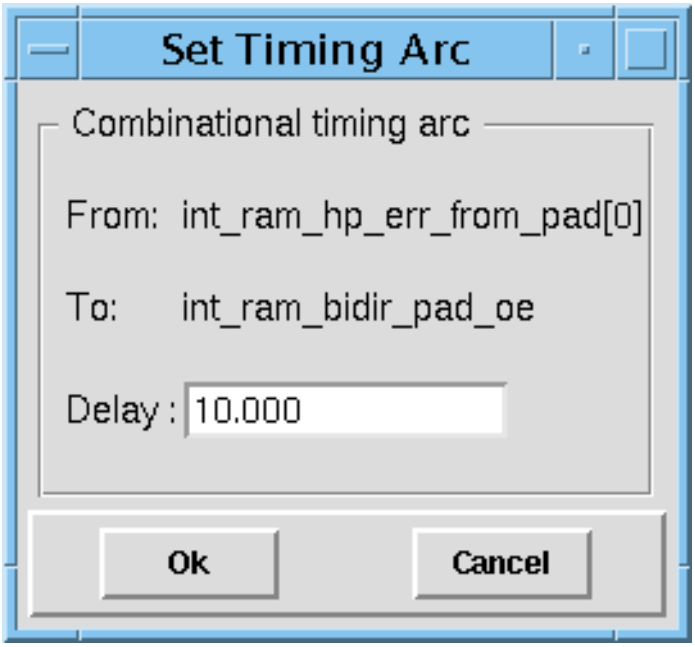
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- What-If Timing Analysis

Set Timing Arc

If the timing arc is already defined for a pin, use the Set Timing Arc form (Black Box What-If Timing Analysis – Browser – Set timing arcs) to change the delay value.

➤ Choose *Timing – What-If Timing Analysis* and then click on the *Set/Create timing arcs* widget on the Black Box Timing Analysis form.



Set Timing Arc Fields and Options

From	Displays the name of the clock input port.
To	Displays the name of the data input port.
Delay	Specify the delay value.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `setWhatIfSeqDelay`
- `setWhatIfCombDelay`

- `setWhatIfTimingCheck`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

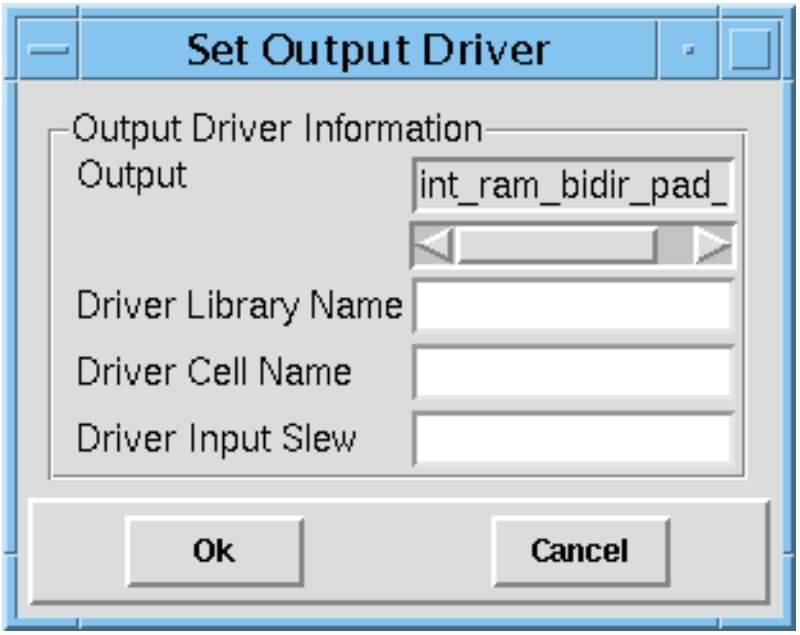
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- Blackbox What-If Timing Analysis

Set Output Driver

Use the Set Output Driver form to specify the output and bidirectional ports that have the specified type of cell within the blackbox as drivers on the interface nets. You cannot specify two different drivers for two timing arcs ending at the same output port. The Encounter software stores the drive type specification, and uses it to create a timing arc after you specify the delay.

➤ Choose *Timing – What-If Timing Analysis* and then click on the *Set Output Driver* widget on the Black Box Timing Analysis form.



Set Output Driver Fields and Options

Output	Displays the name of the output port.
Driver Library Name	Specifies the name of the timing library.
Driver Cell Name	Specifies the name of the cell. If there are two cells with the same name, the software uses the first one found. The software considers only buffers and inverters.

Driver Input Slew

Specifies the slew at the input of the driver cell. If you specify the slew value, the software creates a one-dimensional timing table depending on the output capacitance.
If you do not specify the slew value, the software creates a two-dimensional timing table with input slew and output capacitance values. In this case, the software assumes that there is no slew variation between the blackbox input port and the driver input pin.
You must use this parameter in the normalized timing model mode.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfDriveType`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

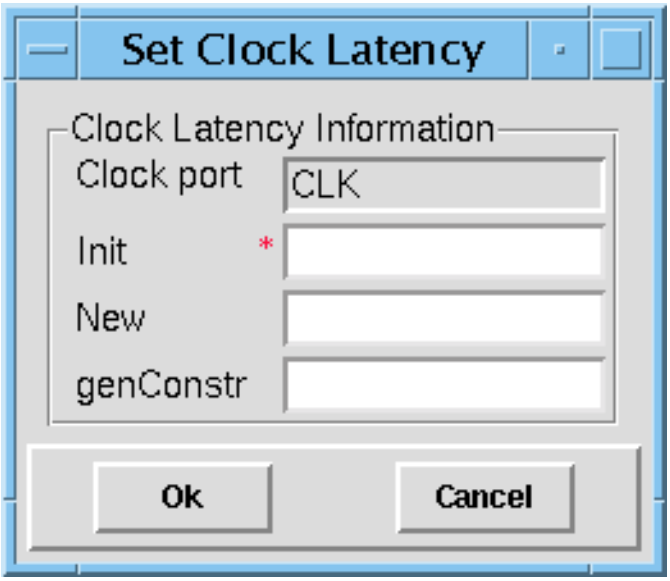
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- Blackbox What-If Timing Analysis

Set Clock Latency

Use the Set Clock Latency form to specify the clock insertion delay from a clock input port to register clock input pins within a blackbox.

➤ Choose *Timing – What-If Timing Analysis* and then click on the *Set Clock Latency* widget on the Black Box Timing Analysis form.



Set Clock Latency Fields and Options

Init

Specifies the current clock insertion delay value. This value indicates the clock insertion delay used when the software generates the original timing model. This value is used for timing checks or sequential timing arcs. You must specify this value before modifying a timing check or a sequential timing arc. If you modify at least one timing arc, you cannot directly change the clock latency value. You must first delete the timing arc specifications of the blackboxes using the `deleteWhatIfTimingAssertions` command.

New	Specifies the new clock latency value. This value modifies the clock insertion delay. As the clock insertion delay is included in the timing arc value specified using the `setWhatIfSeqDelay` or `setWhatIfTimingCheck` command, the Encounter software adds the difference between the current and new clock latency value to all timing arcs starting from the specified clock port. Therefore all timing arcs starting from the specified clock port, including the timing arcs that were not modified using the blackbox timing commands, are modified.
genConstr	Specifies the latency to consider in the blackbox timing constraints generation. By default, the value is automatically set to the current clock insertion delay. If you do not modify the latency value, the generated SDC constraints reflect the timing analysis done at the top level. If you set a latency value other than current clock insertion delay, the timing analysis is not impacted.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setwhatIfClockLatency`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

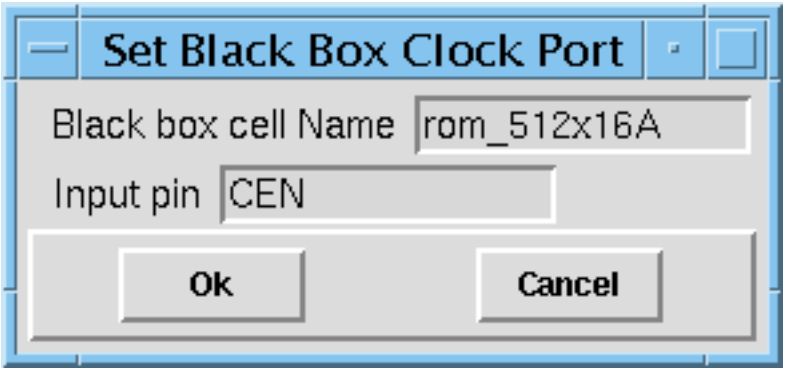
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- Blackbox What-If Timing Analysis

Set Black Box Clock Port

Use the Set Black Box Clock Port form to define a port as a clock port. The form displays the port information.

➤ Choose *Timing – What-If Timing Analysis* and then click on the *Set black box clock port* widget on the Black Box Timing Analysis form.



Set Black Box Clock Port Fields and Options

Black box cell Name	Displays the name of the blackbox.
Input pin	Displays the name of the input pin that will get set as the clock port.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfClockPort`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

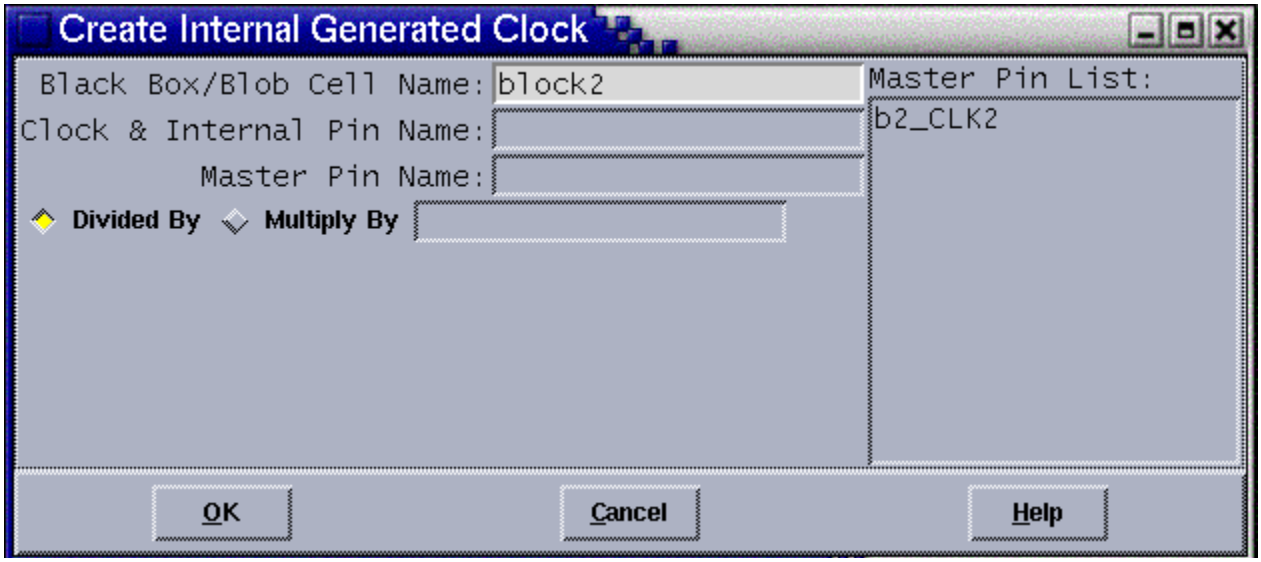
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- What-If Timing Analysis

Create Internal Generated Clock

Use the Create Internal Generated Clock form to create a pin inside a blackbox or a blackblob and to define a generated clock on the pin.

1. Choose *Timing – What-If Timing Analysis.*
2. In the Browser, select the blackbox or the blackblob inside which you want to create the internal pin, and then click on the *Generate Internal Clock* widget. The Create Internal Generated Clock form appears.



Create Internal Generated Clock Fields and Options

Black Box/Blob Cell Name	Displays the name of the blackbox or blackblob.
Clock & Internal Pin Name	Specifies the name of the internal pin that will get created inside the blackbox or the blackblob. The same name is used for the generated clock that will be defined on the pin.
Master Pin Name	Specifies the source from which the derived clock is generated. **Note:** The source must be an existing clock port and a clock should be available on this port. You can select a source from the list of existing clock sources displayed in *Master Pin List.*

Divided By	Specifies the frequency division factor. The generated clock period is equal to the master clock period multiplied by this parameter. For example, if the value of this parameter is 2, the generated clock period is two times the master clock period.
Multiply By	Specifies the frequency multiplication factor. The generated clock period is equal to the master clock period divided by this parameter. For example, if the value of this parameter is 2, the generated clock period is half the master clock period.
Master Pin List	Displays the available clock sources.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `createWhatIfInternalGeneratedClock`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- What-If Timing Analysis

Black Box What-If Timing Analysis – Options

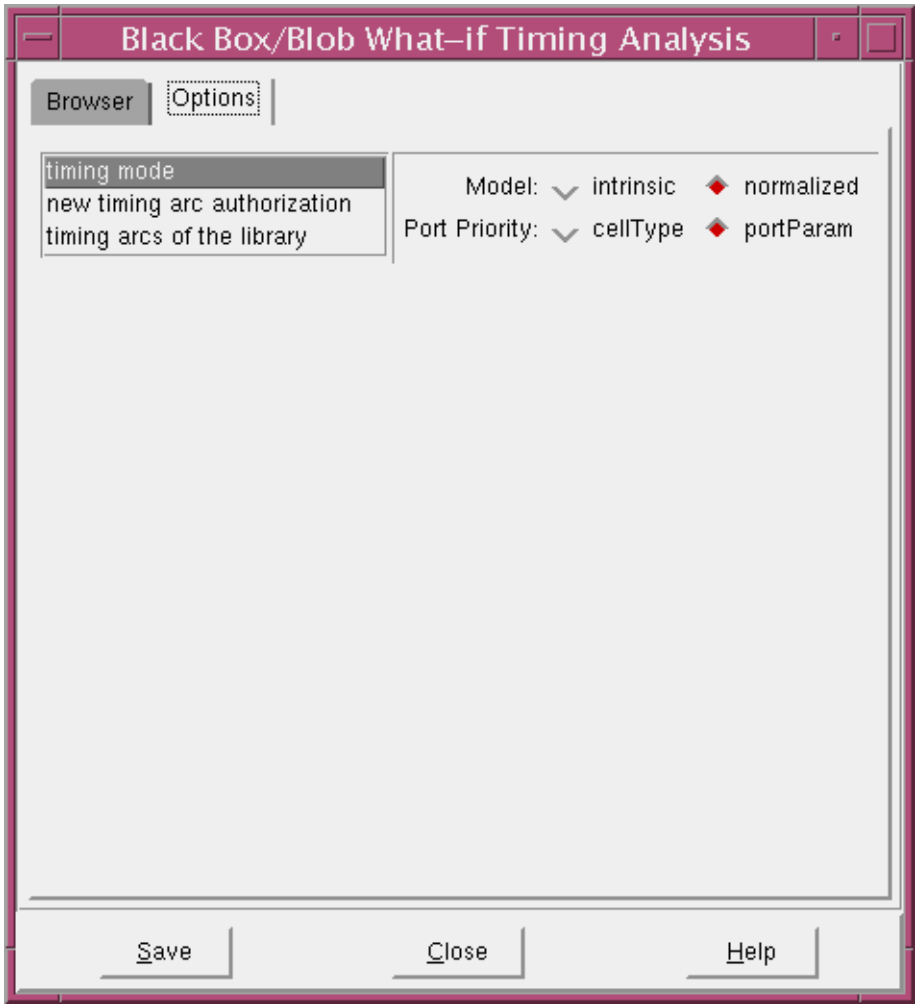
The *Options* page of the Black Box What-If Timing Analysis form enables you to specify timing mode, set new timing arc, and enable the set timing arcs option. The *Options* page contains the following subpages:

- Black Box What-If Timing Analysis – Options – timing mode on page 1452
- Black Box What-If Timing Analysis – Options – new timing arc authorization on page 1455
- Black Box What-If Timing Analysis – Options – timing arcs of the library on page 1457

Black Box What-If Timing Analysis – Options – timing mode

Use the *timing mode* page of the Black Box What-If Timing Analysis form to specify the type of timing model for blackbox analysis.

➤ Click on the *Options* page of the Black Box What-if Timing Analysis form.



Black Box What-If Timing Analysis Fields and Options

Model	Select the timing model (*intrinsic* or *normalized*).
intrinsic	Specifies the intrinsic timing model mode.
normalized	Specifies the normalized timing model mode. This is the default mode.
Port Priority	On output and input ports, parameters such as capacitance value, maximum capacitance values, maximum transition value, or the maximum fanout value can come from the driver (`setWhatIfDriveType` command or `setWhatIfLoadType` command) or they can be set through the `setWhatIfPortParameters` command. Use the Port Priority option to specify which of these values take precedence in case of a conflict. *Important* *The value of the portPriority parameter is frozen once a what-if timing arc has been defined. This avoids inconsistencies between the timing analysis files and the files that you can generate (such as whatif assertions, timing model, or SDC) if you change the port priority subsequently.*
cellType	Specifies that the parameter values set through the `setWhatIfDriveType` command or `setWhatIfLoadType` command take precedence.
portParam	Specifies that the parameter values set through the `setWhatIfPortParameters` command take precedence.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `setWhatIfTimingMode`

For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

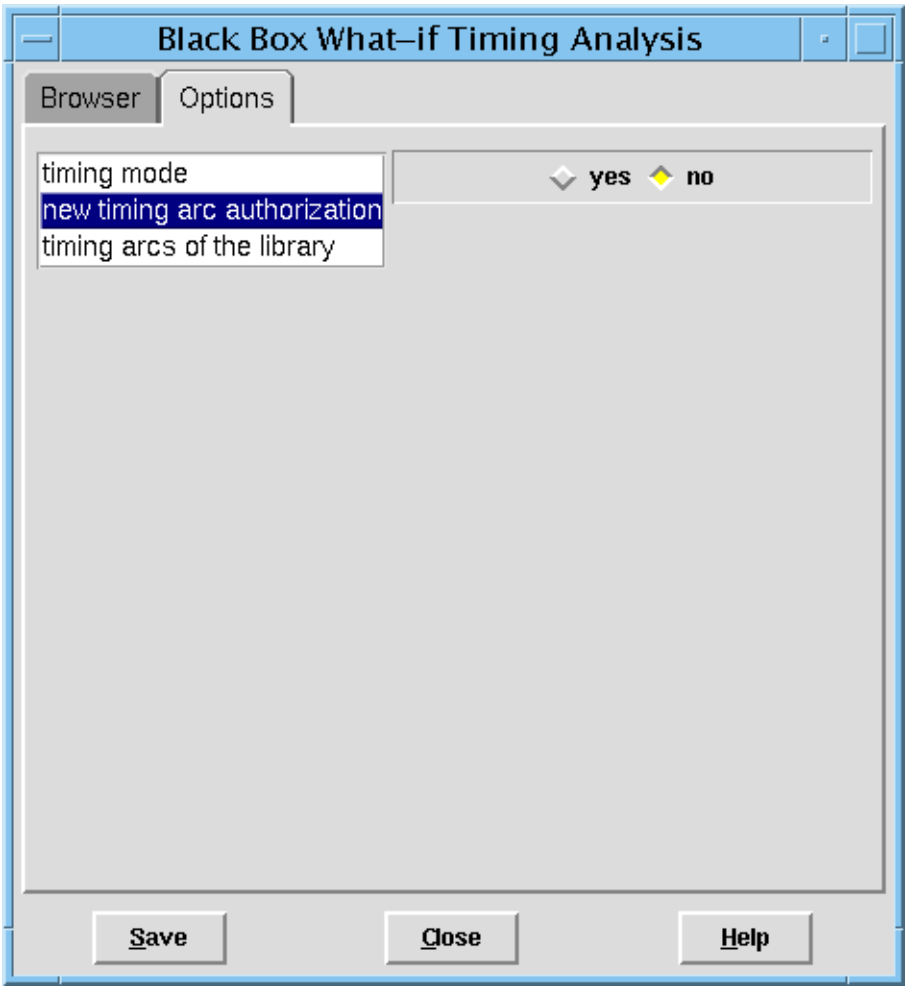
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- Performing What-If Timing Analysis

Black Box What-If Timing Analysis – Options – new timing arc authorization

Use the *new timing arc authorization* page of the Black Box What-If Timing Analysis form to enable creation of new timing arcs.

➤ From the *Options* page, select the *new timing arc authorization* category.



Black Box What-If Timing Analysis – Options – new timing arc authorization Fields and Options

yes	Enables creation of new timing arcs.
no	Disables creation of new timing arcs.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `setWhatIfCombDelay`
- `setWhatIfSeqDelay`
- `setWhatIfTimingCheck`

All the related text commands must be used with `-force` option to enable this feature. For more information, see “Blackbox Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

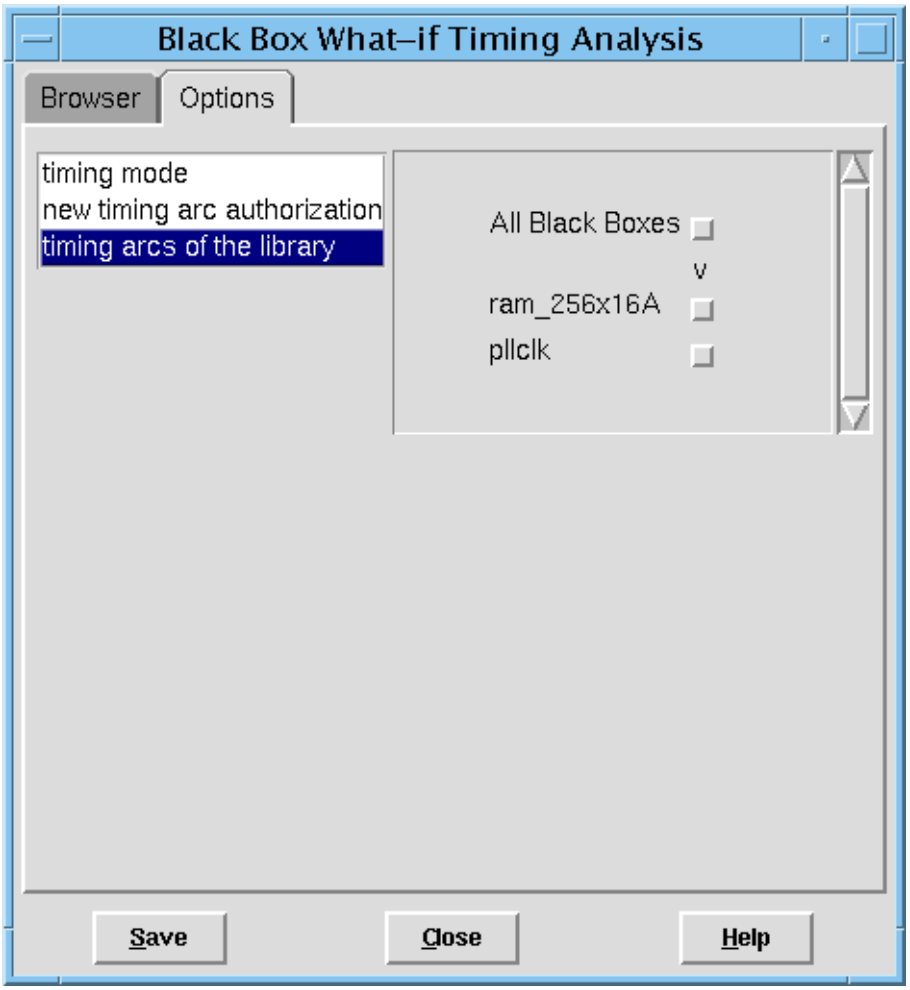
For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

- What-If Timing Analysis

Black Box What-If Timing Analysis – Options – timing arcs of the library

Use the *timing arcs of the library* page of the Black Box/Blob What-If Timing Analysis form to display the original timing arcs from the timing model in the *Browser* page.

➤ From the *Options* page, select the *timing arcs of the library* category.



Black Box What-If Timing Analysis – Options – timing arcs of the library Fields and Options

All Black Boxes	Allows you to display timing arcs for all blackboxes.
Blackbox selections	Select the specific black boxes for which you want to display the timing arcs.

Related Text Commands

There is no related text command.

Related Topics

For information on the following topic, see “What-If Timing Analysis” in the *Encounter User Guide*.

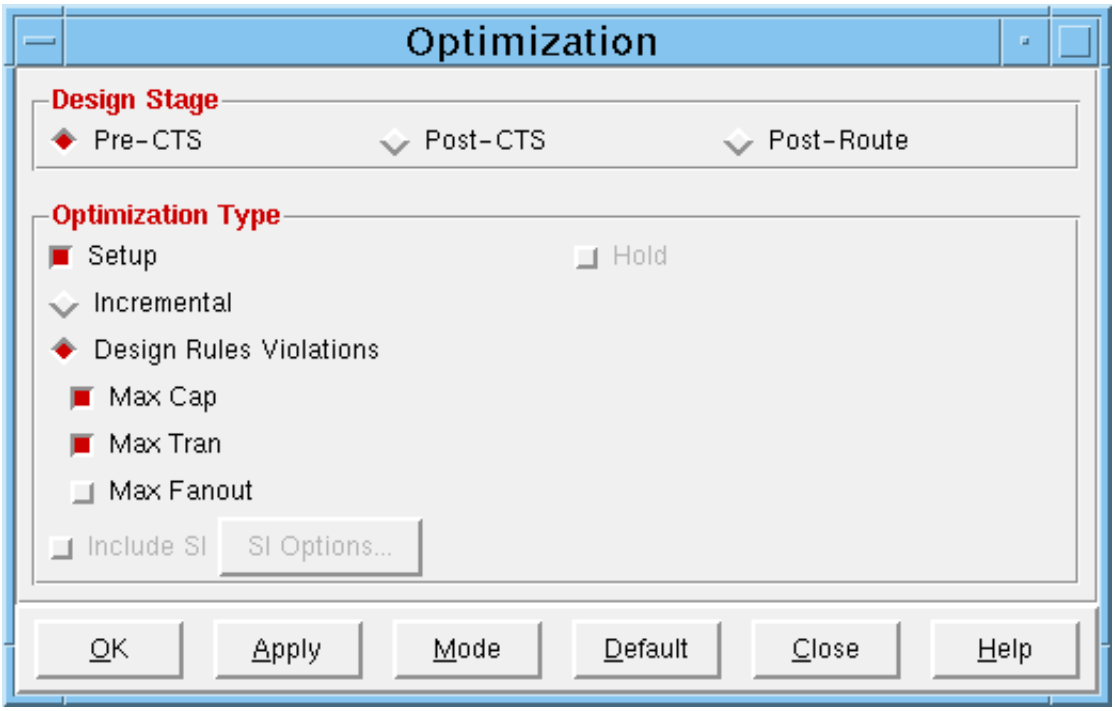
- What-If Timing Analysis

Optimize

Use the *Optimization* form to make the following improvements to your design:

- Reduce path delays
- Improve transition times
- Correct capacitance violations

➤ Choose *Timing – Optimize*.



Timing – Optimization Fields and Options

Design Stage *Pre-CTS*	Performs timing optimization on placed design before the clock tree is built. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. *Default:* Selected
Post-CTS	Performs timing optimization after the clock tree is built. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. In this mode, if you are running *Useful Skew* and you have already detail routed the clock, the Encounter software performs ECO routing using the NanoRoute® router. *Default:* Deselected
Post-Route	Performs timing optimization on routed designs. By default, repairs DRVs and setup violations for all path groups. If the worst negative slack found during the first optimization pass does not occur on a register-to-register path, the software performs an additional optimization for the register-to-register critical paths. In this mode, the software performs ECO routing using the NanoRoute router. *Default:* Deselected
Optimization Type *Setup*	Corrects setup time violations. *Default:* Selected in all modes.
Hold	Corrects hold time violations. *Default:* Deselected. Available in *Post-CTS* and *Post-Route* modes.
incremental	Performs incremental optimization on all path groups. *Default:* Deselected
Design Rules Violations	Specifies the type of design rule violations to correct. *Default:* Selected. Unavailable if *Incremental* is selected, or if *Pre-CTS* mode and *Low* effort (on the *Mode Setup – Optimization* form) are selected.

Max Cap — Corrects maximum capacitance violations in the design based on the threshold specified in the SDC constraints file or in the timing libraries.
Default: Selected. Available only if *Design Rule Violations* is selected.

Max Tran — Corrects maximum transition violations in the design based on the threshold specified in the SDC constraints file or in the timing libraries.
Default: Selected. Available only if *Design Rule Violations* is selected.

Max Fanout — Corrects maximum fanout-load violations.

In the library, each cell output pin might have a `maxfanout` constraint defined, and each input pin might have a `fanout_load` defined. The Encounter software checks `maxfanout` against the total `fanout_load` that the output pin drives in the netlist. A violation exists if the total fanout load exceeds the `maxfanout`. You can override these limits by specifying new limits in the SDC file.

If `maxfanout` or `fanout_load` are not defined in the library, the Encounter software does not perform maximum fanout repair.
Default: Deselected. Available only if *Design Rule Violations* is selected.

Include SI — Corrects signal integrity violations for designs routed in signal integrity prevention mode.
Default: Deselected. This option is available in *Post-Route* mode only.

SI Options — Opens the Fix Crosstalk form, enabling you to select options for repairing noise-on-delay and glitch noise violations. This option is available only in *Post-Route* mode, and only if you select *Include SI*.

Related Text Commands

For information on the following commands, see “Timing Optimization Commands” in the *Encounter Text Command Reference*.

- `optDesign`
- `setAnalysisMode`
- `setOptMode`
- `setClockDomains`
- `setSIMode`
- `setUsefulSkewMode`

Related Topics

For information on the following topics, see “Optimizing Timing” in the *Encounter User Guide*.

- Performing Pre-CTS Optimization
- Performing Post-CTS Optimization
- Performing Postroute Optimization
- Useful Skew

Interactive ECO

The Interactive ECO feature enables you to perform manual incremental updates to the design to repair timing or transition time violations. The Interactive ECO form contains the following four pages:

- Interactive ECO – Add Repeater on page 1464
- Interactive ECO – Change Cell on page 1468
- Interactive ECO – Delete Repeater on page 1471
- Interactive ECO – Display Buffer Trees on page 1473

Interactive ECO – Add Repeater

Use the *Add Repeater* page of the Interactive ECO form to add buffers or a pair of inverters.

➤ Choose Interactive ECO from the Timing menu and click on the *Add Repeater* tab.

Interactive ECO - Add Repeater Fields and Options

Net	Type the net name, or click on a displayed net in the design display window and click *Get Selected*.
Get Selected	Displays the name of a selected net. If you click on the *Get Selected* button on this form without first selecting a net, the software issues an error message.
Terms	Provides two methods for specifying the buffer connection

All Terms	Connects the added buffer to drive all the receivers. Use this to reduce the delay and output transition time of a weak driver driving a large capacitive load.
Listed Terms	Connects the added buffer to drive the listed receivers, and provides full flexibility for building an arbitrary buffer connection.
New Cell	Enter the cell type name of the buffer cell to add, or click on the arrow to right of the field and select a buffer from the list
Place Mode	The following options specify various aspects for ECO placement.
Default	The software automatically determines a location and places the new cell.
Don't Place Cells	Specifies that the inserted cells should not be placed.
Location	Specifies where the buffer should be inserted.
First Buf/Inv X Y	Specifies the X and Y locations for the buffer or first inverter. You can use the automatically assigned location, enter the location, or click on an area in the design display window and click *get coord.*
	If the cell is a buffer and location is specified, the newly created buffer is placed at the specified location. If the cell is an inverter and only one location is specified, both inverters will be placed at the same location.
Second Inv X Y	Specifies the X and Y locations for the second inverter.You can use the automatically assigned location, enter the location, or click on an area in the design display window and click *get coord.*
Offload	Specifies the manner of buffer insertion for slack or load reduction.
By Slack (ns)	Inserts a buffer to offload the paths with less than the specified slack threshold from the driver of a net with multiple cells. This option ignores the `term` option, if it is provided.

By Location

Inserts a buffer at a the specified location on a net to reduce the load on the net driver. The tool determines the buffer direction by tracing backward on the net to find the buffer driving the wire segment at the new buffer location. The driven segment is connected to the input terminal of the new buffer.

get coord

Retrieves and displays the X and Y coordinates for a specified location in the design window.

Relative Distance wire cut to the sink (%):

Specifies the location of the buffer based on its distance from the sink or the driver pin. The value is a number between 0 and 1. A low value (0.1) places the buffer near the sink; a high value (0.9) places the buffer near the driver.

Offload (ns):

Offloads all paths with less than the specified slack threshold (in nanoseconds) from the driver of a net with multiple cells. This option ignores the `term` option, if it is provided.

By Location (x y)

Specifies the x and y coordinates for the location of the buffer or inverter pair to insert. If no location is specified, the tool will automatically determine a location.

If the cell is a buffer and location is specified, the newly created buffer is placed at the specified location. If the cell is an inverter pair and only one location is specified, both inverters will be placed at the same location.

Radius (um):

Specifies the radius in which the added instances are free to move. If no legal location can be found in the specified radius, the cells would be placed at the specified location resulting in an overlap with other cells. In that case, you should perform legalization.

Do Refine Placement

This button allows you to optionally legalize the placement of ECO changes.

Eval

Evaluates the effect on timing if you add *New Cell*. These values are reported but not applied, so you can experiment with different cell types.

Note: This option is active only if the design is routed.

Eval All	Evaluates the effect on timing for all the cell types available for *New Cell*. The timing report shows the effects of all the cell types, enabling you to select the best cell for your design. **Note:** This option is active only if the design is routed.
Apply	Applies your selections.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `ecoAddRepeater`
- `attachIOBuffer`

For more information, see “Interactive ECO Commands” in the *Encounter Text Command Reference*.

Related Topics

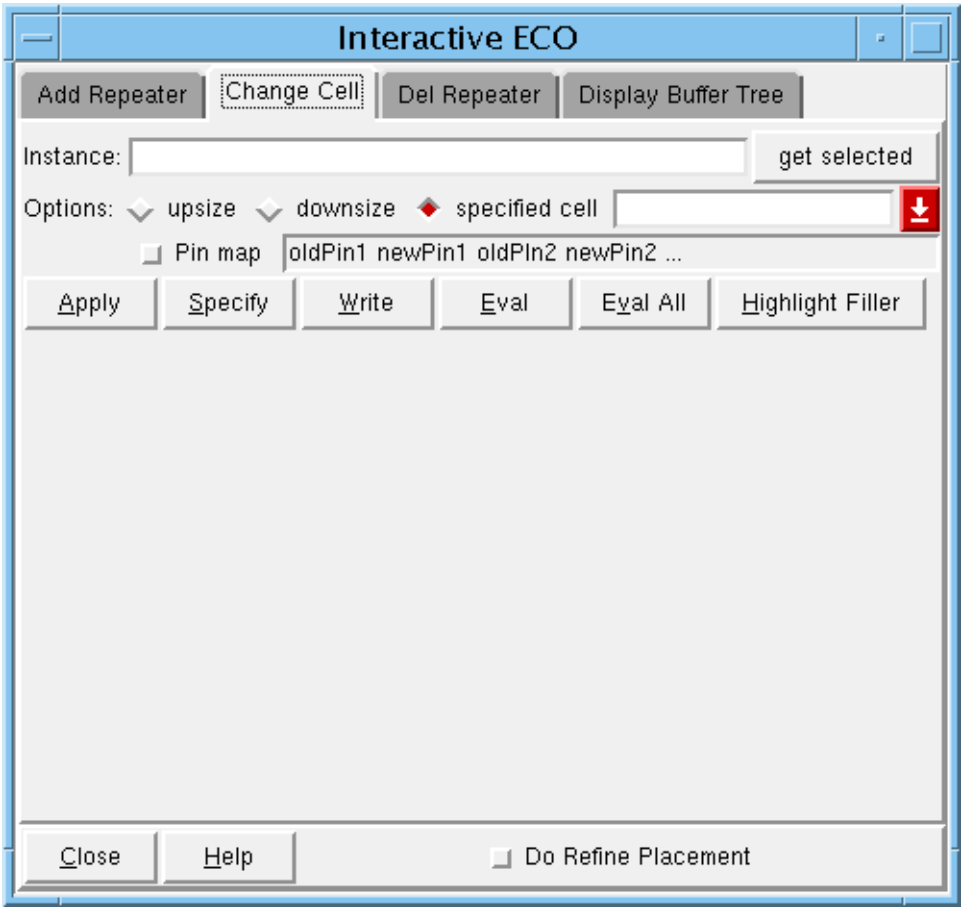
For information on the following topic, see “ECO” in the *Encounter User Guide*.

- Adding Buffers

Interactive ECO – Change Cell

Use the *Change Cell* page of the Interactive ECO form to upsize or downsize an instance. This drives a large load to improve the driver delay and the transition time at the receivers. This can also downsize an instance on the noncritical path to reduce the loading of its driver on the critical path.

➤ Choose Interactive ECO from the ECO menu and click on the *Change Cell* tab.



Interactive ECO - Change Cell Fields and Options

Instance	Enter the hierarchical instance name to be changed.

Get Selected	Displays the name of a selected instance. If you click on the *Get Selected* button on this form without first selecting an instance, the software issues an error message.
Options:	Select from the following options
upsize	Upsizing an instance that drives a large load can improve the driver delay and the transition time at the receivers.
downsize	Downsizing an instance on the noncritical path can reduce the loading of its driver on the critical path.
specified cell	Enter the name of the placement cell, or use the pull-down menu to select a cell.
Pin map	Specifies the pin mapping for the new cell based on the old cell.
Do Refine Placement	This button allows you to optionally legalize the placement of ECO changes.
Eval	Evaluates the effect on timing if you upsize or downsize a cell, or change to a different cell. These values are reported but not applied. **Note:** The option is active only if the design is placed.
Eval All	Evaluates the effect on timing for all the options available. **Note:** The option is active only if the design is placed.
Apply	Applies your selections.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `ecoChangeCell`

For more information, see “Interactive ECO Commands” in the *Encounter Text Command Reference*.

Related Topics

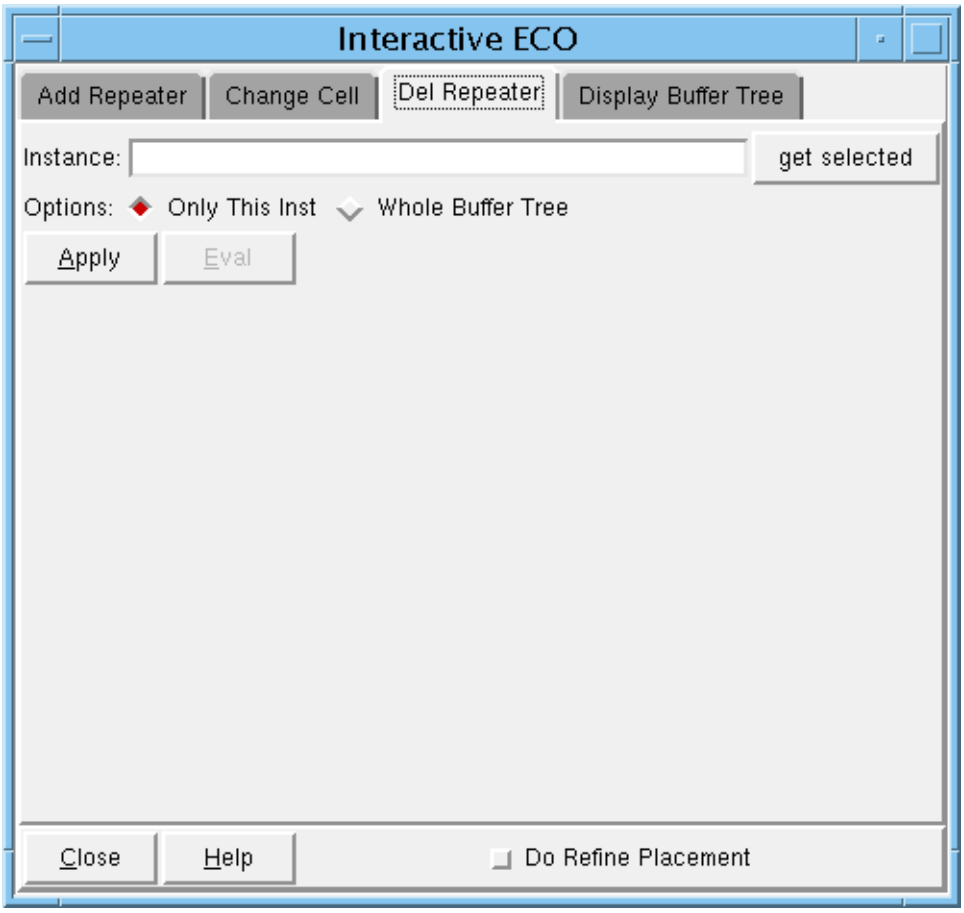
For information on the following topic, see “ECO” in the *Encounter User Guide*.

- Changing the Cell

Interactive ECO – Delete Repeater

Use the *Del Repeater* page of the Interactive ECO form to delete redundant buffers that cause extra delay. Buffers are typically over-added by synthesis tools based on wireload models.

➤ Choose Interactive ECO from the ECO menu and click on the *Del Repeater* tab.



Interactive ECO - Del Repeater Fields and Options

Instance	Enter the name of the buffer instance to be removed.
Get Selected	Displays the name of a selected instance. If you click on the *Get Selected* button on this form without first selecting an instance, the software issues an error message.
Only This Inst	(Default) Deletes only the selected instance.

Whole Buffer Tree	Automatically traverses the buffer tree associated with the instance, and removes the buffers in the same buffer tree.
Do Refine Placement	This button allows you to optionally legalize the placement of ECO changes.
Eval	Evaluates the effect on timing if you delete the specified instances or the buffer tree. These values are reported but not applied until you click *Apply*. **Note:** This option is active only if the design is routed.
Apply	Applies your selections.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `ecoDeleteRepeater`

For more information, see “Interactive ECO Commands” in the *Encounter Text Command Reference*.

Related Topics

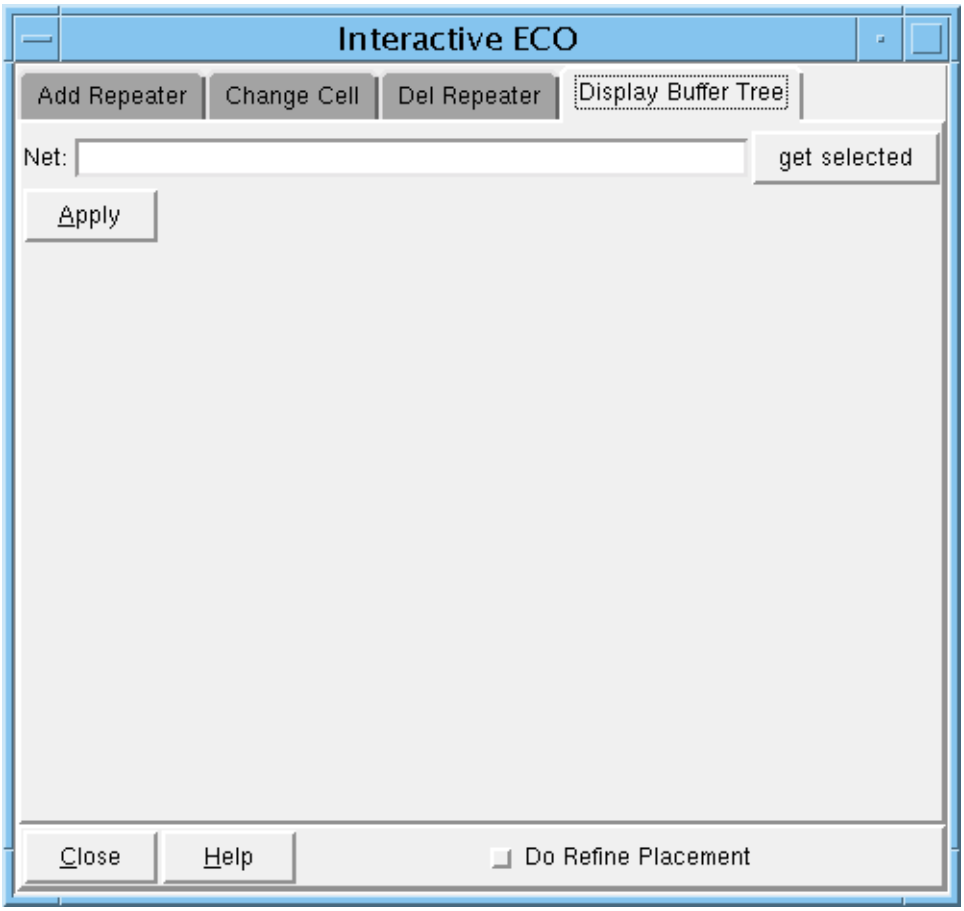
For information on the following topic, see “ECO” in the *Encounter User Guide*.

- Deleting Buffers

Interactive ECO – Display Buffer Trees

Use the *Display Buffer Tree* page from the Interactive ECO form to inspect the routing topology of the buffer tree. If the buffer tree requires correction, it can be rebuilt or modified through the other three pages in the Interactive ECO form.

➤ Choose Interactive ECO from the ECO menu and click on the *Display Buffer Trees* tab.



Interactive ECO - Display Buffer Tree Fields and Options

Net	Enter the name of the net to be selected.
Get Selected	Displays the name of a selected net. If you click on the *Get Selected* button on this form without first selecting a net, the software issues an error message.
Do Refine Placement	Legalizes the placement of ECO changes.

Apply	Applies your selections.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `displayBufTree`

For more information, see “Interactive ECO Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “ECO” in the *Encounter User Guide*.

- Displaying Buffer Trees

Timing Library

The Timing Library menu provides the following commands that allow you to examine the contents of a timing library, and to generate a report on its cell information.

- Timing Library – Check on page 1476
- Timing Library – Report on page 1477

Timing Library – Check

The *Check* menu command examines the contents of the timing library and reports any inconsistencies in a log file. Use this command after importing the design and timing library.

➤ Choose *Timing – Timing Library – Check*.

Related Text Commands

The following text command provides equivalent or additional functionality:

■ `checkTimingLibrary`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

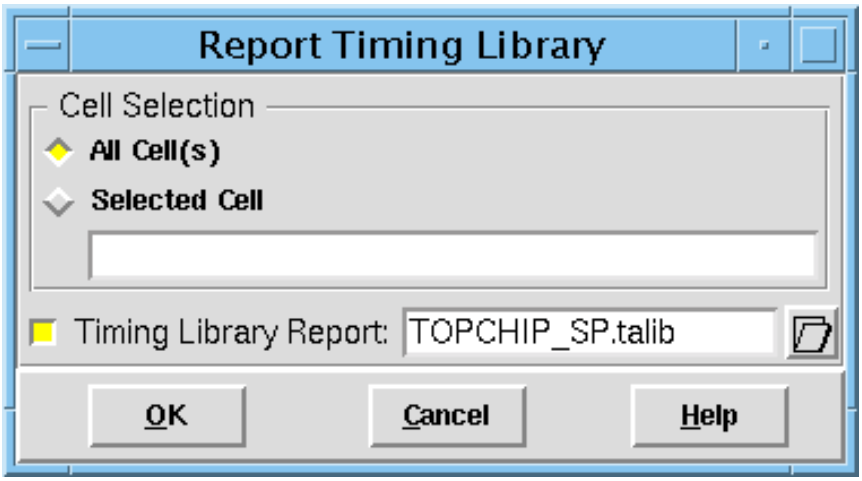
For information on the following topic, see “Timing Analysis” in the *Encounter User Guide*.

■ Reading Timing Libraries

Timing Library – Report

Use the Report Timing Library form to output the cell information to a report file after importing the design and loading the timing library. The report file is generated in ASCII format.

➤ Choose *Timing – Report – Timing Library*.



Report Timing Library Fields and Options

All Cell(s)	Reports timing information for all cells. This is the default option.
Selected Cell	Reports timing information on the cells specified in the text box.
Timing Library Report	Specify a filename or click the file folder icon to choose a file. If you do not select this option, the report is displayed on the Encounter console. The default filename is `TopCellName.talib`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `reportTimingLib`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “Timing Analysis” in the *Encounter User Guide*.

- Analyzing Timing Problems

Report

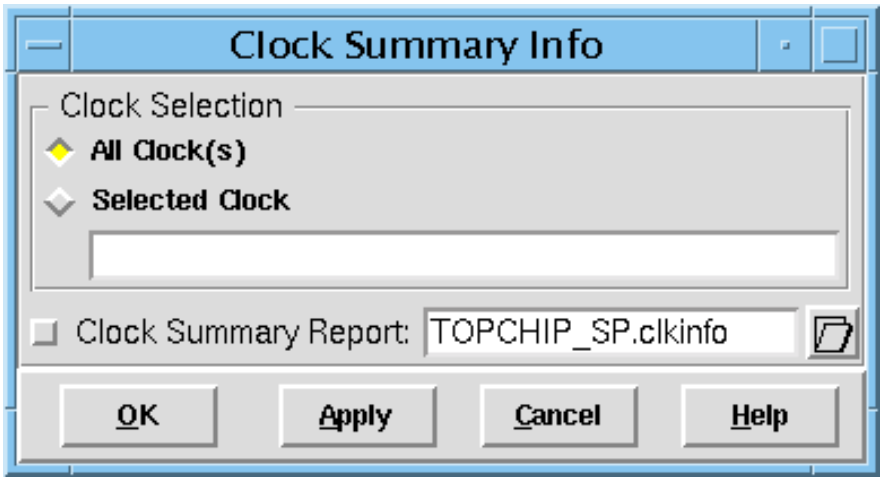
The Report menu provides the following commands for generating clock waveform and cell footprints reports:

- Clock Waveform on page 1480
- Cell Footprint on page 1482

Clock Waveform

Use the Clock Summary Info form to generate reports containing the clock information from the timing constraints file.

➤ Choose *Timing – Report – Clock Waveform.*



Report Clock Waveform Fields and Options

All Clocks(s)	Reports clock information for all clocks. This is the default option.
Selected Clock	Reports clock information for the clocks specified in the text box.
Clock Summary Report	Specify a filename, or click the file folder icon to choose a file. If you do not select this option, the report is displayed on the Encounter console. The default filename is `TopCellName.clkinfo`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `report clocks`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

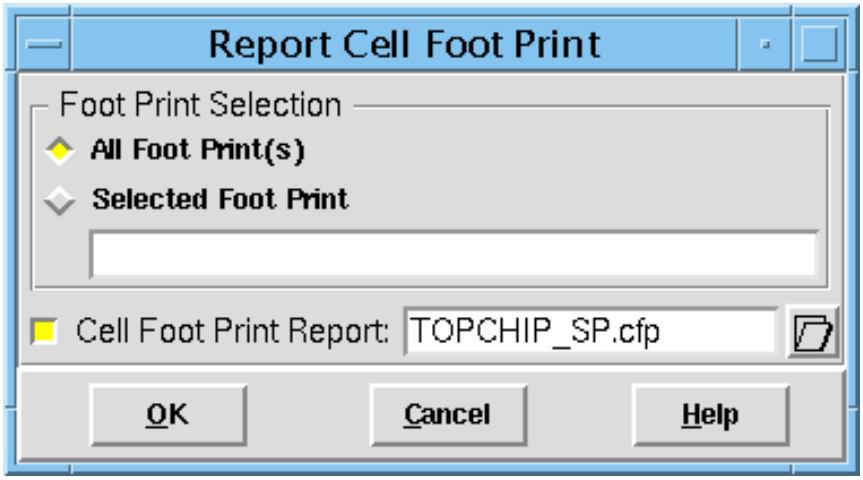
For information on the following topic, see “Timing Analysis” in the *Encounter User Guide*.

- Analyzing Timing Problems

Cell Footprint

Use the Report Cell Foot Print form to output the cell footprint information to a report file after importing the design and reading the timing library. This report file contains the cell names, footprint names, the rising and falling drive resistance values, and the functions.

➤ Choose *Timing – Report – Cell Footprint*.



Report Cell Footprint Fields and Options

All Foot Print(s)	Reports information for all cells. This is the default option.
Selected Foot Print	Reports information on the cells specified in the text box.
Cell Foot Print Report	Specify a filename, or click the file folder icon to choose a file. If you do not select this option, the report is displayed on the Encounter console. The default filename is `TopCellName.cfp`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `reportFootPrint`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

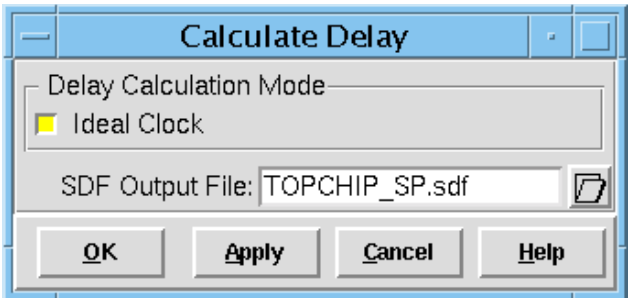
For information on the following topic, see “Timing Analysis” in the *Encounter User Guide*.

- Analyzing Timing Problems

Calculate Delay

Use the Calculate Delay form to calculate delays and generate an SDF file containing delay information.

➤ Choose *Timing – Calculate Delay*.



Calculate Delay Fields and Options

Ideal Clock	Forces the clock nets on each flip-flop clock input pin to use 0 ps. You can change the ideal default clock transition time in the *Timing* page in the Design Import form. The clock buffer delays are read from the timing library.
SDF Output File	Specifies the name of the SDF file to which to output the calculation results. Alternatively, click the file folder icon to choose a file. *Default:* `topModule.sdf`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `delayCal`

For more information, see “Delay Calculation Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “Calculating Delay” in the *Encounter User Guide*.

- Running Delay Calculation

Generate

The Generate menu provides the following commands to generate capacitance tables and wireload models:

- Capacitance Table on page 1486
- Wire-Load Model on page 1489

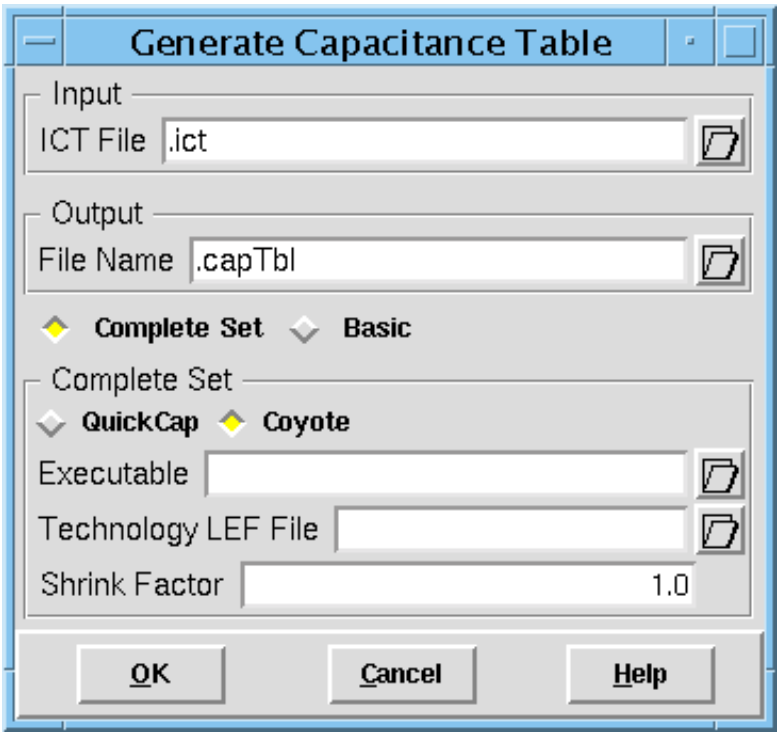
Capacitance Table

Use the Generate Capacitance Table form to replace the rough estimate of the parasitic parameters in the technology file with accurate data from a 2-D and a 3-D field solver. If you do not generate a capacitance table, the tool creates an internal capacitance table that contains rough estimates of the parasitic parameters.

Important

Generating a capacitance table is CPU-intensive and can take a full day to run for newer technologies. Use the `generateCapTbl` standalone executable which can be found in the `/bin` directory of your Encounter hierarchy. The standalone executable runs independent of Encounter; it has the same syntax as the `generateCapTbl` command.

➤ Choose *Timing – Generate – Capacitance Table*.



Generate Capacitance Table Fields and Options

ICT File	Specifies the name of the ICT file.
File Name	Specifies the output file name that will contain the capacitance table.
Complete Set *Basic*	Selects the type of capacitance table to generate. If you select the *Basic* option, the remaining options on the form are unavailable. If you select *Complete Set*, you must choose either QuickCap or Coyote as the executable that will generate the capacitance table. **Note:** Use the *Complete Set* option to generate an extended capacitance table with more accurate parasitics.
QuickCap	QuickCap is available from Random Logic Corporation.
Coyote	The Coyote executable is part of the Encounter package and can be found in the Encounter hierarchy. There is no additional license required. Default: Coyote

Executable	Specifies the complete, absolute path of the executable file. For example:
	`/cad/SOC32/sun4v/tools/bin/coyote`
	for Coyote
	`/cad/random_logic_corp/sun/quickcap`
	for QuickCap

Technology LEF File	
	Specifies the name of the technology LEF file. If the LEF is provided, routing pitch, wire widths, and non-default routing rule information will be used to optimize the capacitance table generation.
Shrink Factor	Specifies the value by which the measurements in the optional LEF file have to be shrunk for the technology used with this design. The default value is `1`.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `generateCapTbl`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

Related Topics

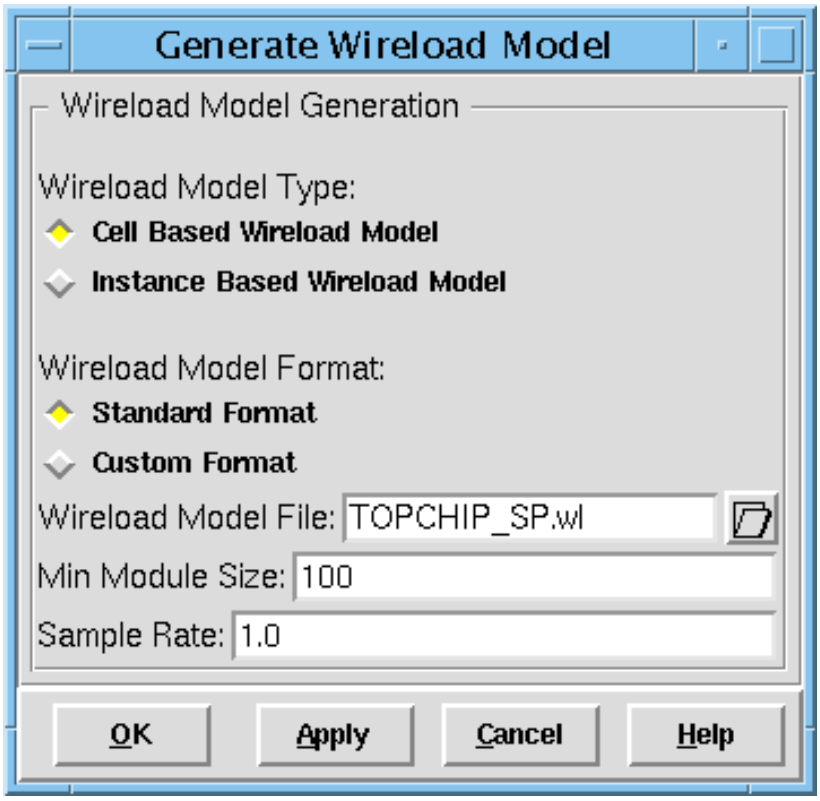
For information on the following topics, see “RC Extraction” and “Appendix A” in the *Encounter User Guide*:

- Generating a Capacitance Table
- Creating the ICT File

Wire-Load Model

Use the Generate Wireload Model form to generate the hierarchical and flat wireload model data. If the operating condition or the scaling factors are changed, you must run extraction to update the extracted RC data before generating new wireload models.

➤ Choose *Timing – Generate – Wire-Load Model*.



Generate Wireload Model Fields and Options

Cell Based Wireload Model

Generates the hierarchical and flat wireload models for cell types used in the design. A wireload model is generated for each cell type. The cell-based model is used for logic synthesis work. This is the default wireload model type.

Instance Based Wireload Model

Generates the hierarchical and flat wireload models for instantiated cell types in the design. A wireload model is generated for each instantiated cell type. The instance-based model is used for simulation work.

Standard Format — Specifies the standard wireload format, which is the default wireload format.

Custom Format — Specifies the custom wireload format. This is also known as the table wireload format. This format is more accurate than the standard format.

Wireload Model File — Either enter a file name or click on the icon to choose a file. The default file name is `TopCellName.wl`.

Min Module Size — Specify the minimum number of cells or instances a mode must contain before a model is generated. The default size is `100`. For a listing of cells or instances where models were not generated, either because of module size or because they contain no internal nets, see the synthesis control script files.

Sample Rate — Specify the *Sample Rate* of the net capacitance distribution for calculating the wireload model. The rate can range from `0.0` to `1.0`.
Default: `1.0`

Related Text Commands

The following text command provides equivalent or additional functionality:

- `wireload`

For more information, see “Timing Commands” in the *Encounter Text Command Reference*.

13

SI Menu

This chapter presents the *SI* menu forms:

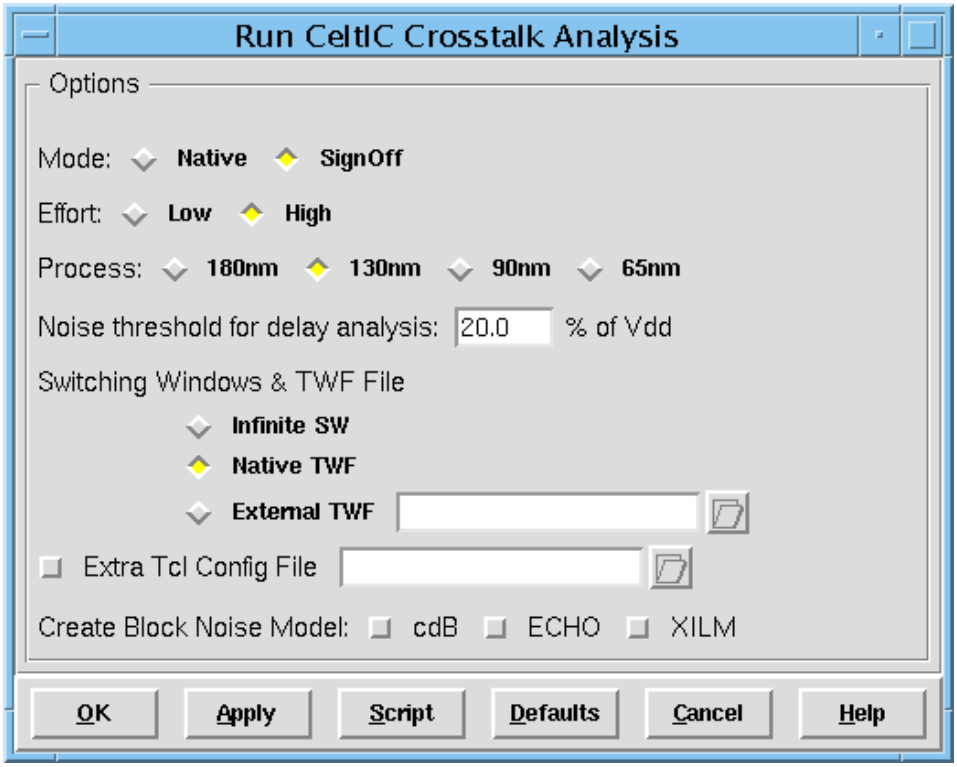
- Run CeltIC Crosstalk Analysis on page 1494
- Display Noise Net on page 1497
- Fix Crosstalk on page 1502

Run CeltIC Crosstalk Analysis

Use the Run CeltIC Crosstalk Analysis form to specify noise analysis information, such as mode, effort, process, and block noise models.

Note: Before performing crosstalk analysis, you must generate RC values for crosstalk coupling capacitance. Use the `setExtractRCMode` command to set RC extraction mode and the `extractRC` command to execute the extraction. Applying switching windows automatically calls the `setExtractRCMode -detail -noReduce` command.

➤ Choose *SI – Run CeltIC Crosstalk Analysis*.



Run CeltIC Crosstalk Analysis Fields and Options

Mode

Specifies which version of CeltIC to use to perform crosstalk analysis.

Note: The runtime for native and standalone is about the same.

Native

Uses the natively-integrated version of CeltIC.

	Signoff	Uses the standalone version of CeltIC. This produces sign-off quality results based on SPICE-like simulations with glitch propagation, sensitivity, and latch-mode analysis using crosstalk noise libraries.
Effort	Specifies the level of effort the tool puts forth during crosstalk analysis. *Default: High*	
	Low	Performs a faster analysis, while trading minimal accuracy for improved run time. Low effort uses a larger time step for simulation compared to high effort.
	High	Produces the best accuracy and should always be selected for final sign-off. High effort uses a smaller time step for simulation compared to low effort.
Process	Specifies the design geometry being used. *Default: 130nm*	
Noise Threshold for delay analysis		
	Enables you to raise the filtering threshold to more than 20 percent of VDD to reduce CeltIC run time. If the noise is higher than the threshold, CeltIC calculates the delay changes. *Default:* `20.0`	
Switching Windows & TWF File		
	Specifies which timing window files to use. *Default: Native TWF*	
	Infinite SW	States that all aggressors can switch at the same time. The resulting analysis is more pessimistic. You can use infinite switching windows when the timing constraints information is not well defined.
	Native TWF	Uses a timing window file generated by Encounter that is based on delay calculations.
	External TWF	Uses a third-party timing window file.
Extra Tcl Config File	Allows you to specify an additional configuration file for CeltIC.	

Create Block Noise Model

cdB	Creates a cdB noise library of the analyzed block for use in a hierarchical methodology.
ECHO	Creates an ECHO noise model of the analyzed block for use in a hierarchical methodology.
XILM	Creates a Interface Logic Module with Xcaps (XILM) for use in hierarchical noise analysis.

Note: Click *Script* if you want to only generate a command script, instead of using the Run CeltIC Crosstalk Analysis form.

Related Text Commands

- `runCeltIC`
- `setSIMode`

For more information, see “Signal Integrity Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “Analyzing and Repairing Crosstalk” in the *Encounter User Guide*:

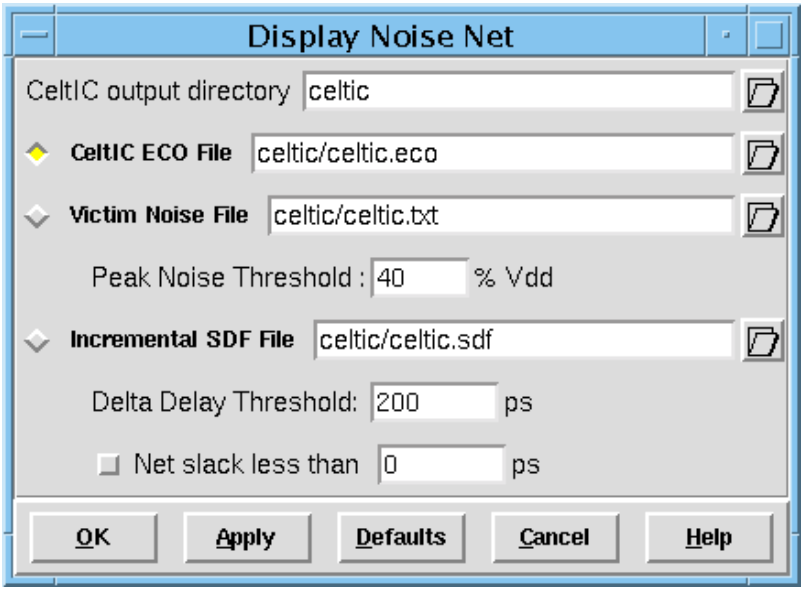
- “Analyzing Crosstalk”

Display Noise Net

Use the Display Noise Net form to specify the files and parameters for displaying net noise. Clicking *OK* or *Apply* opens the CeltIC Result Browser form, which you can then use to browse net noise. For more information, see the "CeltIC Result Browser" on page 1499.

Note: In order to view the noise nets after incremental crosstalk repair, you must first rerun the `runCeltic` command to update the CeltIC `.eco` and `.txt` files.

➤ Choose *SI – Display Noise Net*.



Display Noise Net Fields and Options

CeltIC output directory	Specifies the CeltIC directory in which to find the CeltIC noise analysis report files.
CeltIC ECO File	Displays glitch violations recorded in the specified CeltIC ECO file. *Default:* `celtic/celtic.eco`
Victim Noise File	Specifies the victim/aggressor net file to be used in the browser. *Default:* `celtic/celtic.txt`
	Peak Noise Threshold:

Displays glitch violations based on the victim peak noise as a percentage of VDD.

Default: `40`

Incremental SDF File

Displays noise-induced delay violations based on the specified incremental SDF file.

Default: `celtic/celtic.sdf`

Delta Delay Threshold:

Displays nets with delta delays equal to or greater than the specified threshold value.

Default: `200` ps

Net slack less than

Displays nets with slacks that are less than the specified value.

Default: `0` ps

Related Text Commands

- `viewCeltIC`

For more information, see “Signal Integrity Commands” in the *Encounter Text Command Reference*.

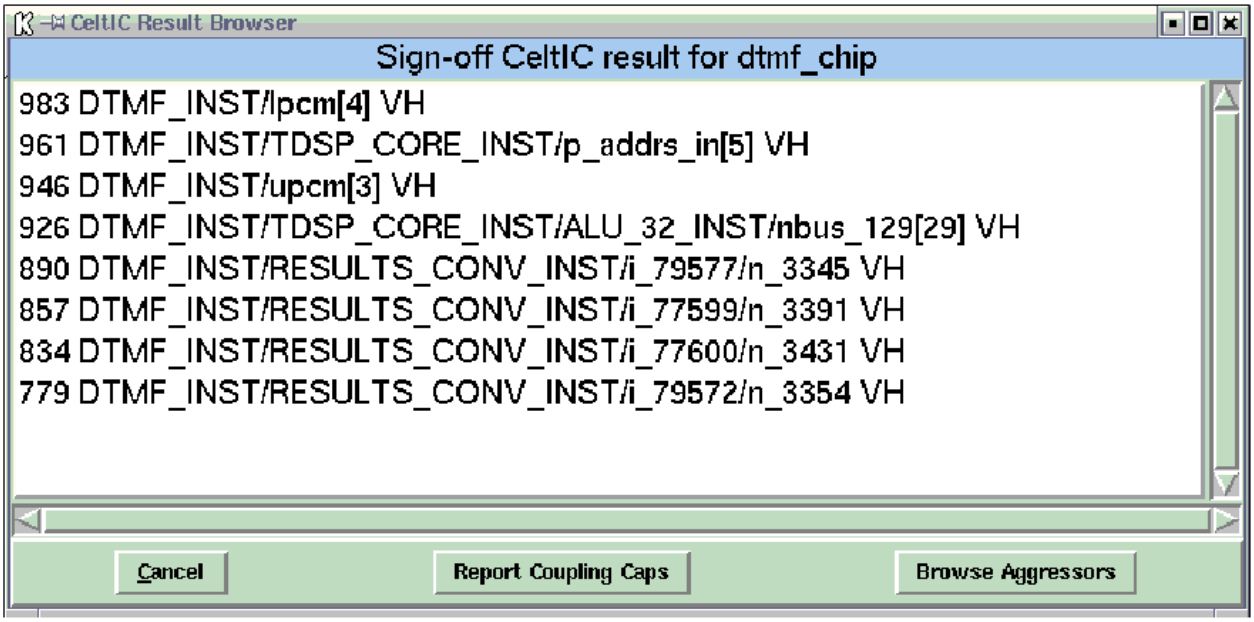
Related Topics

For information on the following topic, see “Analyzing and Repairing Crosstalk” in the *Encounter User Guide*:

- “Analyzing Crosstalk”

CeltIC Result Browser

The CeltIC Result Browser displays a sorted list of victim nets that suffer from the greatest amount of coupling noise.



Using CeltIC Result Browser

1. Use the Display Noise Net form to set up the options for the CeltIC Result Browser form. Click *OK* or *Apply*.

   After the report is read, the CeltIC Result Browser form opens.

   Note: The report will depend on which of the three radio buttons is selected in the Display Noise Net form (*Peak Noise Threshold*, *CeltIC ECO File*, or *Incremental SDF File*).

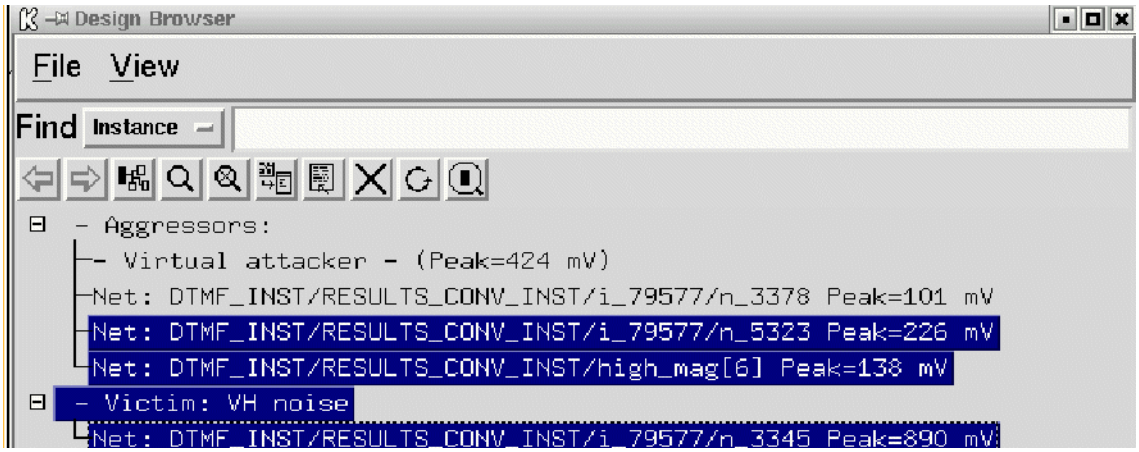
2. To view a net in the design display area, double-click on one of the nets in the list.

   The net is selected and zoomed-in automatically.

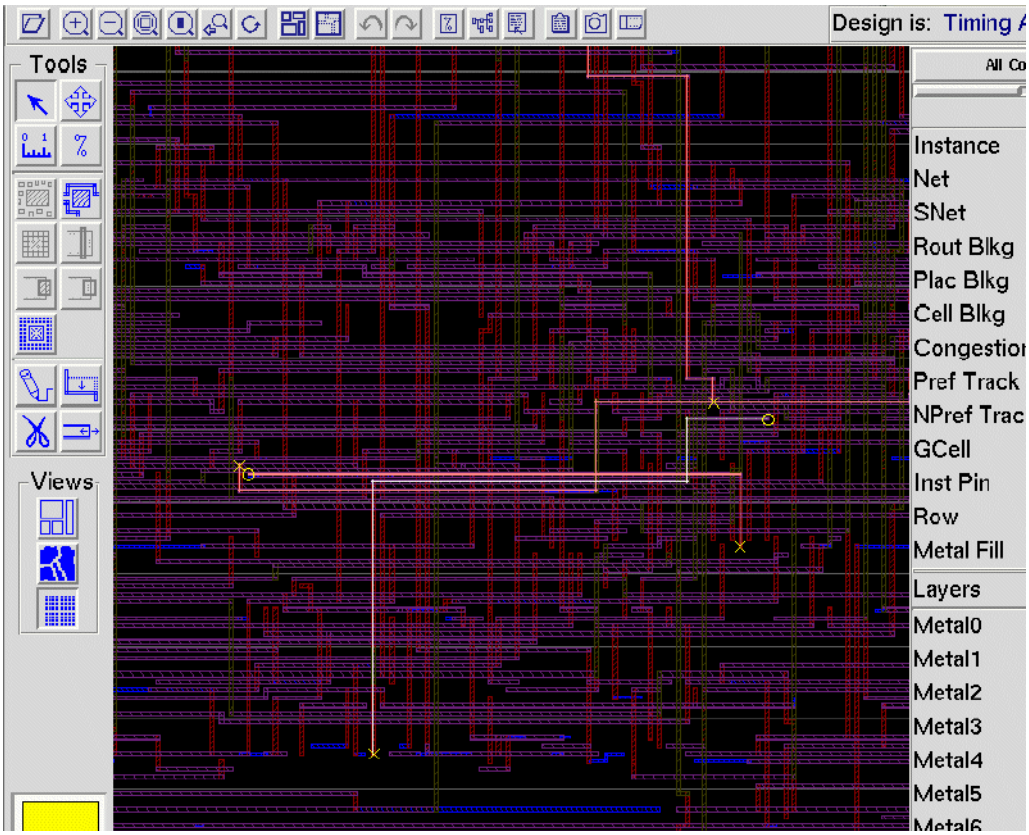
3. To highlight aggressors and victim nets at the same time, click the *Browse Aggressors* button.

   The Design Browser window will open. Press `Ctrl` and click on multiple nets in the design browser, then choose *View – Zoom Selected*.

4. To view the highlighted nets in the design display area, click on any of the nets in the Design Browser window, then choose *View – Zoom Selected.*



5. To view all victim and aggressor nets, use the Design Browser and press `Ctrl` or `Shift`, then click with the mouse. The victims net are shown in white; the aggressor nets are shown in red.



6. To get information about coupling capacitance on selected nets, click *Report Coupling Caps* from the CeltIC Result Browser form.

Related Text Commands

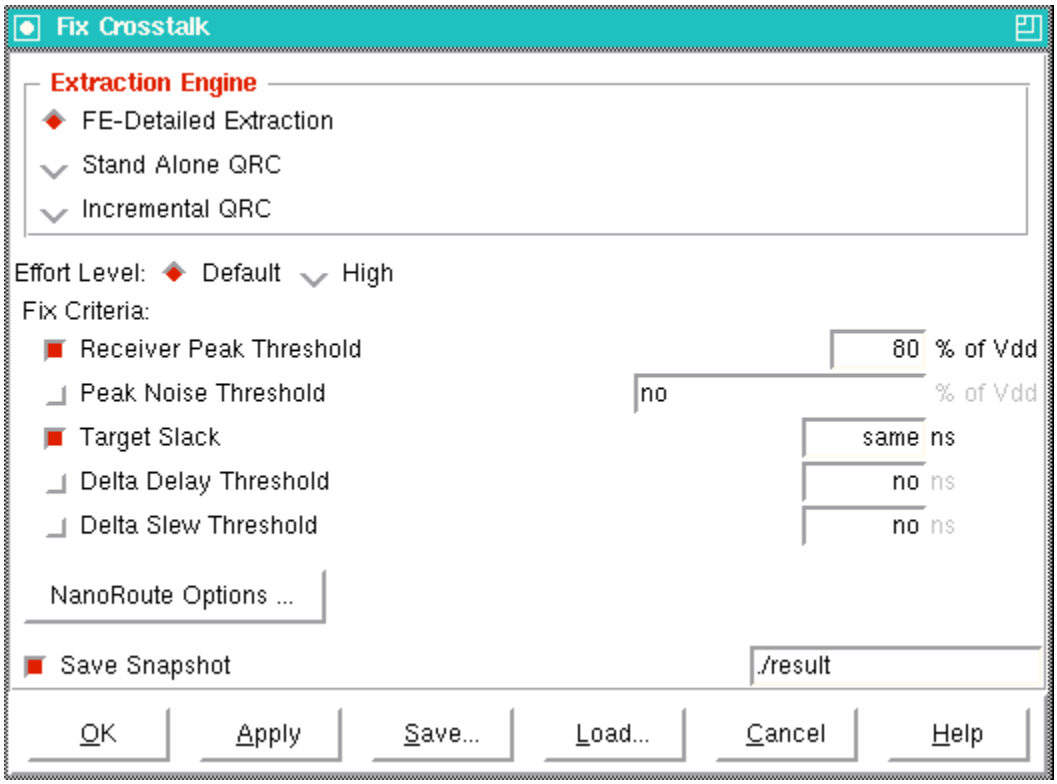
- `reportCouplingCaps`
- `viewCeltIC`

For more information, see “Signal Integrity Commands” in the *Encounter Text Command Reference*.

Fix Crosstalk

Use the Fix Crosstalk form to run incremental (native CeltIC) or sign-off (standalone CeltIC) analysis and repair, to repair noise-on-delay and glitch noise violations. Encounter can repair noise violations using driver resizing, buffer insertion, downsizing rip-up aggressors, or soft spacing routing.

➤ Choose *SI – Fix Crosstalk*.



Fix Crosstalk Fields and Options

Extraction Engine

FE-Detailed Extraction

Uses native RC extraction (detailed) and standalone CeltIC NDC for crosstalk analysis and repair. The extracted parasitics are used for both static timing analysis (including cross-coupling) and signal integrity analysis.

Standalone QRC

Uses QRC standalone sign-off extraction and standalone CeltIC NDC for sign-off crosstalk analysis and repair. This performs a complete sign-off quality extraction and crosstalk analysis and repair of the entire design.

Incremental QRC

Uses native QRC incremental extraction and native CeltIC incremental crosstalk analysis for post-route optimization and SI closure. Extracts the parasitics on only the nets (and neighboring nets) connected to the cells that have been moved, changed, or resized, and nets re-routed due to SI routing changes.

Effort Level

Default Repairs only SI-induced delays and glitch violations on selected nets.

High Enables concurrent timing and SI fixing. This option enables optimization for both base timing and SI-induced delays and glitch violations (concurrently) on the full design.

Note: Using this argument may significantly impact run time.

Fix Criteria

Receiver Peak Threshold

Repairs glitches based on the metric of the peak noise of the receiver output across one channel connected component (CCC).

Default: `80` for sign-off mode; `20` for incremental mode

For more information on the threshold setting for sign-off mode, see the `stability_thresh` global variable in the *CeltIC NDC Command Reference*.

Peak Noise Threshold

Repairs glitch violations based on the metric of the victim peak noise.

Default: No

Target Slack

Repairs whole-path total noise delay.

Default: `same`

Delta Delay Threshold

Repairs larger incremental delays due to noise on a single driver stage.

Default: no

Delta Slew Threshold

Repairs larger delta slews due to noise on a single driver stage.

Default: no

NanoRoute Options

Opens the NanoRoute form to reroute the violating nets with extra spacing. You can either use native or standalone (using Batch mode) NanoRoute to reroute the violating nets.

For more information, see *"Route – NanoRoute"*.

Save Snapshot

Saves the database information for each iteration.

Default: `./result`

Related Text Commands

- `setSIMode`
- `optDesign -postRoute -si`

For more information, see “Signal Integrity Commands” in the *Encounter Text Command Reference*.

Related Topics

For information on the following topic, see “Analyzing and Repairing Crosstalk” in the *Encounter User Guide*:

- Repairing Crosstalk Violations

14

Verify Menu

- Verify Connectivity on page 1508
- Verify Metal Density on page 1514
- Verify Cut Density on page 1519
- Verify Geometry on page 1524
- Verify Process Antenna on page 1533
- Verify AC Limit on page 1535
- Verify Mixed Signal Constraints on page 1539
- Verify Mixed Signal Routing Constraints Filter Output on page 1547

Verify Connectivity

Use the Verify Connectivity form to detect conditions such as opens, unconnected wires (geometric antennas), unconnected pins, loops, partial routing, and unrouted nets. When you verify connectivity, the software generates violation markers in the design window and reports violations. Verifying connectivity does not have database impact unless you save the design, which also saves the violation markers.

Types of Violations Reported

- Antennas

  Unconnected wires (dangling wires). For more information, see Types of Antenna Violations Reported in the “Verifying Violations” chapter of the *Encounter User Guide*.

- Opens

  Parts of nets, such as wires or pins, that are connected to each other but are missing a connection to the net as a whole. Marks each part of a net that is missing a connection as an open and displays a violation marker between the parts.

- Loops

- Unconnected pins

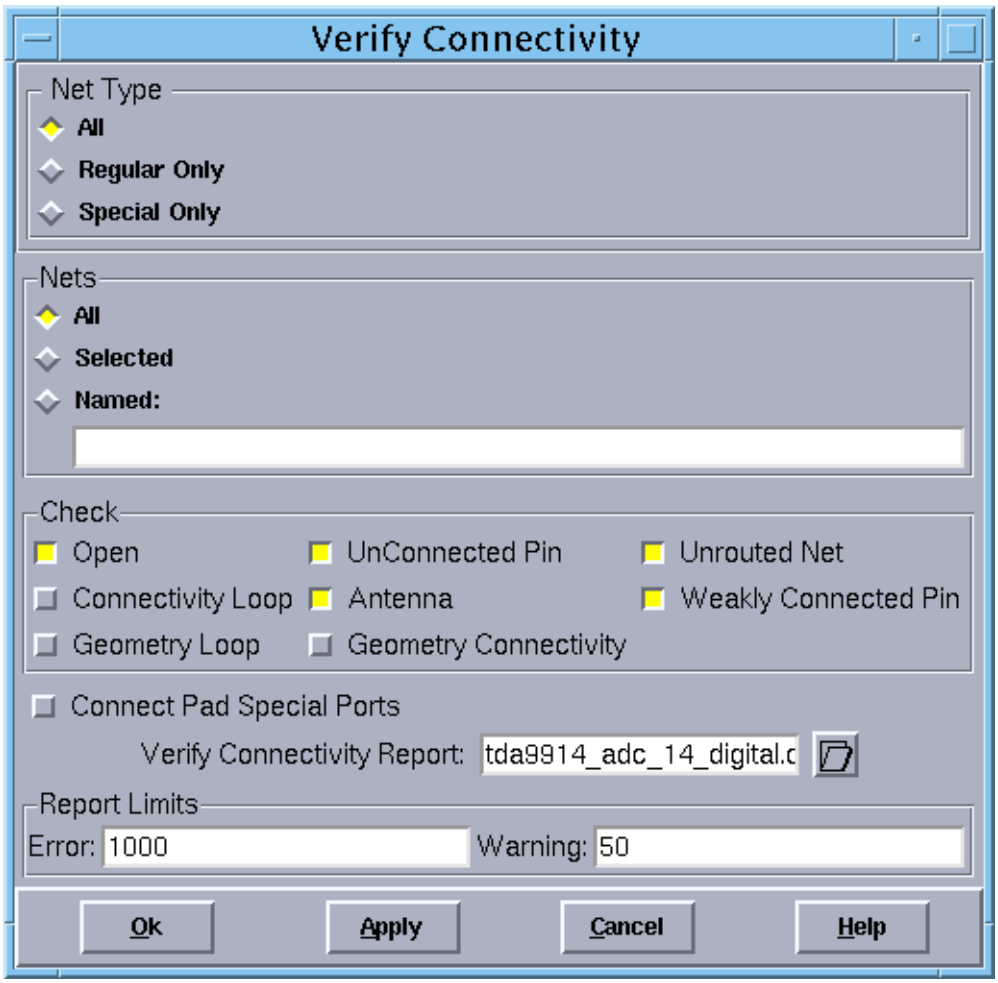
  Pins that are not connected to any other objects

Checks for Opens, Unconnected Pins, and Unrouted Nets

The following combinations of connectivity checks are not enabled:

Open	***Unconnected Pin***	***Unrouted Net***
Off	On	On
Off	On	Off
Off	Off	On

➤ Choose *Verify – Verify Connectivity*.



Verify Connectivity Fields and Options

Net Type	Select one of the following options. *Default: All*	
	All	Checks all nets, including those that have been previously verified.
	Regular Only	Checks only regular nets.
	Special Only	Checks only special nets.
Nets	Select one of the following options. *Default: All*	

All — Checks all nets of the type specified in the *Net Type* panel.

Selected — Checks only nets in the selected set that are of the type specified in the *Net Type* panel.

Named — Checks only nets of the name specified that are of the type specified in the *Net Type* panel. You can use wildcards (* and ?) when you specify the net names.

Check — Select one or more of the following options:

Open — Checks for open violations. Opens are parts of nets, such as wires or pins, that are connected to each other but are missing a connection to the net as a whole.

UnConnected Pin

Checks for pins that are not connected to any objects.

Unrouted Net — Checks for nets that are not routed.

Connectivity Loop

Checks for connectivity loops in regular wires.

The Encounter software detects connectivity loops based on the end points of the center line of a regular wire segment or the center of a via.

Important

Connectivity Loop, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.

Antenna — Checks for violations due to unconnected wires (also called geometrical antennas or dangling wires). For more information, see Types of Antenna Violations Reported in the “Verifying Violations” chapter of the *Encounter User Guide*.

Weakly Connected Pin

Checks for routing to more than one port of the weakly connected pin ports. When this option is selected, Verify Connectivity marks a Weakly Connected Pin violation in one of the ports of the pin.

Geometry Loop

Checks for loop violations of regular nets using a geometrical model. The nets do not have to overlap on the center line. When you specify this option, the Encounter software does not perform any other connectivity checks.

Select this option if you use a third-party router that does not route using the centerline connection routing technique. In this case, *Connectivity Loop* might not detect connectivity loop violations.

Important

Connectivity Loop, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.

Geometry Connectivity

Checks for connectivity violations of regular wires. Uses a geometrical model instead of the center-line model. In other words, if the wires overlap at any point, they are considered to be connected—they do not have to connect at the center line.

Use this parameter if you manually change the routing or use a third-party router that does not route using the centerline connection routing technique.

Important

Connectivity Loop, *Geometry Loop*, and *Geometry Connectivity* are mutually exclusive.

Connect Pad Special Ports

Treats power and ground pins modelled as “weak connect” as though they are “strong connect” in order to avoid false violations. Specifying this parameter can mask real violations if the I/O has no driving connection between the geometries, as can be the case in libraries where there are several small rings instead of one large ring, due to maximum width constraints.

Verify Connectivity Report

Specifies the report file for connectivity violation data.

Report Limits Error

Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded.
Default: `1000`

pgnet	Checks tie-high and tie-low nets for process antenna violations.
noIOPinDefault	Specifies that the following LEF keywords are not applied to the I/O pins in the design: ■ `ANTENNAINPUTGATEAREA` ■ `ANTENNAINOUTDIFFAREA` ■ `ANTENNAOUTPUTDIFFAREA`

Related Text Commands

- `verifyConnectivity`

Verify Metal Density

Use the Verify Metal Density form to check the metal density for each routing layer and the density of large macros. When you verify the metal density, the Encounter software checks the density against the values specified by the LEF file or the `setMetalFill` command. If the density is not specified, the software uses internal default settings.

The `verifyMetalDensity` command can run without `setMetalFill`. The sequence is

- If the LEF file has window size and density defined, the Encounter database also has them, so `verifyMetalDensity` gets them from the database.
- If the LEF file does not have window size and density defined, the `verifyMetalDensity` uses internal default values.

  Note: The `setMetalFill` command is a user-override command that provides constraints at the run time for each session. These constraints have precedence over the LEF/database values.

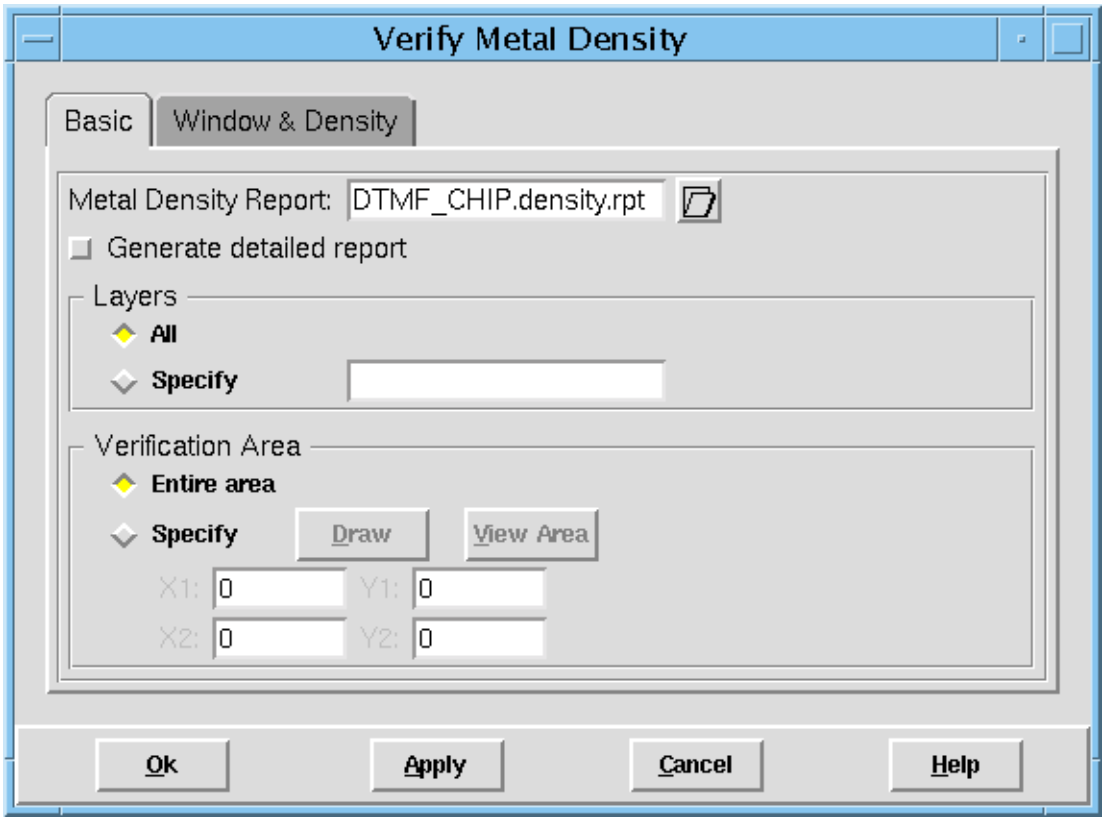
The Verify Metal Density form has two pages:

- Verify Metal Density – Basic on page 1515
- Verify Metal Density – Window & Density on page 1517

Verify Metal Density – Basic

Use the *Basic* page of the Verify Metal Density form to set options for specify options for the metal density report and the area on which to perform the metal density check.

➤ Choose *Verify – Verify Metal Density*.



Verify Metal Density – Basic Fields and Options

Metal Density Report Specifies the report file. The default file name is `designName.density.rpt`.

Generate detailed report

Generates a detailed metal density report.

Layers Select one of the following options:

All Verifies all layers.

	Specify	Verifies the names of the layers that you specify.
Verification Area	Select one of the following options:	
	Entire area	Verifies the entire area.
	Specify	Verifies metal density in the area you specify by using one of the following methods: ■ Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. ■ Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields. ■ Using the *View Area* button to retrieve the coordinates of the current viewing area in the Encounter design display window.

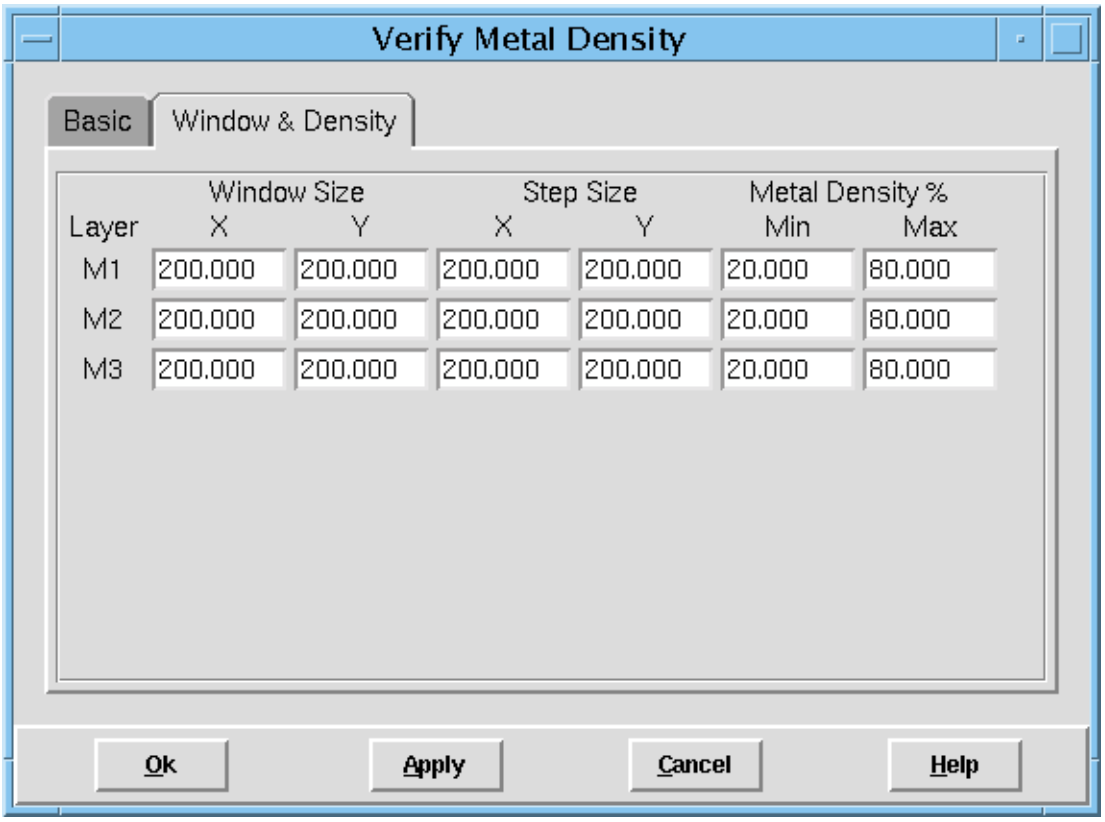
Related Text Commands

- `verifyMetalDensity`
- `setMetalFill`

Verify Metal Density – Window & Density

Use the *Window & Density* page of the Verify Metal Density form to specify window size, step size, and metal density percentage for each layer.

➤ Choose *Verify – Verify Metal Density* and click on the *Windows & Density* tab.



Verify Metal Density – Window & Density Fields and Options

Window Size	Specify the X and Y coordinates for each layer of the design.
Step Size	Specify the X and Y coordinates for each layer of the design.
Metal Density %	Specify the minimum and maximum values for each layer of the design.

Note: The values that you specify here are updated in the form that is displayed using the *Route – Metal Fill* command.

Related Text Commands

- `verifyMetalDensity`
- `setMetalFill`

Verify Cut Density

The Verify Cut Density form enables you to check the density of specified cut layers or areas of cut layers, or the cut density of the whole chip.

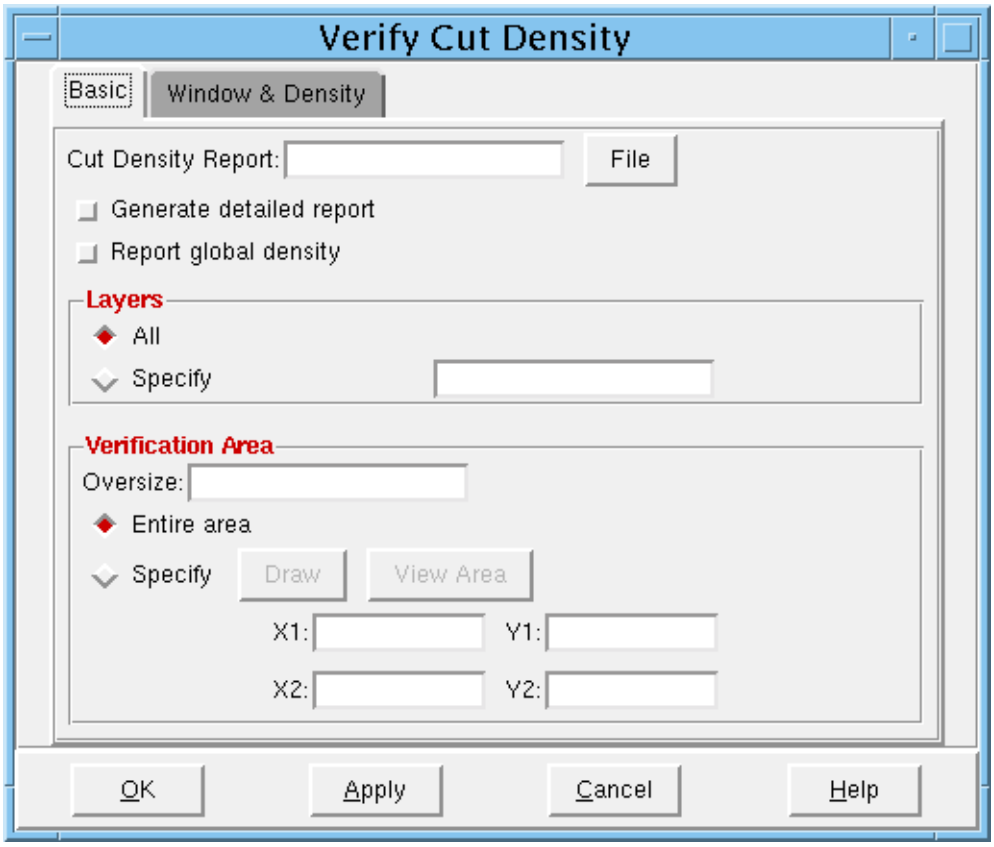
The Verify Cut Density form contains the following pages:

- Verify Cut Density – Basic on page 1520
- Verify Cut Density – Window & Density on page 1522

Verify Cut Density – Basic

Use the *Basic* page of the Verify Cut Density form specify options for the cut density report and the area to check.

➤ Choose *Verify – Verify Cut Density* and click the *Basic* tab.



Verify Cut Density – Basic Fields and Options

Cut Density Report

Specifies the report file for the cut density violation information. *Default:* `designName.cutdensity.rpt`

Generate detailed report

Generates a detailed cut density report.

Report global density

		Checks the density across the entire design for the specified cut layers and writes the results to the report file.
Layers	Specifies the cut layers to verify. Select one of the following options:	
	All	Check density on all cut layers.
	Specify	Checks density only the the specified layers. Use the following format to specify layer names: `{V12 V23}`
Verification Area Oversize	Specifies an offset value for the area to verify. The value is in user units (not in DBU), and can be positive or negative. A positive value adds to the area that is verified. For example, if the design covers the area from `(0,0)` to `(100,100)` and you specify `10`, the software checks the area from `(-10,-10)` to `(110,110)`. *Default:* `0`	
Entire	Checks the entire area on the specified layers.	
Specify	Checks the area within the bounding box you specify.	

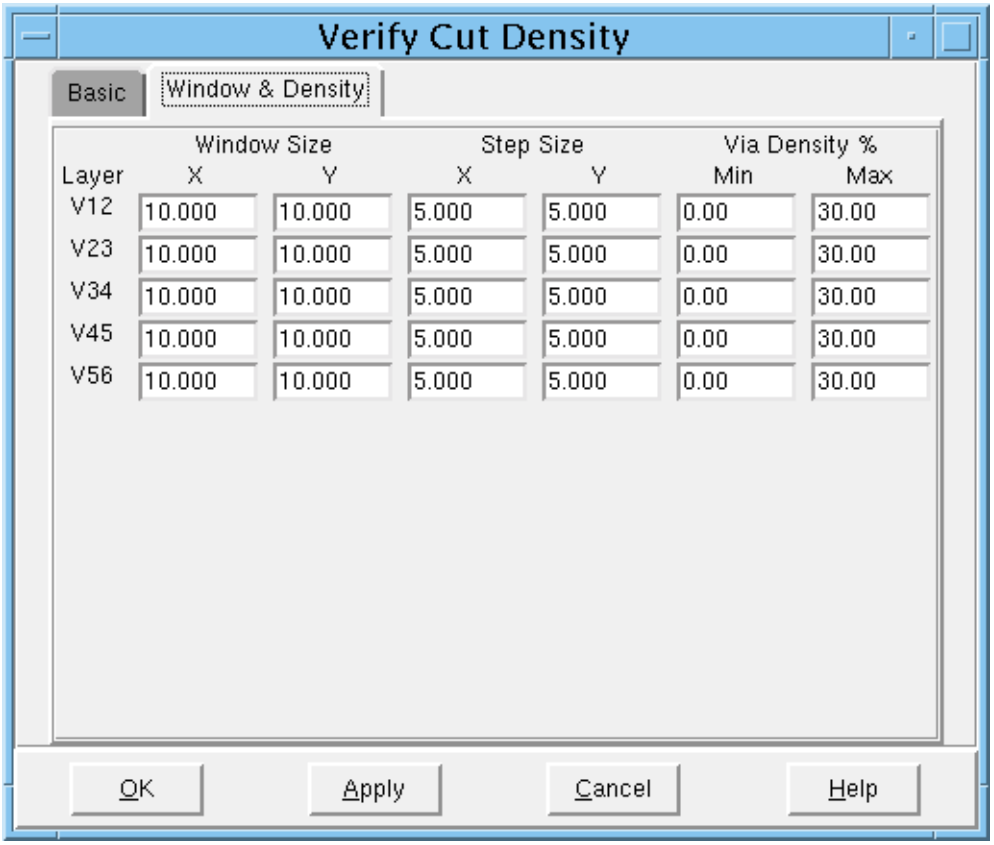
Related Text Commands

- `verifyCutDensity`

Verify Cut Density – Window & Density

Use the Window & Density page of the Verify Cut Density form to specify window size, step size, and metal density percentage for each layer.

➤ Choose *Verify – Verify Cut Density* and click the *Window & Density* tab.



Verify Cut Density – Window & Density Fields and Options

Window Size	Specify the X and Y coordinates for each cut layer.
Step Size	Specify the X and Y coordinates for each cut layer.
Via Density %	Specify the minimum and maximum values for each cut layer.

Related Text Commands

- `verifyCutDensity`

Verify Geometry

Use the Verify Geometry form to verify the widths, spacing, and internal geometry of objects and the wiring between them.

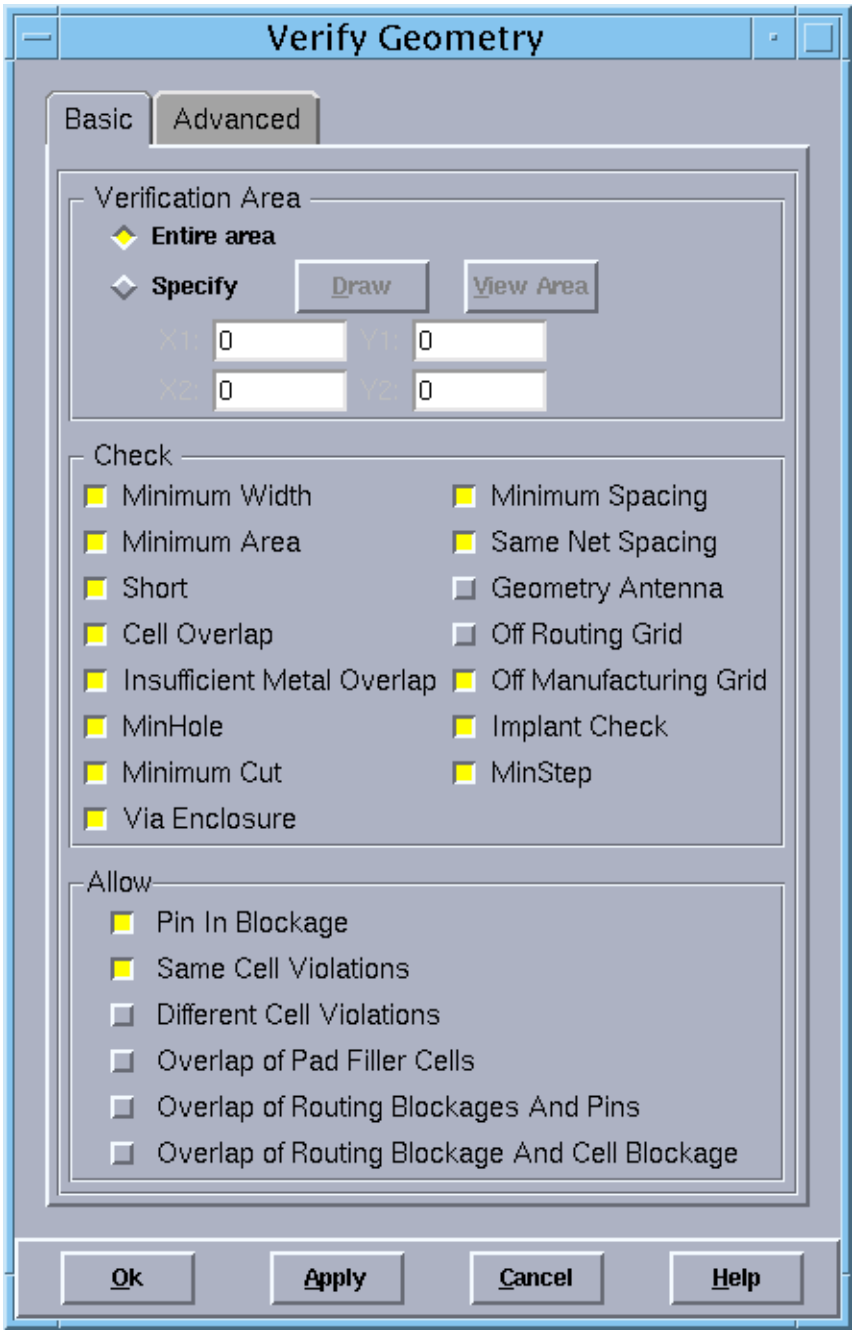
The Verify Geometry form has two pages:

- Verify Geometry – Basic on page 1525
- Verify Geometry – Advanced on page 1530

Verify Geometry – Basic

Use the *Basic* page of the Verify Geometry form to specify options for basic geometry checks.

➤ Choose *Verify – Verify Geometry* and click the *Basic* tab.



Verify Geometry – Basic Fields and Options

Verification Area — Select one of the following options:

- *Entire Area* — Verifies all geometries in the whole design, based on the settings on this form.
- *Specify* — Verifies geometries in the area you specify by using one of the following methods:
  - Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields.
  - Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields.
  - Using the *View Area* button to retrieve the coordinates of the current viewing area in the Encounter design display window.

Check — Select one or more of the following options:

- *Minimum Width* — Checks that special wire geometries in the design are not smaller than the minimum default size for that layer, as specified in the LEF file.
- *Minimum Area* — Checks objects smaller than the `AREA` specified in the `LAYER` section of the LEF file.

  If `AREA` is not defined for a layer in LEF, and `TOPOFSTACKONLY` via is defined, Verify Geometry sets the value of `AREA` for that layer as the area of the bottom rectangle of the `TOPOFSTACKONLY` via.
- *Short* — Checks for shorts between two geometries belonging to different nets.
- *Cell Overlap* — Checks for overlapping cells in the routed design, as well as overlapping blockages from different components.

Insufficient Metal Overlap

Checks that the overlap of two geometries meets the minimum size requirement for the layer.

MinHole

Checks violations where the minimum area of the hole is less than the minimum enclosed area defined in the LEF file.

Minimum Cut

Checks whether vias have the number of cuts specified by the `MINIMUMCUT` rule. The rule specifies the number of cuts a via must have when it is on a wide wire or pin whose width is greater than width. The rule applies to all vias touching a particular metal layer.

Via Enclosure

Checks whether via enclosures meet the specified required x and y enclosure values for the bottom and top metal layers.

Minimum Spacing

Checks that the spacing between two geometries does not violate the minimum spacing rule in the LEF file.

Same Net Spacing

Checks for violations between two geometries belonging to the same net. These violations can occur when minimum spacing is less than the value defined by the `SAMENET SPACING` rule in the LEF file or stack via with no corresponding `STACK` keyword in the `SAMENET SPACING` rule are present.

Geometry Antenna

Checks for wires that do not terminate at wires, pins or vias and vias that do not terminate at wires, vias, or pins.

Off Routing Grid

Checks that each geometry covers at least one grid point on the routing grid. This check reports two kinds of violations; no-grid and off-grid. No-grid violations are reported for blockages, pins, special wire, and special vias that do not enclose a grid point. The off-grid violations are reported for regular vias whose centers do not lie on-grid and for regular wires whose startpoint and endpoint do not lie on the routing grid.

Off Manufacturing Grid

Checks that corners of each geometry cover a point on the manufacturing grid.

Implant Check

Checks violations on implant layers. Use this parameter when you run `verifyGeometry` before inserting filler cells.

MinStep Checks for minimum step violations.

Allow Select one or more of the following options:

Pin In Blockage Allows pin and obstruction shorts on the same component.

Same Cell Violations

Allows same-cell violations. This parameter is disabled when *Different Cell Violations* is selected.

Different Cell Violations

Allows violations between two different cells. When this option is selected, the following three parameter are disabled:

- *Same Cell Violations*
- *Overlap of Routing Blockages And Pins*
- *Overlap of Routing Blockage and Cell Blockage*

Overlap of Pad Filler Cells

Allows overlap violations between pad filler cells.

Blockage Overlap of Routing Blockages And Pins

Allows a routing obstruction to overlap a pin. This parameter is disabled when *Different Cell Violations* is selected.

Overlap of Routing Blockage and Cell Blockage

Allows overlapping cell and routing obstructions. This parameter is disabled when *Different Cell Violations* is selected.

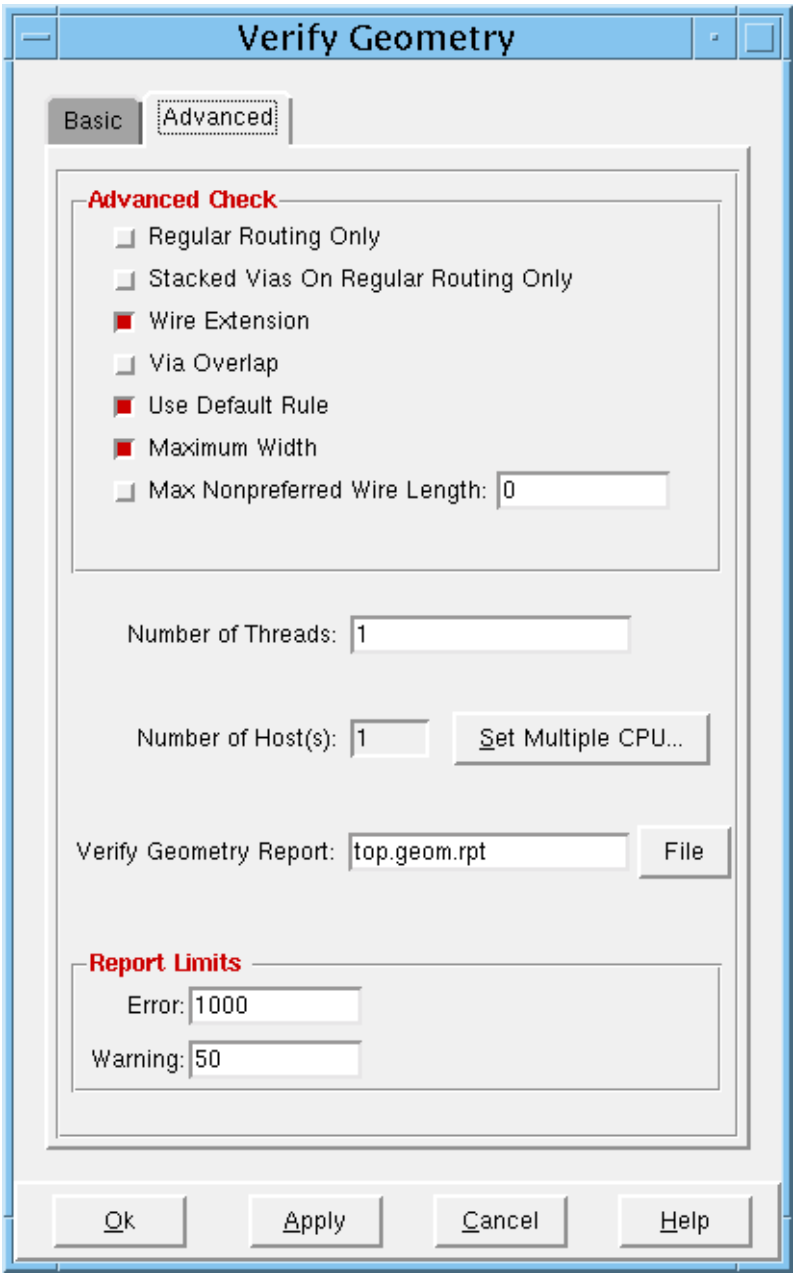
Related Text Commands

- `verifyGeometry`

Verify Geometry – Advanced

Use the *Advanced* page of the Verify Geometry form to specify advanced checks.

➤ Choose *Verify – Verify Geometry* and click on the *Advanced* tab.



Verify Geometry – Advanced Fields and Options

Regular Routing Only

Checks for violations in regular routing only. All special geometries are ignored.

Note: The Verify Geometry feature does not check regular routing in X-style designs, so this option is disabled when the software detects X routing.

Stacked Vias On Regular Routing Only

Checks for stacked vias in regular routing only. All stacked via violations in special routing are ignored.

Wire Extension

Checks that wires are extended by the amount specified in the `WIREEXTENSION` definition in the Layer (Routing) section of the LEF file, and checks that vias dropped onto pins also satisfy wire extension.

Via Overlap

Checks for overlapping vias.

Use Default Rule

Ignores nondefault spacing rules for spacing violations. Uses default rules for spacing violations.

By default, spacing larger than the minimum spacing in nondefault rules are “soft” rules, that is, preferred spacing rules that are not enforced by the router and not checked by `verifyGeometry`.

If you select this option, `verifyGeometry` treats nondefault spacing rules as “hard” rules and creates violations whenever they are not met.

Maximum Width

Checks objects whose widths are greater than the `MAXWIDTH` specified in the Layer section of the LEF file.

Merge

Merges same-net geometries to determine width-dependent spacing. If you do not use this option, the Encounter software uses the shape of the object from the database. If you do use this option, the software merges the overlapping same-net objects to create maximum overlapping rectangles. If the LEF file contains width-dependant rules, the software reports different results with or without *Merge* option.

Max Nonpreferred Wire Length

Sets the maximum length for wires in the nonpreferred routing direction.
Default: `0`

Number of Threads

Specifies the number of threads used for verifying geometry in multi-thread mode. You need additional licenses for additional threads. After the first license, each additional license enables three threads.

Important

The Verify Geometry feature does not use the Multiple CPU Processing form or `setMultiCpuUsage` command for multi-threading. In addition, if you are running distributed processing, this command ignores the setting for this option.

Number of Host(s)

Displays the number of hosts specified for distributed processing. This is a non-editable field. To change the number of hosts, click the *Set Multiple CPU* button, which opens the Set Multiple CPU Processing form. For more information, see "Multiple CPU Processing" on page 373.

Verify Geometry Report

Specifies the filename for the Verify Geometry Report. The file contains detailed information that is suitable for debug purposes only. For a concise list of violations, use the Violation Browser report file.

Error

Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded.
Default: `1000`

Warning

Specifies the maximum number of warnings to report. After this number is reached, the verification process ends.
Default: `50`

Related Text Commands

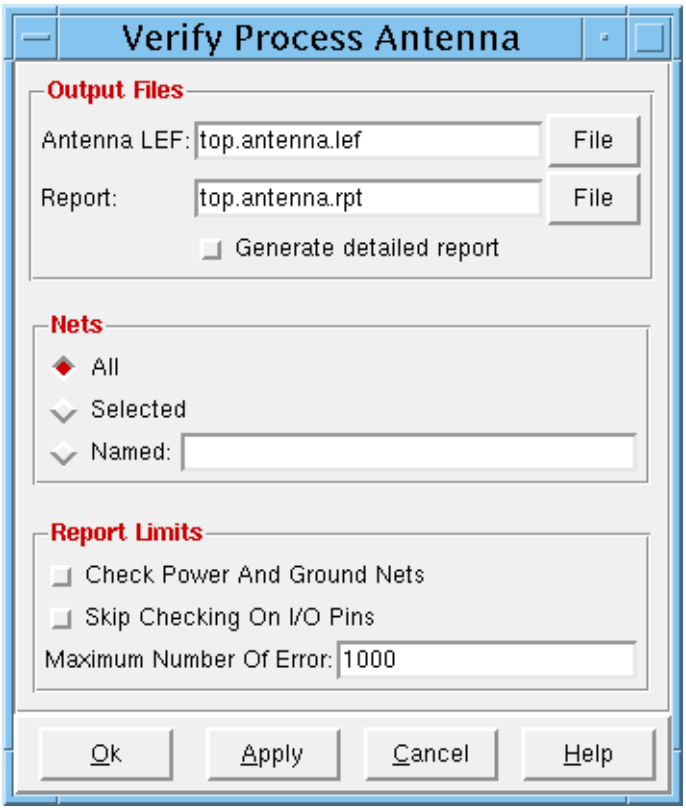
- `verifyGeometry`

Verify Process Antenna

Use the Verify Process Antenna form to verify Process Antenna Effect (PAE) violations in the routed design.

> **Note:** Verify Process Antenna also checks for maximum floating area violations in the design. For more information, see `verifyProcessAntenna` in the *Encounter Text Command Reference*.

➤ Choose *Verify – Verify Process Antenna*.



Verify Process Antenna Fields and Options

Output Files	Displays the names of the output files this command creates.
Antenna LEF	Specifies the LEF file that contains the antenna information for the I/O pins of the design.
Report	Specifies the report file. *Default:* `design.antenna.rpt`

Generate detailed report

Generates a detailed report containing process antenna information for all nets, including those without violations. For more information, see "Sample Process Antenna Report" in the *Encounter User Guide*.

Nets

Select one of the following options:

All	Reports violations for all the nets in the design.
Selected	Reports violations for selected nets only.
Named	Reports violations for only the nets named in this field. Separate names with a space.

Report Limits

Lets you specify what to check and the maximum number of errors to report.

Check Power and Ground Nets

Checks tie-high and tie-low nets for process antenna violations.
Default: Off

Skip Checking on I/O Pins

Does not check I/O pins for errors. The following LEF keywords are not applied to the I/O pins in the design:

- `ANTENNAINPUTGATEAREA`
- `ANTENNAINOUTDIFFAREA`
- `ANTENNAOUTPUTDIFFAREA`

Maximum Number of Error

Specifies the maximum number of errors to report. The software generates a warning message if this number is exceeded.
Default: `1000`

Related Text Commands

- `verifyProcessAntenna`

Verify AC Limit

Use the Verify AC Limit form to check for AC current violations on signal nets.

Calculates the root mean square current (Irms) at the driver output and compares it to the `ACCURRENTDENSITY` tables in the LEF file that contain the Irms limits for routing layers. Generates an error and attaches a violation marker to a net if the calculated Irms for a net exceeds the `ACCURRENTDENSITY` Irms limit for a routing layer or width used by the net.

Computes the root mean square current (Irms) from the slew rates of the signal, the capacitance of the net, and the toggle-rate frequency as computed by timing analysis commands like `buildTimingGraph` and `check_timing` (and the values can be written out with the `-report` parameter). If there is more than one timing view in use, uses the default setup view (controlled by `set_default_view -setup` *`viewName`* command).

setup view (controlled by `set_default_view -setup` *`viewName`* command).

Tip

For increased accuracy on long wires, use SignalStorm® to calculate Irms. In the AC Limit report file, Irms values that are calculated using SignalStorm end with dollar signs ($). To enable SignalStorm calculation, run the following command before running `verifyACLimit`:

```
setDelayCalMode -engine signalStorm
```

For more information, see `setDelayCalMode` in the *Encounter Text Command Reference*.

`verifyACLimit` checks each routing segment separately, eliminating false violations that might be caused by assuming the same current for the entire route. This feature is useful for calculating current at the inputs where it is not as strong due to branching and tapering of wires.

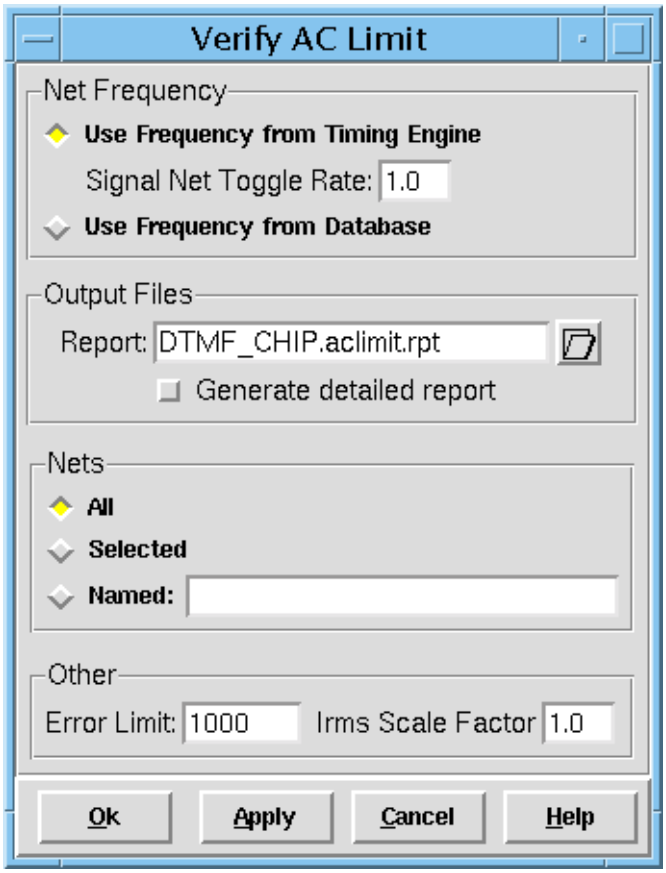
Routing with loops in it, like a clock-mesh, is ignored although the initial driver output and wiring Irms that connect to a mesh can be computed if SignalStorm delay calculation is used.

`verifyACLimit` also checks the `ACCURRENTDENSITY` tables for the following conditions and takes the following actions:

- If there is no table for a routing layer, the software gives a warning and assumes an infinite limit for the layer.
- If `PEAK` and `AVERAGE` tables are present, the software ignores them.

Note: This command reports the AC current density in `mA`. The LEF file specifies it in `mA/micron`. To convert the LEF specification, the `verifyACLimit` command reads the value in `mA/micron` and multiplies it by the wire width.

➤ Choose *Verify – Verify AC Limit.*



Verify AC Limit Fields and Options

Use Frequency from Timing Engine

Uses the frequency from the timing engine as the effective frequency (F_{eff}) per net. The Encounter software estimates the effective frequency from the timing analysis engine by using the frequency of the associated clock. The effective frequency of the net is half the associated clock frequency times the toggle rate, because the output of a flip-flop and downstream logic only changes at half the rate of the input clock.

Specify the following option to set the toggle rate for signal nets:

Signal Net Toggle Rate

Specifies the toggle rate for signal nets. A value of 1.0 means that if a flip-flop is clocked by a 20 Mhz clock, it changes state on 100% of the clock cycles. Therefore the signal has 20 million transitions which is half the number of transitions of the input clock. Therefore the final signal net frequency is 10 Mhz.
Range: `0.0` to `1.0`.
Default: `1.0`

Use Frequency from Database

Uses the database frequency value as the effective frequency per net. You cannot use this option if you set a value in the *Signal Net Toggle Rate* field.

You use the `verifyACLimitSetFreq` command to set the effective frequency on each net in the database from the timing analysis results. You can then use the `dbNetFrequency` and `dbSetNetFrequency` Tcl functions to check or modify any given net before using the *Use Frequency from Database* option. The frequency values are stored in Hertz in the database.

Report

Specifies the report file. The default file name is *`design`*`.aclimit.rpt`. The report file includes name of the net, Irms, interpolated `ACCURRENTDENSITY` limit (I_{limit}), layer, width, X and Y location, rise and fall time, effective frequency for the net (F_{eff}), Cnet and Vdd for each net.

Specify the following option to generate a detailed report:

Generate detailed report

Generates a detailed AC limit report containing the information for all nets, including those without violations.

Nets

Select one of the following options:

All — Reports violations for all the nets in the design.

Selected — Reports violations for selected nets only.

	Named	Reports violations for only the nets named in this field. Separate names with a space.
Others	Specify the following options:	
	Error Limit	Specifies maximum number of errors to report. The software generates a warning message if this number is exceeded. *Range:* `0` to `1000000` *Default:* `1000`.
	Irms Scale Factor	Specifies the scale factor for root mean square current (I_{rms}). The Encounter software multiplies Irms value by the scale factor before checking for violations. The software uses a square wave to approximate current. To use a triangular wave approximation, specify `1.15`. *Range:* `0.0` to `10.0` *Default:* `1.0`

Related Text Commands

- `verifyACLimit`
- `verifyACLimitSetFreq`

Verify Mixed Signal Constraints

The *Verify* menu's Verify Mixed Signal Constraints form enables you to check that the routing and electrical mixed signal constraints are met and to generate a violation report.

The Verify Mixed Signal Constraints form contains the following pages:

- Verify Mixed Signal Constraints – Routing on page 1540
- Verify Mixed Signal Constraints – Electrical on page 1545

Verify Mixed Signal Constraints – Routing

Use the *Routing* page of the Verify Mixed Signal Constraints form to check that nets routed by the mixed signal router meet the constraints specified by the mixed signal routing constraint editor and generate a violation report. You can limit the violations reported by specifying high and low values for spacing violations, resistance, and width to report.

The verifier checks that net resistance, capacitance, width, and minimum via cut constraints are met. In addition, it checks the following types of nets:

- Bus routing

  Specified nets have the same width and spacing and, optionally, the same topology.

- Differential pairs

  The parasitic load on driving pins of the nets must be equal.

- Do not cross nets

  Potentially noise-causing nets are prohibited from crossing noise-sensitive nets.

- Matched nets

  Nets must be the same length.

- Routed nets

  Nets must meed width, resistance, capacitance, and minimum via cut constraints.

- Shielded nets

  Noise-critical nets are shielded by special nets on their right and left sides, or on the right, left, top, and bottom sides.

Maximum and Minimum Resistance Constraints

Nets must meet maximum and minimum resistance requirements. The verifier marks a violation on the output pin of the instance or block driving the net if the maximum resistance is greater than the maximum resistance specified by the constraint or if the minimum resistance is less than the minimum resistance specified by the constraint.

The software calculates resistance for a net with *n* segments using the following formula:

Resistance =
((*resistivity of segment_1*) x
(*length of segment_1*)/*width of segment_1*)) +

... +
((*resistivity of segment_n*) x
(*length of segment_n*)/*width of segment_n*)) +
resistance of via_1 +
... +
resistance of via_n

Maximum Capacitance Constraints

Nets must meet maximum capacitance requirements. The verifier marks a violation on the output pin of the instance or block driving the net if the capacitance exceeds the maximum resistance specified by the constraint.

The verifier and the mixed signal router use the same formula for calculating the capacitance.

The software calculates capacitance using the following formula:

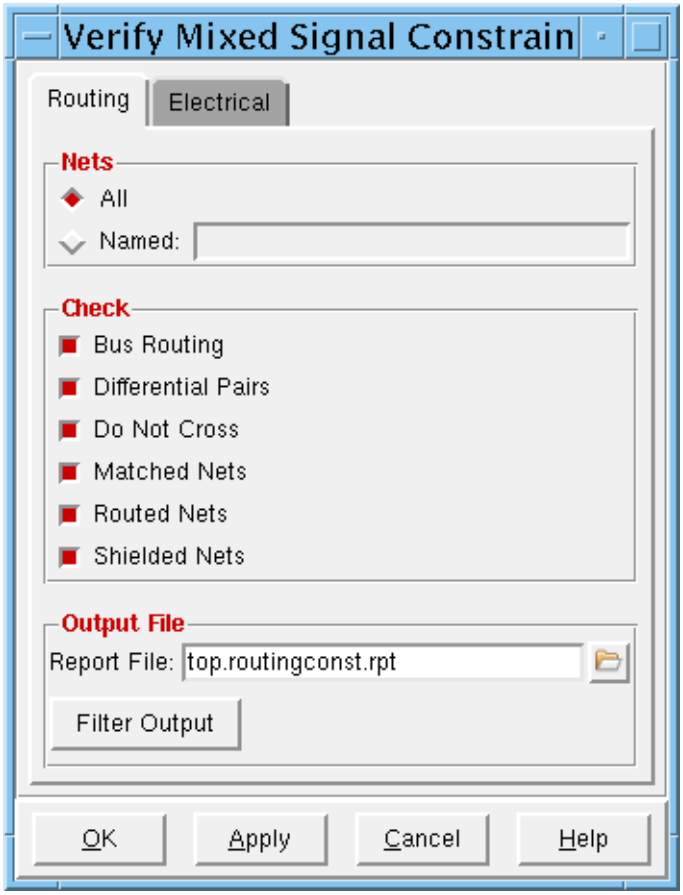
Total capacitance =
area capacitance + *side capacitance*

Minimum Cuts Constraints

Vias must not have less than the specified minimum number of cuts.

For more information on the mixed signal constraints, see Mixed Signal Router on page 1230.

➤ Choose *Verify – Verify Mixed Signal Constraints*, then click the *Routing* tab.



Verify Mixed Signal Constraints – Routing Fields and Options

Nets — Specifies the nets to check.

- *All* — Specifies all nets.
- *Named:* — Specifies named nets.

Check — Specifies the type of verification checks. Select one or more of the following options:

- *Bus Routing* — Checks constraints on bus routes, in which specified nets are routed with the same width and spacing.

Differential Pairs

Checks constraints on differential pair routing, in which the router attempts to match the parasitic load on driving pins of specified nets.

Do Not Cross

Checks that the specified noise-generating nets do not cross specified nets that are noise sensitive.

Matched Nets

Checks constraints on matching routing, in which the router attempts to create routes that are the same length. Matching routing is not limited to two nets, and the nets are not required to be topologically the same.

Routed Nets

Checks that other nets routed by the mixed signal router meet constraints on width, resistance, and capacitance.

Shielded Nets

Checks shielded routing, including regular shielding in which noise-critical nets are shielded on their right and left sides, and coaxial shielding, in which nets are shielded on the right, left, top, and bottom sides.

Constraints for shielding include the names of the nets to shield (signal nets), the names of the shielding nets (power or ground nets), the width of the shielding net, and the spacing between the shielded nets and the shielding nets.

Report File: Specifies the report file that lists the mixed-signal violations. *Default:* `designName.constraints.rpt`.

Filter Output Opens the Verify Mixed Signal Routing Constraints Filter Output form.

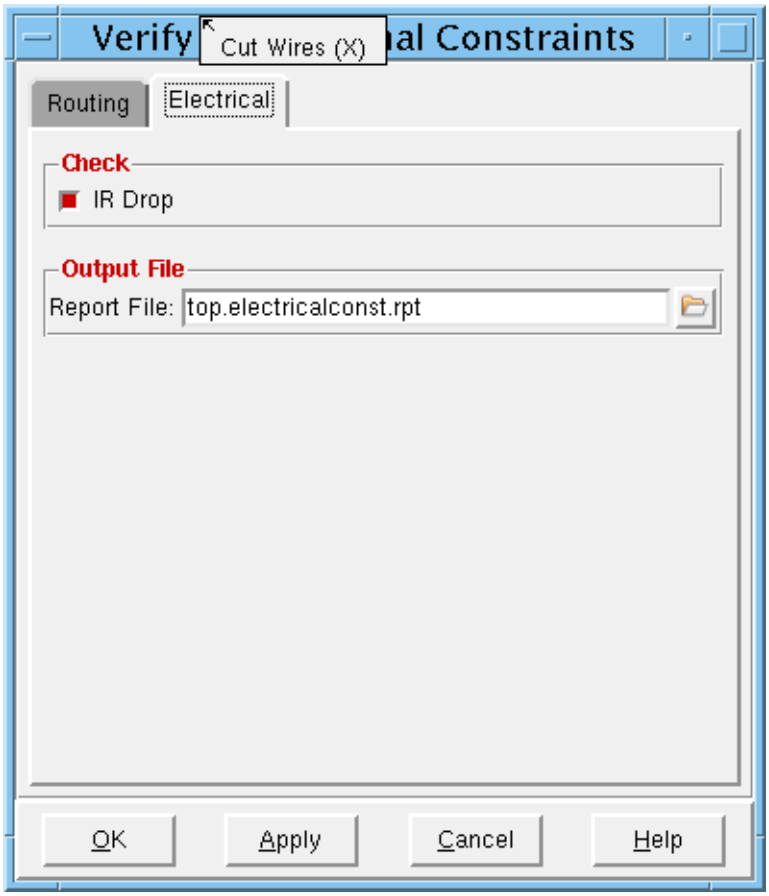
Related Text Commands

- `verifyAnalogRoutingConstraints`

Verify Mixed Signal Constraints – Electrical

Use the *Verify Mixed Signal Constraints – Electrical* page to check that noise constraints on mixed signal nets are met.

➤ Choose *Verify – Verify Mixed Signal Constraints*, then click the *Electrical* tab.



Verify Mixed Signal Constraints – Electrical Fields and Options

IR Drop

Checks for IR drop violations that are greater than the maximum specified by the mixed signal constraints.

Important

Before you check the IR drop, you must run `updatePower` to set the actual value for instance pin IR drop. Otherwise, all the IR drop values with instance pin are 0, and you will not see any IR drop violations.

Report File:

Specifies the report file that lists the mixed-signal violations. *Default:* `designName.constraints.rpt`.

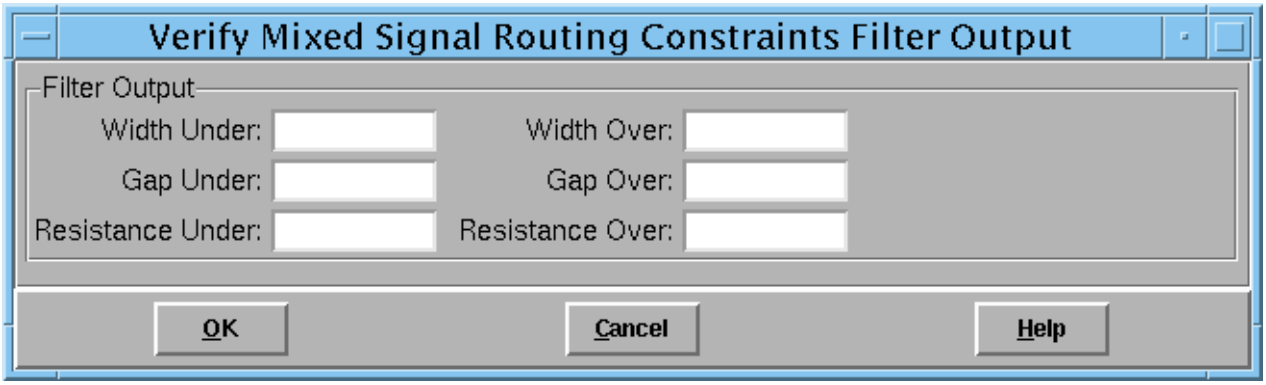
Related Text Commands

- `verifyElectricalConstraints`

Verify Mixed Signal Routing Constraints Filter Output

Use the Verify Mixed Signal Routing Constraints Filter Output form to specify limits on the violations to report.

➤ Choose *Verify – Verify Mixed Signal Constraints* and select the *Routing* tab, then click the *Filter Output* button.



Verify Mixed Signal Routing Constraints Filter Output Fields and Options

Width Under	Does not report width violations that are less than the specified value.
Width Over	Does not report width violations that are greater than the specified value.
Gap Under	Does not report spacing violations that are less than the specified value.
Gap Over	Does not report spacing violations that are greater than the specified value.
Resistance Under	Does not report resistance violations that are less than the specified value. Uses the same resistance formula the mixed signal constraint editor and router use. For more information, see *Max Res*.
Resistance Over	Does not report resistance violations that are greater than the specified value. Uses the same resistance formula the mixed signal constraint editor and router use. For more information, see *Max Res*.

15

Tools Menu

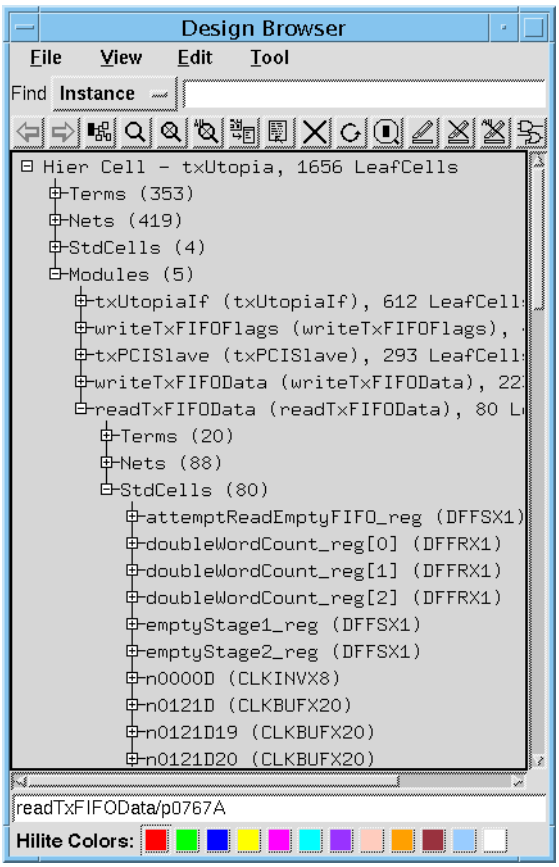
- Design Browser on page 1550
- Attribute Editor on page 1554
- Connectivity Browser on page 1556
- Schematics on page 1557
- Floorplan Toolbox on page 1567
- Flip Chip Toolbox on page 1568
- Violation Browser on page 1570
- Load Violation Report on page 1578
- Clear Violation on page 1580
- Conformal on page 1581
- Report Yield on page 1617
- Mixed Signal on page 1619
- Log Viewer on page 1666
- Screen Capture on page 1669
- Express Flow Tool on page 1673

Design Browser

Use the Design Browser to navigate through the chip's design hierarchy. You can use the Design Browser to view the design hierarchy tree at any time after the design is imported. The Design Browser also makes it easier to highlight specific modules, instances, or nets in the design display area.

You can use the widgets in the Design Browser to open forms to navigate through displays, and perform actions. From the Design Browser, you can access the Connectivity Browser to display the number of nets between instances, and the Attribute Editor to display an object's type, name, and attributes.

➤ Choose *Tools – Design Browser*, or click the *Design Browser* widget on the toolbar.



Design Browser Fields and Options

File The *File* menu provides the following options:

Load	Displays the Load Design Browser File form. Enter the filename and the format of the placement file.
Save As	Displays the Save Design Browser File form. Specify the filename. The recommended extension is `.dbf`.
Quit	Closes the Design Browser Window.
View	The View *menu* provides the following options:
Refresh	Redraws the Design Browser display.
Zoom Selected	Zooms into an object (that you have selected in the Design Browser) in the design display area.
Sort By Size	Displays instances in the order of the number of cells in the instances. Deselect the *View – Sort By Size* option to display instances sorted alphabetically by name.
Accumulate Results	Traces the hierarchical path for the selected object in the design display area.
Edit	The Edit menu provides the following option:
Delete Group/Group Member	Deletes an individual instance from a user-defined group, or to delete an entire user-defined group.
Tool	The *Tool* menu provides the following options:
Get Selected	Displays a selected object in the Design Browser
Attribute Editor	Opens the Attribute Editor. For more information, see "Attribute Editor" on page 1554.
Connectivity Browser	Opens the Connectivity Browser. For more information, see "Connectivity Browser" on page 1556.
Find	This pull-down menu lets you to view hierarchy information for a specific object. Objects highlighted in the Design Browser can be seen highlighted in the Encounter main window. You can view information on the following object types:
Instance	Entering the name of an instance in the field and pressing `Return` displays that instance and its hierarchy in the Design Browser window. You can traverse to the next hierarchy by double-clicking on the instance name. Along with the instance name, the instance's cell type and number of cells it contains are displayed.

Net	Entering the name of a net in the field and pressing `Return` displays that net and its hierarchy in the Design Browser window. Double-clicking the net name displays the net connection.
Group	Entering the name of an instance group in the field and pressing `Return` displays that instance group and its hierarchy in the Design Browser window. Before entering a group name, the group name must be specified by using either the `createInstGroup` or `addInstToInstGroup` text commands.

Design Browser Tool Widgets

You can use the widgets in the Design Browser to navigate through displays, open tools, make selections, and perform actions.

Widget	Description
	Previous—Displays viewable data in a reverse direction.
	Next—Displays viewable data in a forward direction.
	Connectivity Browser—Opens the Connectivity Browser.
	Select—Selects an object in the design display area.
	Deselect—Deselects an object in the design display area.
	Deselect All—Deselects all objects in the design display area.
	Get Selected—Gets the selected object and displays it in the Design Browser.
	Attribute Editor—Opens the Attribute Editor for the highlighted instances.
	Delete Group/Group Member—Deletes selected floorplan object instance groups.
	Refresh—Refreshes the Design Browser display.

Widget	Description
	Zoom Selected—Zooms in on a highlighted selection.
	Highlight—Highlights an object in the design display area.
	Dehighlight—Dehighlights an object in the design display area.
	Dehighlight All—Dehighlights all objects in the design display area.
	Show Schematic—Opens the Module Schematic Viewer.

Attribute Editor

Use the Attribute Editor to display an object's type, name, and attributes. The contents of the Attribute Editor form change depending on the object selected in the design.

Note: For Special Route objects, you can select layer, shape, and status from the pull-down menu.

There are several ways to open the Attribute Editor.

To open the Attribute Editor from the design display window, do the following:

- For a single object, double-left click on an object, or left click on the object to highlight it and click the *Attribute Editor* widget.
- For multiple objects, left click on the objects to highlight and click the *Attribute Editor* widget.

To open the Attribute Editor from the Violation Browser:

- Click the *Attribute Editor* button in the Violation Browser.
- Double-click a violation in the Violation Browser.

To open the Attribute Editor from the Design Browser, do the following:

1. Choose *Tools – Design Browser*, or left click the *Design Browser* widget on the Encounter toolbar.
2. In the Design Browser, highlight or left click on an object or a set of objects.
3. Click the *Attribute Editor* from the Design Browser tool widgets.

Note: The Attribute Editor displays different attributes, depending on the objects selected.

Attribute Editor Fields and Options

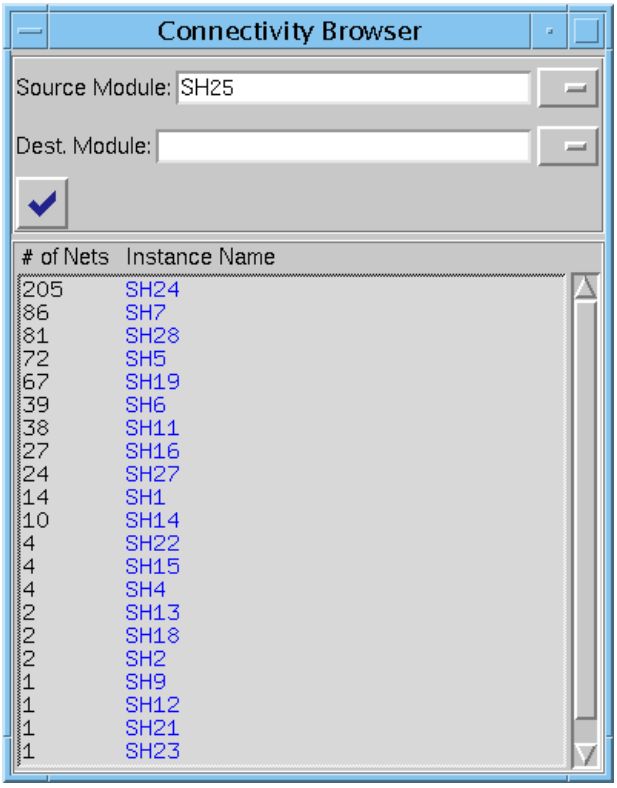
Object Type	Specifies the type of object currently selected.
Index	If you select more than one object, this will indicate the object's number in the sequence. For example, 1 of 34. Click *Next* to display the attributes of the next object in the sequence, or *Prev* to view the previous object. Use the pull-down menu to select an object.

OK	Applies your changes to the selected objects and closes the window.
Apply	Applies your changes to the object.
Apply All	Applies changes to the selected multiple objects. **Note:** When selecting objects of different types, only the objects with the same attribute selections are affected. The *Apply All* button is grayed out by default. To access this, click on the field name or type to highlight a blue row. Not all fields support the *Apply All* button, only attributes that can be changed in multiple objects, such as *Orientation*, *Location*, and *Status*.
Add Prop	Allows you to add a property name and value.
Delete Prop	Allows you to delete a property name and value.
Close	Closes the Attribute Editor window.

Connectivity Browser

Use the Connectivity Browser to display connections from a source module to a destination module, including module guides, blocks, I/O blocks, and standard cells.

1. Choose *Tools – Design Browser*, or click the *Design Browser* widget on the toolbar.
2. Highlight a module in the Design Browser and click the *Connectivity Browser* widget.



Connectivity Browser Fields and Options

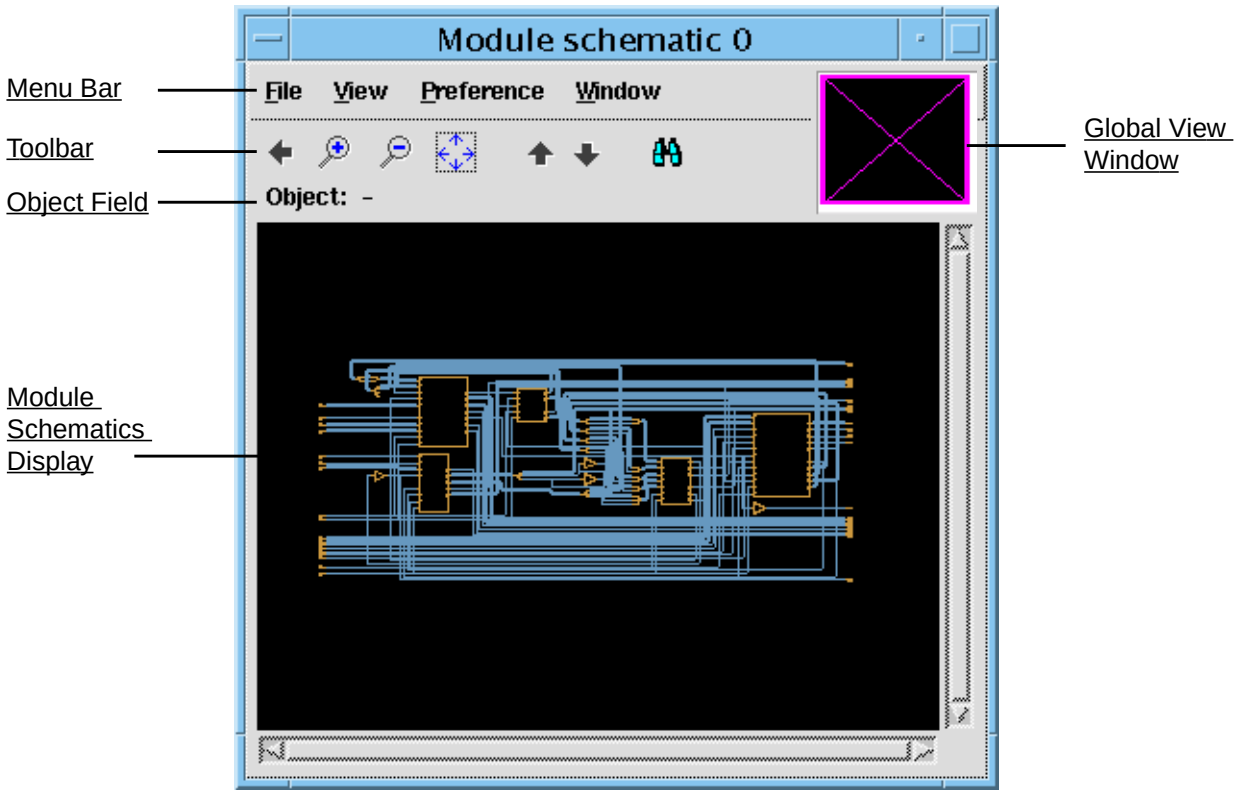
Source Module Instance	Specify the name of the instance
Destination Module	Use this pull-down menu to select the destination module.
Check	Displays the connection information.

Schematics

Use the Encounter Module Schematic Viewer with the Design Browser to explore the hierarchical design's connectivity, the relationship of modules and instances, and design changes, such as CTS, OPT, and ECO. It also allows you to do cross-probing from this Schematic Viewer to the Encounter Layout view to help give you flexibility and immediate feedback to debug and diagnose your design.

You can open the Module Schematic Viewer in the following ways:

- From the Main Encounter window, choose *Tools – Schematics*.
- From the Design Browser, select a module and click the Show Schematics icon.
- From the Timing Debug environment (*Tools – Debug Timing*), do one of the following:
  - Double-click to select one of the paths on the timing critical path list to open the Timing Analyzer form and select the Schematic tab to change the view to schematic.
  - Select one of path on the timing critical path list and click the *Schematic* icon at upper right corner of the path list.



Menu Bar

- File Menu on page 1558
- View Menu on page 1558
- Preference Menu on page 1559
- Window Menu on page 1559

File Menu

Options	Description
Print	Opens the Print Schematic form where you can choose printer options.

View Menu

Options	Description
Port Name	Displays instance/block port names.
Pin Name	Displays I/O pin names.
Instance Name	Displays instance names.
Net Name	Displays net names.
Primitive Instance Type Name	Displays primitive instance type names.
Highlight Cursor Object	Highlights objects as you pass the cursor over them.
Zoom In	Displays the schematic in greater detail. Each selection zooms in one level.
Zoom Out	Displays more contents of the schematic. Each selection zooms out one level.
Zoom to Full Window	Displays the entire schematic within the display area.
Pan – Left/Right/Up/Down	Displays a view to the left of, right of, above, or below the current schematic view.
Complete View	Returns to the original full schematic view.

Options	Description
Change Color	Opens the Color Selection form where you can change the color of the selected object.
Next Color	Changes the selected object's color to the next available color.
Display Information Box	With the cursor over an object, this displays an information box that identifies the object by name and lists pertinent details about the object.

Preference Menu

Options	Description
Color Settings	Opens the Color Settings form so you can change default color and style settings for the schematic objects.
Font Settings	Opens the Font Settings form so you can change default font size and style settings for the schematic display.

Window Menu

The *Windows* menu lists all of the active Schematic viewer windows for your Encounter session. Click on a window name to bring it to the front of your screen.

Choose *Cascade Window* to refresh your desktop and display the main Encounter window on top with all other open windows in a cascading view to the left of the main window.

Toolbar

Toolbars provide a quick way to access the most commonly used commands. This section describes the toolbar items, which are available for flattened and module schematics, except where noted.

Icon	Action	Description
	Last View	Click this widget to toggle the display between the previous location or zoom level and the current location or zoom level.

Icon	Action	Description
	Zoom In	Click this widget to display a smaller area of the schematic in greater detail. Each click zooms in one level. The equivalent bindkey is `Z` (`Shift-Z`).
	Zoom Out	Click this widget to display a larger area of the schematic in less detail. Each click zooms out one level. The equivalent bindkey is `z`.
	Zoom to Full	Click this widget to display the entire schematic within the display area. The equivalent bindkey is `f`.
	Push View Up	Displays the parent level hierarchy. To push the view up to a higher-level schematic, select an instance in the Module Schematics window and click this icon.
	Push View Down	Displays the lower level hierarchy. To push the view down to a lower-level schematic, select an instance in the Module Schematics window and click this icon.
	Find	Click this widget to open the Find Schematic Object form to specify an object to highlight in the display area.

Object Field

The *Object* field is located under the toolbar. When you scroll over an object, this field displays the object type, name, and ID number.

Global View Window

The global view window identifies the location of the current view in the schematic display area, relative to the entire area. The global view is identified by the pink crossbox. When you display an entire schematic in the area, the crossbox encompasses the global view window. When you zoom and pan through the schematic in the display area, the crossbox identifies where you are relative to the entire schematic.

- To define a new global view, left-click and drag the mouse to create a new crossbox in the global view window.
- To pan left, right, up, or down in the schematic display, right-click and drag the crossbox in the global view window.

  Note: You can also pan in the schematic display area by right-clicking and holding the `Shift` key in the area, and dragging the mouse left, right, up, or down.

Module Schematics Display

The schematic display area constitutes the major portion of this window. To change the default display properties for objects, use the Color Selection and Color Settings forms.

Pop-Up Menu

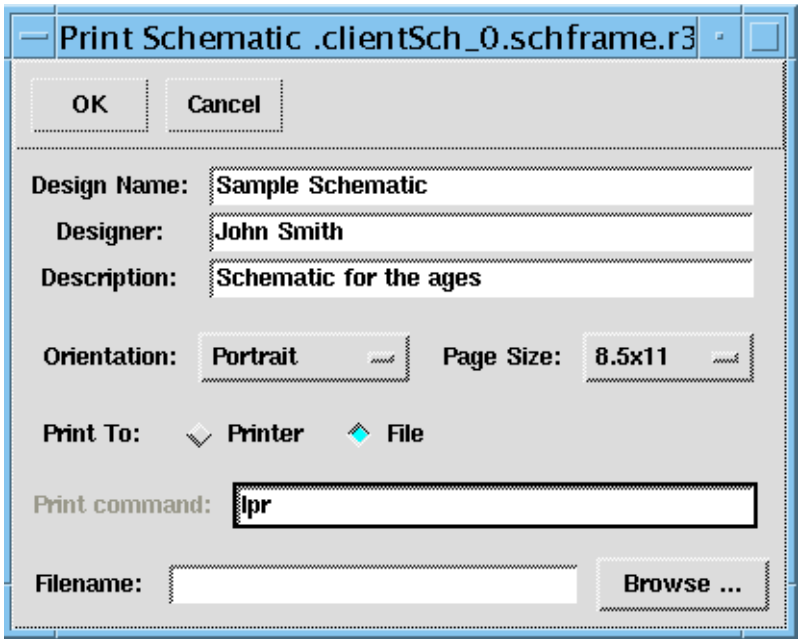
To access the pop-up menu, right-click over an object in the Module Schematics window. To select an option, scroll down and highlight the option. The following table describes the options that are available for the Module Schematics pop-up menu.

Options	Description
Fan-in Cone (For Critical Path View Only)	Manipulates schematic views of fan-ins. Select an instance or block port to run these commands. This submenu has the following options: ■ *Open*—Opens the fan-in cone of an object. ■ *Close*—Closes a fan-in cone.
Fan-out Cone (For Critical Path View Only)	Manipulates schematic views of fanouts. Select an instance or block port to run these commands. This submenu has the following options: ■ *Open*—Opens the fanout of an object. ■ *Close*—Closes a fanout cone.
Open Next Level Instance View	Display next-level views for instances. Click on an instance to select it and right-click on this option.
Close Next Level Instance View	Closes a next-level instance views. Click on an instance to select it and right-click on this option.
Trace Driver	Traces all of the possible drivers of a selected instance or signal and highlight the corresponding instances. The highlight color for drivers is yellow.
Trace Load	Traces all of the possible loads of a selected instance or signal and highlight the corresponding instances. The highlight color for loads is red.
Trace Connectivity	Traces all of the possible drivers and loads of a selected instance or signal and highlights connectivity from an object's driver to its load. The highlight colors for drivers and loads are yellow and red.

Print Schematic

Use the Print Display Area form to print the schematic in the display area.

➤ Choose *File - Print*.



Print Schematic Fields and Options

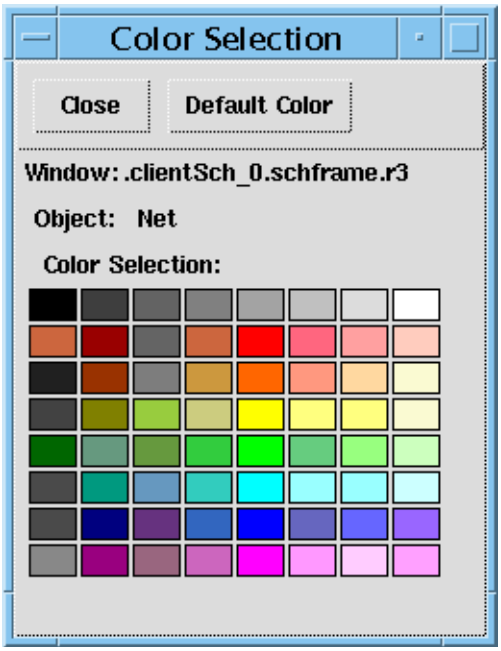
Design Name	Specifies the name of the design. This information appears in the bottom left corner of the printout.
Designer	Specifies the designer name. This information appears in the bottom left corner of the printout.
Description	Specifies a description. This information appears in the bottom left corner of the printout.
Orientation	Specifies the page orientation. Choose *Portrait* or *Landscape*.
Page Size	Specifies the page size. Choose a standard page size of *8.5X11* or use the pull-down menu to specify a custom size.

Print To	Specifies the print output destination. If you choose *Printer*, type a print command in the appropriate field. If you choose *File*, type a filename in the appropriate field or use the *Browse* button to locate the appropriate file through the Print File window.

Color Selection

Use the Color Selection form to change the color of an object in the schematic viewer.

➤ Click an object to select it, and choose *View - Change Color*.



Color Selection Fields and Options

Window	Identifies which schematic window was active when you selected this option.
Object	Displays the name of the selected object that will change color.
Color Selection	Displays the color palette. Click a color to apply a new color to an object.

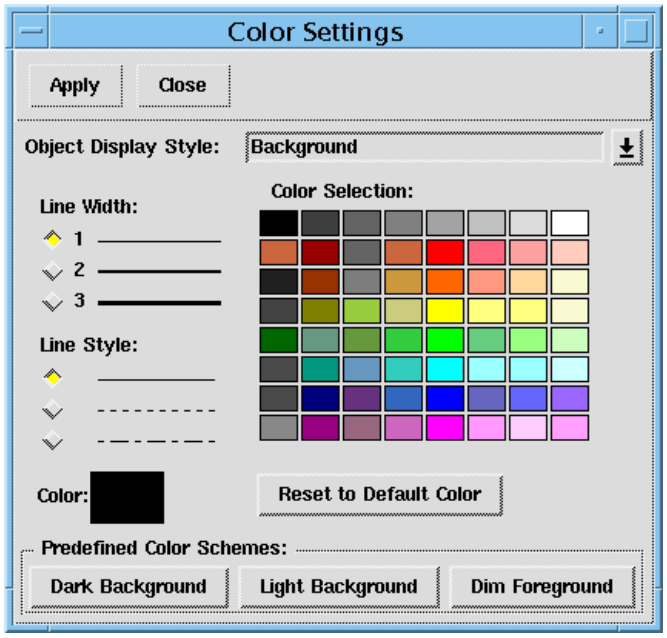
Changing an Object's Color to the Next Color on the Palette

To apply the next available color on the palette, you do not have to re-select the object. Instead, choose *View - Next Color*. You can do this repeatedly.

Color Settings

Use the Color Settings form to change default color settings.

➤ Choose *Preferences – Color Settings*.



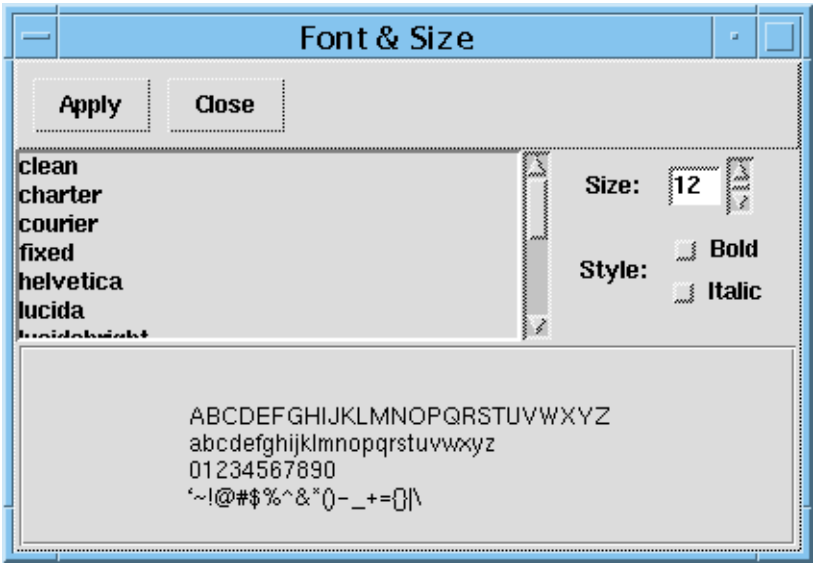
Color Settings Fields and Options

Object Display Style	Click the pull-down menu to select an object type.
Line Width	Specifies the line width.
Line Style	Specifies the line style.
Color Selection	Displays the color palette. Click a color to apply a new color to an object. The color appears in the *Color* field.
Reset to Default Color	The object type reverts to the default color.
Predefined Color Schemes	Specifies the schematics display area color. The default is *Dark Background*.

Font Settings

Use the Font Settings form to change default font size and style settings for the schematic display.

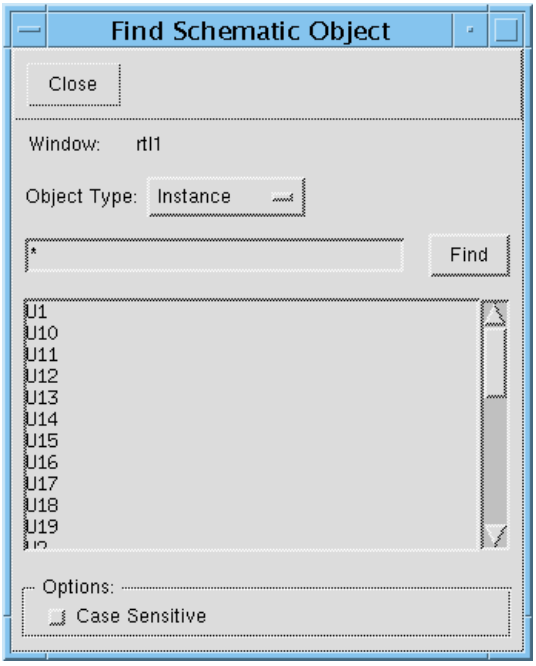
➤ Choose *Preferences – Font Settings*.



Find Schematic Object

Use the Find Schematic Object form to find and highlight a specified object in the schematic display area.

➤ Click the *Find* icon.

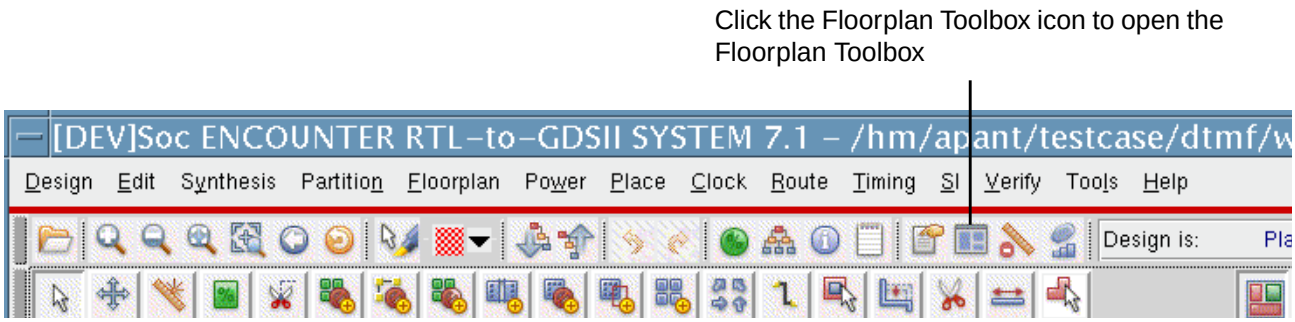


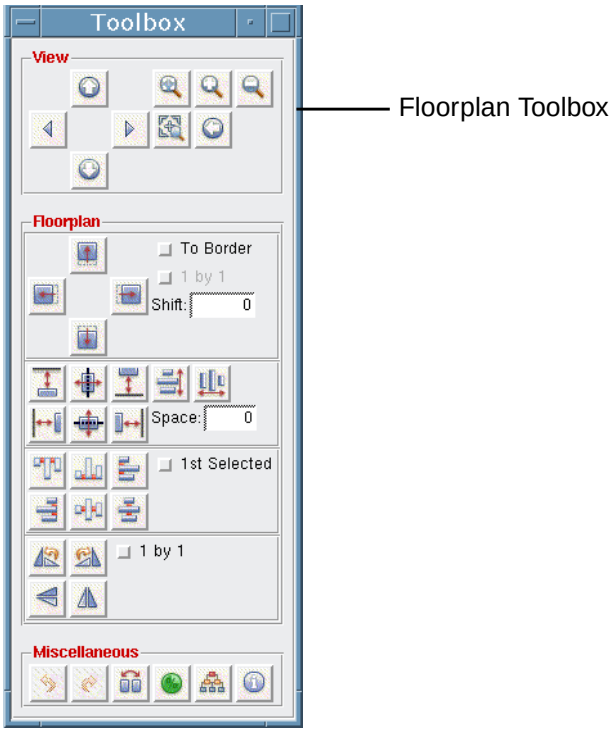
Find Schematic Object Fields and Options

Window	Identifies which schematic window was active when you selected this option.
Object Type	Use the pull-down menu to select an object type.
Name Field (below *Object Type*)	Click in the name field and type the name of the gate, or a portion of the name with wildcard characters. Clicking *Find* will display the results in the list box below this field. Double-click a gate name to highlight the object in the schematic display area.
Case Sensitive	Specifies that the search is case sensitive.

Floorplan Toolbox

The Floorplan Toolbox provides access to the commonly used features during floorplanning. To open the Floorplan Toolbox, click on the Floorplan Toolbox icon in the main window.





You can use the Floorplan toolbar to:

- Use display-related commands such as zoom, fit, and pan.
- Access the floorplanning interactive commands such as shift, align, space, rotate, and flip objects.
- Perform other functions such as swap selected objects, display/calculate effective query utilization, and so on

Flip Chip Toolbox

Use the Flip Chip Toolbox menu to perform all flip chip design flow tasks. The Flip Chip Toolbox menu contains the most commonly used forms in the flip chip design flow.

➤ To open the Flip Chip Toolbox form, choose *Tools – Flip Chip Toolbox*.

The Flip Chip Toolbox contains the following items:

- Create Bump Array

  Opens the Create Bump Array form. Use the Create Bump Array form to specify bump array parameters.

- Create Row

  Opens the Create Core Rows form. Use the Create Core Rows form to create rows for the specified site, both inside and outside the core area, but within the die.

- Create Area I/O Row

  Opens the Create Area IO Rows form. Use the Create AreaIO Rows form to specify I/O driver row parameters.

- Assign Signals

  Opens the Assign Signals form. Use the Assign Signals form to assign and unassign signals to tile pins or bumps.

- Assign Power/Ground

  Opens the Assign Power/Ground Bumps form. Use the Assign Power/Ground Bumps form to assign power and ground nets to bumps and tiles.

- Unassign Bump

  Use the Unassign Bump menu item to unassign bumps and tiles.

➢ To use the Unassign Bump menu item, select the bump or tile pin to be unassigned, then choose *Tools – Flip Chip Toolbox – Unassign Bump*. There is no form for this menu item.

- Swap Signals

  Use the Swap Signals menu item to swap signals between two bumps. Either one or both of these bumps must be assigned.

➢ To use the Swap Signals menu item, select the signals to be swapped, then choose *Tools – Flip Chip Toolbox – Swap Signals*. There is no form for this menu item.

- Place Flip Chip I/O

  Opens the Place Flip Chip I/O form. Use the Place Flip Chip I/O form to place area and peripheral I/O cells.

- Route Flip Chip

  Opens the Flip Chip Route form that contains the following two pages:

  - Flip Chip Route – Basic

    Use the Flip Chip Route – Basic form to create special route wires to power bumps.

  - Flip Chip Route – Advanced

    Use the Flip Chip Route – Advanced form to create regular route wires to signal bumps.

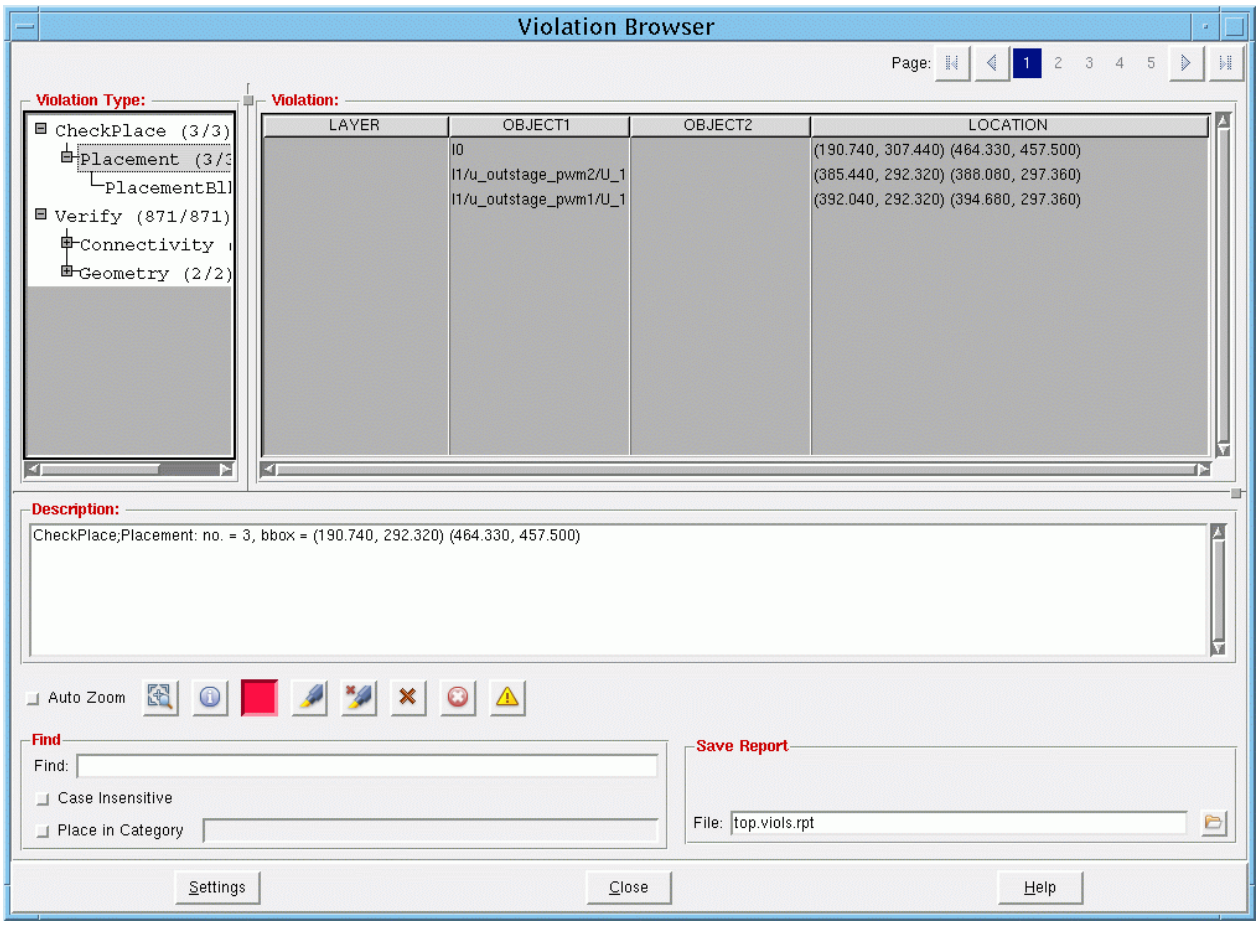
Violation Browser

Use the Violation Browser to display violations and lithography hotspots, mark violation markers as false or true, delete violation markers, and specify a report file.

The *Settings* button on the Violation Browser provides access to the following form:

- Violation Browser Settings on page 1574

➤ Choose *Tools – Violation Browser*.



Violation Browser Fields and Options

Violation Type

Lists the violation types in a hierarchy window.

To show or hide a violation, select it in the *Violation* or *Violation Type* window and click the right mouse button. Select *Show* or *Hide* from the pop-up window.

The numbers in parentheses after each violation type represent the number of violations of that type displayed in the main Encounter window and the total number of violations of that type. The count includes true and false violations.

For example, if *Verify – Connectivity – Open (479/503)* means that there are 503 Open violations and 479 of those violations are shown the main Encounter window.

Violation

For the highlighted *Violation Type*, displays the names of the objects with violation markers and their locations.

Description

Displays the layer and bounding box for the violation.

Note: Layer is not included for placement violations.

You can select text in the *Description* text box and copy and paste it to another window. You cannot edit text in the *Description* text box.

Auto Zoom

Automatically zooms in the selected violations as you browse through the violations.

Fit Violation—Displays the violation within the design display area.

Attribute Editor—Opens the *Attribute Editor* and populates it with the highlighted violations. Double click on a violation to update fields in the Attribute Editor. For more information, see "Attribute Editor" on page 1554.

Highlight Color—Select this button to specify the color to highlight a violation.

Highlight Violations—Highlights the selected violation in the design display area. To highlight the violation, select the highlight color from the color palette, and then click the *Highlight* button.

	De-Highlight Violations—Removes the highlight from the selected violation in the design display area.
	Delete Violations—Deletes all selected violations from the design database. Markers are also removed from the design display area and the list of violations.
	Mark Violations as False—Marks the selected violation as a false violation. These violations are stored in the database as false violations. You must select the *False Violations* option in the *Violation Types* panel to view the violations that you mark as false.
	Mark Violations as True—Marks the selected violation as a true violation.
Find	Searches for the specified text and highlights it in the *Violation* window. This field recognizes pattern matching, so you can type `*153*` to search for all objects with the string 153 as part of their *LOCATION*. Press *Enter* to find the specified text.
Case Insensitive	Specifies whether the text in the *Find* text entry box is case sensitive.
Place in Category	Creates a category in the *Violation Type* window and adds the highlighted object to the category. Categories are not saved.
Save Report File	Specifies the report file that contains all the violation information. The browser and the report file list the violations in the same order.

Related Text Commands

- `checkPlace`
- `createMarker`
- `violationBrowser`
- `violationBrowserReport`

Related Topics

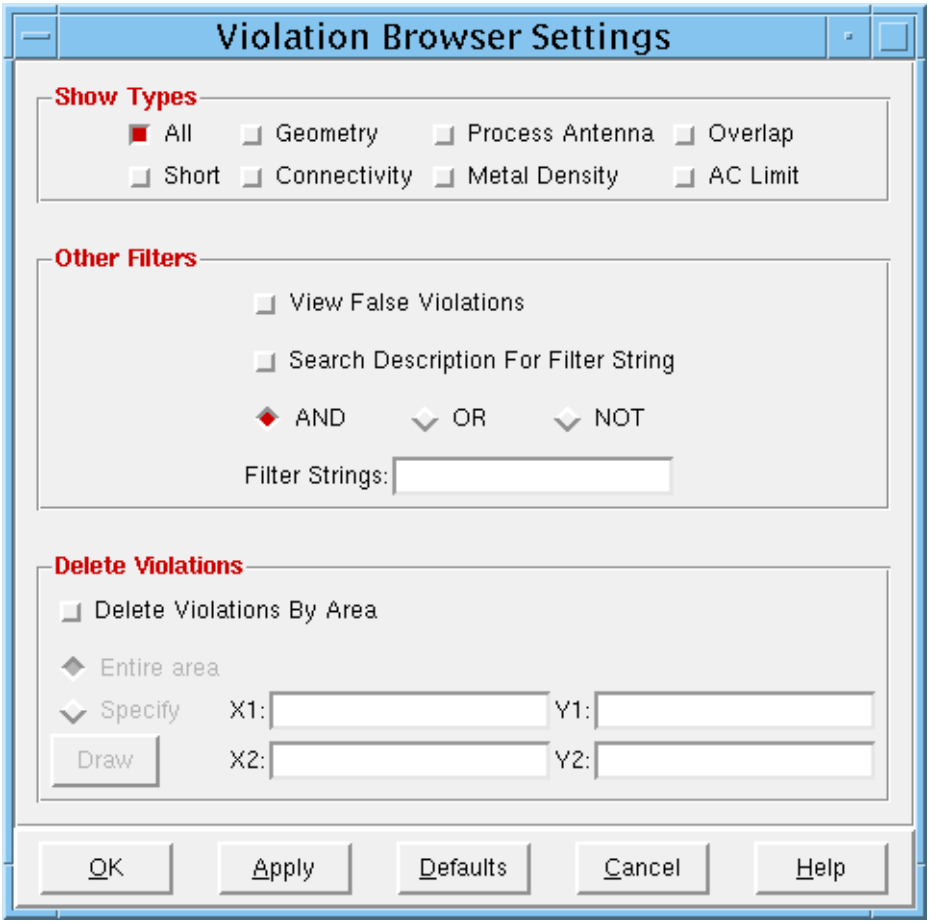
For information on the following topic, see “Verifying Violations” in the *Encounter User Guide*:

- Viewing Violations With the Violation Browser

Violation Browser Settings

Use the Violations Browser Settings form to specify the settings for displaying violations and lithography hotspots.

➤ Choose *Tools – Violation Browser* and click the *Settings* button.



Violation Browser – Settings Fields and Options

Show Types

Lists the types of violations to display or hide in the Violation Browser. Select one or more of the following options:

All	Displays all violations.
Geometry	Displays geometry violations.
Process Antenna	Displays process antenna violations.
Overlap	Displays overlap violations.
Short	Displays short violations.
Connectivity	Displays connectivity violations.
Metal Density	Displays metal density violations.
AC Limit	Displays AC limit violations.

Show Area

Displays violations in the entire area or a specified portion of the area. Specify the portion of the area by using one of the following methods:

- Using the *Draw* button and your mouse to create a rectangular area in the design. The software displays the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields.
- Manually enter the coordinates in the *X1*, *Y1*, *X2*, and *Y2* fields.

Other Filters

Specify additional conditions by selecting one or more of the following options:

View False Violations

Displays violations that you have marked as false.

Search Description For Filter String

Searches for text in the violation message (in the bottom portion of the Violation Browser window) and the violation description (in the top portion of the Violation Browser window).

AND OR NOT

- The *AND* and *OR* conditions work on single strings or multiple strings.
- The *NOT* condition works only on a single string.

Filter Strings

Specifies a text string in the violation message (in the bottom portion of the Violation Browser). When you specify a text string, the Violation Browser searches the message of each violation and displays only the violations whose messages match the search conditions.

To specify a list of strings, separate each string with a space.

To specify a literal string with space in it, enclose the string in double quotation marks. For example, you can specify strings such as the following:

- `M5`
- `(600, 500)`
- `M3 (700, 400)`
- `"Pin of Net"`

Delete Violations Enables you to delete all violations or delete violations in the specified area only.

Delete Violations By Area

Enables you to delete violations in the area you specify on this form or the area you select with the mouse.

Entire area Deletes the types of violations specified in the entire core design area.

Specify Specifies an area from which to delete violations. Only the types of violations specified by this form are deleted.

Draw ... Lets you use the mouse to outline an area from which to delete violations.

Related Text Commands

- `createMarker`
- `violationBrowser`
- `violationBrowserReport`

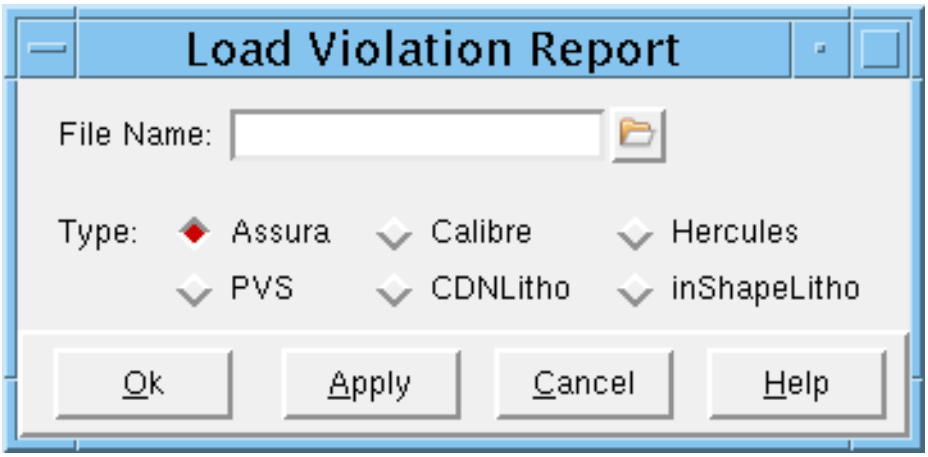
Related Topics

- Viewing Violations With the Violation Browser

Load Violation Report

Use the Load Violation Report form to load a violation marker file or a hotspot interface format (HIF) file and create markers that the Encounter software can interpret. After you load the file, you can view the markers in the Violation Browser. The Encounter Auto Query feature displays the rule names for the markers.

➤ Choose *Tools – Load Violation Report*.



Load Violation Report Fields and Options

File Name

Specifies the marker file to load.

Type

Specifies the type of marker file.

The following file types contain violation markers:

- *Assura*
- *Calibre*
- *PVS*
- *Hercules*

The following types contain hotspot markers, which are used to identify areas susceptible to lithography problems:

- *CDNLitho*
- *inShapeLitho*

Related Text Commands

- `loadViolationReport`

Related Topics

- Viewing Violations With the Violation Browser

Clear Violation

Use the *Tools – Clear Violation* menu command to clear all the violation markers in your design.

➤ Choose *Tools – Clear Violation*.

There is no GUI form for this command.

Related Text Commands

There are no related text commands. This feature is available only through the Encounter *Tools* menu.

Conformal

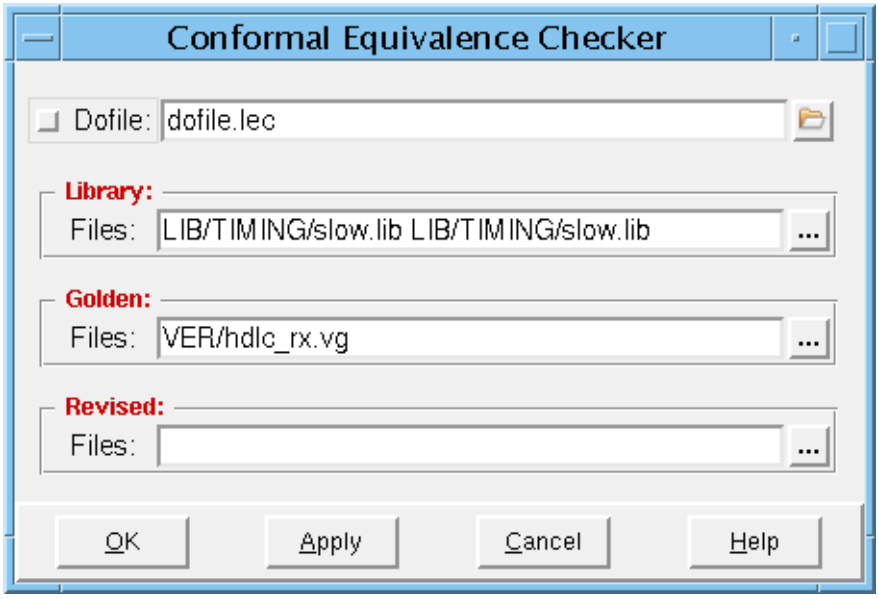
The *Conformal* submenu provides access to the following features:

- Conformal Equivalence Checker on page 1582
- Conformal Check Constraints on page 1583
- Conformal Check Budget Constraints on page 1588
- Conformal Check Assembled Constraints on page 1597
- Conformal Derive Critical False Path on page 1604
- Conformal Promote Constraints on page 1611

Conformal Equivalence Checker

Use the Conformal Equivalence Checker form to perform equivalency checking.

➤ Choose *Tools – Conformal – Verify Design Equivalence*.



Conformal Equivalence Checker Form Fields and Options

Dofile	Specifies the name of the dofile to create. You can enter the name of the dofile or click the *Browser* icon select a dofile from the Open Dofile browser window. Will use the file specified in this field. Will generate the dofile using the default name.
Library	Specifies the full path of the library file. You can enter the path or click … to open the Library Files window to select a file.
Golden	Specifies the full path of the Golden design file. You can enter the path or click … to open the Golden Files window to select a file.
Revised	Specifies the full path of the Revised design file. You can enter the path or click … to open the Revised Files window to select a file.

Conformal Check Constraints

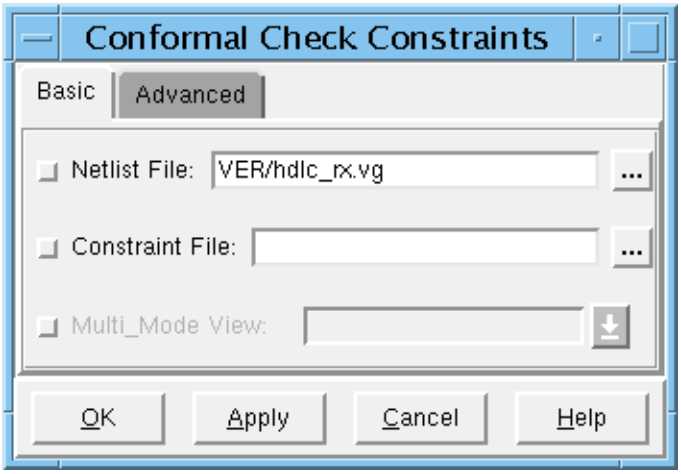
The Conformal Check Constraints form contains the following pages:

- Conformal Check Constraints - Basic on page 1584
- Conformal Check Constraints - Advanced on page 1586

Conformal Check Constraints - Basic

Use the *Basic* page of the Conformal Check Constraints form to check the quality of constraints for the current design using the Conformal Constraint Designer software. This performs checks for exceptions, clocks, unconstrained ports and invalid SDC command syntax.

➤ Choose *Tools – Conformal – Check Constraints*, then click the *Basic* tab.



Conformal Check Constraints – Basic Fields and Options

Netlist File	Specifies the name of the netlist file. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Netlist Files browser window.
Constraint File	Specifies the constraint file(s) to analyze using Conformal Constraint Designer. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Constraint Files browser window.

Multi_Mode View

Specifies the multi-mode view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option.

Note: Multi-mode constraints and views must already be specified.

If you do not specify a constraint file, the current design SDC file is passed to the Conformal software for analysis

Related Text Command

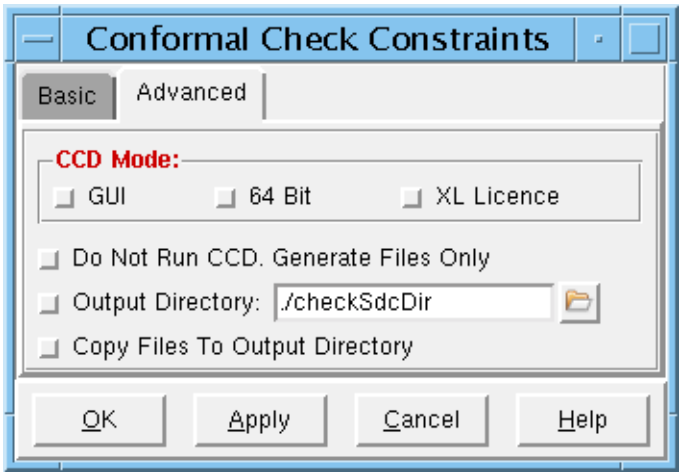
For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `checkSdcCCD`

Conformal Check Constraints - Advanced

Use the *Advanced* page of the Conformal Check Constraints form to specify additional constraint checking options.

➤ Choose *Tools – Conformal – Check Constraints*, then click the *Advanced* tab.



Conformal Check Constraints – Advanced Fields and Options

GUI

Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Encounter session—you can continue to run additional Encounter commands while the CCD GUI mode session is running in parallel.

The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script.

Conformal log messages are not echoed to the Encounter log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option).

Default: Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Encounter command is executed until the CCD script has completed.

64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Encounter software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license
Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click the *Browser* icon select a directory from the Output Directory browser window. *Default*: `./checkSdcDir`
Copy Files to Output Directory	Copies all design files present in the Conformal script to the Conformal run directory. You can use the *Output Directory* option to specify the run directory.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `checkSdcCCD`

Conformal Check Budget Constraints

Use the Conformal Check Constraints form to check the time budget directory's top and block constraints against their pre-partitioned original chip SDCs. Conformal Constraint Designer performs checks for hierarchical constraint mismatches, exceptions, clocks, unconstrained ports, and invalid SDC command syntax.

For more information on SDC checks that the Conformal Constraint Designer software uses to verify SDC data, see the "SDC Rule Checks" chapter of the *Encounter Conformal Constraint Designer Reference Manual*.

You can use this form after running the `savePartition` command.

To use this feature, specify the path to the Conformal Constraint Designer installation before running Encounter.

Note: You must have previously run `deriveTimingBudget -ccd` to generate time budget CCD dofiles and CCD clock map files. These dofile scripts are automatically detected by this form in the *Partition Directory*.

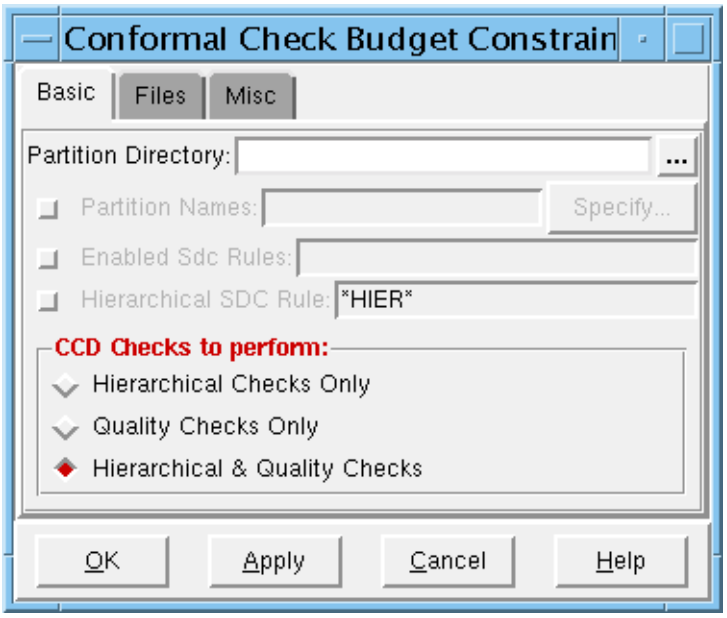
The Conformal Check Constraints form contains the following pages:

- Conformal Check Budget Constraints - Basic on page 1589
- Conformal Check Budget Constraints - Files on page 1591
- Conformal Check Budget Constraints - Misc on page 1593

Conformal Check Budget Constraints - Basic

Use the *Basic* page of the Conformal Check Constraints form to specify most common settings.

➤ Choose *Tools – Conformal – Check Budget Constraints*, then click the *Basic* tab.



Conformal Check Budget Constraints – Basic Fields and Options

Partition Directory	Specifies the budget or partition directory. Time budget constraints and clockmap files are automatically detected by the `checkBudgetSdcCCD` command in the specified partition directory. You can enter the name or click *…* to select a directory.
Partition Names	Specifies the partition names whose constraints should be checked against the original pre-partition chip SDCs. You can enter the name or click the *Specify* button to select a partition name. *Default*: All top and block level partitions under the user-specified partition directory are checked by the CCD software against their original pre-partition chip constraints.

Enabled SDC Rules	Allows specification of user-enabled or disabled rules in CCD to be used during quality rule checking of partition constraints. You can define multiple added and deleted disabled rules. *Default*: A default set of rules are defined on script initialization. The user-enabled rules are added after this default set of rules.
Hierarchical SDC Rule	Specifies the rules to be checked during hierarchical rule checking. *Default*: `*HIER*`
Hierarchical Checks Only	Specifies that only hierarchical rule checking be performed by the CCD software.
Quality Checks Only	Specifies that only quality rule checking for each partition be performed by the CCD software.
Hierarchical & Quality Checks	Specifies that both hierarchical and quality rule checking be performed by the CCD software.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

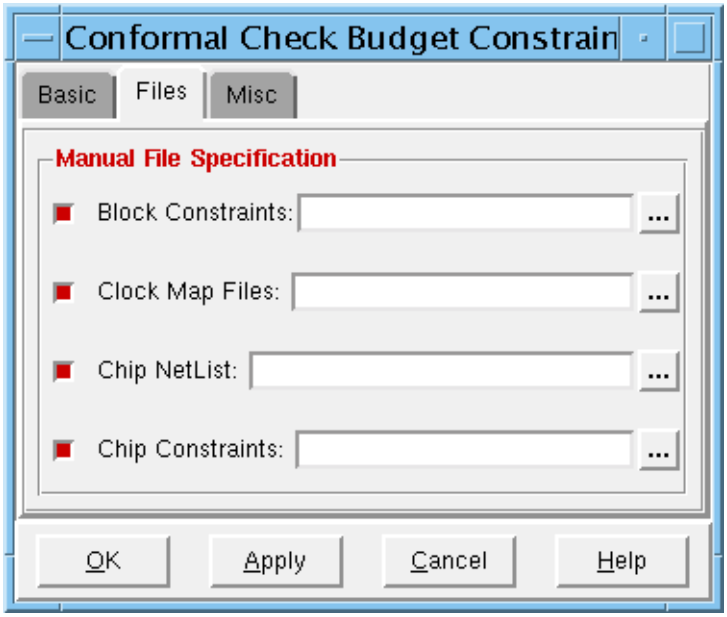
- `checkBudgetSdcCCD`

Conformal Check Budget Constraints - Files

Use the *Files* page of the Conformal Check Constraints form to specify constraint, mapping, and netlist files manually. You can use this page after saving the partition information to the current or specified directory

Note: You must have previously run `deriveTimingBudget -ccd` to generate time budget CCD dofiles. These dofile scripts are automatically detected by this form in the *Partition Directory*.

➤ Choose *Tools – Conformal – Check Budget Constraints*, then click the *Files* tab.



Conformal Check Budget Constraints – Files Fields and Options

Block Constraints

Allows manual specification of the budgeted constraints files to be used during Conformal Constraint Designer analysis. You can enter the name or click … to select a file or files.

Default: Constraints are automatically detected in the partition directory.

Clock Map Files	Allows manual specification of the clock map file(s) that contain hierarchically equivalent clocks. This option is useful for overriding clock map files. You can enter the name or click *…* to select a file or files. *Default*: The netlist is automatically detected from the Encounter database. In most cases, the clock map file(s) are automatically detected from the Encounter database and passed to CCD without having to use this option.
Chip Netlist	Allows manual specification of the original chip netlist file(s) to analyze using CCD. This option is useful for overriding chip netlist settings You can enter the name or click *…* to select a file or files. *Default*: The netlist is automatically detected from the Encounter database.
Chip Constraints	Allows manual specification of the original chip constraints file(s) to analyze using CCD. This option is useful for overriding chip constraints. You can enter the name or click *…* to select a file or files. *Default:* Constraints are automatically detected from the Encounter database.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

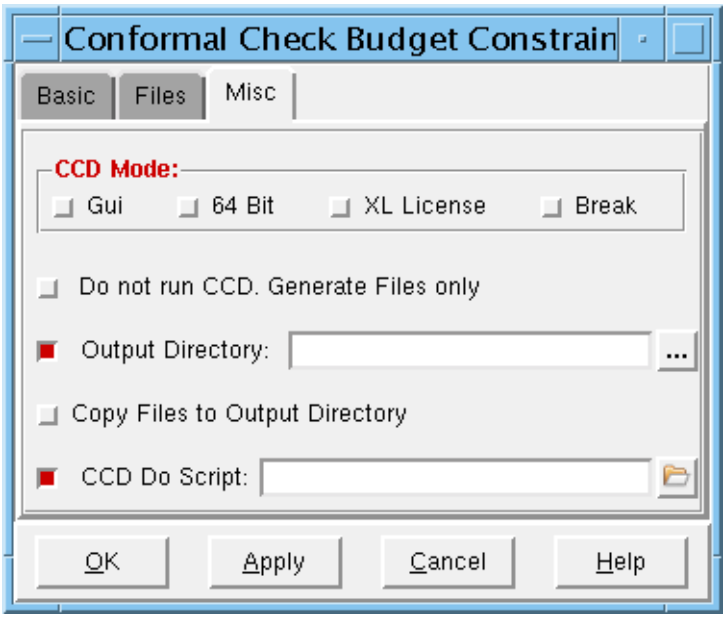
- `checkBudgetSdcCCD`

Conformal Check Budget Constraints - Misc

Use the *Misc* page of the Conformal Check Constraints form to specify additional options for checking the time budget directory's top and block constraints against their pre-partitioned original chip SDCs. You can use this page after saving the partition information to the current or specified directory.

Note: You must have previously run `deriveTimingBudget -ccd` to generate time budget CCD dofiles. These dofile scripts are automatically detected by this form in the *Partition Directory*.

➤ Choose *Tools – Conformal – Check Budget Constraints*, then click the *Misc* tab.



Conformal Check Budget Constraints – Misc Fields and Options

Gui

Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Encounter session—you can continue to run additional Encounter commands while the CCD GUI mode session is running in parallel.

The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script.

Conformal log messages are not echoed to the Encounter log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option).

Default: Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Encounter command is executed until the CCD script has completed.

64 Bit

Specifies 64-bit CCD.

Default: 32-bit CCD, or 64-bit if the Encounter software starts in 64-bit mode.

XL License

Runs the Conformal Constraint Designer software with the XL license.

Default: CCD L license

Break

Specifies that the generated dofile should contain a “break” command after checking each partition constraints file. This is useful for interactive debug of partition constraints using the SDC Rule Manager. After browsing quality checks in the SDC Rule Manager, type `continue` to proceed on the CCD command line.

The CCD software will then proceed to check the next partition and then break again, until finally all partition constraints have been checked.

Note: This option is only available with the *Gui* option.

Default: CCD will not perform any breaks. Interactive debug of partition constraint’s quality checks using the SDC Rule Manager will not be possible. The SDC Rule Manager will only display hierarchical rule check results.

Quality checks can be examined instead in the individual partition reports in the following file:

```
checkBudgetSdcDir/
rule_check.quality.<partitionName>.rpt
```

Do Not Run CCD. Generate Files Only

Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.

Output Directory

Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click *…* to select a directory.

Default: `./checkBudgetSdcDir`

Copy Files to Output Directory

Copies all design files present in the Conformal script to the Conformal run directory. You can use the *Output Directory* field to specify the run directory.

CCD Do Script

Specifies an existing dofile script that should be passed to the CCD software for execution. You can enter the name or click the *Browser* icon select a file.

Default: A new dofile script is generated based on user specified `checkBudgetSdcCCD` options and used to run the CCD software.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `checkBudgetSdcCCD`

Conformal Check Assembled Constraints

The Conformal Check Assembled Constraints form contains the following pages:

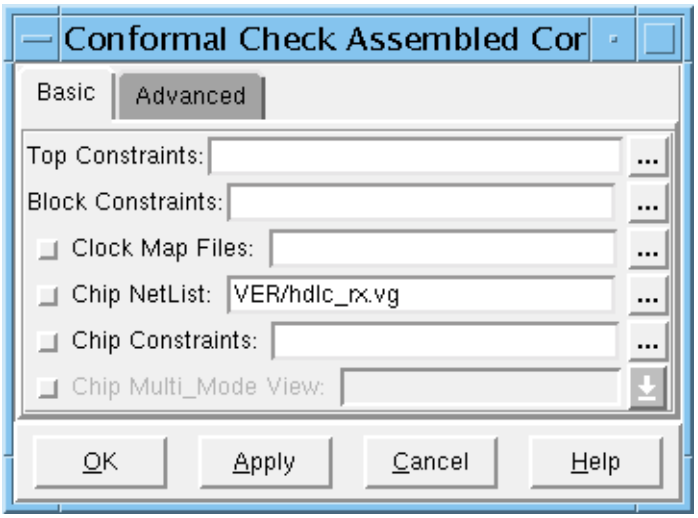
- Conformal Check Assembled Constraints - Basic on page 1598
- Conformal Check Assembled Constraints - Advanced on page 1601

Conformal Check Assembled Constraints - Basic

Use the *Basic* page of the Conformal Assembled Check Constraints form to check pre-assembled design top and block constraints against post-assembled design chip constraints. The Conformal Constraint Designer performs checks for hierarchical constraint mismatches, exceptions, clocks, unconstrained ports, and invalid SDC command syntax. You can use this form after running the `assembleDesign` command.

For more information on SDC checks that the Conformal Constraint Designer uses to verify SDC data, see the “SDC Rule Checks” chapter of the *Encounter Conformal Constraint Designer Reference Manual*.

➤ Choose *Tools – Conformal – Check Assembled Constraints*, then click the *Basic* tab.



Conformal Check Assembled Constraints – Basic Fields and Options

Top Constraints	Specifies the pre-assembly top level constraint file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Top Constraints Files browser window.

Block Constraints

Specifies the pre-assembly block constraints. You must provide either one combination or multiple combinations of both instance name(s) and corresponding constraint file name(s).

For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Block Hierarchical Instances & Constraints browser window.

Clock Map Files

Specifies clock map file(s) that contain hierarchically equivalent clocks. For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Clock Map File browser window.

Note: Use the clock map files previously generated when running the `deriveTimingBudget -ccd` command.

Default: Partition map file.

Chip Netlist

Specifies the chip netlist file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Chip Netlist browser window.

Default: Current netlist file. If the design has changed since loading or saving the design, a new netlist is written out and passed to the software.

Chip Constraints

Specifies the chip constraint file(s). For multiple files, separate each filename with a space. You can enter the name(s) or click … to select them from the Chip Constraint File browser window.

Default: Current SDC file.

Chip Multi_Mode View

Specifies the multi-mode chip-level view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option.

Note: Multi-mode constraints and views must already be specified.

Related Text Command

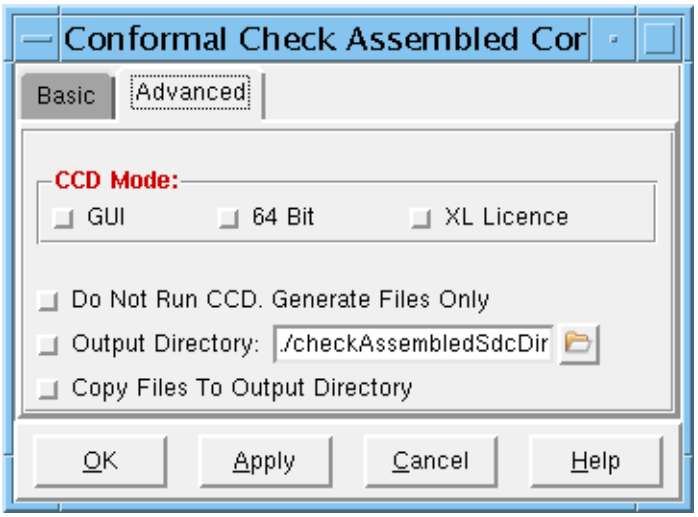
For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `checkAssembledSdcCCD`

Conformal Check Assembled Constraints - Advanced

Use the *Advanced* page of the Conformal Check Assembled Constraints form to specify additional options for checking pre-assembled design top and block constraints against post-assembled design chip constraints.

➤ Choose *Tools – Conformal – Check Assembled Constraints*, then click the *Advanced* tab.



Conformal Check Assembled Constraints – Advanced Fields and Options

GUI	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Encounter session—you can continue to run additional Encounter commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Encounter log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Encounter command is executed until the CCD script has completed.
64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Encounter software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license
Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click the *Browser* icon select a directory from the Output Directory browser window. *Default*: `./checkAssembledSdcDir`
Copy Files to Output Directory	Copies all design files present in the Conformal script to the Conformal run directory. You can use the *Output Directory* option to specify the run directory.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `checkAssembledSdcCCD`

Conformal Derive Critical False Path

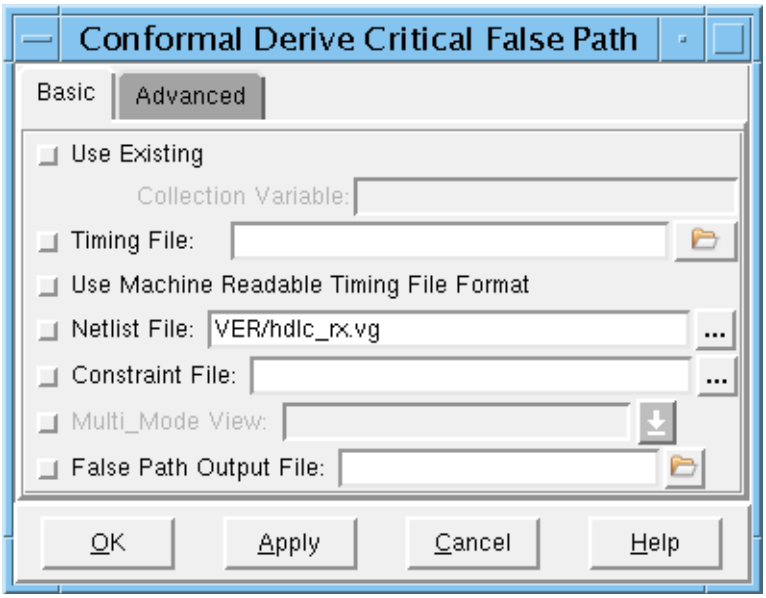
The Conformal Derive Critical False Path form contains the following pages:

- Conformal Derive Critical False Path - Basic on page 1605
- Conformal Derive Critical False Path - Advanced on page 1608

Conformal Derive Critical False Path - Basic

Use the *Basic* page of the Conformal Derive Critical False Path form to analyze critical false paths based on Encounter CTE timing information and constraints. A set of false paths are output which can be loaded into Encounter. These false paths can eliminate unnecessary netlist optimizations and can improve design area and timing. You can use this form after loading design with timing constraints.

➤ Choose *Tools – Conformal – Derive Critical False Paths*.



Conformal Derive Critical False Path – Basic Fields and Options

Use Existing

Specifies a previously generated collection of timing paths to be used to pass timing information to the CCD software. The timing paths contained in the user-defined collection are then passed to the CCD software in a Standard Format Timing File.

To generate this collection of timing paths, use the `report_timing -collection` option along with your own set of reporting options as required.

Default: The software performs timing analysis. A collection containing the timing paths is used to generate a standard format timing file to pass to the CCD software.

Timing File

Specifies previously generated timing debug file to pass to the Conformal Constraint Designer software. You can enter the name or click the *Browser* icon select a file from the Timing File browser window.

You can generate this machine readable timing file. For example, for maximum slack value, you can run the following command:

```
report_timing -machine_readable -max_points 30000 \
-nworst 100 -max_slack 0.20 > timing_debug.rpt
```

Default: Timing analysis is performed to generate a machine readable timing file to pass to the software.

Use Machine Readable Timing File Format

Specifies that the machine readable format should be used when passing timing file information to the CCD software.

Default: The CCD standard format is used to pass timing file information to the CCD software.

Netlist File

Specifies the name of the netlist file. For multiple files, separate each filename with a space. You can enter the name(s) or click *…* to select them from the Netlist Files browser window.

Default: Passes the existing design netlist to the software. If the design has changed since previously loading or saving the design, a new netlist is written out and passed to the Conformal Constraint Designer software.

Constraint File

Specifies the constraint file(s) to analyze using Conformal Constraint Designer. For multiple files, separate each filename with a space. You can enter the name(s) or click *…* to select them from the Constraint Files browser window.

Default: Passes the existing design constraints to the software. If the design has changed since previously loading or saving the design, a new constraint file is written out and passed to the software.

Multi_Mode View	Specifies the multi-mode view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option. This view is also used by CTE to generate the timing debug file to pass to the Conformal Constraint Designer software. **Note:** Multi-mode constraints and views must already be specified. *Default*: If you do not specify the `-constraints` option, the current design SDC file is passed to the Conformal software for analysis.
False Path Output File	Specifies the name of the output false-path file. You can enter the name or click the *Browser* icon select a file from the False Path Output File browser window. *Default*: `criticalFalsePaths.sdc`. This file is generated in output directory specified by the *Output Directory* option.

Related Text Command

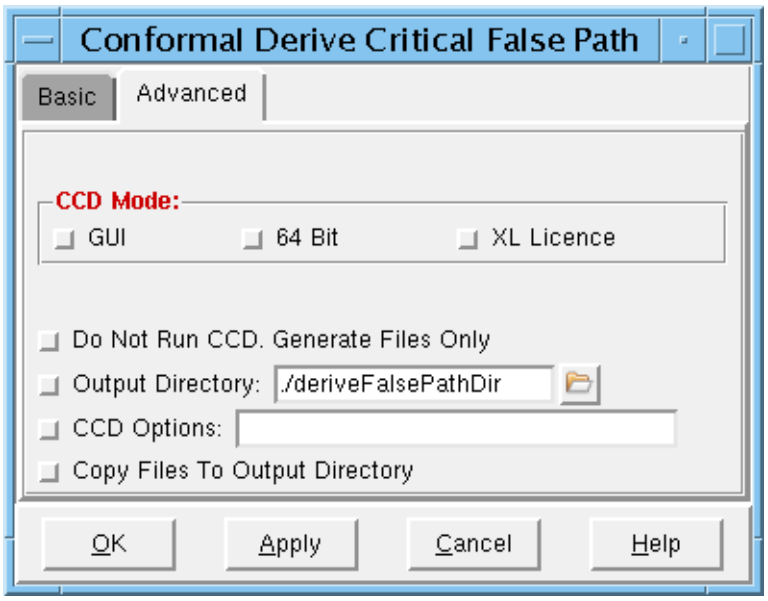
For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `deriveFalsePathCCD`

Conformal Derive Critical False Path - Advanced

Use the *Advanced* page of the Conformal Derive Critical False Path form to specify additional options to analyze critical false paths in CCD based on Encounter-CTE timing information and constraints.

➤ Choose *Tools – Conformal – Derive Critical False Paths*, then click the *Advanced* tab.



Conformal Derive Critical False Path – Advanced Fields and Options

GUI	Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Encounter session—you can continue to run additional Encounter commands while the CCD GUI mode session is running in parallel. The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script. Conformal log messages are not echoed to the Encounter log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option). *Default:* Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Encounter command is executed until the CCD script has completed.
64 Bit	Specifies 64-bit CCD. *Default:* 32-bit CCD, or 64-bit if the Encounter software starts in 64-bit mode.
XL License	Runs the Conformal Constraint Designer software with the XL license. *Default:* CCD L license
Do Not Run CCD. Generate Files Only	Specifies that the Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.
Output Directory	Specifies the name of the directory in which to generate CCD script and log files. You can enter the name or click the *Browser* icon select a directory from the Output Directory browser window. *Default*: `./deriveFalsePathDir`

CCD Options	Specifies how you want the Conformal Constraint Designer software to handle exception validation and exception generation. For a table of available strings, see the `deriveFalsePathCCD` command documentation.
Copy Files to Output Directory	Copies all design files present in the Conformal script to the Conformal run directory. You can use the *Output Directory* option to specify the run directory.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `deriveFalsePathCCD`

Conformal Promote Constraints

The Conformal Promote Constraints form contains the following pages:

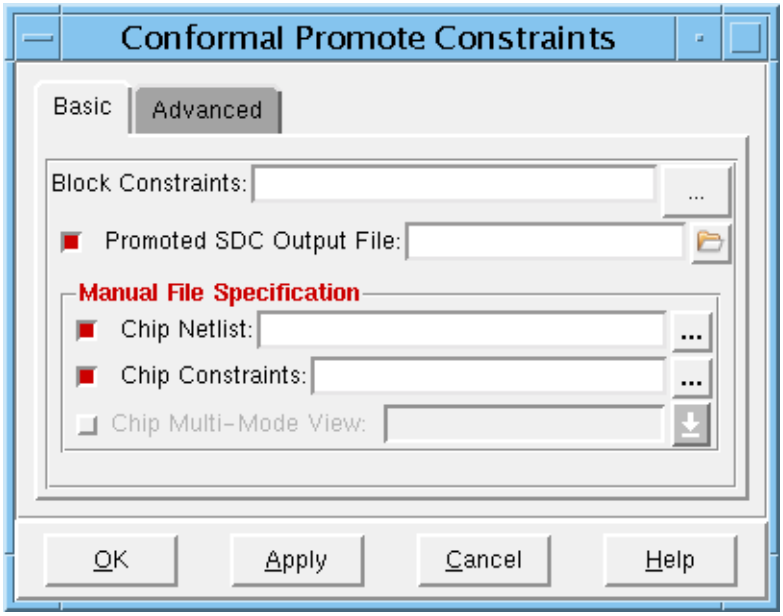
- Conformal Promote Constraints - Basic on page 1612
- Conformal Promote Constraints - Advanced on page 1614

Conformal Promote Constraints - Basic

Use the *Basic* page of the Conformal Promote Constraints form to generate top level constraints using Conformal Constraint Designer by promoting block-level constraints to the top level, integrating them with any existing chip-level constraints.

To use this feature, specify the path to the Conformal Constraint Designer installation before running Encounter.

➤ Choose *Tools – Conformal – Promote Constraints*.



Conformal Promote Constraints – Basic Fields and Options

Block Constraints	Specifies the block constraints to be passed to Conformal Constraint Designer for SDC promotion. You must provide either one combination or multiple combinations of both instance name(s) and corresponding constraint file name(s).
Promoted SDC Output File	Specifies the output SDC file. *Default*: `promotedChip.sdc`. This file is generated in output directory specified by the *Output Directory* option in this form's *Advanced* page.

Chip Netlist

Allows manual specification of the original chip netlist file(s) to analyze using Conformal Constraint Designer. This option is useful for overriding chip netlist settings. You can enter the name or click `...` to select a file or files.

Default: The netlist is automatically detected from Encounter database.

Chip Constraints

Specifies the SDC chip constraint file(s) to be passed to Conformal Constraint Designer for SDC promotion. You can enter the name or click `...` to select a file or files.

Note: This option cannot be used in conjunction with *Chip Multi-Mode View.*

Default: Passes the existing design constraints to the software. If the design has changed since loading or saving the design, a new constraint file is written out and passed to the software.

Chip Multi-Mode View

Specifies the multi-mode chip-level view name. If a design has multiple modes, you can specify which set of view constraints to pass to Conformal with this option.

Note: Multi-mode constraints and views must already be specified.

Default: If you do not use the *Chip Constraints* option, the current design SDC file is passed to the Conformal software for analysis.

Related Text Command

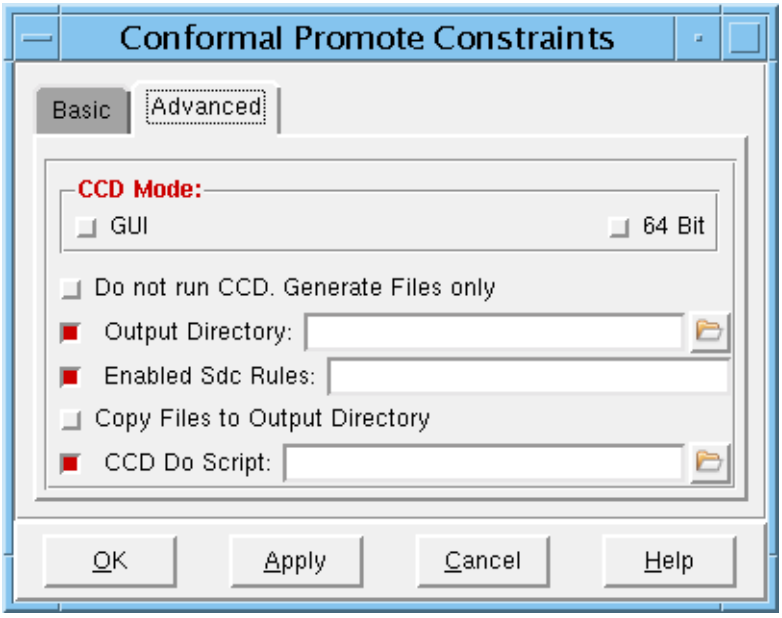
For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `promoteSdcCCD`

Conformal Promote Constraints - Advanced

Use the *Advanced* page of the Conformal Promote Constraints form to specify additional options to promote block-level constraints to the top level.

➤ Choose *Tools – Conformal – Promote Constraints*, then click the *Advanced* tab.



Conformal Promote Constraints – Advanced Fields and Options

GUI

Runs the Conformal Constraint Designer software in GUI mode. This runs as a parallel job separate from the Encounter session—you can continue to run additional Encounter commands while the CCD GUI mode session is running in parallel.

The software does not exit at the end of the session, so you can continue interactive debugging in the standalone Conformal GUI after completion of the CCD script.

Conformal log messages are not echoed to the Encounter log file. The software creates a separate Conformal log file in the CCD run directory (see the *Output Directory* option).

Default: Off. The Conformal Constraint Designer software exits at the end of the session. In non-GUI mode, the software is not run as a parallel job, therefore no Encounter command is executed until the CCD script has completed.

64 Bit

Specifies 64-bit CCD.

Default: 32-bit CCD, or 64-bit if the Encounter software starts in 64-bit mode.

Do not run CCD. Generate Files only

Specifies that Conformal Constraint Designer software does not start, however, the CCD script is generated. You can use this option if you need to customize CCD run scripts.

Output Directory

Specifies the name of the directory in which to generate CCD script and log files.

Default: `./promoteSdcDir`.

Enabled SDC rules

Allows specification of user-enabled or disabled rules in CCD to be specified during CCD do file initialization. You can define multiple added and deleted disabled rules.

Default: The following default set of rules are defined on script initialization:

```
add rule instance -def
```

The user-enabled rules are added after this default set of rules.

Copy Files to Output Directory	Copies all design files in the Conformal script to the Conformal run directory. You can use the *Output Directory* option to specify the run directory. *Default*: Design files are not copied to the CCD run directory.
CCD Do Script	Specifies an existing dofile script that should be passed to the CCD software for execution. *Default*: A new dofile script is generated based on user specified `checkBudgetSdcCCD` options and used to run the CCD software.

Related Text Command

For information on the following command, see “Conformal Commands” in the *Encounter Text Command Reference*.

- `promoteSdcCCD`

Report Yield

Use the Report Yield form to generate a yield report for the design and a yield map, similar to a congestion map, that uses colors to indicate the yield loss graphically.

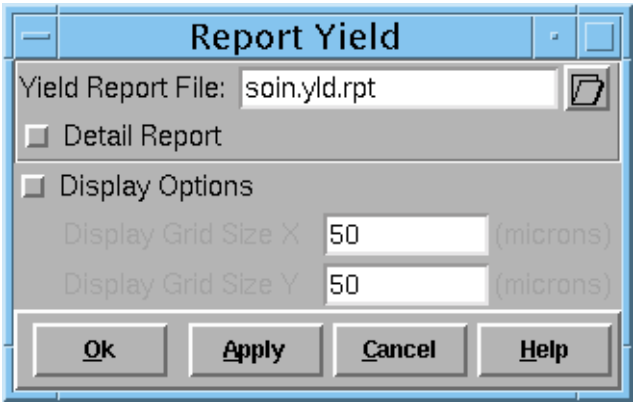
The Encounter software reports the expected defect-limited yield for the design using critical area analysis, based on the technology you are using and the probability of failure of the cells, vias, and point defects in routing. Uses technology-specific data from a yield file supplied by the fabricator.

When you click the *OK* or *Apply* button on the form, the software creates a new yield map and report. When you save the design, the software saves the current yield map. When you restore the design, the yield map is also restored.

Use one of the following methods to display the Report Yield form:

➤ Click the *Report Yield* widget on the toolbar in the main Encounter window.

➤ Choose *Tools – Report Yield*.



Report Yield Fields and Options

Yield Report File	Specifies the yield report name.The report includes an overall yield result you can use to estimate the improvement in yield from different optimization techniques. *Default:* `designName.yld.rpt`

Detail Report	Specifies a detailed report. The detailed report contains the information included in the non-detailed report, plus detailed yield cost per cell and per location.
Display Options	Enables you to change the grid size on the yield map.
Display Grid Size X	Changes the grid size in the horizontal direction. *Default:* `50 microns`
Display Grid Size Y	Changes the grid size in the vertical direction. *Default:* `50 microns`

Related Text Commands

For information on the following related text commands, see “Yield Analysis Commands” in the *Encounter Text Command Reference*:

- `reportYield`
- `loadYieldTechFile`

Related Topics

For information on the following topics, see “Analyzing Yield” in the *Encounter User Guide*:

- “What Effects Does reportYield Consider?”
- “Calculating Failure Probabilities”
- “Displaying the Yield Map”

Mixed Signal

The *Tool* menu's Mixed Signal forms enable you to enter or edit constraints for mixed signal designs and to perform partial design simulation or critical paths simulation of the designs.

The *Mixed Signal* submenu contains the following pages:

- *Constraints*

  Opens the Mixed Signal Constraint Editor form.

- *Simulation*

  Opens the UltraSim form.

Mixed Signal Constraint Editor

Use the Mixed Signal Constraint Editor form to enter, edit, and save mixed signal constraints in the Encounter database. Routing, verification, and other commands read the constraints when they execute.

If you load a `.const` file, the values in the file populate the form and you can edit them.

The following options appear on each constraint editor page, except the *Display All* page.

Add/Update	Adds or edits a constraint on the nets shown in the *Constraint Members* text entry box to virtual memory.
Create	Opens a new, blank page that you can edit.
Copy	Copies the constraint on the current page, so you can use or edit it for another net.
Delete	Deletes the current constraint.
Apply	Overwrites existing constraints with constraints that have been added or updated using the Routing Constraints or Electrical Constraints pages, saves all the constraints in the constraint file as properties assigned to the nets and in the Encounter database. The default filename for a new `.const` file is `topLevelCellName.msroute`*`number`*`.const`. When you click *Apply*, the software increments the number.
Load	Opens the Load MS Constraint form. Use the form to select a constraint file to edit.
Reset	Resets all fields on the form to their status before the current editing session.
Display	Opens the *Display All* page. This page lists all the routing or electrical constraints that are saved in the database. Unlike the other pages, this page is not editable.
Close	Closes the form.
Help	Displays Cadence Help for the page that is displayed.

The Mixed Signal Constraint Editor form contains the following pages:

- Routing Constraints on page 1621
- Electrical Constraints on page 1651

Routing Constraints

Use the *Routing Constraints* page of the Mixed Signal Constraint Editor form to enter, edit, and save mixed signal routing constraints in the Encounter database.

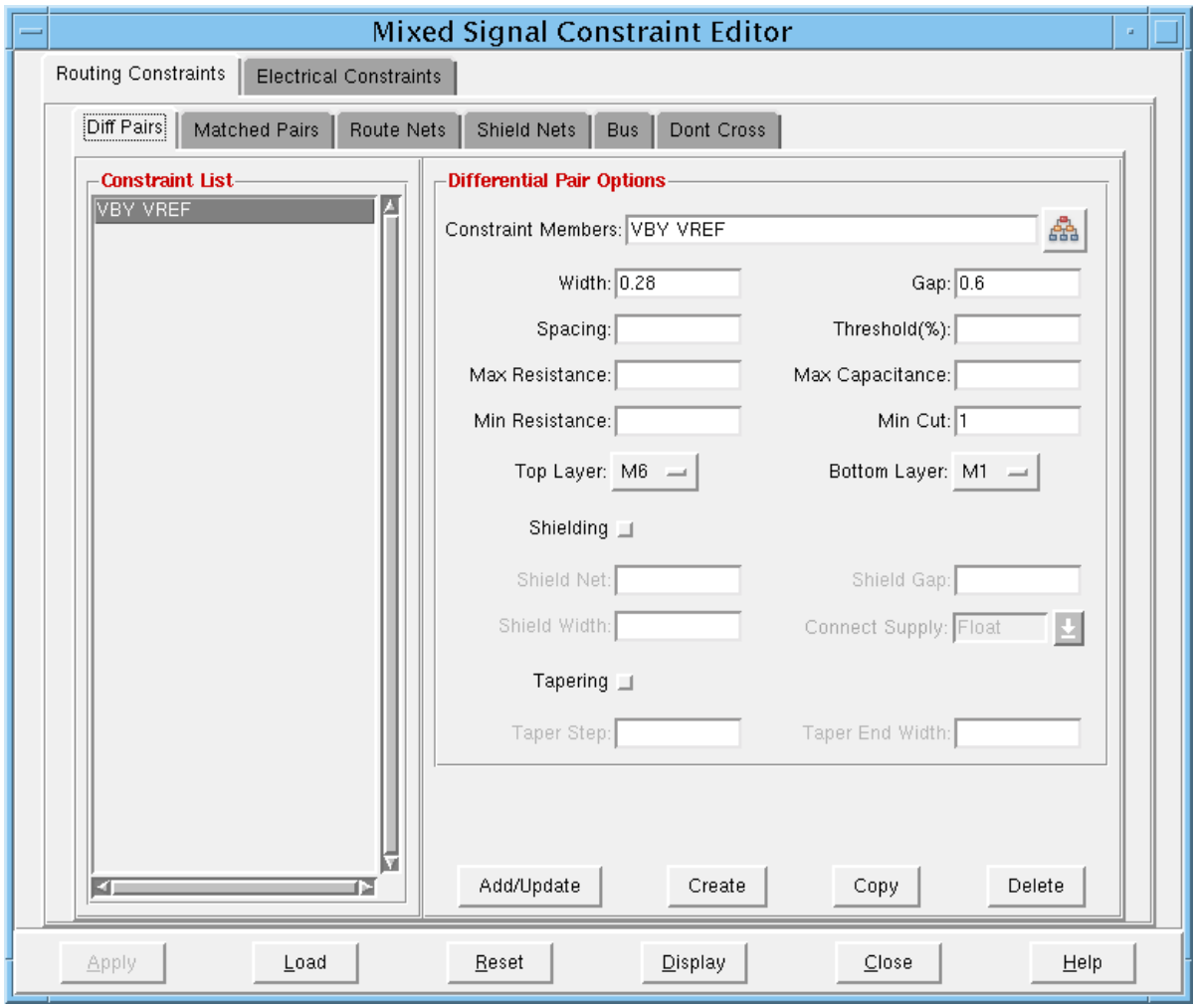
The *Routing Constraints* page contains the following subpages:

- Diff Pairs on page 1622
- Matched Pairs on page 1627
- Route Nets on page 1632
- Shield Nets on page 1637
- Bus on page 1642
- Dont Cross on page 1647
- Display All on page 1649

Diff Pairs

Use the *Diff Pairs* page to constrain nets by width and spacing, in order to match the parasitic load on the nets. You can also use this page to specify constraints for shielded differential pair nets. You can specify a threshold value for the spacing, so the router attempts to meet the spacing but does not create a violation if it misses the spacing by less than the threshold value.

➤ Choose *Tools – Mixed Signal – Constraints*, click the *Routing Constraints* tab, then select *Diff Pairs*.



Diff Pairs Fields and Options

Constraint List

Lists the nets with mixed signal constraints.

Differential Pair Options

Constraint Members Displays the name of the highlighted net or nets on the *Constraint List*.

Opens the Select Constraint Member form, on which you can select nets to constrain. For information, see "Select Constraint Member" on page 1658.

Width Specifies the width of constrained nets, measured in microns.
Default: 0 (minimum width)

Gap Specifies the distance in microns between the two differential pair nets.
Default: Minimum spacing value in the LEF file

Spacing Specifies the distance in microns between the net routed by the mixed signal router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net.
Default: `SPACING` or `SPACINGTABLE` value from the LEF file

Threshold (%) Specifies a percentage value for the variance from the *Gap*, so the router attempts to meet the specified *Gap*, but does not create a violation if it misses the *Gap* by less than the threshold.
Default: 20

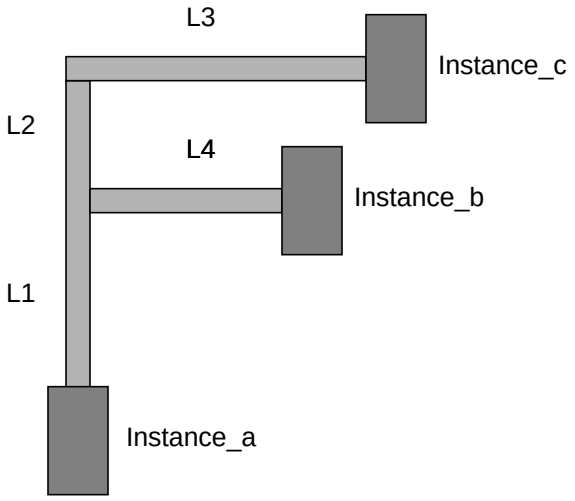
The threshold is calculated by using the following formula:

$$\text{Threshold} = \frac{\textit{Length of the longer net} - \textit{Length of the shorter net}}{\textit{Length of the shorter net}}$$

For example, if the constrained nets are 24 microns and 20 microns, the threshold would be calculated as (24 – 20) / 20 = 0.2 = 20%.

Max Resistance

Specifies the maximum resistance of a net, measured in ohms. The following figure shows a multi-pin net with four segments.



In the estimation phase, the router estimates the resistance using the following formula:

Resistance = (*average resistivity of all metal layers*) x ((L1 + L2 + L3) /(*average width of all metal layers*))

After routing, the router calculates effective resistance using the following formula:

Resistance =
((Resistivity of L1)*(L1/Width of L1)) +
((Resistivity of L2)*(L2/Width of L2)) +
((Resistivity of L3)*(L3/Width of L3)) +
((Resistivity of L4)*(L4/Width of L4))

- If the pin on `Instance_b` is an output pin, valid paths are `L1 + L2 + L3` and `L1 + L4`.
- If the pin on `Instance_b` is a bidirectional pin, valid paths are `L1 + L2 + L3`, `L1 + L4`, and `L4 + L2 + L3`.

Max Capacitance

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.The Encounter software calculates capacitance using the following formula:

Total capacitance =
area_capacitance + *side_capacitance*

Min Resistance

Specifies the minimum resistance of a net, measured in ohms.

Min Cut
Specifies the minimum number of cuts per via.
Default: 1

Top Layer
Specifies the top routing layer.

Bottom Layer
Specifies the bottom routing layer.

Shielding
Enables the shielding options on this page, so you can shield differential pair nets.

Shield Net
Specifies a special net (typically VSS) used to shield the *Constraint Member* net.

Shield Gap
Specifies the distance in microns between the shield (the special net) and the shielded net (the signal net).

Shield Width
Specifies the width of the *Shield Net*, measured in microns.

Connect Supply
Connects shield nets to the supply.

Select one of the following options:

Float
Does not connect the shield—leaves it floating.

Any Point
Connects the shield to the supply at any point along the wire.

One End
Connects the shield to the supply at one end.

Both End
Connects the shield to the supply at both ends.

Tapering
Reduces the wire width to the width of the pin or to a specified width. If you do not select *Taper Step* or *Taper End Width*, the router tapers the wires to the width of the pin in one step.

Note: The width of a wire on a taper step cannot be more than three times the width of the wire on a neighboring step. If you specify values that do not meet this requirement, the router adjusts the values to increse the number of steps. If it cannot meet the requirement by increasing the number of steps, the router issues a warning and does not taper the wire.

Taper Step
Specifies the number of steps the router uses to reduce the wire width.
Default: 1
Maximum: 3

Taper End Width

Specifies the width of the wire after tapering (when the wire connects to the pin).
Default: pin width

Related Topics

For information on the following topics, see Using the Encounter Software in Mixed Signal Designs in the *Encounter User Guide*:

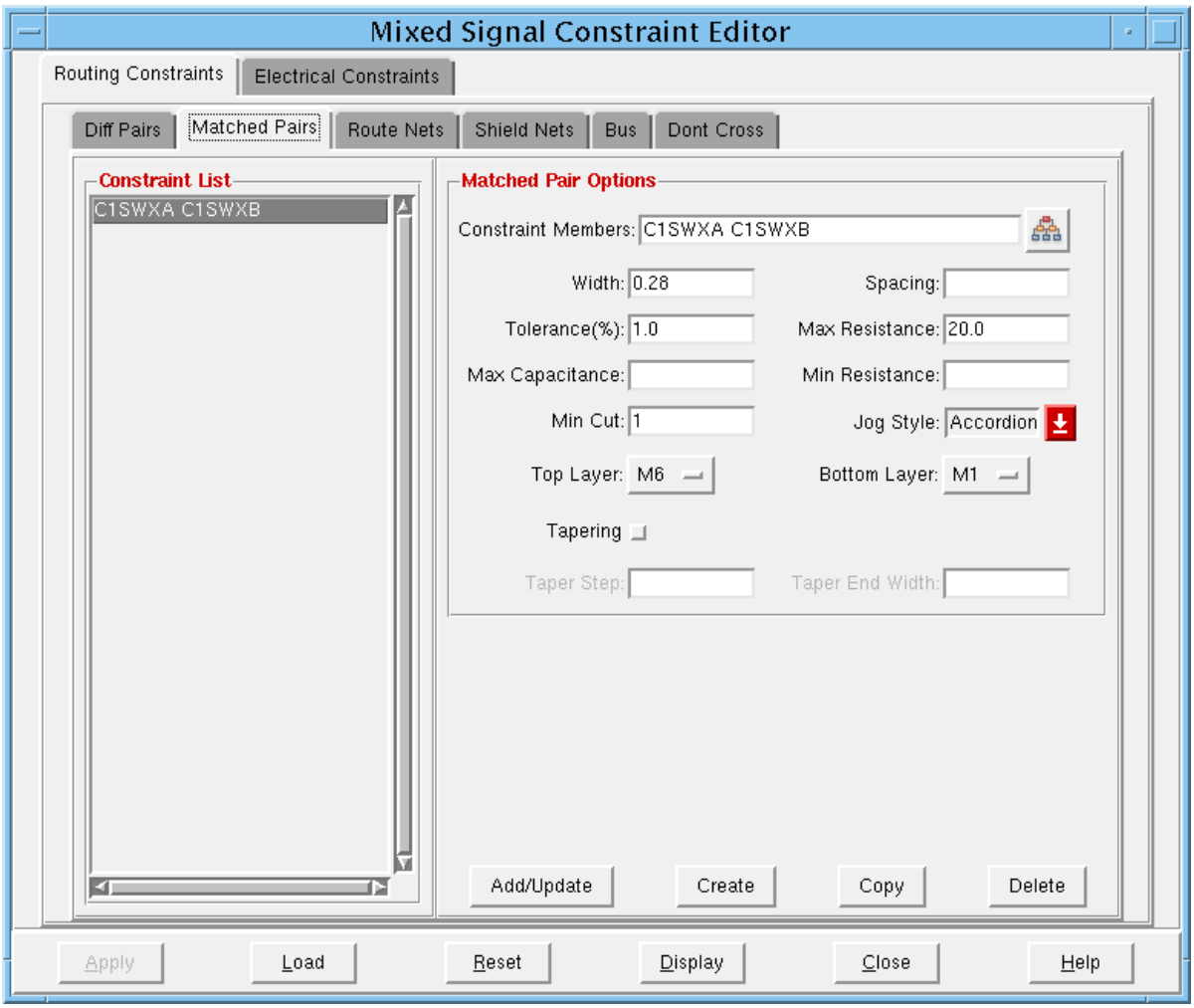
- "Specialized Routing Techniques"
- "Using Routing Constraints"
- "Specialized Constraints and Keyword Descriptions"
- "Creating a Constraint File"
- "Editing a Constraint File"
- "Loading a Constraint File"

Matched Pairs

Use the *Matched Pairs* page to create routes that are the same length. The routes are not required to be the same topologically. Matching nets are not limited to two nets.

You can specify a tolerance factor for the maximum resistance, so the router attempts to meet the specified maximum resistance constraint, but does not create a violation if the resistance exceeds the maximum resistance by less than the tolerance factor.

➤ Choose *Tools – Mixed Signal – Constraints – Routing Constraints*, then select *Matched Pairs*.



Matched Pairs Fields and Options

Constraint List

Lists the nets with mixed signal constraints.

Matched Pair Options

Constraint Members

Displays the name of the highlighted net or nets on the *Constraint List*.

Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Width

Specifies the width of constrained nets, measured in microns.
Default: 0 (minimum width)

Spacing

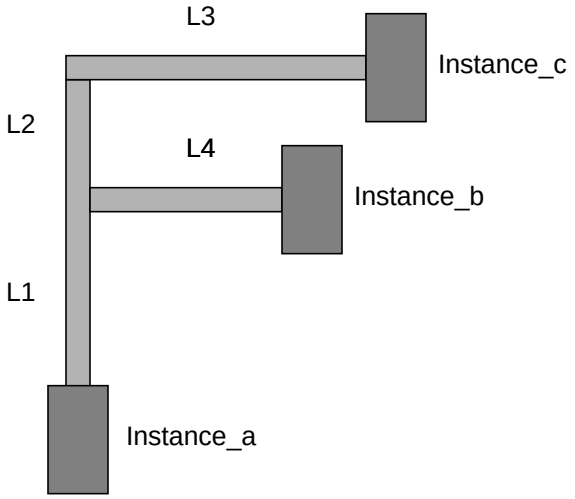
Specifies the distance in microns between the net routed by the mixed signal router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net.
Default: `SPACING` or `SPACINGTABLE` value from the LEF file.

Tolerance (%)

Specifies a tolerance factor for the maximum upper limit on the resistance.
Default: 20

Max Resistance

Specifies the maximum resistance of a net, measured in ohms. The following figure shows a multi-pin net with four segments.



In the estimation phase, the router estimates the resistance using the following formula:

Resistance = (*average resistivity of all metal layers*) x ((L1 + L2 + L3) /(*average width of all metal layers*))

After routing, the router calculates effective resistance using the following formula:

Resistance =
((Resistivity of L1)*(L1/Width of L1)) +
((Resistivity of L2)*(L2/Width of L2)) +
((Resistivity of L3)*(L3/Width of L3)) +
((Resistivity of L4)*(L4/Width of L4))

- If the pin on `Instance_b` is an output pin, valid paths are `L1 + L2 + L3` and `L1 + L4`.
- If the pin on `Instance_b` is a bidirectional pin, valid paths are `L1 + L2 + L3`, `L1 + L4`, and `L4 + L2 + L3`.

Max Capacitance

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.The Encounter software calculates capacitance using the following formula:

Total capacitance =
area_capacitance + *side_capacitance*

Min Resistance

Specifies the minimum resistance of a net, measured in ohms.

Min Cut

Specifies the minimum number of cuts per via.
Default: 1

Jog Style

Accordion

Trombone

Top Layer Specifies the top routing layer.

Bottom Layer Specifies the bottom routing layer.

Tapering Reduces the wire width to the width of the pin or to a specified width. If you do not select *Taper Step* or *Taper End Width*, the router tapers the wires to the width of the pin in one step.

Note: The width of a wire on a taper step cannot be more than three times the width of the wire on a neighboring step. If you specify values that do not meet this requirement, the router adjusts the values to increse the number of steps. If it cannot meet the requirement by increasing the number of steps, the router issues a warning and does not taper the wire.

Taper Step

Specifies the number of steps the router uses to reduce the wire width.
Default: 1
Maximum: 3

Taper End Width

Specifies the width of the wire after tapering (when the wire connects to the pin).
Default: pin width

Related Topics

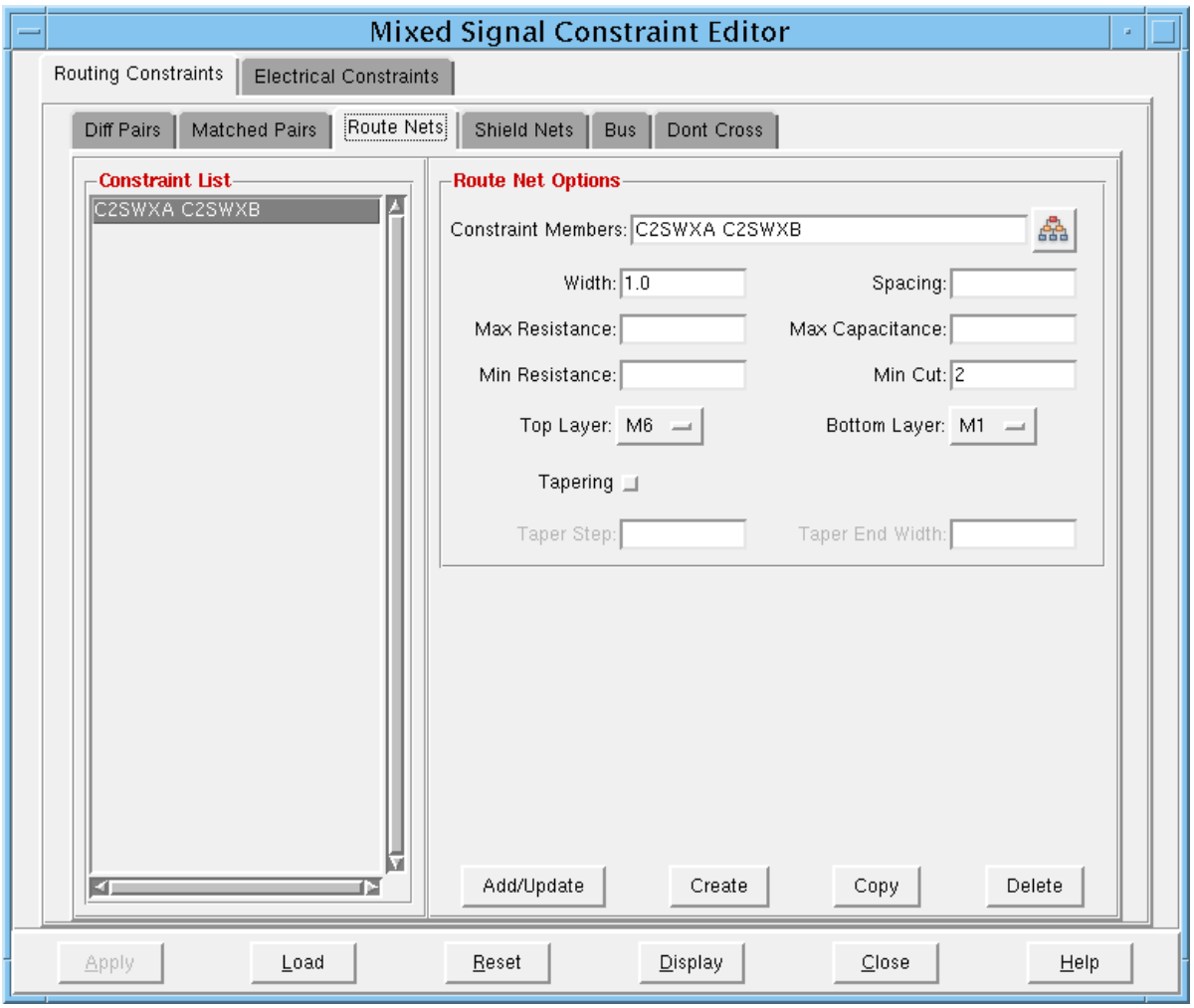
For information on the following topics, see “Using the Encounter Software in Mixed Signal Designs” in the *Encounter User Guide*:

- “Specialized Routing Techniques”
- “Using Routing Constraints”
- “Specialized Constraints and Keyword Descriptions”
- “Creating a Constraint File”
- “Editing a Constraint File”
- “Loading a Constraint File”

Route Nets

Use the *Route Nets* page to create width, resistance, capacitance, minimum via cut, routing layer, and tapering constraints.

➤ Choose *Tools – Mixed Signal – Constraints – Routing Constraints,* then select *Route Nets*.



Route Nets Fields and Options

Constraint List

Lists the nets with mixed signal constraints.

Route Net Options

Constraint Members

Displays the name of the highlighted net or nets on the *Constraint List*.

Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Width

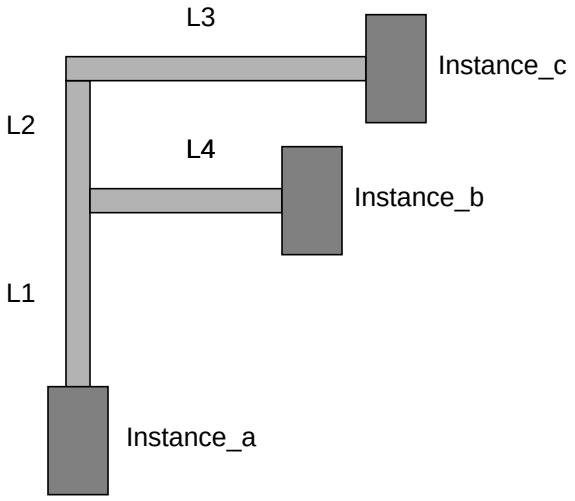
Specifies the width of constrained nets, measured in microns.
Default: 0 (minimum width)

Spacing

Specifies the distance in microns between the net routed by the mixed signal router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net.
Default: `SPACING` or `SPACINGTABLE` value from the LEF file.

Max Resistance

Specifies the maximum resistance of a net, measured in ohms. The following figure shows a multi-pin net with four segments.



In the estimation phase, the router estimates the resistance using the following formula:

Resistance = (*average resistivity of all metal layers*) x ((L1 + L2 + L3) /(*average width of all metal layers*))

After routing, the router calculates effective resistance using the following formula:

Resistance =
((Resistivity of L1)*(L1/Width of L1)) +
((Resistivity of L2)*(L2/Width of L2)) +
((Resistivity of L3)*(L3/Width of L3)) +
((Resistivity of L4)*(L4/Width of L4))

- If the pin on `Instance_b` is an output pin, valid paths are `L1 + L2 + L3` and `L1 + L4`.
- If the pin on `Instance_b` is a bidirectional pin, valid paths are `L1 + L2 + L3`, `L1 + L4`, and `L4 + L2 + L3`.

Max Capacitance

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.The Encounter software calculates capacitance using the following formula:

Total capacitance =
area_capacitance + *side_capacitance*

Min Resistance

Specifies the minimum resistance of a net, measured in ohms.

Min Cut
Specifies the minimum number of cuts per via.
Default: 1

Top Layer
Specifies the top routing layer.

Bottom Layer
Specifies the bottom routing layer.

Tapering
Reduces the wire width to the width of the pin or to a specified width. If you do not select *Taper Step* or *Taper End Width*, the router tapers the wires to the width of the pin in one step.

Note: The width of a wire on a taper step cannot be more than three times the width of the wire on a neighboring step. If you specify values that do not meet this requirement, the router adjusts the values to increse the number of steps. If it cannot meet the requirement by increasing the number of steps, the router issues a warning and does not taper the wire.

Taper Step
Specifies the number of steps the router uses to reduce the wire width.
Default: 1
Maximum: 3

Taper End Width
Specifies the width of the wire after tapering (when the wire connects to the pin).
Default: pin width

Related Topics

For information on the following topics, see “Using the Encounter Software in Mixed Signal Designs” in the *Encounter User Guide*:

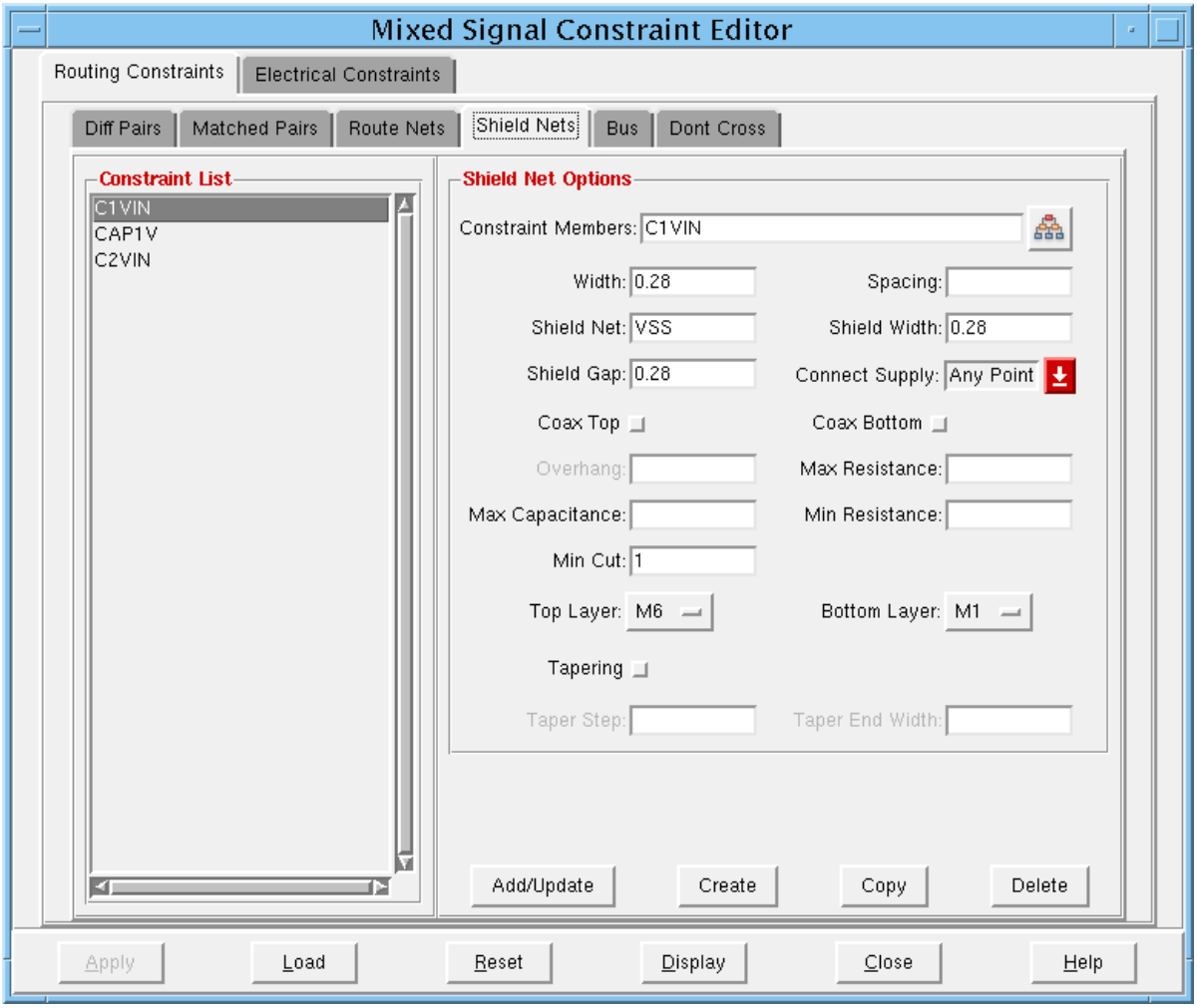
- “Specialized Routing Techniques”
- “Using Routing Constraints”
- “Specialized Constraints and Keyword Descriptions”
- “Creating a Constraint File”
- “Editing a Constraint File”
- “Loading a Constraint File”

Shield Nets

Use the *Shield Nets* page to enter or edit constraints for shielded routing, in which noise-critical signal nets are shielded by special nets.

- To specify options for shielding differential pair nets, use the *Diff Pairs* page. For more information, see "Diff Pairs" on page 1622.
- To specify options for shielding buses, use the *Bus* page. For more information, see "Bus" on page 1642.

➤ Choose *Tools – Mixed Signal – Constraints – Routing Constraints*, then select *Shield Nets*.



Shield Nets Fields and Options

Constraint List

Lists the nets with mixed signal constraints.

Shield Nets Options

Constraint Members

Displays the name of the highlighted net or nets on the *Constraint List*.

Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Width

Specifies the width of constrained nets, measured in microns.
Default: 0 (minimum width)

Spacing

Specifies the distance in microns between the net routed by the mixed signal router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net.
Default: `SPACING` or `SPACINGTABLE` value from the LEF file.

Shield Net

Specifies a special net (typically VSS) used to shield the *Constraint Member* net.

Shield Width

Specifies the width of the *Shield Net*, measured in microns.

Shield Gap

Specifies the distance in microns between the shield (the special net) and the shielded net (the signal net).

Connect Supply

Connects shield nets to the supply.

Select one of the following options:

Float	Does not connect the shield—leaves it floating.
Any Point	Connects the shield to the supply at any point along the wire.
One End	Connects the shield to the supply at one end.
Both End	Connects the shield to the supply at both ends.

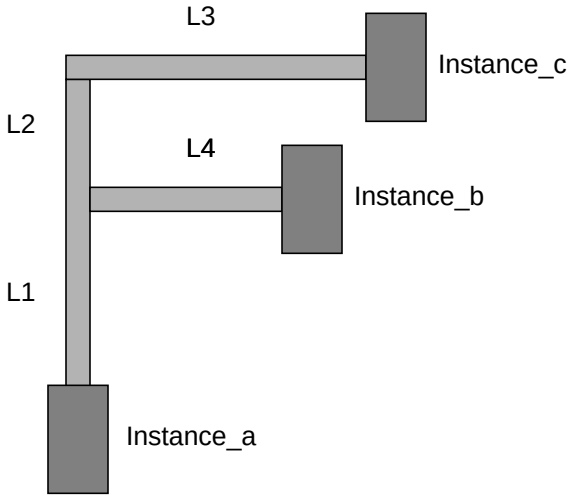
Coax Top

Specifies a shield net on the next higher metal layer in the same direction as the *Constraint Member* net.

Coax Bottom Specifies a shield net on the next lower metal layer in the same direction as the *Constraint Member* net.

Overhang Specifies one-half of the difference between the width of the signal net and the width of the bottom and top shield nets.

Max Resistance Specifies the maximum resistance of a net, measured in ohms. The following figure shows a multi-pin net with four segments.



In the estimation phase, the router estimates the resistance using the following formula:

Resistance = (*average resistivity of all metal layers*) x ((L1 + L2 + L3) /(*average width of all metal layers*))

After routing, the router calculates effective resistance using the following formula:

Resistance =
((Resistivity of L1)*(L1/Width of L1)) +
((Resistivity of L2)*(L2/Width of L2)) +
((Resistivity of L3)*(L3/Width of L3)) +
((Resistivity of L4)*(L4/Width of L4))

- If the pin on `Instance_b` is an output pin, valid paths are `L1 + L2 + L3` and `L1 + L4`.
- If the pin on `Instance_b` is a bidirectional pin, valid paths are `L1 + L2 + L3`, `L1 + L4`, and `L4 + L2 + L3`.

Max Capacitance

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.The Encounter software calculates capacitance using the following formula:

Total capacitance =
area capacitance + side capacitance

Min Resistance

Specifies the minimum resistance of a net, measured in ohms.

Min Cut

Specifies the minimum number of cuts per via.
Default: 1

Top Layer

Specifies the top routing layer.

Bottom Layer

Specifies the bottom routing layer.

Tapering

Reduces the wire width to the width of the pin or to a specified width. If you do not select *Taper Step* or *Taper End Width*, the router tapers the wires to the width of the pin in one step.

Note: The width of a wire on a taper step cannot be more than three times the width of the wire on a neighboring step. If you specify values that do not meet this requirement, the router adjusts the values to increse the number of steps. If it cannot meet the requirement by increasing the number of steps, the router issues a warning and does not taper the wire.

Taper Step

Specifies the number of steps the router uses to reduce the wire width.
Default: 1
Maximum: 3

Taper End Width

Specifies the width of the wire after tapering (when the wire connects to the pin).
Default: pin width

Related Topics

For information on the following topics, see “Using the Encounter Software in Mixed Signal Designs” in the *Encounter User Guide*:

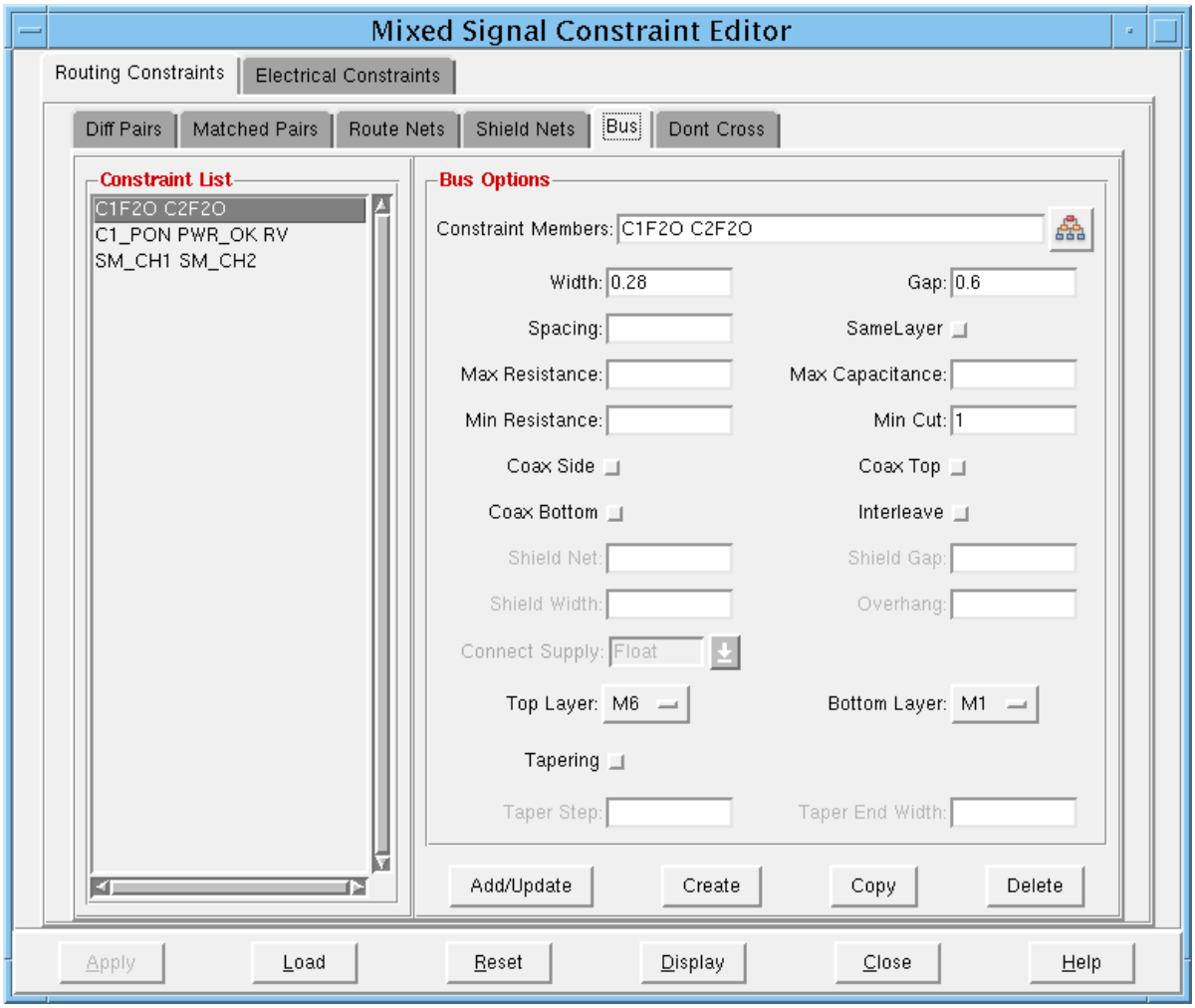
- “Specialized Routing Techniques”

- “Using Routing Constraints”
- “Specialized Constraints and Keyword Descriptions”
- “Creating a Constraint File”
- “Editing a Constraint File”
- “Loading a Constraint File”

Bus

Use the *Bus* page to route specified nets with the same width and spacing. You can control the width, the spacing between the nets, the maximum and minimum resistance, maximum capacitance of the nets, the minimum number of cuts in the vias, and whether the nets must be routed on the same layer. Bus routing is sometimes called river routing or bundle routing.

➤ Choose *Tools – Mixed Signal – Constraints – Routing Constraints*, then select *Bus*.



Bus Fields and Options

Constraint List

Lists the nets with mixed signal constraints.

Bus Options

Constraint Members

Displays the name of the highlighted net or nets on the *Constraint List*.

Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Width

Specifies the width of constrained nets, measured in microns. *Default:* 0 (minimum width)

Gap

Specifies the distance in microns between the nets in the bus.

Spacing

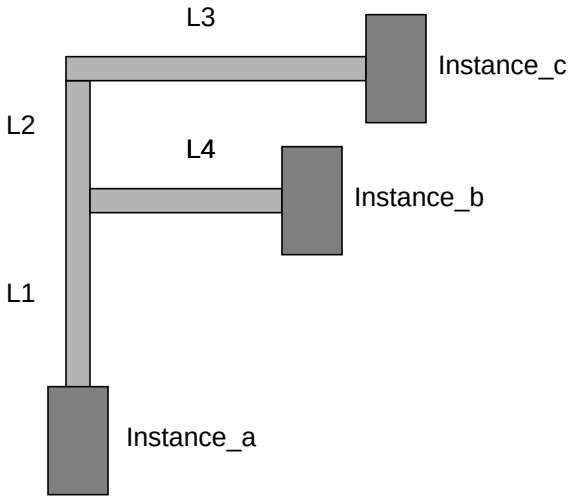
Specifies the distance in microns between the nets routed by the mixed signal router and all other routes. The router uses the spacing value to limit the effect of coupling capacitance on the total capacitance of the net.

SameLayer

Routes all the bits of the bus on the same layer.

Max Resistance

Specifies the maximum resistance of a net, measured in ohms. The following figure shows a multi-pin net with four segments.



In the estimation phase, the router estimates the resistance using the following formula:

Resistance = (*average resistivity of all metal layers*) x ((L1 + L2 + L3) /(*average width of all metal layers*))

After routing, the router calculates effective resistance using the following formula:

Resistance =
((Resistivity of L1)*(L1/Width of L1)) +
((Resistivity of L2)*(L2/Width of L2)) +
((Resistivity of L3)*(L3/Width of L3)) +
((Resistivity of L4)*(L4/Width of L4))

- If the pin on `Instance_b` is an output pin, valid paths are `L1 + L2 + L3` and `L1 + L4`.
- If the pin on `Instance_b` is a bidirectional pin, valid paths are `L1 + L2 + L3`, `L1 + L4`, and `L4 + L2 + L3`.

Max Capacitance

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.The Encounter software calculates capacitance using the following formula:

Total capacitance =
area_capacitance + *side_capacitance*

Min Resistance

Specifies the minimum resistance of a net, measured in ohms.

Min Cut
Specifies the minimum number of cuts per via.
Default: 1

Coax Side
Specifies a shield net on the left and right sides of the *Constraint Member* net.

Coax Top
Specifies a shield net on the next higher metal layer in the same direction as the *Constraint Member* net.

Coax Bottom
Specifies a shield net on the next lower metal layer in the same direction as the *Constraint Member* net.

Interleave

Shield Net
Specifies the special net used as a shield for the constrained net.

Shield Gap
Specifies the distance in microns between the shield (the special net) and the shielded net (the signal net).

Shield Width
Specifies the width of the right and left *Shield Net*, measured in microns.

Overhang
Specifies one-half of the difference between the width of the signal net and the width of the bottom and top shield nets.

Top Layer
Specifies the top routing layer.

Bottom Layer
Specifies the bottom routing layer.

Tapering
Reduces the wire width to the width of the pin or to a specified width. If you do not select *Taper Step* or *Taper End Width*, the router tapers the wires to the width of the pin in one step.

Note: The width of a wire on a taper step cannot be more than three times the width of the wire on a neighboring step. If you specify values that do not meet this requirement, the router adjusts the values to increse the number of steps. If it cannot meet the requirement by increasing the number of steps, the router issues a warning and does not taper the wire.

Taper Step
Specifies the number of steps the router uses to reduce the wire width.
Default: 1
Maximum: 3

Taper End Width

Specifies the width of the wire after tapering (when the wire connects to the pin).
Default: pin width

Related Topics

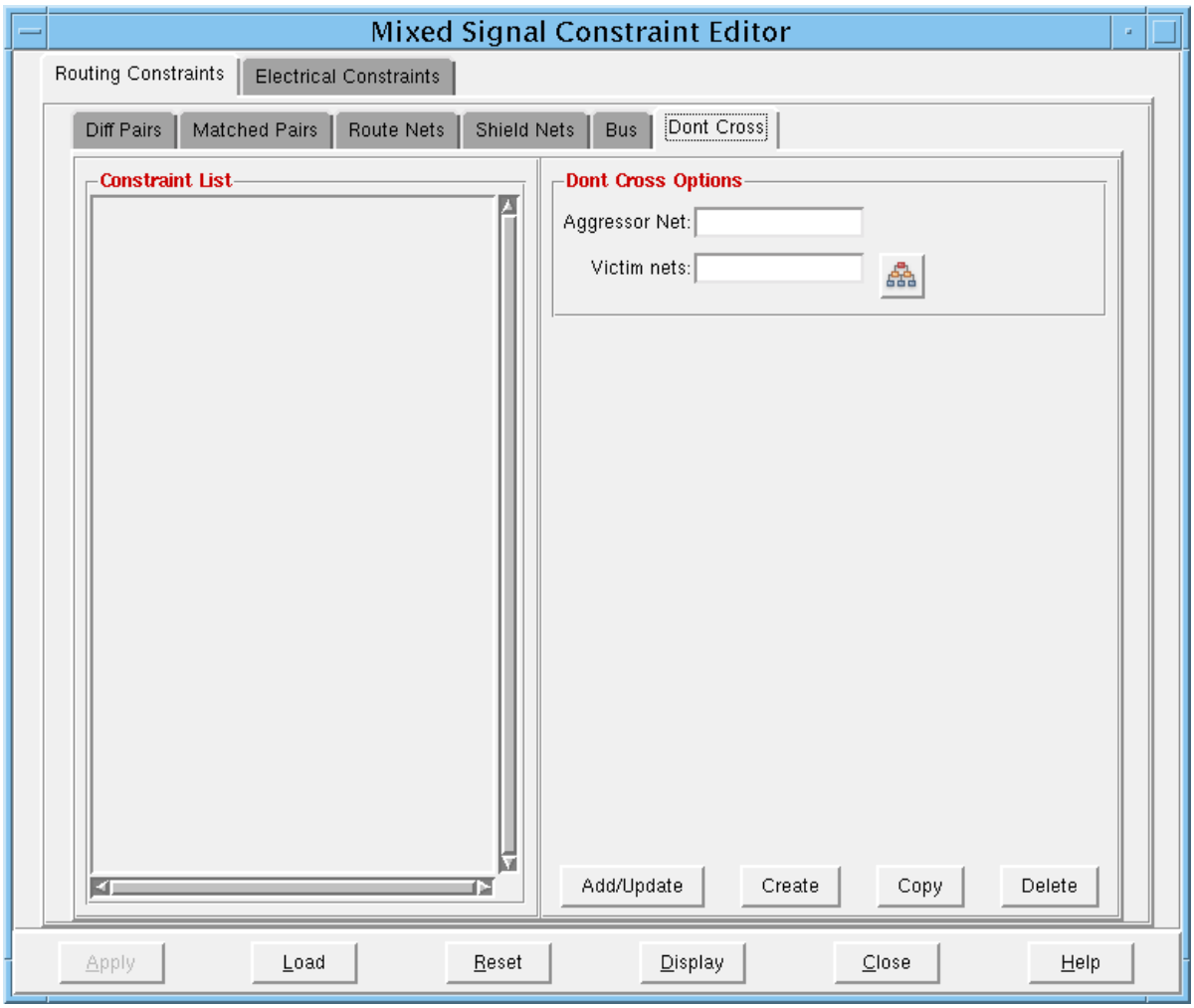
For information on the following topics, see “Using the Encounter Software in Mixed Signal Designs” in the *Encounter User Guide*:

- “Specialized Routing Techniques”
- “Using Routing Constraints”
- “Specialized Constraints and Keyword Descriptions”
- “Creating a Constraint File”
- “Editing a Constraint File”
- “Loading a Constraint File”

Dont Cross

Use the *Dont Cross* page to prohibit noise-generating nets from crossing noise-sensitive nets. Don't cross constraints are typically used to prevent digital signals from crossing analog nets.

➤ Choose *Tools – Mixed Signal – Constraints – Routing Constraints*, then select *Dont Cross*.



Dont Cross Fields and Options

Constraint List	Lists the nets with mixed signal constraints.

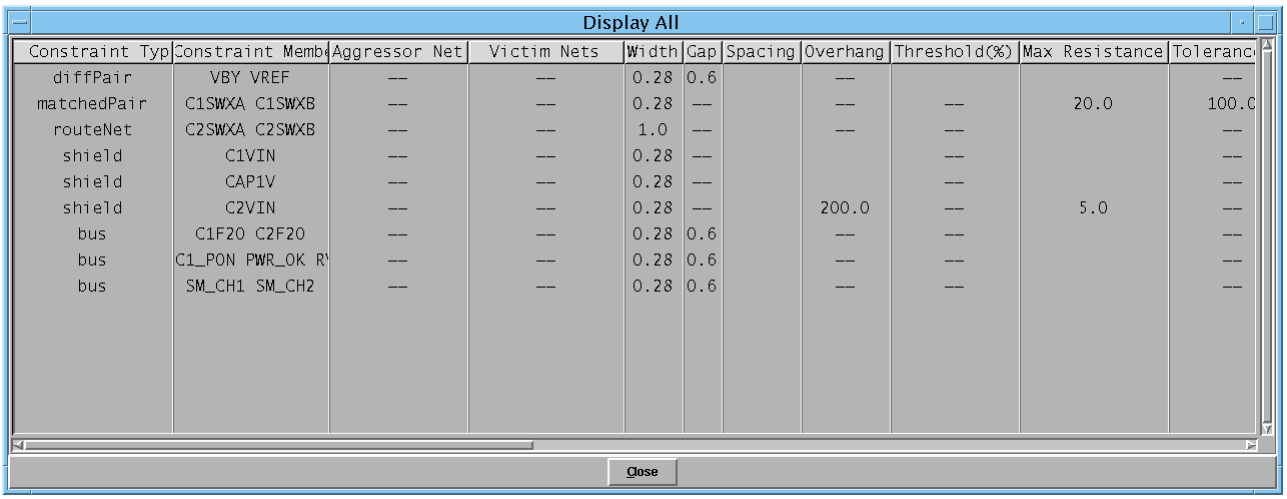
Dont Cross Options

Aggressor Net	Specifies a net that is likely to generate noise. If you specify a net, the software creates a constraint that prohibits the net from crossing nets specified as *Victim Nets*.
Victim Nets	Specifies the noise-sensitive nets that the specified *Aggressor Net* must not cross.
	Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Display All

Use the *Display All* page to display all the mixed signal routing constraints. You cannot use this page to edit the constraints.

➤ Choose *Tools – Mixed Signal – Constraints*, then click the *Display All* button.



Constraint Typ	Constraint Memb	Aggressor Net	Victim Nets	Width	Gap	Spacing	Overhang	Threshold(%)	Max Resistance	Toleranc
diffPair	VBY VREF	--	--	0.28	0.6		--			--
matchedPair	C1SWXA C1SWXB	--	--	0.28	--		--	--	20.0	100.0
routeNet	C2SWXA C2SWXB	--	--	1.0	--		--	--		--
shield	C1VIN	--	--	0.28	--			--		--
shield	CAP1V	--	--	0.28	--			--		--
shield	C2VIN	--	--	0.28	--		200.0	--	5.0	--
bus	C1F20 C2F20	--	--	0.28	0.6		--	--		--
bus	C1_PON PWR_OK R	--	--	0.28	0.6		--	--		--
bus	SM_CH1 SM_CH2	--	--	0.28	0.6		--	--		--

All Fields and Options

Type	Specifies the constraint type.
Constraint Members	Specifies the nets to which the constraint applies.
Width	Specifies the width of the constrained nets, measured in microns.
Shield Net	Specifies the special net used as a shield for the constrained net.
Shield Width	Specifies the width of the right and left *Shield Net*, measured in microns.
Gap	Specifies the target spacing between constrained nets, measured in microns. *Default:* `SPACING` or `SPACINGTABLE` value from the LEF file.
Max_Res	Specifies the maximum resistance of a net, measured in ohms. For more information, see *"Max Resistance"* on page 1624.

Tolerance

Specifies a tolerance factor for the maximum upper limit on the resistance.
Default: 20

Overhang

Specifies one-half of the difference between the width of the signal net and the width of the bottom and top shield nets.

Threshold

Specifies a value for the difference in target spacing, so the router attempts to meet the specified *Gap*, but does not create a violation if it misses the *Gap* by less than the threshold.
Default: 20%.

The threshold is calculated by using the following formula:

$$\text{Threshold} = \frac{\textit{Length of the longer net} - \textit{Length of the shorter net}}{\textit{Length of the shorter net}}$$

For example, if the constrained nets are 24 microns and 20 microns, the threshold would be calculated as (24 – 20) / 20 = 0.2 = 20%.

Max_Cap

Specifies the maximum routing capacitance of a net. The router changes layers, routing width, or path of the net to meet the constraint.

The Encounter software calculates capacitance using the following formula:

$$\text{Total capacitance} = \textit{area_capacitance} + \textit{side capacitance}$$

Min_Res

Specifies the minimum resistance of a net, measured in ohms.

Min_Cuts

Specifies the minimum number of via cuts.

Connect Supply

Connects the shield net to the supply.

Same Layer

Routes the bits of the bus on the same layers.

Coax Top

Specifies a shield net on the next higher metal layer in the same direction as the *Constraint Member* net.

Coax Bottom

Specifies a shield net on the next lower metal layer in the same direction as the *Constraint Member* net.

Coax Side

Specifies a shield net on the left and right sides of the *Constraint Member* net.

Electrical Constraints

Use the *Electrical Constraints* page to specify maximum IR drop constraints and to identify design objects as analog.

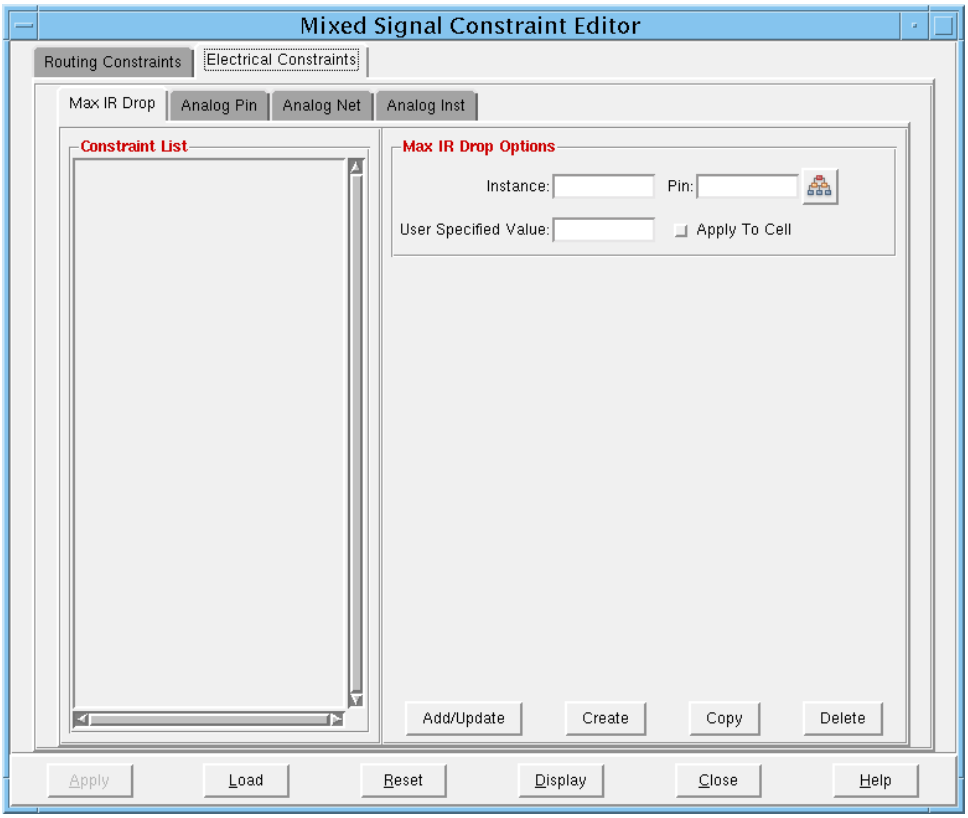
The *Electrical Constraints* page contains the following subpages:

- Max IR Drop on page 1652
- Analog Pin on page 1654
- Analog Net on page 1655
- Analog Inst on page 1656
- Display All on page 1657

Max IR Drop

Use the *Max IR Drop* page to specify maximum IR Drop constraints for design objects.

➤ Choose *Tools – Mixed Signal – Constraints – Electrical Constraints,* then select *Max IR Drop*.



Max IR Drop Fields and Options

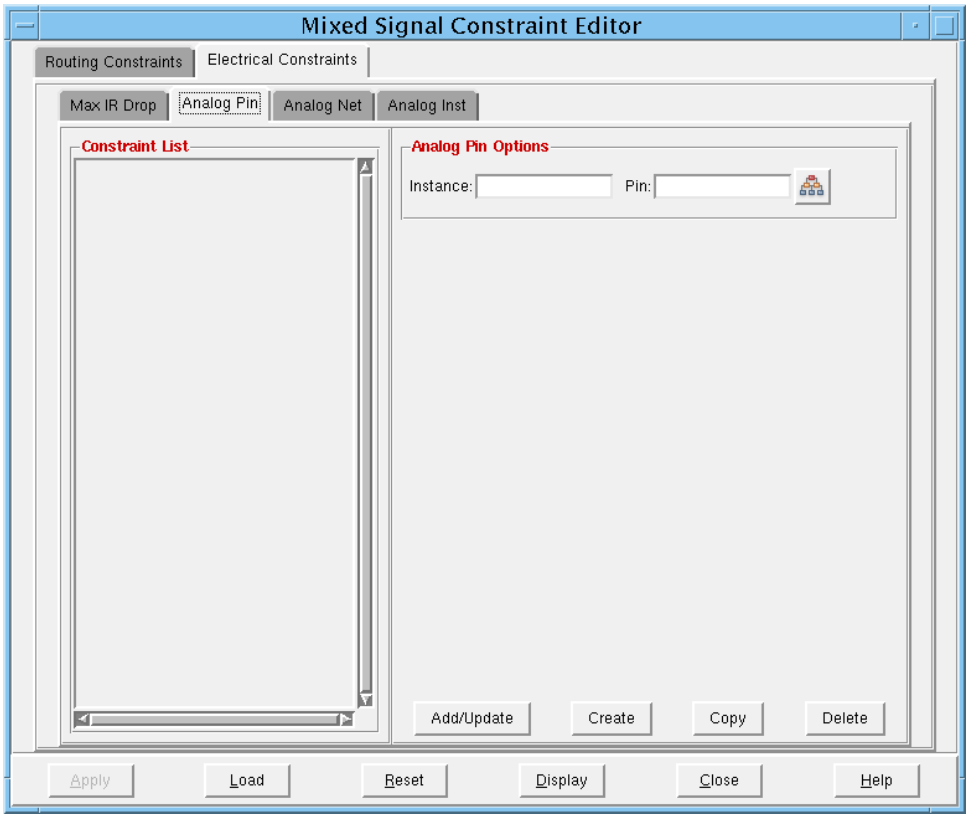
Constraint List	Lists the objects with mixed signal constraints.
Max IR Drop Options	
Instance	Specifies an instance of a cell.
Pin	Specifies a pin.

	Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.
User Specified Value	Specifies the maximum acceptable value for IR drop for the master cell, instance, or pin.
Apply To Cell	Applies the constraint to a cell master, not just to an instance of the cell.

Analog Pin

Use the *Analog Pin* page to identify analog instances or instance pins.

➤ Choose *Tools – Mixed Signal – Constraints – Electrical Constraints,* then select *Analog Pin*.



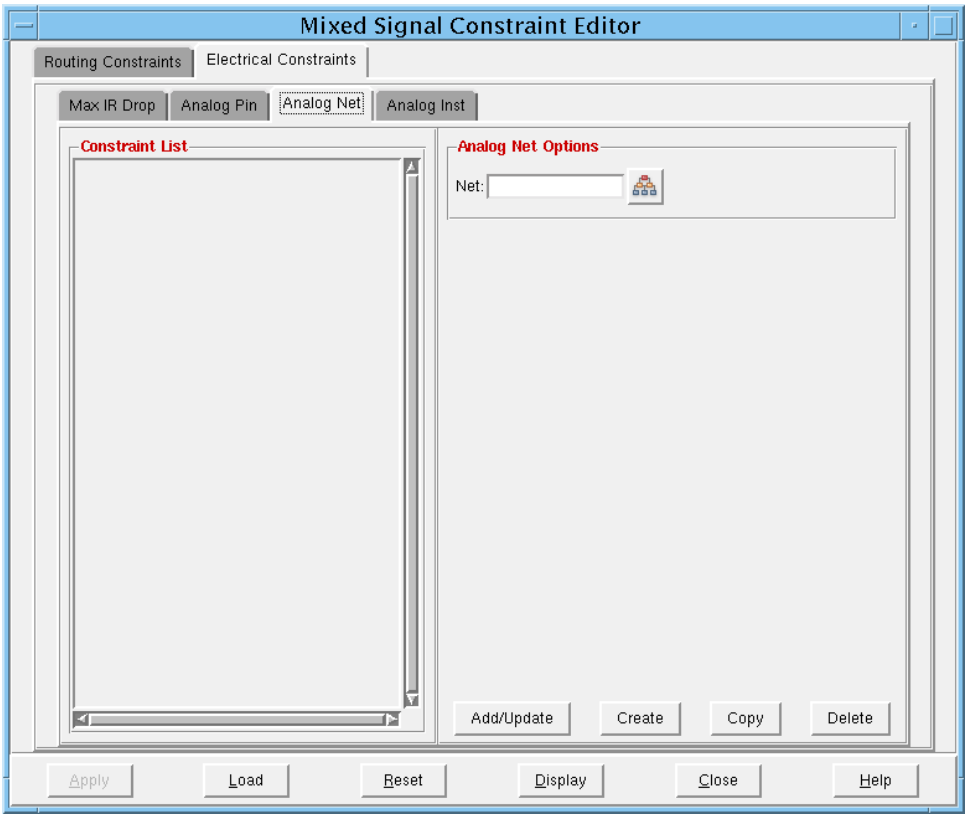
Analog Pin Fields and Options

Constraint List	Lists the nets with mixed signal constraints.
Analog Pin Options	
Instance	Specifies an instance to identify as analog.
Pin	Specifies a pin to identify as analog.
	Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Analog Net

Use the *Analog Net* page to identify analog nets.

➤ Choose *Tools – Mixed Signal – Constraints – Electrical Constraints,* then select *Analog Net*.



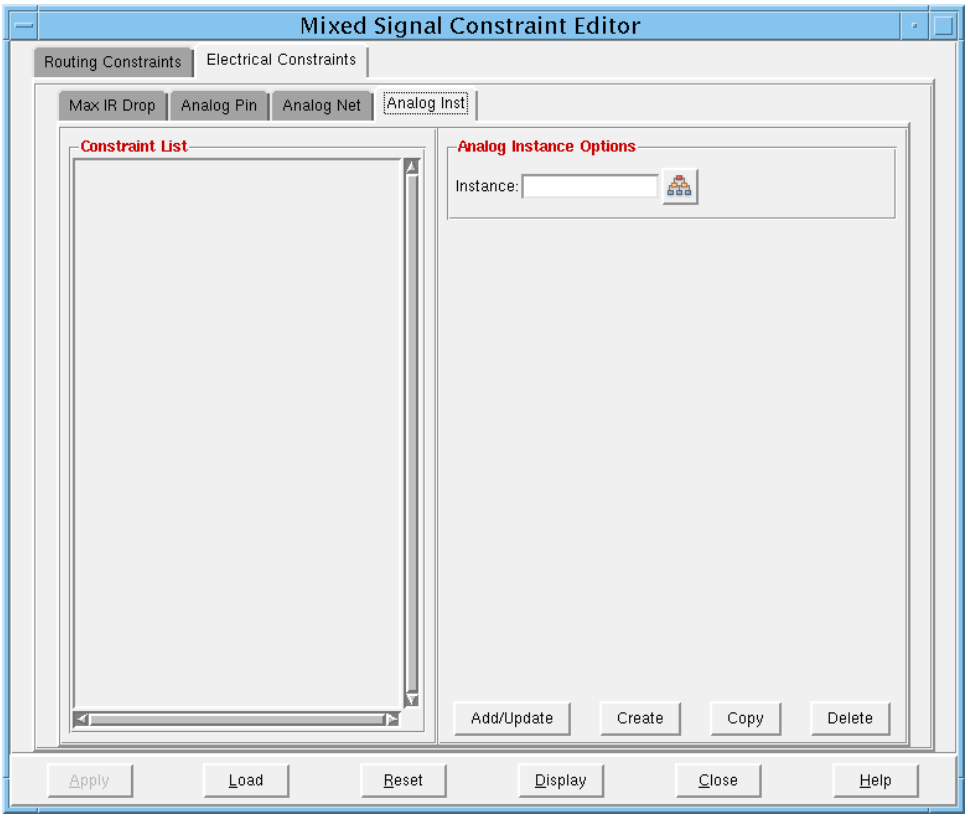
Analog Net Fields and Options

Constraint List	Lists the nets with mixed signal constraints.
Analog Net Options	
Net	Specifies a net to identify as analog.
	Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Analog Inst

Use the *Analog Pin* page to identify instances as analog.

➤ Choose *Tools – Mixed Signal – Constraints – Electrical Constraints,* then select *Analog Inst*.



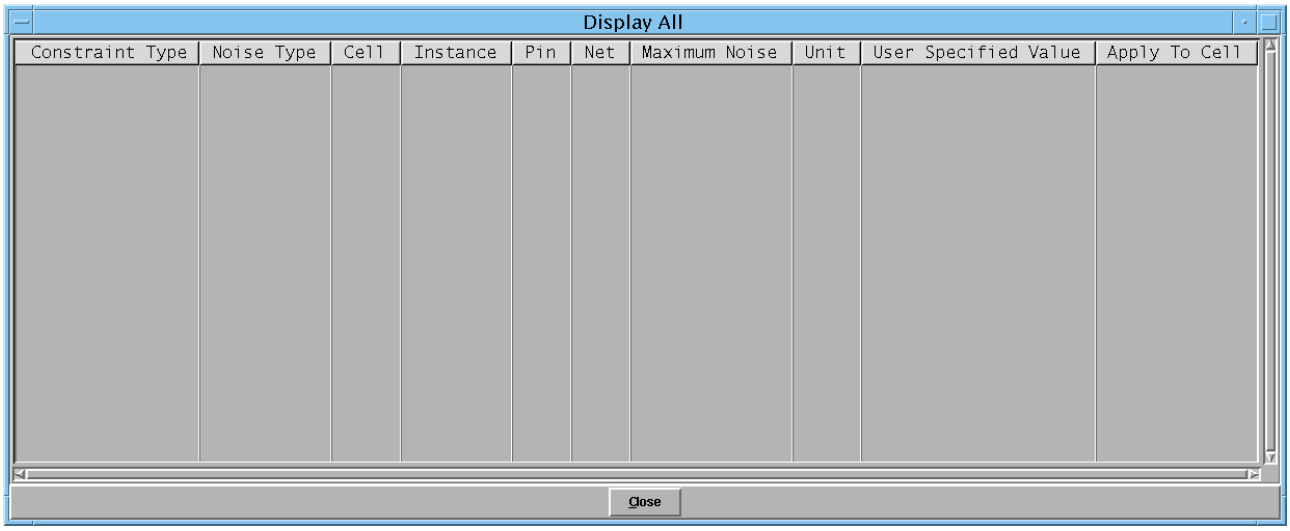
Analog Inst Fields and Options

Constraint List	Lists the nets with mixed signal constraints.
Analog Instance Options	
Instance	Specifies an instance to identify as analog.
	Opens the Select Constraint Member form, on which you can select objects to add, replace, or delete in the constraint editor. For information, see "Select Constraint Member" on page 1658.

Display All

Use the *Display All* page to display all the electrical mixed signal constraints. You cannot use this page to edit the constraints.

➤ Choose *Tools – Mixed Signal – Constraints – Electrical Constraints,* then click the *Display* button.



All Fields and Options

Constraint Type	Specifies the type of constraint.
Type	
Cell/Instance	Specifies a cell or instance as analog.
Net	Specifies a net as analog.
Pin	Specifies a pin as analog.

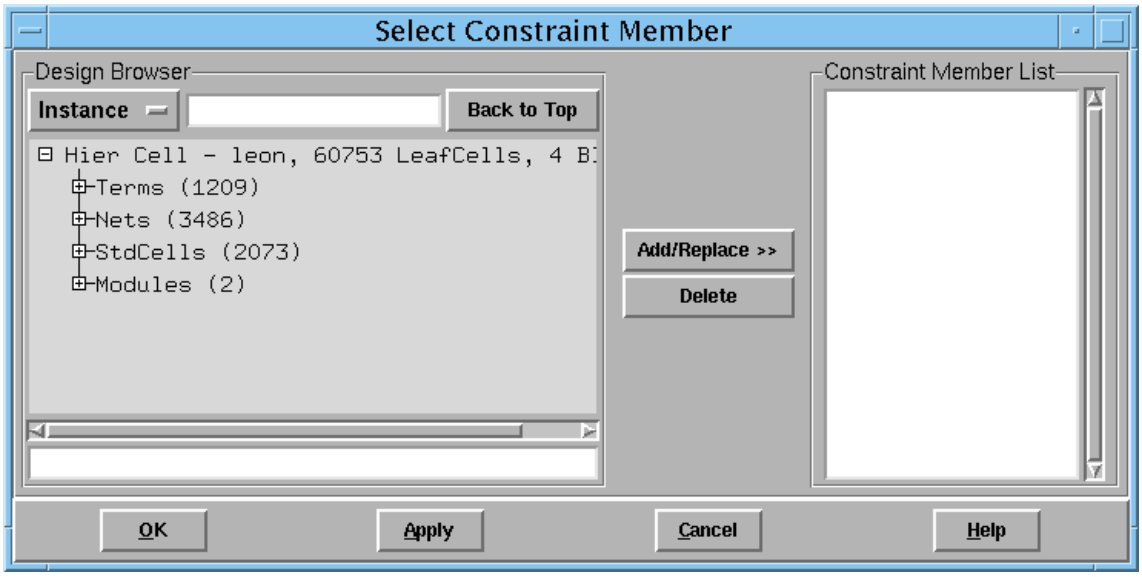
Select Constraint Member

Use the Select Constraint Member form to add, replace, or delete objects from mixed signal constraints.

1. Choose *Tools – Mixed Signal – Constraints*.
2. Click the *Hierarchy* button on the Mixed Signal Constraint Editor form if no constraints are listed in the *Constraint Members* text entry box. If nets are listed in the *Constraint Members* text entry box, first click the *Create* button to create a new constraint, then click the *Hierarchy* button.

   This is the *Hierarchy* button:

   The Selected Constraint Member form is displayed.



Select Constraint Member Fields and Options

Design Browser	The Select Constraint Member form is a design browser you can use to select objects to add, edit, or delete from the constraints.
Instance	Displays a list of instances in the browser window.

Net	Displays a list of nets in the browser window.
Group	
Cell	Displays a list of cells in the browser window.
Back to Top	Goes to the top of the hierarchy.
Add/Replace ...	Adds or replaces the selected objects in the display.
Delete	Deletes the selected objects from the display.
Constraint Member List	Displays a list of objects that are added to the *Constraint Members* text entry box on the Mixed Signal Constraint Editor form.

UltraSim

Use the UltraSim form to generate a command and the necessary files to run the Virtuoso® UltraSim™ Fast-SPICE simulator or run one of the following types of simulation using the simulator:

- Simulation of mixed-signal blocks
- Simulation of critical paths in a mixed signal design

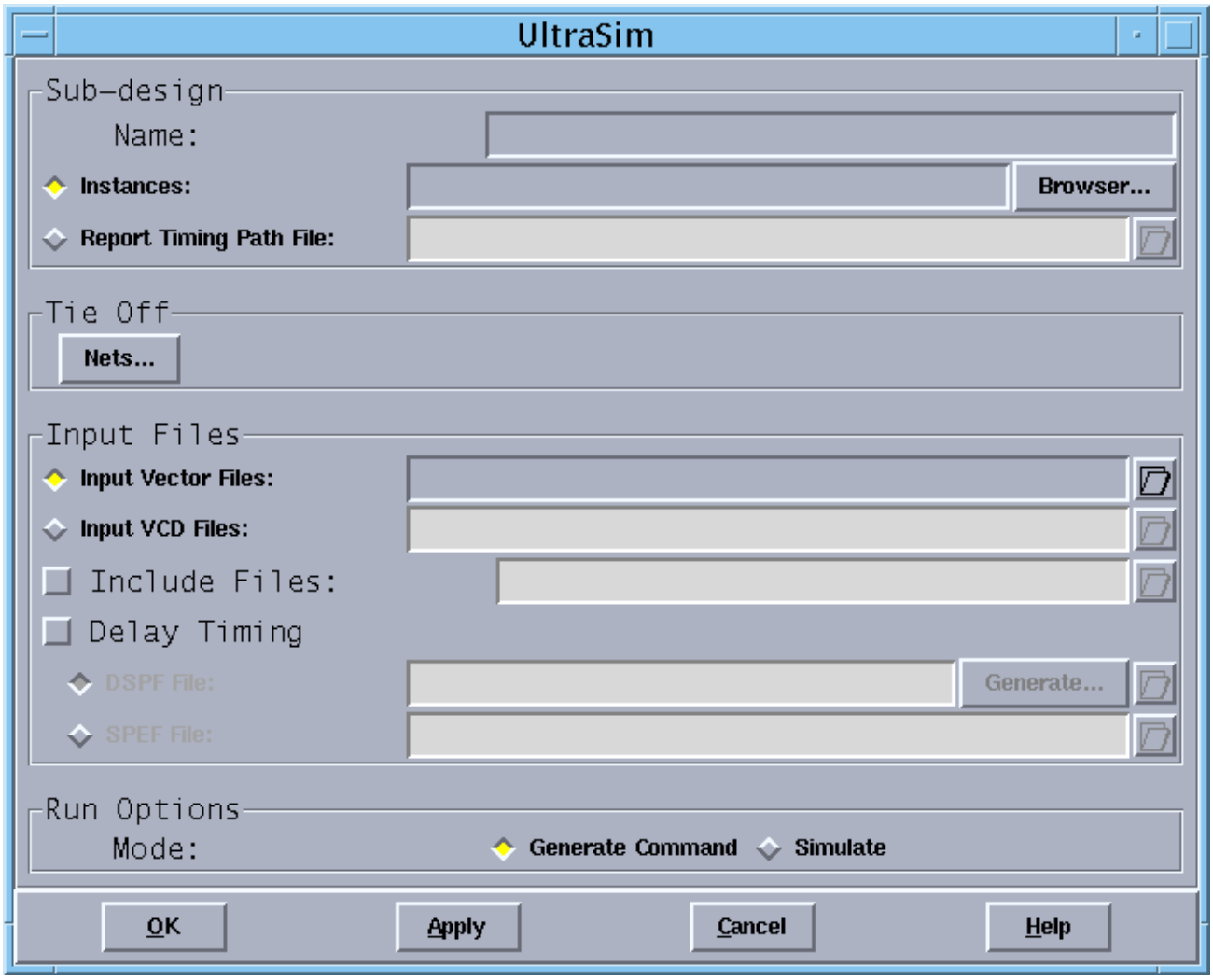
Before you run simulation, the design must be completely placed and routed and the resistance and capacitance extracted.

For information on using the Virtuoso UltraSim simulator, see the *Virtuoso UltraSim User Guide*.

The UltraSim form provides access to the following forms:

- Input Instances on page 1663
- Tie-Off Nets on page 1664

➤ Choose *Tools – Mixed Signal – Simulation*.



UltraSim Fields and Options

Sub-design	The instances, interconnect nets between the instances, and the I/O pins for the instances on which to run simulation.
Name	Specifies a name for the subdesign.
Instances	Specifies the components on which to run simulation. You can type the names of the components or click *Browser* to open the Input Instances form. Select the instances on the form. For information, see "Input Instances" on page 1663.

Report Timing Path File

Specifies the timing report file generated by the `report timing` command.

Tie Off

Nets

Opens the Tie Off Nets form, which lists the input nets in the subdesign. For more information, see "Tie-Off Nets" on page 1664.

Input Files

Input Vector Files

Specifies the input vector files to use for simulation.

Input VCD Files

Specifies value change dump (VCD) files to use for simulation.

Include Files

Specifies additional files necessary for simulation, such as SPICE models and library files.

Delay Timing

DSPF File

Specifies the standard parasitic format (SPF) or detailed standard parasitic format (DSPF) file. Click the *Generate* button to generate the file automatically.

SPEF File

Specifies the standard parasitic exchange format (SPEF) file.

Run Options

Mode

Generate Command

Creates all the necessary files to run simulation and saves the files in the `feusim/`*`subDesignName`* directory.

Does not run simulation.

Simulate

Creates the necessary files and runs simulation. Saves the files and the output in the `feusim/`*`subDesignName`* directory.

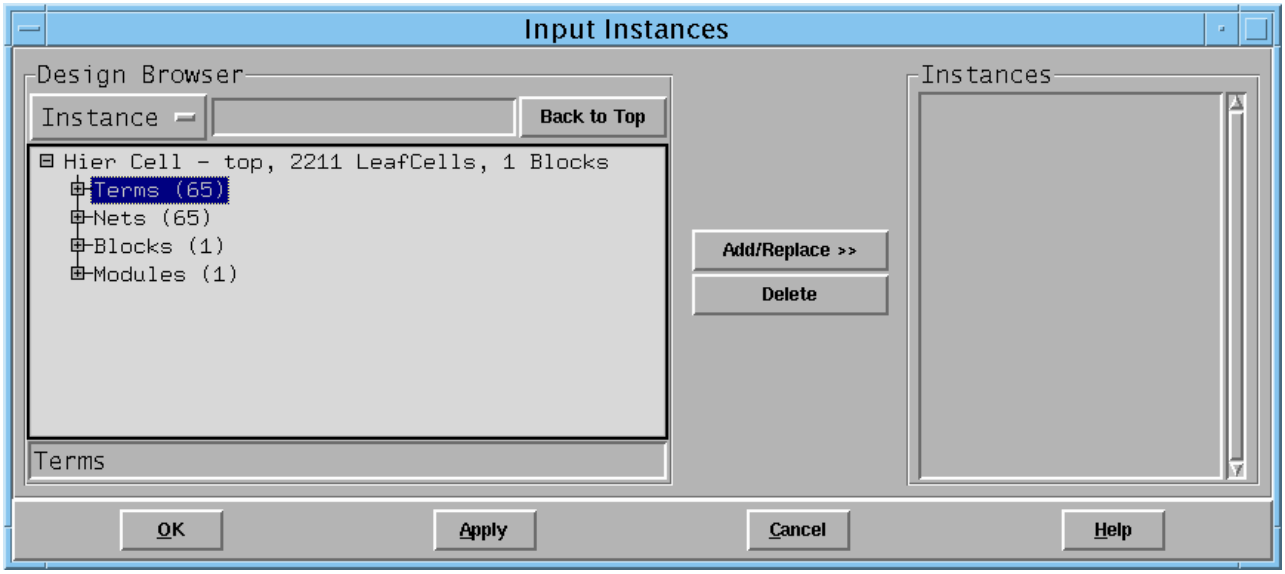
Related Text Commands

- `runUltraSim`

Input Instances

Use the Input Instances form to list the input nets in the subdesign.

1. Choose *Tools – Mixed Signal – Simulation*.
2. Click the *Browser* button on the UltraSim form.

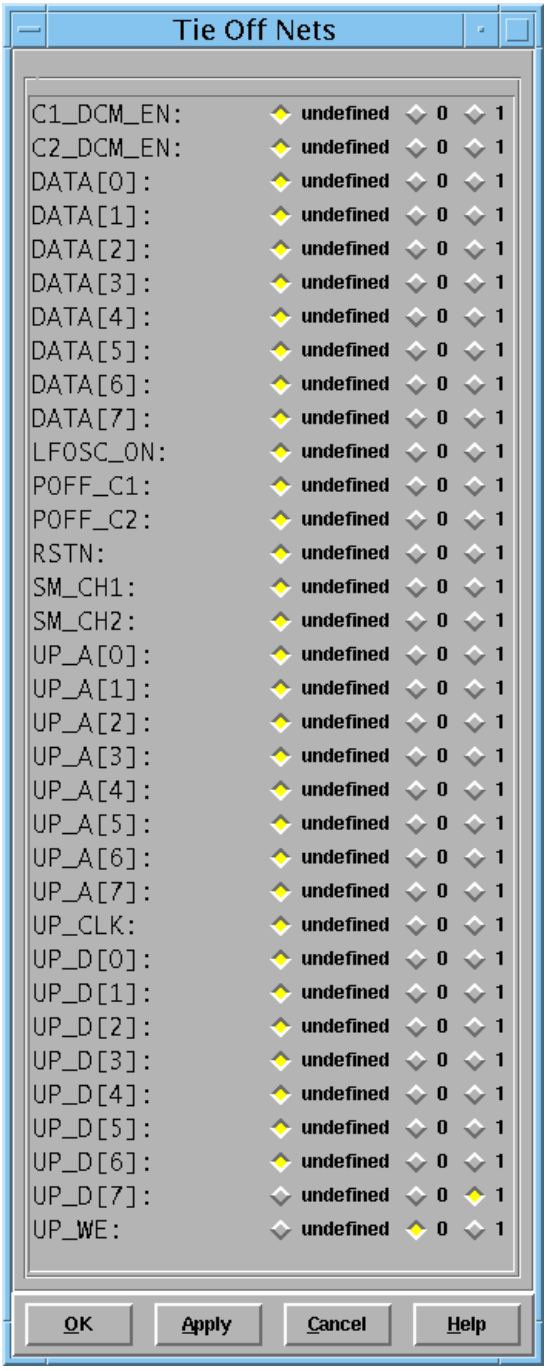


Input Instances Fields and Options

Design Browser	The Input Instance form is a design browser you can use to select objects to add, edit, or delete.	
	Instance	Displays a list of instances in the browser window.
	Net	Displays a list of nets in the browser window.
	Group	
	Cell	Displays a list of cells in the browser window.
Back to Top	Goes to the top of the hierarchy.	
Add/Replace	Adds or replaces selected objects to the Instances window.	
Delete	Deletes selected objects from the Instances window.	
Instances	Displays a list of objects to add to the subdesign.	

Tie-Off Nets

Use the Tie-Off Nets form to specify the value of the listed Tie-Off Nets.



Tie-Off Nets Fields and Options

The column on the left side of the form is the list of nets input nets in the subdesign.

undefined

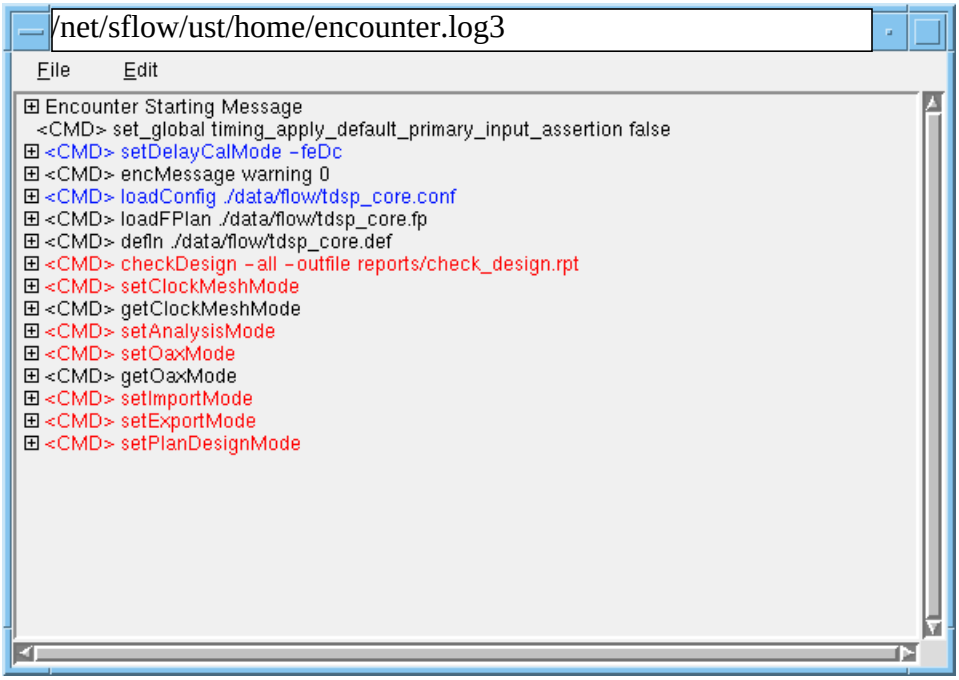
0

1

Log Viewer

Use the *Log Viewer* menu command to open up a log file in a separate console window for viewing.

➤ Choose *Tools – Log Viewer*, select the log file you want to view, then click *Open*.



The log file displayed contains [+] and [-] markers that expand and collapse command information, so that you can control how much detail you want to read. Additionally, log messages are color coded for easier identification: blue messages denote warnings, red messages denote errors.

By default, the software opens the current log file, and updates it in real time. If you specify a log file name, the software opens up the specified log file.

You can use the *Log Viewer* menu command more than once to view multiple log files in separate console windows simultaneously. However, you cannot open multiple versions of the current log file.

Menu Bar

- File Menu
- Edit Menu

File Menu

Open	Opens a log file in a separate console window.
Quit	Closes the log file.

Edit Menu

Find	Opens the Find in this log file form, which can be used to search the log file content for specific words and commands.
Expand All	Expands all command information in the log file.
Suppress All	Collapses command information in the log file.

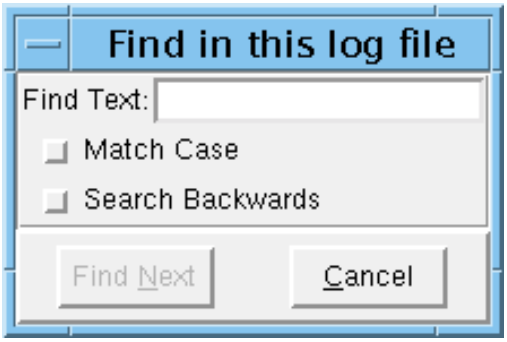
Related Text Commands

- `viewLog`

Find in this log file

Use the Find in this log file form to search the log file contents for strings, words, and commands.

➤ From the *Log Viewer* console window menu, choose *Edit – Find*.



Fields and Options

Find Text	Searches the log file contents for the specified text.
Match Case	Specifies that the software should search only for content that matches the specified text exactly.
Search Backwards	Searches backward through the log file.

Screen Capture

- Dump To GIF File on page 1670
- Screen Dump on page 1671
- Display Screen Dump on page 1672

Dump To GIF File

Use the Dump To GIF File menu command to save the snapshot of the current screen to a GIF file.

Screen Dump

Use the Screen Dump menu command to take a snapshot of the current screen. The file name is in timestamp format that shows when the snapshot was taken. The gzipped file, with the `.gz` extension, is listed in the text window.

➤ Choose *Tools – Screen Dump*.

Display Screen Dump

Use the Display Screen Dump menu command to view snapshots.

➤ Choose *Tools – Display Screen Dump*.

Express Flow Tool

Use the Express Flow Tool forms and menu commands to specify the options for setting up and running flow scripts.

To access the Express Flow Tool from the Encounter main menu:

1. Make sure your environment is set up to run the Express Flow Tool. The following environment variables are initialized to their default values. If your design environment requires other path names, be sure to set these variables before using the `launchEFT` command.

- `FMS_PATH` *`fms_path`*

  Specifies the search path for EFT. EFT automatically sets `FMS_PATH` and uses it internally.

- `FMS_STATUS_DB_PATH` *`db_path`*

  Specifies the path and name to the results database (steps.db). By default, this variable is set to `$PROJECT_ROOT/steps.db`. To point to another database, set the variable before you invoke EFT. For example:

  ```
  setenv FMS_STATUS_DM_PATH /home/user/steps.db
  ```

- `PROJECT_ROOT` *`path`*

  Specifies the directory location where EFT expects to find all files related to the design. EFT also creates the run directory at this location. The default is set to the current working directory. You can override the default by specifying a different `PROJECT_ROOT` *`path`* variable before you launch Encounter. For example:

  ```
  setenv PROJECT_ROOT /usr2/project/turboEagle
  ```

- `FMS_GEN_SCRIPTS`

  Specifies the directory where EFT writes the template body scripts. The default directory is set to `$PROJECT_ROOT/stepScripts/template`.

- `FMS_STEP_LOGS`

  Specifies the directory where EFT stores the log file for each step. The default directory is set to `$PROJECT_ROOT/`*`RUN`*`/logs/`*`flowName/id`*`.log`.

- `FMS_SAVE_RESTORE`

  Specifies the directory where the data is saved for each step. The default directory is set to `$PROJECT_ROOT/`*`RUN`*`/stepResults`.

- `FMS_SCRIPT_DIR`

  Specifies the directory where the master generated script is written. The default directory is set to `$PROJECT_ROOT/RUN`.

- `FMS_USER_SCRIPTS`

  Specifies the directory to look for the Tcl files for `importTclFlow`. The default directory is set to the current working directory.

2. Start Encounter.

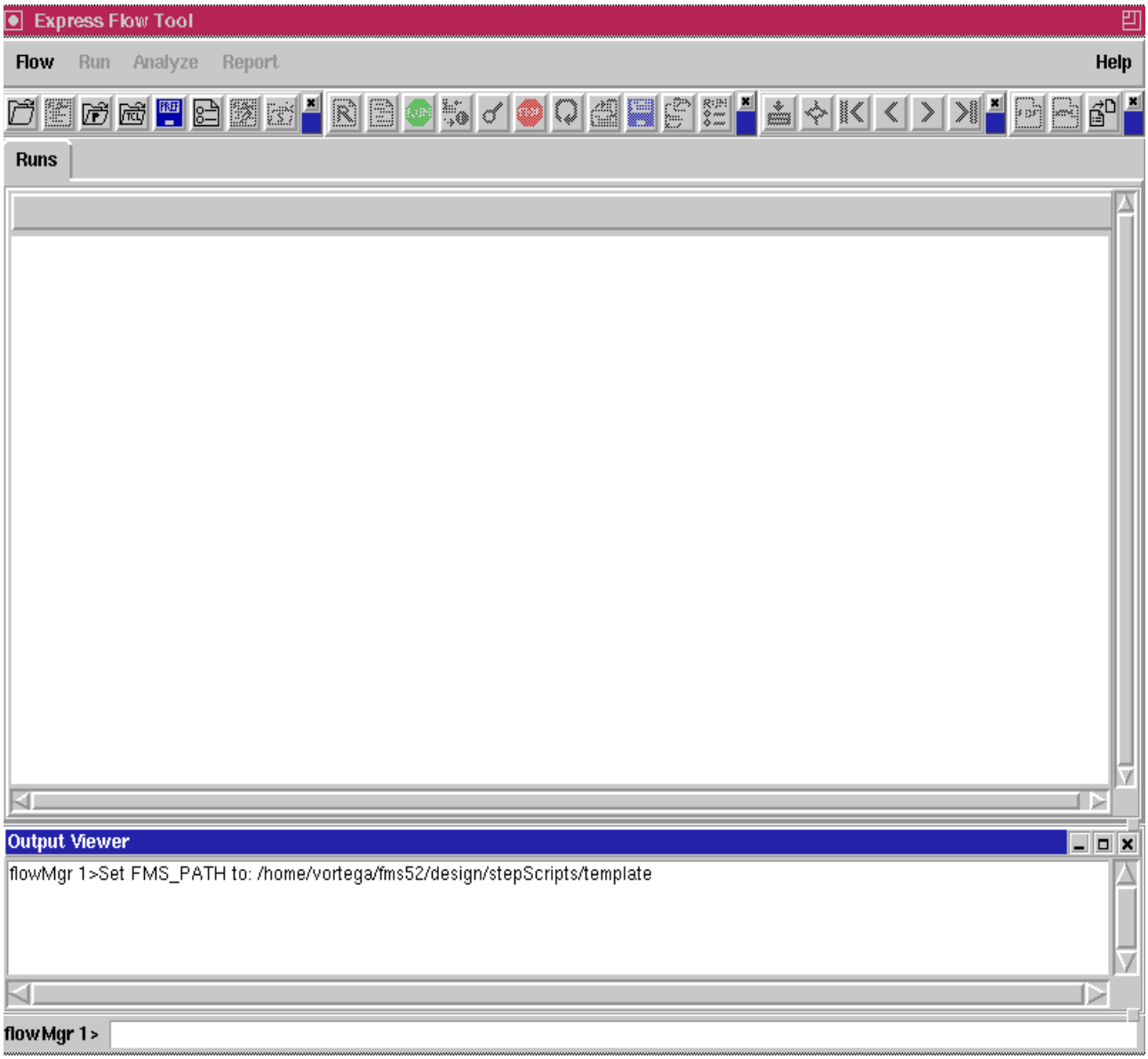
   The *Express Flow Tool* option appears at the bottom of the *Tools* pull-down menu.

3. Choose *Tools* from the main menu, and then select *Express Flow Tool* from the pull-down menu.

   The main EFT form appears.

   Note: EFT can also be run by typing `launchEFT` at the Encounter prompt.

Main EFT Form



Express Flow Tool Fields and Options

Flow	Presents a pull-down menu with the following options:	
	Import Tcl...	Presents a form where you can select and import a Tcl file. See Import Tcl on page 1683 for details.
	Select Flow...	Presents a form where you can select a subflow defined in the main flow class. See Select Flow on page 1685 for details.
	Load	Presents forms that allow you to select and load a preferences or a Tcl file. See Load Preferences File on page 1686 and Load Tcl File on page 1687 for details.
	Save	Presents a form that allows you to save preferences to a file. See Save Preferences on page 1689 for details.
	Preferences...	Presents a form that allows you to define the colors, view, and update intervals for the status display. See Preferences on page 1690 for details.
	Exit	Exits from the Express Flow Tool.
Run	Presents the pull-down menu for creating a run and generating and running flow scripts.	
	New...	Presents a form where you can specify the arguments for a new run of the flow. See New Run on page 1694 for details.
	Generate Script	Generates a set of scripts based on the flow and the run arguments for the current run.
	Run Script	Runs the generated script for the current run.
	Generate & Run Script	Runs a combination of the *Generate Script* and *Run Script* options for the current run.

	View Script...	Displays a browser form from which you can select and view generated script files for the current run. See View Script on page 1695 for details.
	Stop Script	Stops the currently running script based on the current run.
	Refresh	Redraws the display and updates results.
	Load State...	Displays a form from which you can select and load a state file applicable to the current run. See Load Run State File on page 1697 for details.
	Save State...	Displays a form that allows you to specify or select a file and the state options applicable to the current run. See Save Run State on page 1698 for details.
	Options...	Displays a form for selecting options for running the generated scripts applicable to the current run. See Options on page 1701 for details.
Analyze	Presents the pull-down menu with options related to selecting runs and applying status filters.	
	Specify Run...	Presents a from through which you can select the runs you want to view. By default, *All Runs* is selected. See Specify Run on page 1703 for details.
	View/Edit Status Conditions...	Presents a form to customize the status conditions for a step result. See View/Edit Status Condition on page 1705.
Report	Presents the pull-down menu for generating and viewing reports.	
	Write PDF...	Saves the results in PDF format. See Report – Write PDF on page 1720 for details.

	Write HTML...	Saves the results in HTML. See Report – Write HTML on page 1722 for details.
	Preferences...	Displays a form which allows you to select the fonts and format for the PDF and HTML output files. See Report Preferences – PDF and HTML on page 1724 for details.
Flow Definition Header Menu	Displays the name of the selected flow in the left-hand column of the display. If you right-click on the name of the flow, the following menu items are shown:	
	Set Current Run	Sets this run as the current run. Many of the Tcl commands can operate on the current run. The *Run* menu as well as the toolbar icons also operate on the current run.
	Delete	Removes this run from memory and the SQLite database. It also backs up the run directory on disk.
	Generate Script	Generates a set of scripts based on the flow and the run arguments for the current run.
	Run Script	Runs the generated script for the current run.
	Generate & Run Script	Runs a combination of the *Generate Script* and *Run Script* options for the current run.
	View Script…	Displays a browser form from which you can select and view generated script files for the current run. See View Script on page 1695 for details.
	Stop Script	Stops the currently running script based on the current run. **Note**: This is applicable only when running EFT in standalone mode.
	Refresh	Redraws the display and updates results.

	Load State...	Displays a form which allows you to select a state file to be loaded. See Load Run State File on page 1697 for details.
	Save State...	Displays a form which allows you to specify a file name and options for saving a state file for the flow. See Save Run State on page 1698 for details.
	Configure Flow...	Enables the flow steps to be used in the run. See Configure Flow on page 1699 for details. Also see Configure Run on page 1707.
	Options...	Displays a form for selecting options for running the generated scripts applicable to the current run. See Options on page 1701 for details.
	View Run Graph...	Displays the sequence of steps in a graphical format instead of a table format. This is useful for viewing steps that run in parallel. See View Run Graph on page 1718 for details.
Flow Step (left side)	Displays the names of the flow steps. If you right-click from a flow step, the following menu items are shown:	
	Re-Run Step	Allows you to re-run the selected step.
	Enable Step	Enables the selected step in the flow.
	Edit Step Parameters...	Brings up the variable viewer dialog. This can either be detached or added as part of the main EFT form.
	Reset to Step Choices	If you made changes to any parameters or values for a step, this option resets everything back to the default values.
Run Step (right side)	Shows the names of the selected flow steps for the run in the status color specified. If you select a step, the variables and values are displayed in the parameter pane. If you right click from a step, the following menu items are shown:	

	View Results	Displays a form showing the results of the selected step. See View Results on page 1712 for details.
	Edit Status Conditions	Displays a form allowing you to view and edit the status conditions for the selected step. See View/Edit Status Condition on page 1705 for details.
	Re-Run Step	Allows you to re-run the selected step.
	Enable Step	Enables and disables the selected step.
	Reset to Step Choices	If you made changes to any parameters or values for a step, this option resets everything back to the default values.
Script Tab	Displays links to the template body, head, and tail scripts associated with the selected step.	

Toolbar Commands

The most commonly used Express Flow Tool commands are accessible through the toolbar. This enables you to access a command quickly by just clicking on an icon.

Icon	Description
	Import Tcl Selects and imports a flow.
	Select Flow Selects a subflow defined in the main flow class.
	Load Preferences Selects and loads a preferences or Tcl file.
	Load Tcl File Loads a Tcl file. **Note**: The Tcl file is not parsed by EFT. The Tcl file may contain some Tcl commands that could be used to initialize EFT.
	Save Preferences Saves preferences to a file.

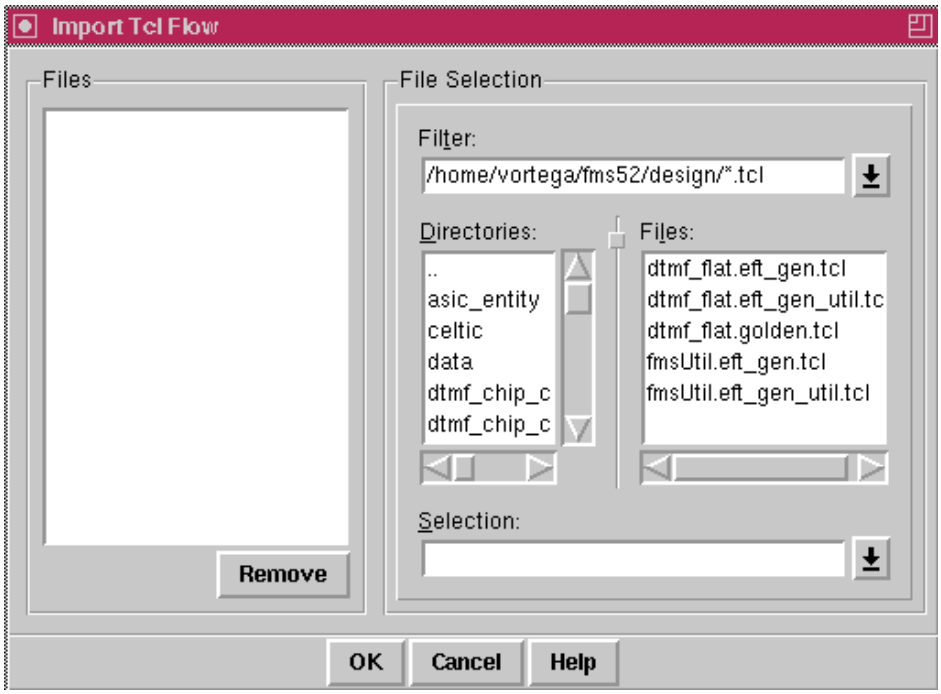
Icon	Description
	Edit/View Preferences Defines the colors, view, and update intervals for the status display.
	Configure Flow Enables the flow steps to be used in the run.
	Load Flow State Selects and loads a state form applicable to the current run.
	Create New Run Specifies the arguments for a new run of the flow.
	Generate "Current Run" Script Generates a set of scripts based on the flow and the run arguments for the current run.
	Run "Current Run" Script Runs the generated script for the current run.
	Generate & Run "Current Run" Script Runs a combination of the *Generate Script* and *Run Script* options for the current run.
	View "Current Run" Script Selects and views the generated script files for the current run.
	Stop "Current Run" Script Stops the currently running script based on the current run when running EFT in standalone mode.
	Refresh Redraws the display and updates the results.
	Load State To "Current Run" Selects and loads a state file applicable to the current run.
	Save "Current Run" State Saves a state file of the current run based on the save options specified.
	Run Options Selects options for running the generated scripts applicable to the current run.

Icon	Description
	Specify Run Selects the runs you want to view.
	View/Edit Status Condition Customizes the status conditions for a step result.
	First By default, shows the ten most recent runs that were initialized. This is used to view the first ten runs.
	Back Jumps back to show the previous ten runs.
	Next Jumps to the next ten runs.
	Last Jumps to the oldest ten runs.
	Write PDF Report Saves the results in PDF format.
	Write HTML Report Saves the results in HTML format.
	Report Preferences Selects the fonts and format for the PDF and HTML output files.

Import Tcl

Use the *Import Tcl Flow* form to select and import a Tcl file into the Express Flow Tool.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on the *Import Tcl* option.



Import Tcl Flow Fields and Options

Files	Displays the selected Tcl files.	
File Selection	*Filter*	Specifies the type of files to be shown.
	Directories	Displays the names of directory locations.
	Files	Displays a list of Tcl files in the selected directory. Importing the Tcl files requires double clicking on the specified files. Each Tcl file is treated as a subflow in the same flow class definition file. You can switch between the subflows by selecting *Select Flow* from the *Flow* menu.

Selection	Displays or allows you to type in the name of the file.

Related Text Commands

The following text commands provide equivalent or additional functionality:

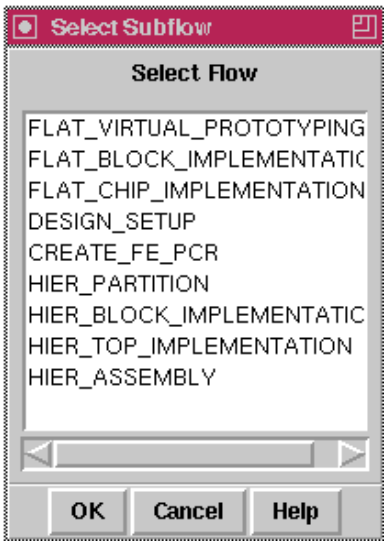
- `importTclFlow`

Select Flow

Use the *Select Subflow* form to select a defined subflow from the Express Flow Tool.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on the *Select Flow* option.

   Note: The first time a new Tcl file is loaded, a dialogue box will appear asking you to initialize a new run. Specify the name of the run directory to create the new run. If you do not specify the run directory, the current working directory (`$cwd`) is used.



Select Subflows Fields and Options

Select Flow	Displays the list of all available subflows in the flow class definition file.

Related Text Commands

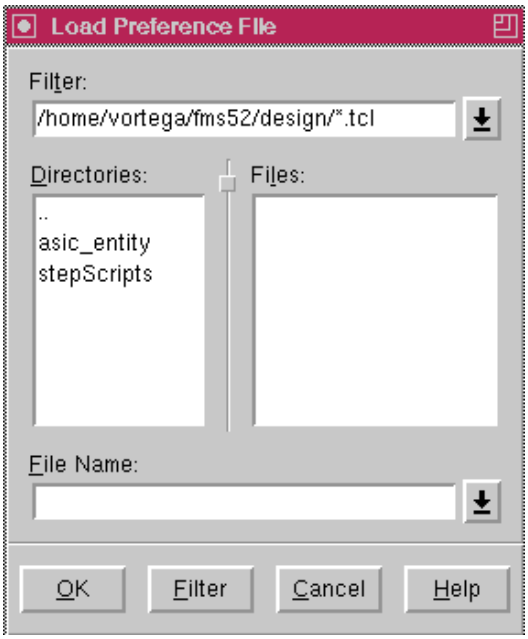
The following text command provides equivalent or additional functionality:

- `getFlows`
- `setCurrentFlow`

Load Preferences File

Use the *Load Preferences File* form to select and load a defined preferences file.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu, click on the *Load* option, and select *Preferences*.



Load Preferences Fields and Options

Filter	Specifies the type of files to be shown.
Directories	Displays the names of directory locations.
Files	Displays a list of files in the selected directory.
File Name	Displays or allows you to type in the name of the file.

Related Text Commands

The following text commands provide equivalent or additional functionality.

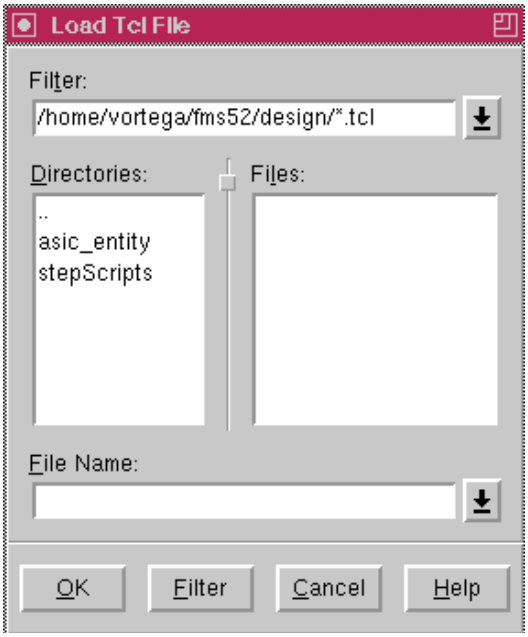
➤ At the Express Flow Tool prompt, enter the following command:

```
% source preference*FileName*.tcl
```

Load Tcl File

Use the *Load Tcl File* form to select and load a Tcl file. A Tcl file typically contains commands that work with the Express Flow Tool, help set up runs, or set up the environment to create arguments or variables

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu, click on the *Load* option, and select *Tcl File*.



Load Tcl Fields and Options

Filter	Specifies the type of files to be shown.
Directories	Displays the names of directory locations.
Files	Displays a list of files in the selected directory.
File Name	Displays or allows you to type in the name of the file.

Related Text Commands

The following text commands provide equivalent or additional functionality.

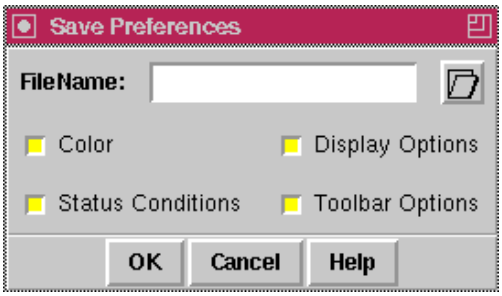
➤ At the Express Flow Tool prompt, enter the following command:

```
% source fileName.tcl
```

Save Preferences

Use the *Save Preferences File* form to specify a filename for saving defined preferences.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu, click on the *Save* option, and select *Preferences*.



Save Preferences Fields and Options

FileName	Specifies the name of the file for saving preferences. The browser icon allows you to select and update an existing file.
Color	Saves defined color preferences.
Display Options	Saves defined display options.
Status Conditions	Saves defined status conditions.
Toolbar Options	Saves defined toolbar options.

Related Text Commands

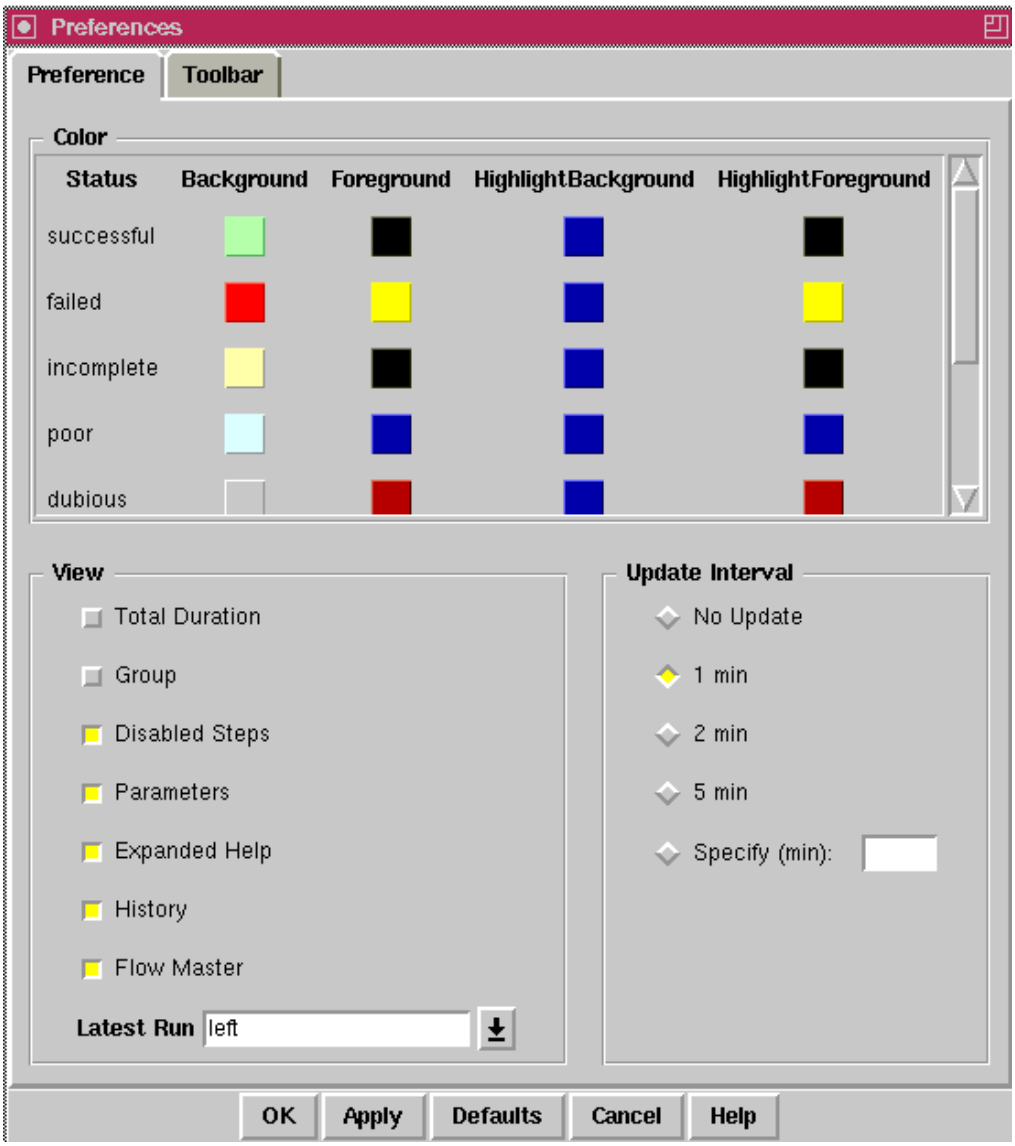
The following text commands provide equivalent or additional functionality:

- `getView`
- `setView`

Preferences

Use the *Preferences* form to assign colors to various status conditions and select the toolbar preferences.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on *Preferences*.



Preferences Fields and Options

Status	Lets you specify the color to assign to each of the possible status conditions. When you click on a color square, a form is displayed that allows you to change the color of the selection.	
	Successful	
	Failed	
	Incomplete	
	Poor	
	Dubious	
	Good	
	Disabled	
Background	Specifies the background color for each of the status conditions.	
Foreground	Specifies the foreground color for each of the status conditions.	
HighlightBackground	Specifies the highlight color to be used on the background for each of the status conditions.	
HighlightForeground	Specifies the highlight color to be used in the foreground for each of the status conditions.	
View	These options control the way information is presented in the Express Flow Tool form.	
	Command Prompt	Specifies whether or not to display the command prompt as part of the GUI. In the integrated version of EFT, the command prompt is part of the GUI.
	Total Duration	Specifies whether or not to display the total duration of the run in the run flow header.
	Group	Specifies whether or not to display group numbers.
	Disabled Steps	Specifies whether or not to display disabled steps. A step can only be turned off if the step of each run is disabled.

	Parameters	Specifies whether or not to display the parameter pane in the GUI.
	Expanded Help	Specifies whether or not to provide expanded help for steps.
	History	Specifies whether or not to display the *History* Tab.
	Flow Master	Specifies whether or not to display the flow master.
	Latest Run	Specifies whether runs are displayed from left to right or right to left. If you select left, the latest run information will appear in the leftmost position with previous flows to the right. Stretch the Express Flow Tool window horizontally to view multiple runs.
Update Interval	Allows you to select the number of minutes to wait before refreshing the status display. The default is one minute.	

The *Toolbar* tab shows all the toolbar icons that are available in the main EFT GUI. You can customize the toolbar by selecting the icons that you want to appear in the GUI.

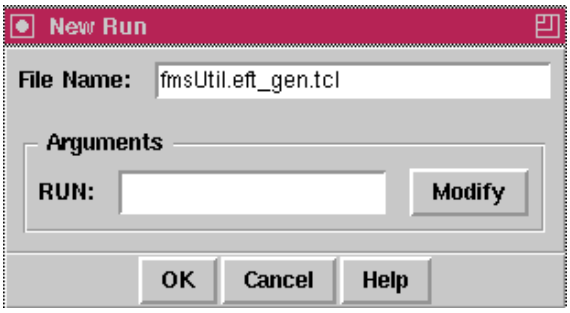
Related Text Commands

There are no related text commands for this functionality.

New Run

Use the *New Run* form to specify the *RUN* argument that defines a new run of the flow.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *New* option.



New Run Fields and Options

File Name — Specifies the default name for the master file.

Arguments — The following *RUN* argument is used to define a new run of the flow.

- *RUN:* — Specifies the name of the new run. By default, *RUN* is set to the current working directory. Use the *Modify* button to specify a directory other than the current working directory. For example, you can select *Modify*, then specify *RUN* as `run1`. The run would then take place in the `run1` directory instead of the current working directory.

Related Text Commands

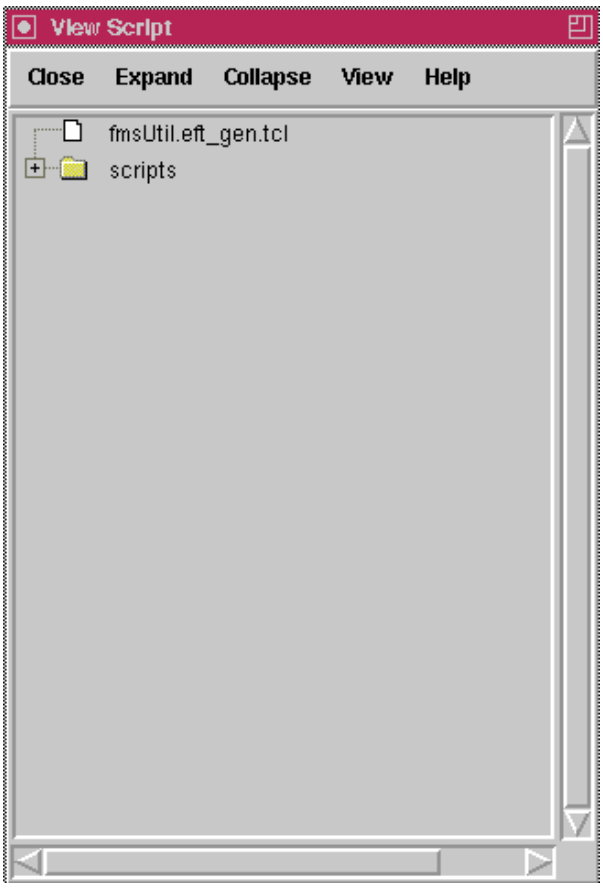
The following text commands provide equivalent or additional functionality:

- `createRun`

View Script

Use the *View Script* form to select and view the scripts generated by the Express Flow Tool.

1. Choose *Tools – Express Flow Tool.*
2. Initialize a run and generate a script.
3. Select the *Run* menu, and click on the *View Script* option.
4. Click on the *Expand* menu command to see the list of scripts generated for each flow step.



View Script Fields and Options

Close	Closes the *View Script* form.
Expand	Expands the flow steps and displays file names for each of the scripts.

Collapse	Collapses the expanded view.	
View	Filters and displays the various scripts available for each step.	
	Validate Scripts	The validate scripts gather metrics from the log or report file after a step completes successfully. These metrics are stored in the `steps.db` file and are displayed in the *View Results* form.
	Body Scripts	The Body scripts contain the command sequence required to run the tool.

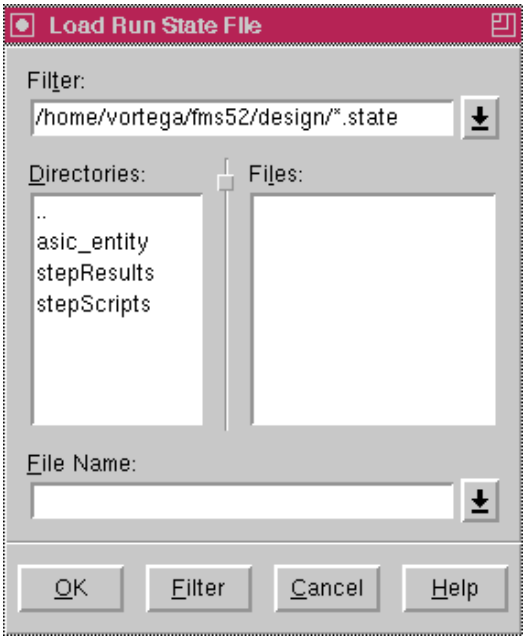
Related Text Commands

There are no related text commands for this functionality.

Load Run State File

Use the *Load Run State File* form to select and load a state form applicable to the current run.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Load State* option.



Load Run State File Fields and Options

Filter	Specifies the type of files to be shown.
Directories	Displays the names of directory locations.
Files	Displays a list of files in the selected directory.
File Name	Displays or allows you to type in the name of the file.

Related Text Commands

The following text command provides equivalent or additional functionality:

- `loadStateFile`

Save Run State

Use the *Save Run State* form to specify or select a file and the state options applicable to the current run.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Save State* option.

Save Run State Fields and Options

Filename	Allows you to specify a filename for saving the state file. Click on the browser icon next to the field to search for existing files. If a filename is specified, it is saved in the run directory. To save the sate file in a different directory, specify the complete path.
Changes Only	Saves the state file which includes changes from the default flow.
Parameters Only	Saves only changed parameters.
All Values	Saves all values whether or not they have changed.

Related Text Commands

The following text command provides equivalent or additional functionality:

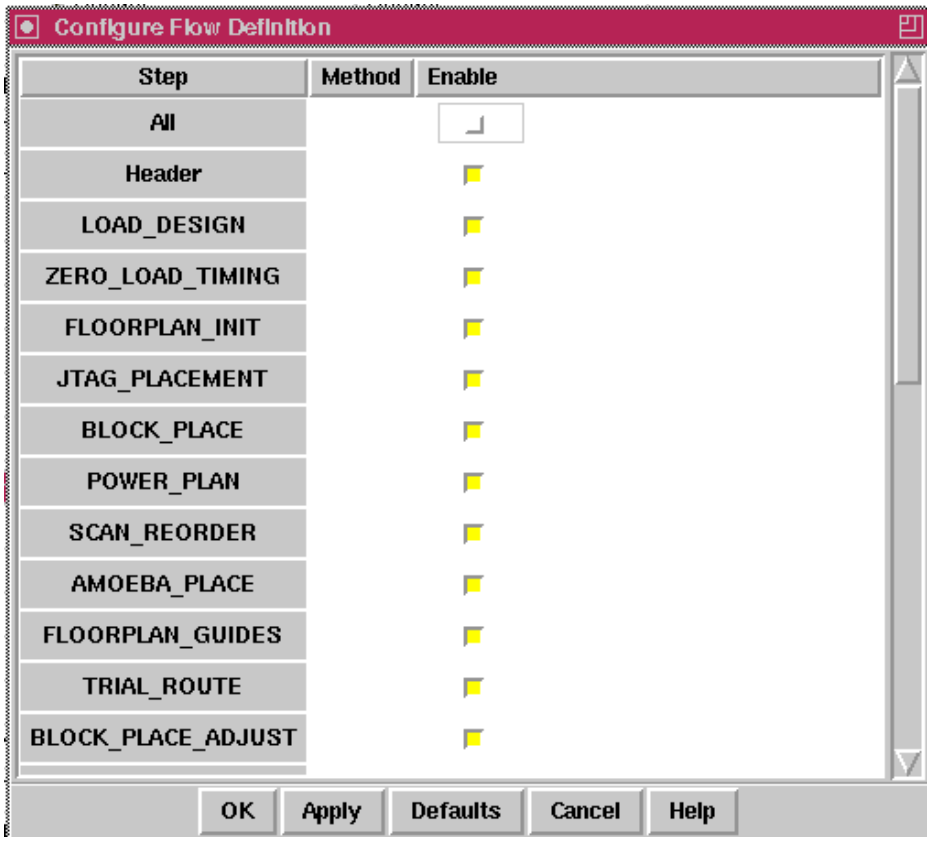
- `saveStateFile`

Configure Flow

Use the *Configure Flow Definition* form to enable the flow steps to be used in the run.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on the *Import* option.
3. Import a flow, right-click on the name of the flow, and select *Configure Flow* from the menu.

Note: The *Configure Flow Definition* form is turned off by default. You can enable this form by choosing *Flow – Preferences* and selecting *Flow Master*. See Configure Run on page 1707 to configure the runs.



Configure Flow Definition Fields and Options

Steps	Displays the names of all the steps in the selected flow.

Enable	Allows you to enable or disable steps. Click on the box to toggle individual steps. To enable or disable all the steps, click on the enable box for *All* methods.

Related Text Commands

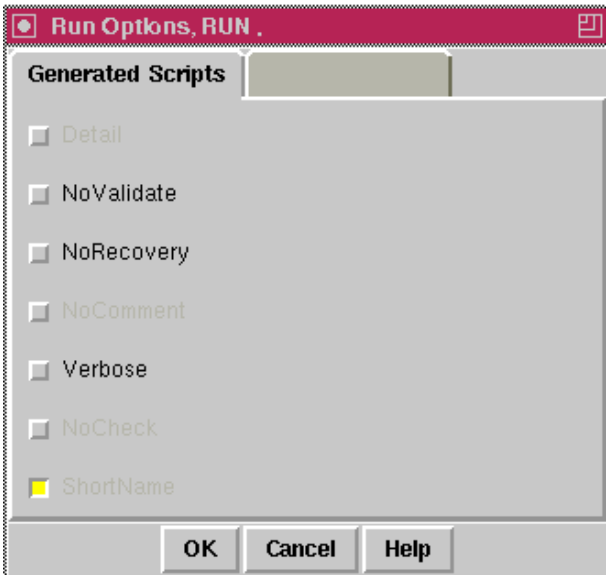
The following text commands provide equivalent or additional functionality:

- `disableSteps`
- `enableSteps`
- `rerun`

Options

Use the *Options* form to specify the options for the scripts generated by the Express Flow Tool or to specify a submit prefix for a run of the flow.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, select *Options,* and then click on the *Generated Scripts* or *Job Submission* tab.



Run Options Fields and Options

Generated Scripts Specifies the options for the scripts generated by the Express Flow Tool.

NoValidate This option removes the validate statement from the begin and end scripts. It does not execute the `stepName.validate.tcl` script for that step. No errors or warnings are recorded.

NoRecovery If you select this option, checkpoint recovery is not enabled. If you run the first part of a flow and then subsequently want to run all the steps in the flow, this option causes the script to start from the beginning rather than from where you left off.

Verbose	This option displays all generated begin and end scripts.

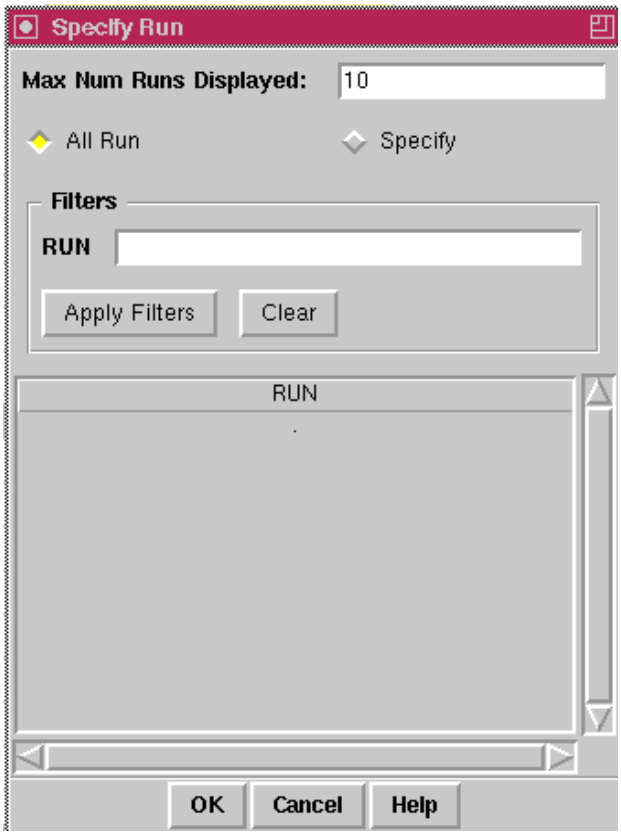
Related Text Commands

There are no related text commands for this functionality.

Specify Run

Use the *Specify Run* form to select the runs of the flow for which you want to see the status conditions.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Analyze* menu, and click on the *Specify Runs* option.



New Run Fields and Options

Max Num Runs Displayed	
	Specifies the maximum number of runs to display in the results area. The default is set at 10, but you can enter a different value.
All Run	Selects all runs for comparison.
Specify	Allows you to select from the list of available runs.

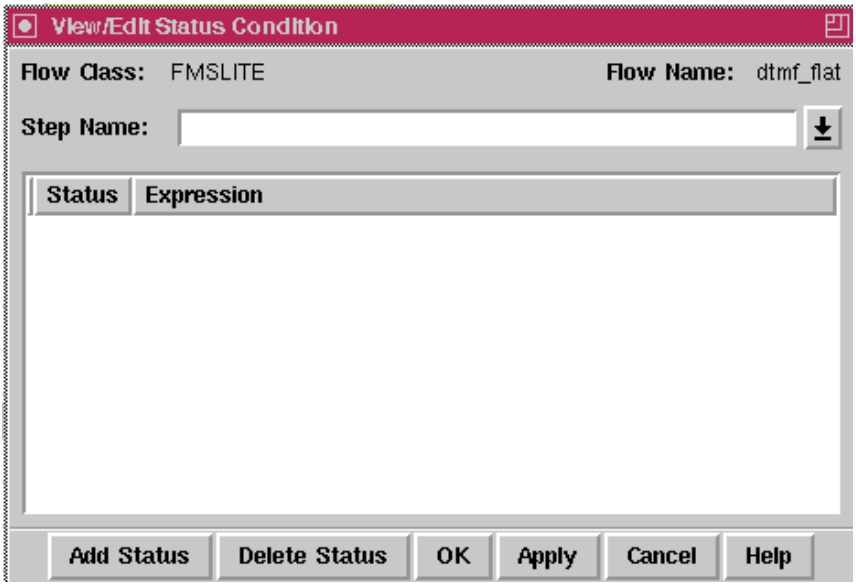
Related Text Commands

There are no related text commands for this functionality.

View/Edit Status Condition

Use the *View/Edit Status Condition* form to view, define, or modify the status conditions that determine what color are used to display results.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Analyze* menu, and click on the *View/Edit Status Conditions* option.



View/Edit Status Condition Fields and Options

Flow Class	Displays the name of the flow class.
Flow Name	Displays the name of the subflow.
Step Name	Displays the name of the step for which you want to view or edit the status conditions.
Status	Allow you to view or select a status condition for the step. Click on the arrow icon to see the list of status conditions to select from.
Expression	Displays the currently defined status conditions or allows you to create or modify a status condition.
Add Status	Adds a new or edited status condition.
Delete Status	Deletes the selected status condition and its expression.

Related Text Commands

The following text commands provide equivalent or additional functionality:

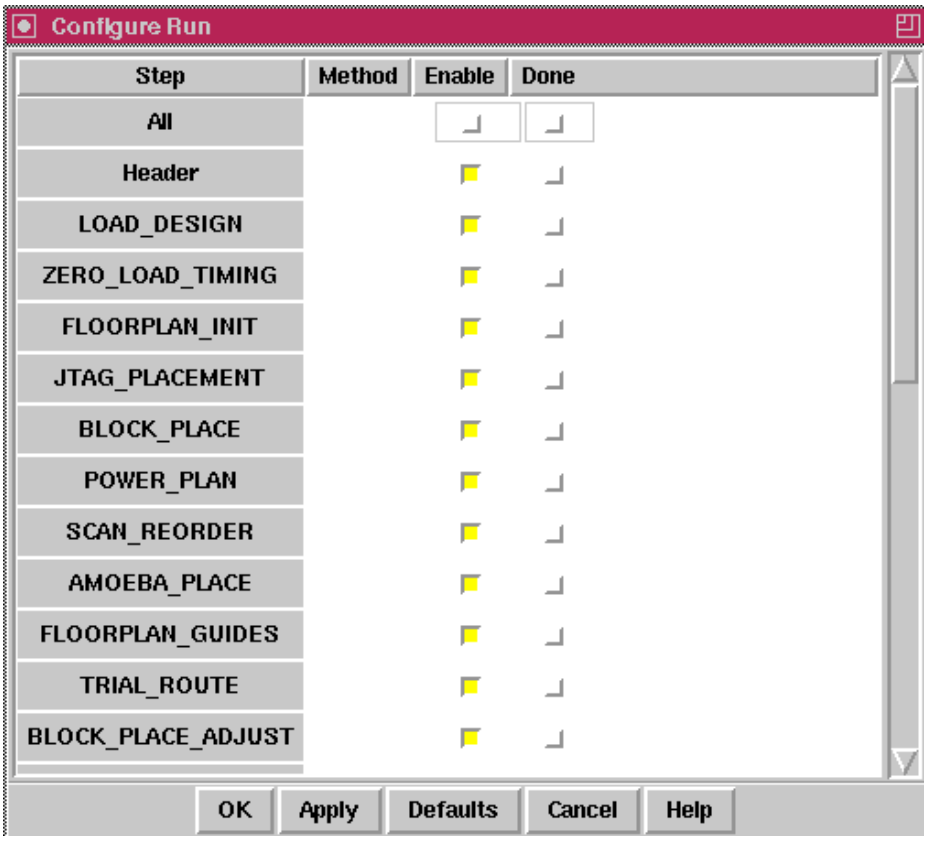
- `setStepStatusFilter`
- `getStepStatusFilter`
- `resetStepStatusFilter`

Configure Run

Use the *Configure Run* form to enable the flow steps to be used in the run.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on the *Import Tcl* option.
3. Import a Tcl file and create a run.
4. Right-click in the box containing the name of the run, and select *Configure* from the menu.

Note: The *Configure Run* form is default for EFT. See Configure Flow on page 1699 to enable the *Configure Flow Definition* form.



Configure Flow Fields and Options

Steps	Displays the names of all the steps in the selected run.

Enable	Allows you to enable or disable steps. Click on the box to toggle individual steps. To enable or disable all the steps, click on the enable box for *All* methods.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `disableSteps`
- `enableSteps`
- `rerun`

Generate Script

The *Generate Script* command on the Express Flow Tool *Run* menu creates a script based on the arguments you specified for the new run.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Generate Script* option. For this option to be available, you must first define a new run or reinitialize a step of an existing run.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `generateScript`

Run Script

The *Run Script* command on the Express Flow Tool *Run* menu runs the latest version of the generated script in the current RUN.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Run Script* option. For this option to be available, you must first define a new run and generate a script.

To rerun a step of an existing run:

1. Right click on the step and select *Rerun Step*.
2. Use appropriate menu selections generate and run the script.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `runScript`

Generate & Run Script

The *Generate & Run Script* command on the Express Flow Tool *Run* menu generates a script and then runs it. This combines the functionality of the *Generate Script* and *Run Script* commands defined earlier.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Generate & Run Script* option. For this option to be available, you must first define a new run.

To rerun a step of an existing run:

1. Right click on the step and select *Rerun Step*.
2. Use appropriate menu selections generate and run the script.

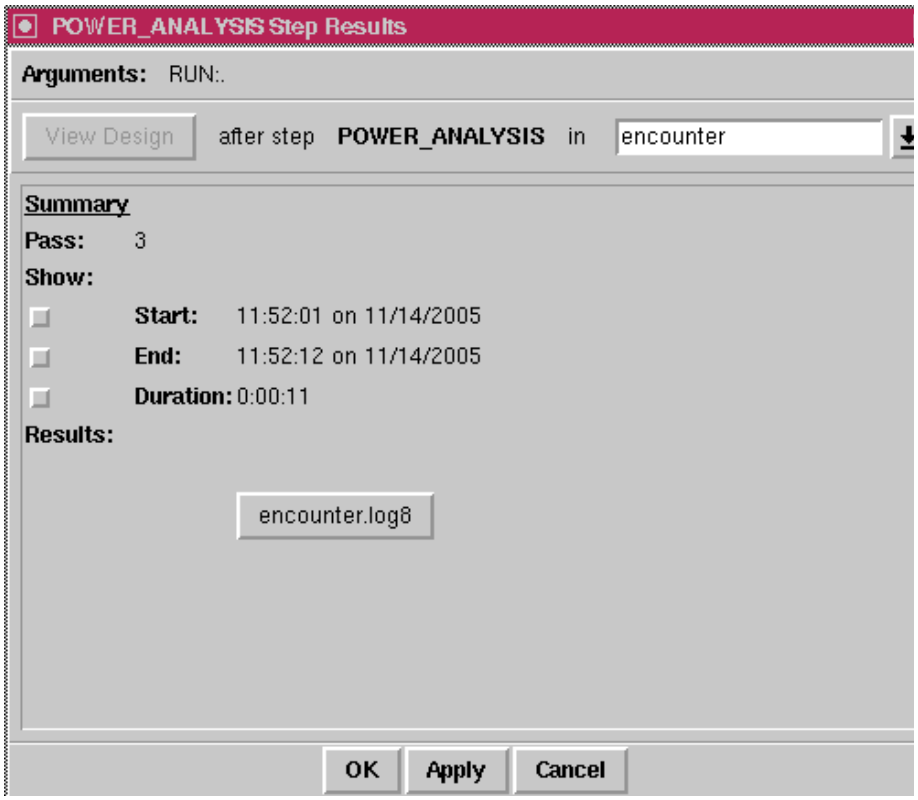
Related Text Commands

- `generateScript`
- `runScript`

View Results

Use the *View Results* form to see the results for a particular step in the flow. You can also view the design at that step in the flow as well as the log files associated with that run for that step.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Flow* menu and click on the *Import* option.
3. Import a flow and create and run a script.
4. Right-click in a box containing the name of a completed step, and select *View Results* from the menu.



View Results Fields and Options

Arguments	Displays the *RUN* arguments for the flow.
Show:	Displays the statistics regarding the start and stop times, and the length of the run. The check boxes allow you to see the data in the Express Flow Tool results area.
Results:	Displays a summary of results for the selected step. The check boxes allow you to see the data in the main Express Flow Tool window.
Log File button	Displays the name of the log file for the selected step. Click on the button to display the entire log for the step in a separate window.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `getCapturedMetrics`
- `getMetricValue`
- `reportMetricValues`

Stop Script

Note: This functionality is only available in the standalone version of EFT, not the integrated version.

The *Run Script* command on the Express Flow Tool *Run* menu cancels the currently running flow script for the current run along with any subordinate scripts.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Stop Script* option. For this option to be available, there must be a script currently running.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `stopScript`

Refresh

The *Refresh* command on the Express Flow Tool *Run* menu updates the results and redraws the Express Flow Tool user interface.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Run* menu, and click on the *Refresh* option.

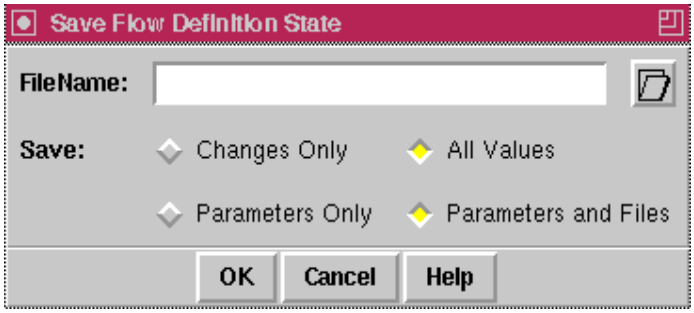
Related Text Commands

There are no related text commands for this functionality.

Save Flow Definition State

Use the *Save Flow Definition State* form to specify a file name and options for saving a state file for the flow.

1. Choose *Tools – Express Flow Tool.*
2. Import a flow.
3. Right click from the box containing the title of the imported flow and select the Save State option.



Load Flow Definition State Fields and Options

Filename	Allows you to specify a filename for saving the state file. Click on the browser icon next to the field to search for existing files. If a filename is specified, it is saved in the PROJECT_ROOT directory. To save the state file in a different directory, specify the complete path.
Changes Only	Saves the state file which includes changes from the default flow.
Parameters Only	Saves only changed parameters.
All Values	Saves all values whether or not they have changed.

Related Text Commands

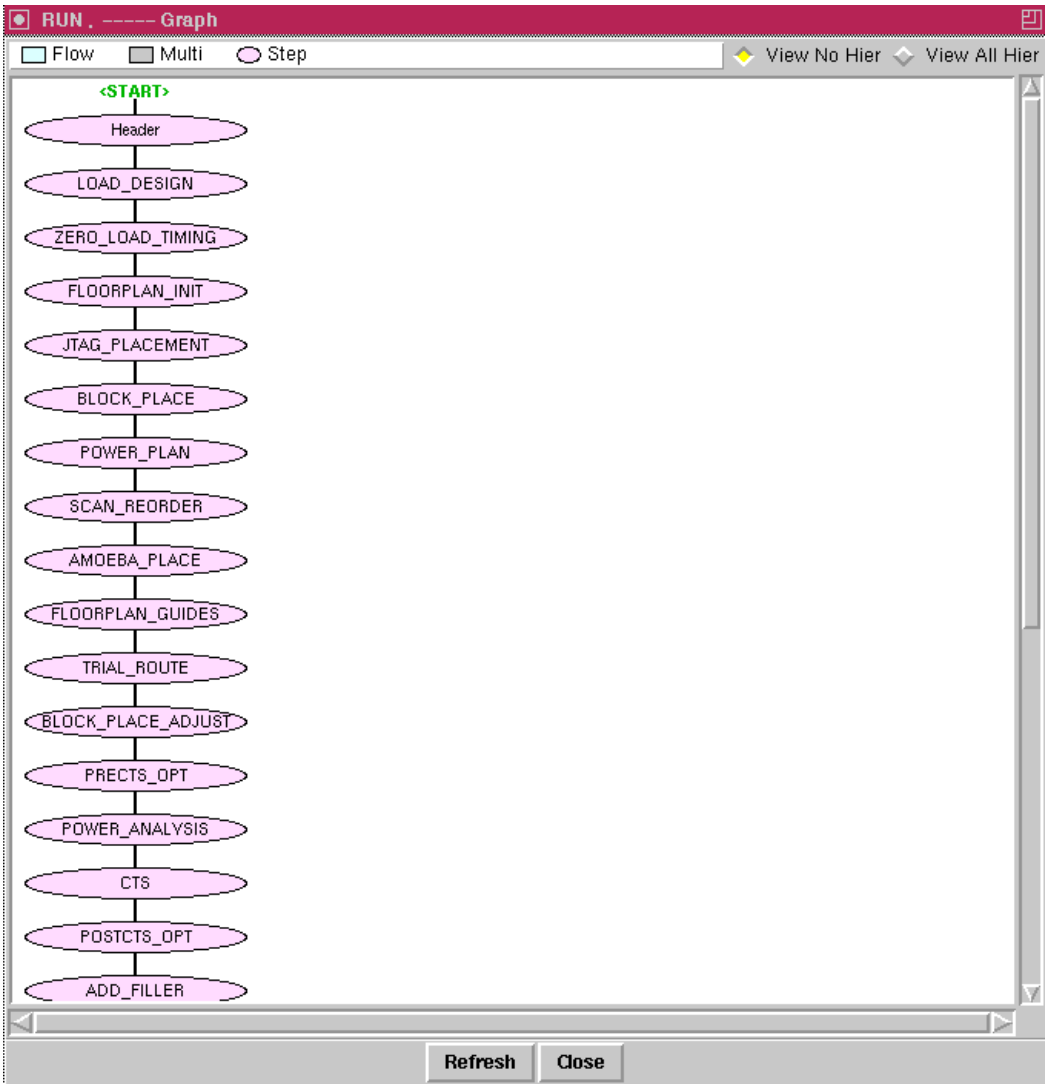
The following text command provides equivalent or additional functionality:

- `saveStateFile`

View Run Graph

Use the *View Run Graph* form to...

1. Choose *Tools – Express Flow Tool.*
2. Import a flow.
3. Right click from the box containing the title of the imported flow and select the *View Run Graph* option.



View Run Graph Fields and Options

View No Hier	Turns off the flow within the flow run graph display.
View All Hier	Turns on the flow within the flow run graph display.

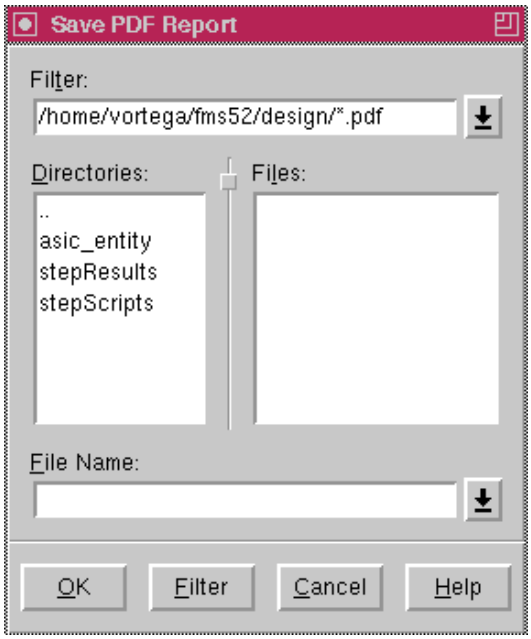
Related Text Commands

There are no related text commands for this functionality.

Report – Write PDF

The *Write PDF* command on the Express Flow Tool *Report* menu saves the results of the run into a PDF file. A form is provided where you specify the name and directory location for the file.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Report* menu, and click on the *Write PDF* option.
3. Select a directory, enter a filename, and then click on the *Save* button.



Report (Write PDF) Fields and Options

Filter	Specifies the type of files to be shown.
Directories	Displays the names of directory locations.
Files	Displays a list of files in the selected directory.
File Name	Displays or allows you to type in the name of the file.

Related Text Commands

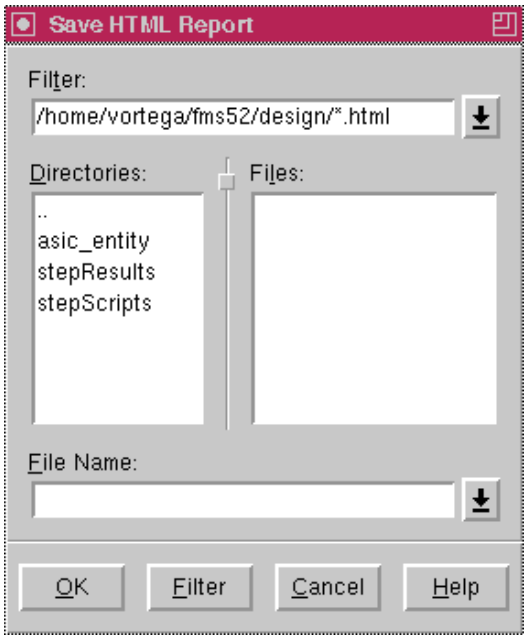
The following text command provide equivalent or additional functionality:

- `writeResultsToPdf`

Report – Write HTML

The *Write HTML* command on the Express Flow Tool *Report* menu saves the results of the run into an HTML file. A form is provided where you specify the name and directory location for the file.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Report* menu, and click on the *Write HTML* option.
3. Select a directory, enter a filename, and then click on the *Save* button.



Report (Write HTML) Fields and Options

Filter	Specifies the type of files to be shown.
Directories	Displays the names of directory locations.
Files	Displays a list of files in the selected directory.
File Name	Displays or allows you to type in the name of the file.

Related Text Commands

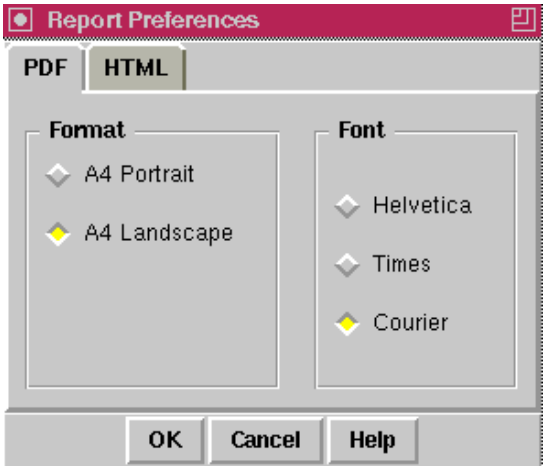
The following text command provide equivalent or additional functionality:

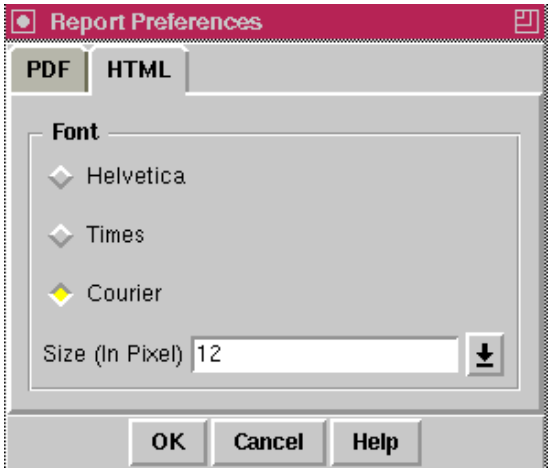
- `writeResultsToHtml`

Report Preferences – PDF and HTML

Use the *Report Preferences* form to select options for formatting PDF and HTML output files.

1. Choose *Tools – Express Flow Tool.*
2. Select the *Report* menu, and click on the *Preference* option.





Report Preferences Fields and Options

PDF	Specifies the options for saving a report in PDF format.	
	Format	Allows you to choose between portrait (vertical) or landscape (horizontal) page orientation for the PDF document.
	Font	Allows you to select from Helvetica, Times, or Courier fonts.
HTML	Specifies the options for saving a report in HTML format.	
	Font	Allows you to select from Helvetica, Times, or Courier fonts.
	Size (in Pixel)	Specifies the type size to use for the HTML output. Click on the arrow icon for a list of available sizes.

Related Text Commands

The following text commands provide equivalent or additional functionality:

- `writeResultstoPdf`
- `writeResultstoHtml`

Index

A

Add End Cap Instances 1039
Add Filler 1041
Add Metal Fill 1243
Add Ring Environment Variables 848
Add Rings
  Advanced 840
  Basic 833
  Via Generation 844
Add Stripe Environment Variables 868
Add Stripes
  Advanced 860
  Basic 852
  Via Generation 864
Add Tie Hi/Lo Instances 1051
Add Via Cell 460
Add Via Fill 1252
Add Well Tap Instances 1036
Add XStripes 873
  Basic 874
  Via Generation 878
Adjust Power Domain to Align Rows 699
Align Instances/Modules 621
All Colors 91
Amoeba view 71
Assign Power/Ground Bumps 674
Assign Signals 672
Attribute Editor 1554
auto query 101
Automatic Floorplan
  Finish Floorplan 566
  Multi Plan Design 569
    Auto Trials 570
    Floorplan Ranking Result 579
    User Options 574
  Plan Design
    Advanced 558
    planDesign 556
  Refine Macro Placement 564
  Report Plan Design 568
Automatic Floorplanner
  Plan Design 555

B

Binding Key 288
Blackbox
  specifying macros 496

C

Calculate Delay 1484
Cell View Specification 985
CeltIC Result Browser 1499
Change Partition View 533
Channel Estimation/FPlan Adjustment 511
Check Floorplan 646
Check Pin Assignment 532
Check Placement 1059
Clear Clock Tree Display 1125
Clear Floorplan 643
Clear Highlight 396
Clear Macro I Source Location
    Display 1004
Clear Pad Location Display 994
Clear Rail Analysis Display 1002
Clear Ruler 398
Clear Scan Display 1066
Clear Spare Cells Display 1064
Clear Violation 1580
Clock Info 1091
Clock Mesh Synthesis
  Save Clock Mesh 1151
  Specify Clock Mesh 1149
  Unspecify Clock Mesh 1150
Clock Tree Analyst
  Clock
    Preference
      Color 1109, 1110
      Display 1107
  Clock Setup 1105
  Find
    Path 1116
    Reconvergence 1115
  Main Window 1102
  Tool
    Dump View 1118
    Find Instance 1111

Tools
List Flip-Flops 1113
Clock Tree Browser 1093
Clock Tree Diagram 1095
Clock Tree SPICE Out 1127
Clock Tree Synthesis
Generate Clock Specification File 1077
Specify Clock Tree Specification Files 1075
Synthesize Clock Tree 1072
Advanced 1079
Basic 1073
Color 93
Cell Coloring for Timing Debug 1395
for Bottleneck Analysis 1392
for BottleneckAnalysis 1394
in Timing Debug Preferences 1390
Set Color Violation for timing debug color preferences 1391
color coding
in Flatten Schematic, change 1563, 1564, 1565
color display 91
Color Preferences 77
Column Width Table 1384
connectivity
trace in module schematic 1561
Connectivity Browser 1556
conventions, syntax and typographic 62
core rows
creating 638
cutting 640
stretching 642
Create Core Rows 638
Create P/G Pin 880
Create Physical Feedthroughs 498
Create Physical Hierarchy 614
Create Power Domain 687
Create Shifter Rows 698
Create Spare Cell 1029
Custom Object Editor 461
Cut Core Rows 640
Cut Power Domain by Overlaps 697

D

Debug Power 934
DEF file specification 193
default color settings
change 1564
in Flatten Schematic, change 1563, 1564, 1565
default font settings
change 1565
default font style settings
change 1565
default line style settings
change 1564
Delete Clock Mesh 1155
Delete Filler 1044
Delete Instances 1044
Delete Power Switches 750
Delete Spare Cell 1033
Delete Tie Hi/Lo Instances 1053
Derive Timing Budget
Basic 520
DeriveTimingBudget
Advanced 523
Design Browser 1550
design display area 67
Design Import 108
Basic 109
Delay Calculation 114
GDS 116
ILM 118
IPO/CTS 120
Multi Mode Multi Corner 137
MMMC Browser 139
OpenAccess 121
Power 123
RC Extraction 125
RTL 129
SI Analysis 130
Timing 132
Yield 135
design views 70
Display Clock Mesh 1162
Display Clock Tree 1122
Display Macro I Source Location 1003
Display Noise Net 1497
Display Options 680
Display Pad Location 993
Display Rail Analysis Results 995
Display Scan Connections 1065
Display Screen Dump 1672
Display Spare Cells 1063
documents, related, list of 63
drivers
trace in module schematic 1561

E

ECO Place 1026
Edit Block Halo 633
Edit Clock Mesh Specification
  Chain 1139
  Constraints 1135
  Local Tree 1147
  Mesh Stage 1144
  Mesh Structure 1141
  Route Types 1133
  Scope 1137
Edit Floorplan 620
Edit Highlight Color 397
Edit IO Row 636
Edit Net Group 454
Edit Net Toggle Probability 940
Edit Pad Location 937
Edit Pin Group 450
Edit Power Plan
  Design 811
  IP Block 817
Edit Power Planning Option 769
  RING
    Connect Layer Range 778
    Jog 775
    Make Via Connect to 782
    Merge 774
    Orthogonal Connection 780
    Partial Intersection Connection 779
    Ring Offset 773
    Ring Style 772
    Split Long Via 781
    Wire Group 776
    Wire Snap 777
  STRIPE
    Block Ring Connection 791
    Block Ring Connection – Jog 787
    Block Ring Connection – Merge 788
    Closest Target 803
    Connection Layer Range 794
    First / Last Stripe 784
    Jog Length 789
    Make Via Connection to 798
    Minimum Length 807
    Orthogonal Connection 796
    Pad / Core Ring Connection 790
    Pad / Core Ring Connection – Jog 786
    Same Layer Target Connection 801
    Same Size Stack Vias 800
    Spacing From Block 806
    Split Long Via 797
    Split Vias 799
    Split Wire 805
    Stripe Boundary 783
    Stripe Breaking 785
    Stripe Over Row 802
    Switch Cell Pin Target 804
    Wire Group 792
    Wire Snap 793
Edit Power Vias
  Advanced 887
  Basic 883
Edit Route
  Miscellaneous 433
  Nets 412
  Override 417
  Route 410
  Shielding 421
  Snap 423
  Via 425
  Widgets 447
  Wire Group 427
Edit Table Column 1377
  Load GTD Preferences File 1380
Edit Via
  Geometry 442
  Viacell 446
EditObject
  CreateNonDefaultRules 458

F

False Path Analysis 1410
fan-ins
  close in module schematic 1561
  open in module schematic 1561
fanouts
  close in module schematic 1561
  open in module schematic 1561
File Menu
  module schematic 1558
Filler 1035
Filler Mode Setup 314
Find An Object By Name 385
Fix Crosstalk 1502
Flip Chip
  Add Bump to Array 666

Create Bump Array 658
Edit Bump Array 662
Flip Chip Route
Advanced 1258
Prototype 1262
Routing Constraints 1266
Routing Style 1259
Splitting 1264
Basic 1254
Flip Chip Toolbox 1568
flip chip widget 74
Flip/Rotate Selected Instances 626
FlipChip 581
floorplan 582
Floorplan view 71
floorplan widgets 73

G

Gate Count Report 263
GDS Export 246
Generate Capacitance Table 1486
Generate FP Guide 648
Generate Regrouped Netlist 650
Generate Wire-Load Model 1489
Global Net Connections 616
Global Timing Debug 1365
Group Pin(s) Move 652

H

Highlight Selected 395
Highlighting MSV Objects
customizing highlight colors 758, 760
power domains 753
signal net/HLS cells 755

I

information box
enable or disable in module schematic 1559
send to transcript window 1559
Input Instances 1663
Insert Feedthrough Buffer 508

K

keyboard shortcuts 104

L

Layer Bias Specification 988
Layer Names Maps Specification 990
Legalize Floorplan 630
Load Clock Tree Trace File 1086
Load DEF File 211
Load FPlan File 206
Load GTD Preferences File 1380
Load IO File 217
Load OA Database 223
Load Partition 204
Load PDF File 215
Load Placement File 207
Load Power Waveform 222
Load Route File 209
Load SDF File 220
Load Shifter/Isolation Cells File 702
Load SPEF File 218
Load TDF File 213
Load Violation Report 1578
Load/Commit CPF 685
loads
trace in module schematic 1561
Log Viewer 1666

M

macros
specifying for blackboxes 496
Main Window 67
Menu Bar
File, for module schematic 1558
Preference, for module schematic 1559
View, for module schematic 1558
Window, for module schematic 1559
Metal Fill Trim 1248
Mixed Signal Constraint Editor 1620
Electrical Constraints 1651
Analog Inst 1656
Analog Net 1655
Analog Pin 1654
Display All 1657
Max IR Drop 1652

Routing Constraints 1621
Bus 1642
Diff Pairs 1622
Display All 1649
Dont Cross 1647
Matched Pairs 1627
Route Nets 1632
Shield Nets 1637
Select Constraint Member (Browser) 1658
Mixed Signal Router 1230
Mode Setup 294
Clock Mesh 295
Analysis 296
Optimization 301
Synthesis 299
CTS 303
Miscellaneous 311
Route/EM 306
Trace 304
Cts
Optimization 309
Filler 314
NanoRoute 316
Optimization 338
Placement 344
RefinePlace 350
ScanReorder 352
StreamOut 354
TieHiLo 357
Trial Route 359
Module Color Preference 580
mouse operation 104
Multi Mode Multi Corner
Add Analysis View 160
Add Constraint Mode 149
Add Delay Corner 151
Add Hold Analysis View 162
Add Library Set 142
Add Object 168
Add Op Cond 144
Add Power Domain 156
Add RC Corner 146
Add Setup Analysis View 164
Edit Constraint Mode 176
Edit Delay Corner 178
Edit Library Set 169
Edit Op Cond 171
Edit Power Domain 181
Edit RC Corner 173
MMMC Browser 139
MMMC Preferences 166
Multiple CPU Processing
Basic 374
Host Setup 377

N

NanoRoute 1209
NanoRoute Mode Setup 316
NanoRoute/Attributes 1210
Netlist Stats 264

O

Object
Find By Name 385
Select By Name 385
Optimization 1459
Optimization Mode Setup 316
Optimize Power Plan
Advanced 904
Basic 901

P

partition widgets 74
Path Analysis
False Path Analysis 1410
Physical view 71
Pin Alignment 407
Pin Editor 399
Place Flip Chip I/O 1019
Place Jtag Logic 1015
Place Mode Setup 343
Place Spare Cell 1031
Place Standard Cells 1017
Power Analysis Simulation-Based 954
Power Analysis Static Mode 944
Power Analysis Statistical Mode 948
Power Domain 490
Power Switch Insertion
Column
Switch Arrangement 747
Ring 710
Pre-CTS Clock Tree Tracer 1082
Search 1087
Search & Hilite 1089
Preference Menu

module schematic 1559
Preferences 265
Design 266
Display 270
Floorplan 277
Selection 280
Windows 282
primitive types
displayed in module schematic 1558
printing
schematic display 1562

R

Rail Analysis
Average Mode 962
Read Activity File
SAF 912
TCF 911
VCD 909
Refine Placement 1023
related documents, list of 63
Relative Floorplan - Clear Constraints 613
Relative Floorplan - Define Array Constraints 605
Relative Floorplan - Generate Constraints 601
Relative Floorplan – Place 590
Relative Floorplan – Pre-Route 599
Relative Floorplan – Reshape 593
Relative Floorplan – Resize 596
Relative Floorplan - Save Constraints 612
Remove Shifter/Isolation Cells 708
Reorder Pin List 405
Repair Power Stripes
Advanced 893
Basic 891
Via Generation 895
Report Clock Mesh 1160
Report Power
Format 930
Report Power 926
Report Power Domain 762
Report Shifter/Isolation Cells 707
Report timing Library 1477
Report Yield 1617
resize 582
resize floorplan 582
Restore Design 195
Restore OA Design 196
Route Clock Mesh 1156
Routing Guide File 1306
Ruler
Clear 398
Run CeltIC Crosstalk Analysis 1494

S

satellite window 98
Save Clock Nets 1126
Save Clock Tree Browser 1100
Save DEF 235
Save Design 200
Save FPlan File 227
Save IO File 240
Save Netlist 233
Save OA Design 202
Save Partition 225
Save PDEF 239
Save Placement File 229
Save Rail Analysis Results 242
Save Route File 231
Save TDF 237
Save Timing Budget 244
Scan
Delete 1056
Mode Setup 352
Reorder 1057
Screen Dump 1671
Select A File (for Net Names) 415
Select A File (for Override Values) 419
Select An Object By Name 385
Select Constraint Member 1658
Select/Delete/Deselect Routes 439
Set Cell/Instance Power 913
Set Color Violation 1391
Set Congestion Map Style 1223
Set Default Switching Activity
Global 916
Specific 918
Set Placement Status 632
Set Power Analysis Mode 923
Set Switching Activity 920
Set Timing Derate 1324
Setup Chip IO
IO Driver Row 668
Setup Metal Fill Options
Size & Spacing 1236
Window & Density 1240
Setup Via Fill Options 1250

Shift Instances/Modules 623
Show Pin Status 678
Show/Hide 380
Snap Loaded Floorplan 628
Space Instances/Modules 625
Special Route Options 437
Specify 1006
Specify Analysis Condition 1311
Specify Analysis Mode 1318
  Advanced 1321
  Basic 1319
Specify Black Box 493
Specify Cell Padding 1009
Specify Electromigration Limits 767
Specify Floorplan 536
Specify Jtag Cell 1011
Specify Operating Condition 1312
Specify Partition 484
Specify Placement Blockage for Strip and Routing Blockage 1013
Specify RC Extraction Mode 1314
Specify Spare Cells 1007
Specify Template Parameter 825
Specify Timing Libraries - Min 693, 695
SRoute
  Advanced
    Block Pins 1180
    Extension Control 1193
    Extra Config Editing 1201
    Pad Pins 1184
    Pad Rings 1187
    Power Domains 1191
    Standard Cell Pins 1189
    Target List Editing 1197
  Basic 1172
  Via Generation 1203
StreamOut Mode Setup 354
Stretch Core Rows 642
Summary Report 258
Swap Signals 677
syntax conventions 62
Synthesize Clock Mesh 1152
Synthesize Power Plan 808

T

TieHiLo 1050
TieHiLo Mode Setup 357
Tie-Off Nets 1664
timing
  interpretation 1432
Timing Debug
  Display or Generate Timing Report 1366
  Edit Table Column 1377
  Global 1365
  Load GTD Preferences File 1380
Timing Debug Preferences
  Bottleneck Analysis 1392
  Cell Coloring 1395
  Color 1390
  General 1388
  Set Color 1394
  Set Color Violation 1391
Timing Path Analyzer
  Edit Table Column 1377
Timing Path Browser
  Load GTD Preferences File 1380
tool widgets 72
toolbar widgets 68
Trial Route 1168
Trim Clock Mesh 1157
typographic conventions 62

U

UltraSim 1660
Unassign Bump/Tile Pin 676
Unpartition 531

V

Verify AC Limit 1535
Verify Connectivity 1508
Verify Cut Density
  Basic 1520
  Window & Density 1522
Verify Geometry 1524
  Advanced 1530
  Basic 1525
Verify Metal Density 1514
  Basic 1515
  Window and Density 1517
Verify Mixed Signal Constraints 1539
  Electrical 1545
  Routing 1540
Verify Mixed Signal Routing Constraints Filter Output 1547
Verify Power Domain 764

Verify Process Antenna 1533
VHDL files 192
VHDL Import 190, 191, 193
View Menu
    module schematic 1558
Violation Browser 1570
Violation Browser Settings 1574
Virtuoso CAR Interface 1268
VoltageStorm Analysis
    Advanced 978
    Basic 969

W

Window Menu
    module schematic 1559
wire editing widgets 75
Write TCF 933
Write Text Report 1382
WRoute 1273
    Advanced 1280
        Crosstalk Options 1297
        Expert Options 1303
        Job Control 1281
        Net Options 1283
        Pin Access 1286
        Process Antenna 1288
        Route Optimization 1301
        Routing Layer Limits 1291
        Search and Repair 1293
        Tapering 1295
    Basic 1274