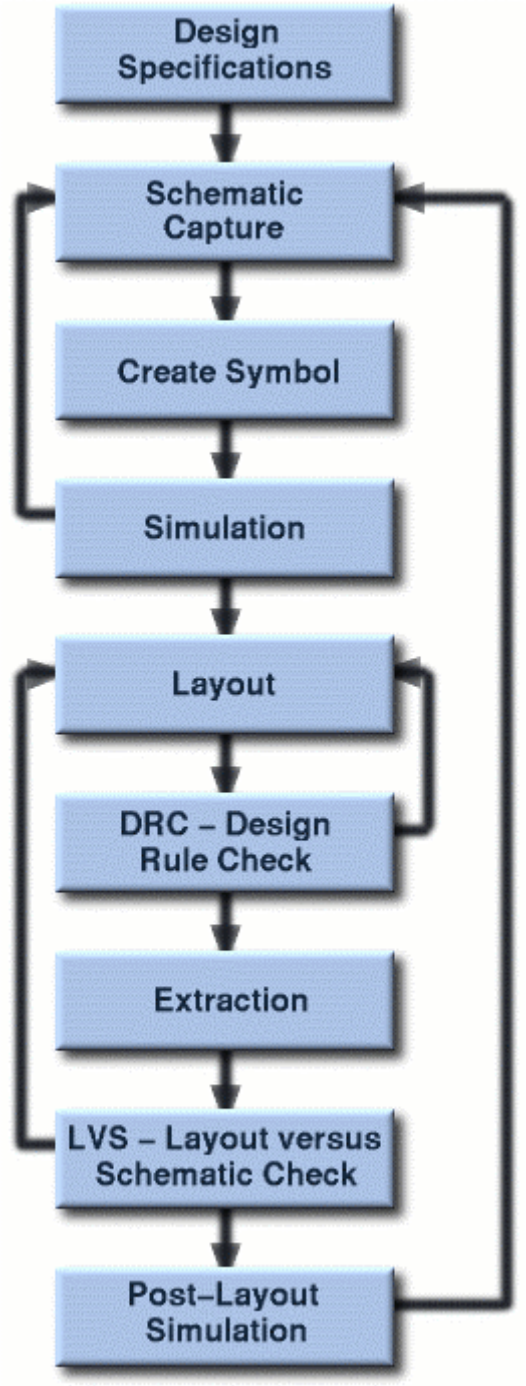
HOMEWORK —PLACE & ROUTE OF STD-CELLS

Prof. Don Bouldin – 19 November 2004



mkdir hw6a

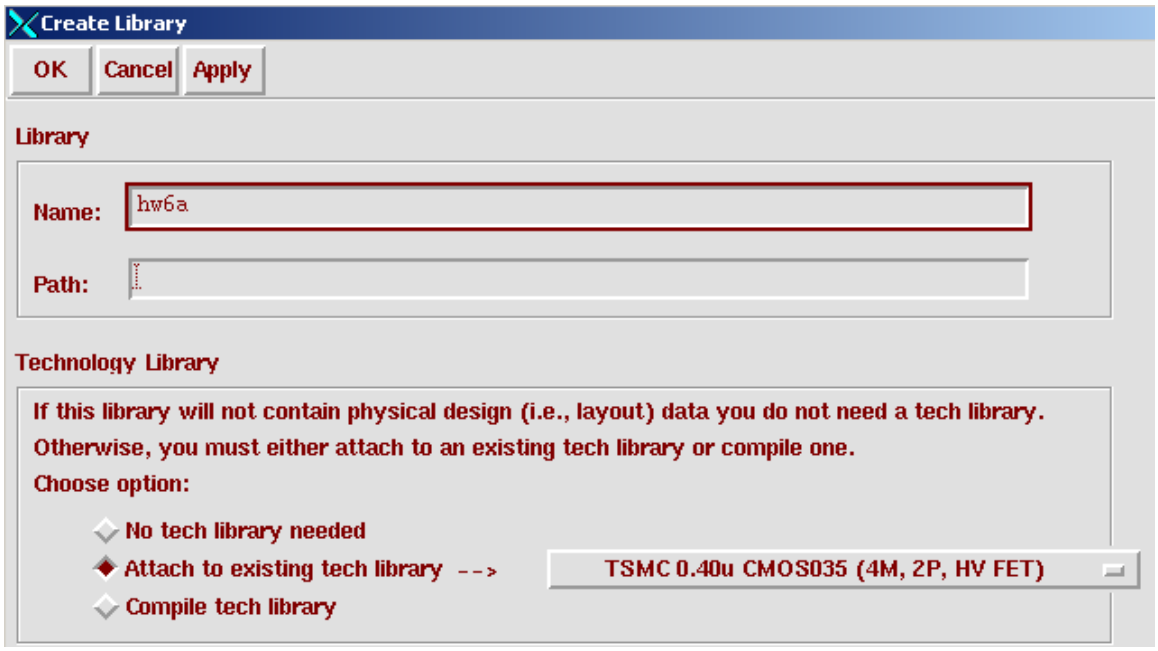
cp /usr/cad/course/iit/ami035_tutorial/cds* hw6a

cp /usr/cad/course/iit/ami035_tutorial/.cds* hw6a

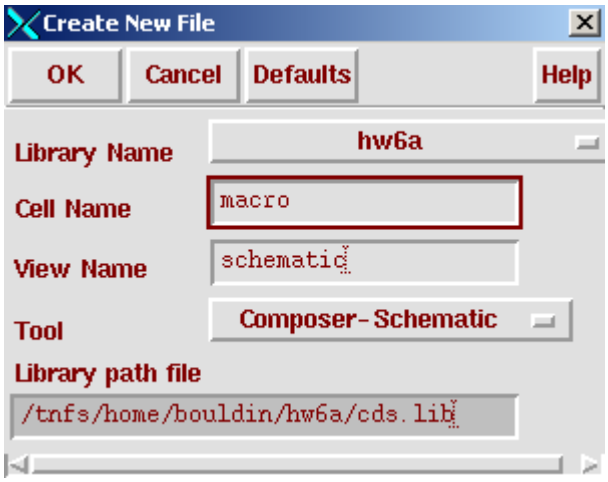
cd hw6a

cadence_tools; icfb&

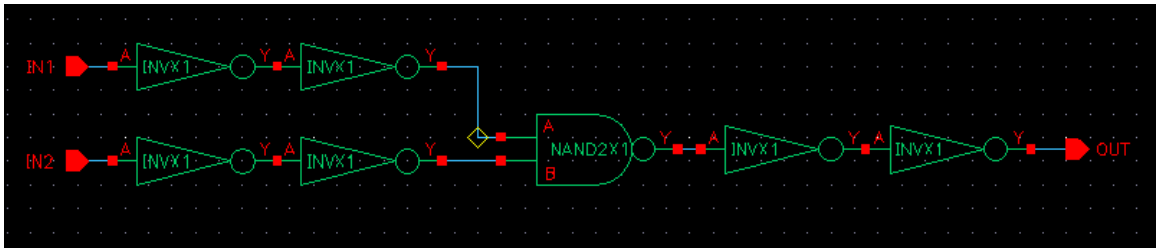
Create a new library and attach to the existing tech library:



Next, create a new cell with a schematic view:



Add the desired instances from the IIT_stdcells_ami035 library. Add wires to connect them and pins for the inputs and output:



Select: Design→Check and Save

When there are no errors or warnings, perform pre-layout simulation using VerilogXL by selecting

Tools→Simulation→Verilog-XL and then Simulation→Start Interactive.

When the simulations show the desired results,

cd macro.run1/ihnl

cp –r /usr/cad/course/ami035_tutorial cds2

cd cds2

cp netlist ami035_tutorial/macro.vh

cd ami035_tutorial

cadence_tools

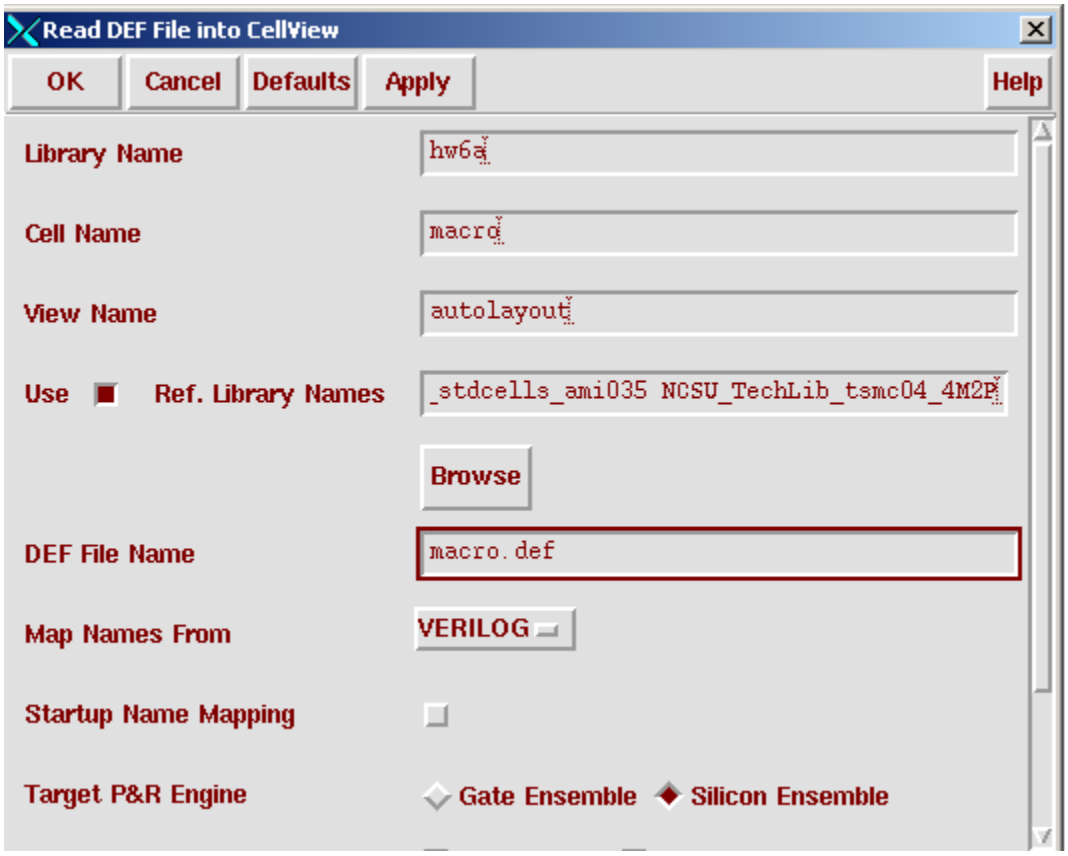
run-seultra

cp macro.def ../../../../

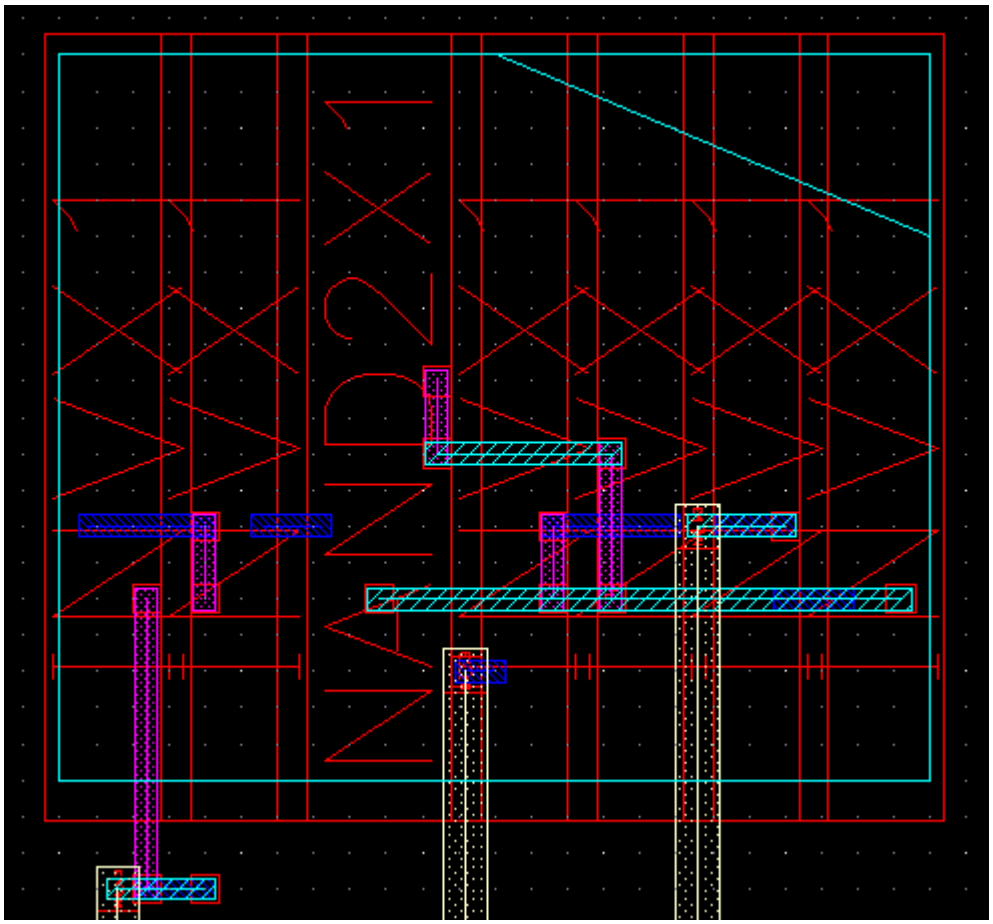
cd ../../../../

Import-def

read-def


Read DEF File into CellView
OK
Cancel
Defaults
Apply
Help
Library Name
hw6a
Cell Name
macro
View Name
autolayout
Use
Ref. Library Names
_stdcells_ami035 NCSU_TechLib_tsmc04_4M2P
Browse
DEF File Name
macro.def
Map Names From
VERILOG
Startup Name Mapping
Target P&R Engine
Gate Ensemble
Silicon Ensemble

The layout will initially look like this:

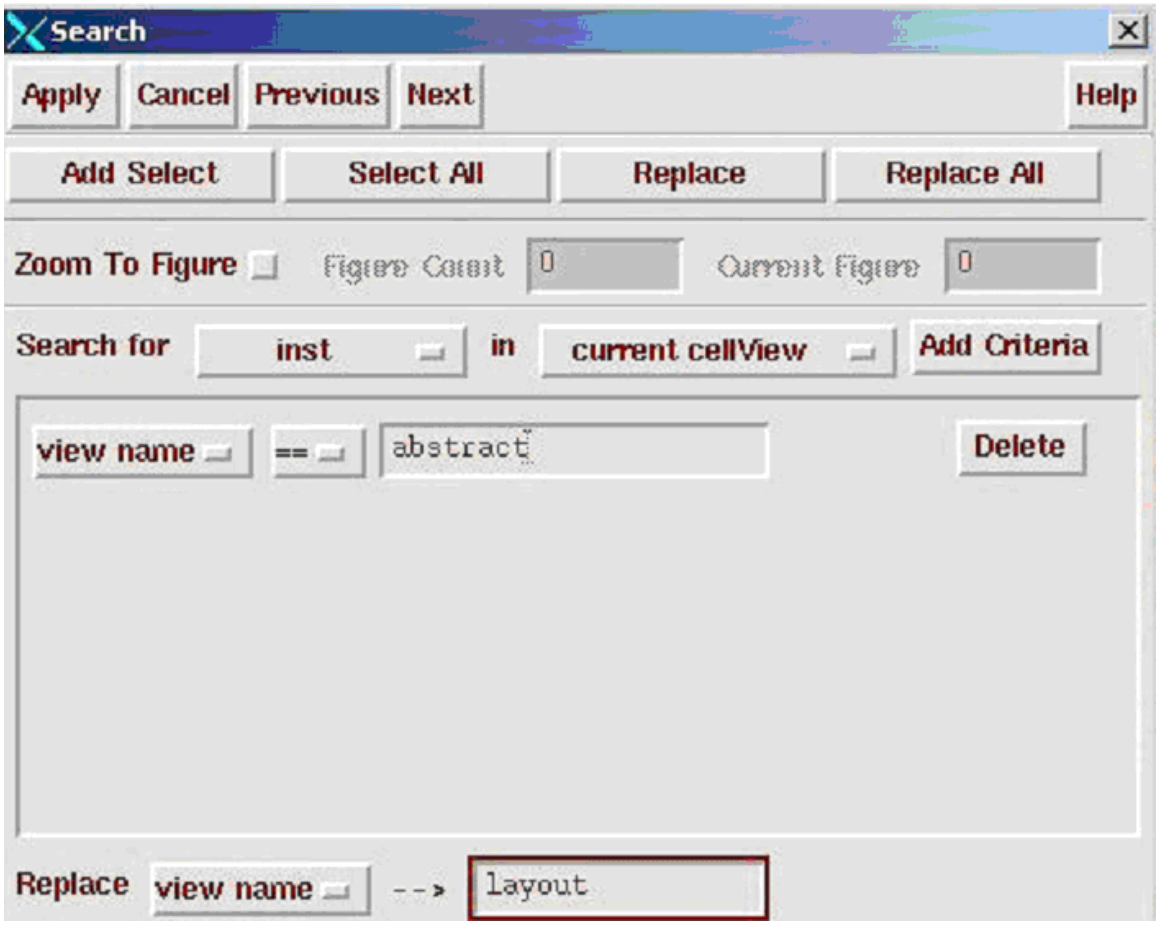


Be sure that cds.lib points to the correct location of the libraries:

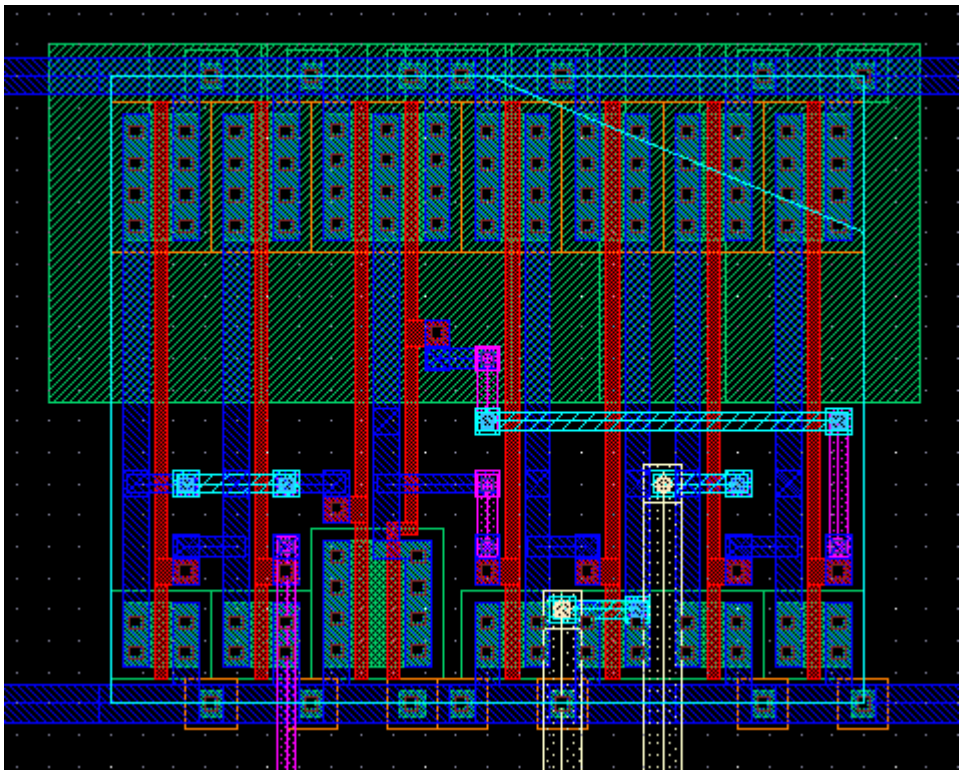
synth_iit035 ./macro.run1/ihnl/cds2/ami035_tutorial/synth_iit035

Then, select Edit→Select-All

Then, select Edit→Search→Add-Criteria and select “cell-view” and fill in “abstract” and then
Near “Replace” select “cell-view” and fill in “layout”.
Now press “Replace-All” and then “cancel”.



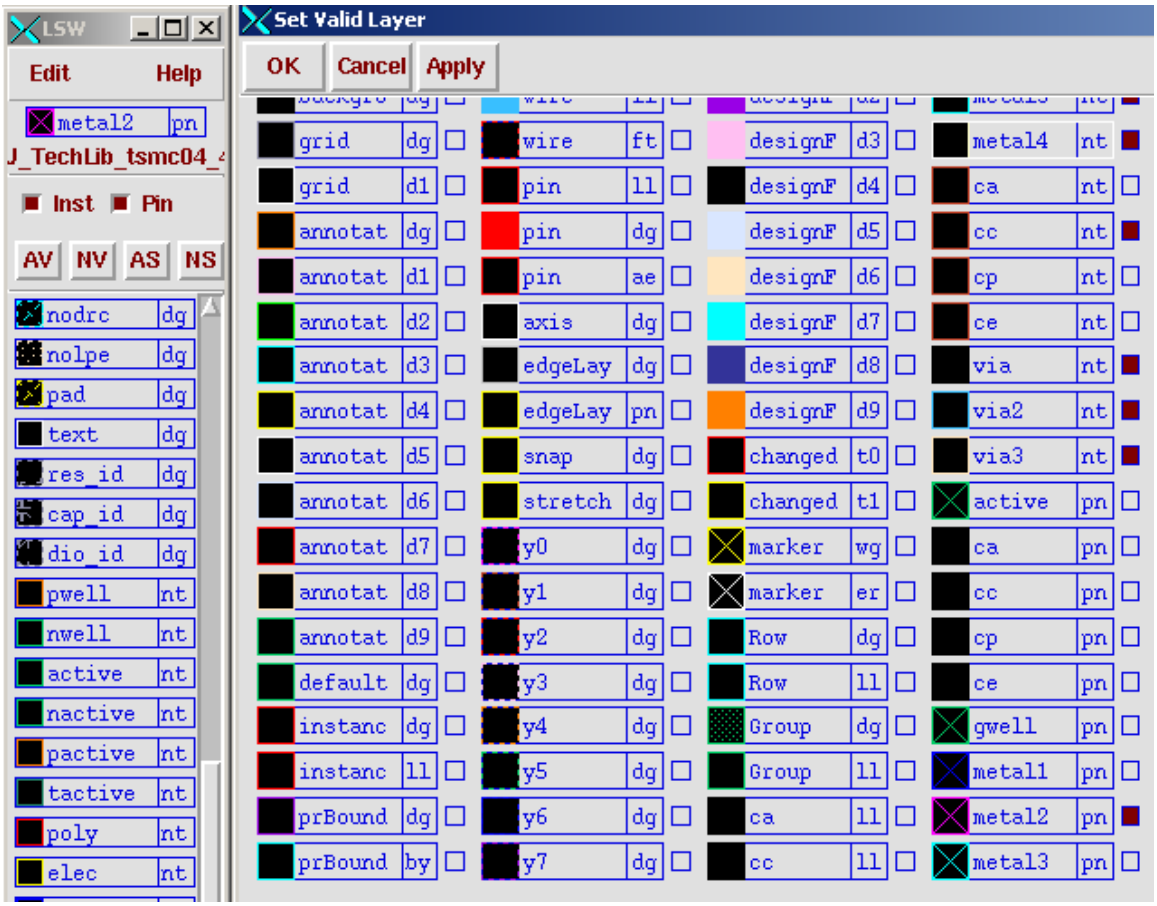
Then, press “shift-f” to flatten the design:



Save-as-layout

Then, double-click on “layout” to open it and then in the LSW pane, select:

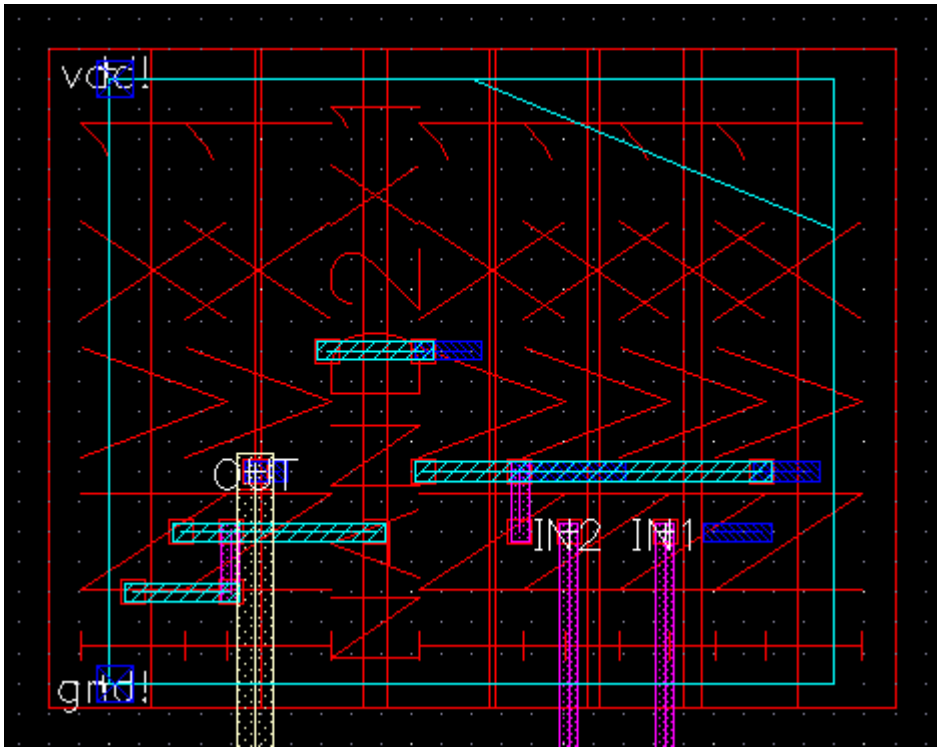
Edit→set-valid-layer and check “metal-2 pn” and then “OK”: Then, select “metal2—pn”.



Create→pin→shape

Then add a rectangular pin on the vdd! bus and another pin on the gnd! Bus.

Also, you can add labels to the layout:



Now, save the layout and verify DRC . Then, extract the layout and perform LVS and Spectre simulation.