A Network on Chip Architecture and Design Methodology

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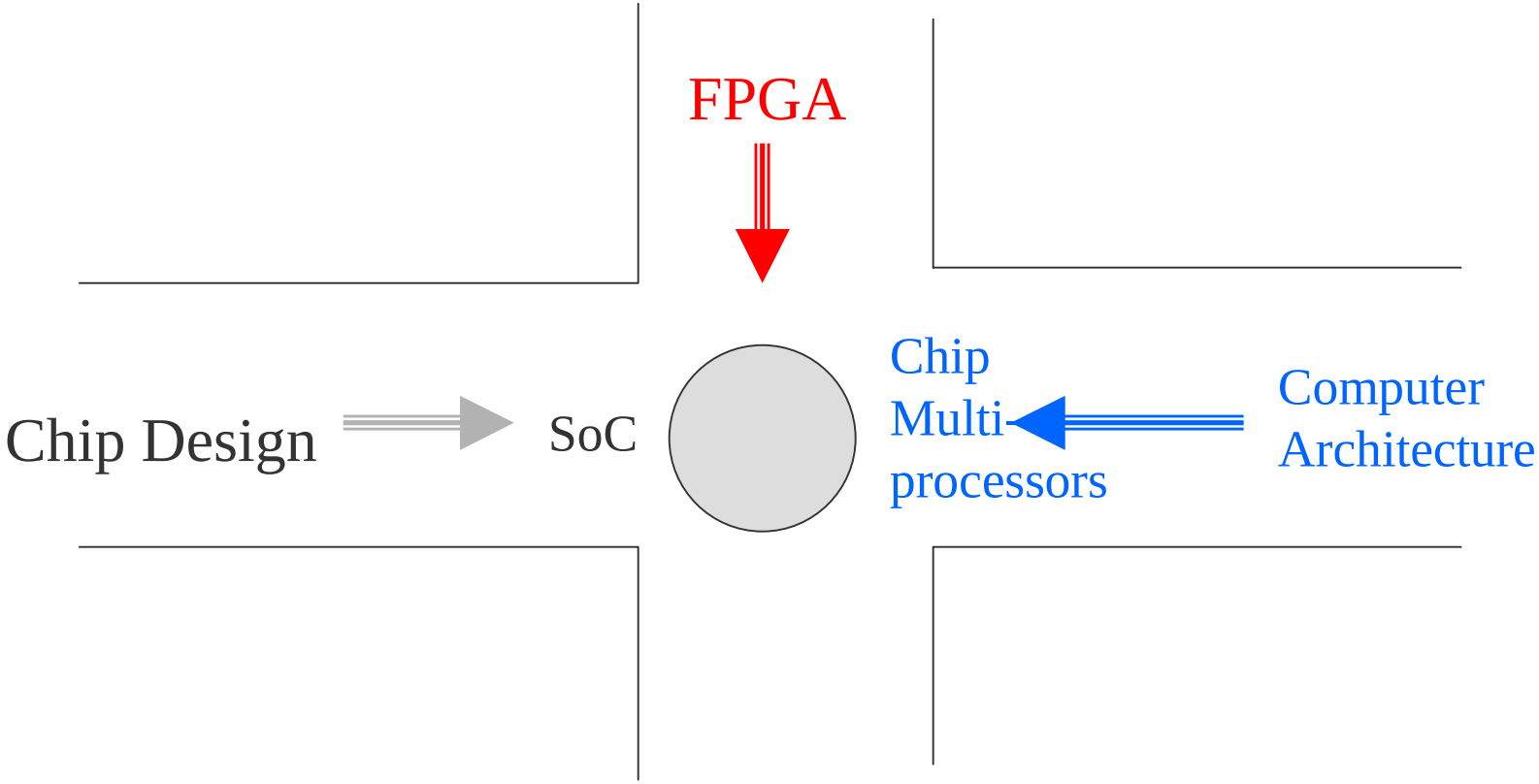
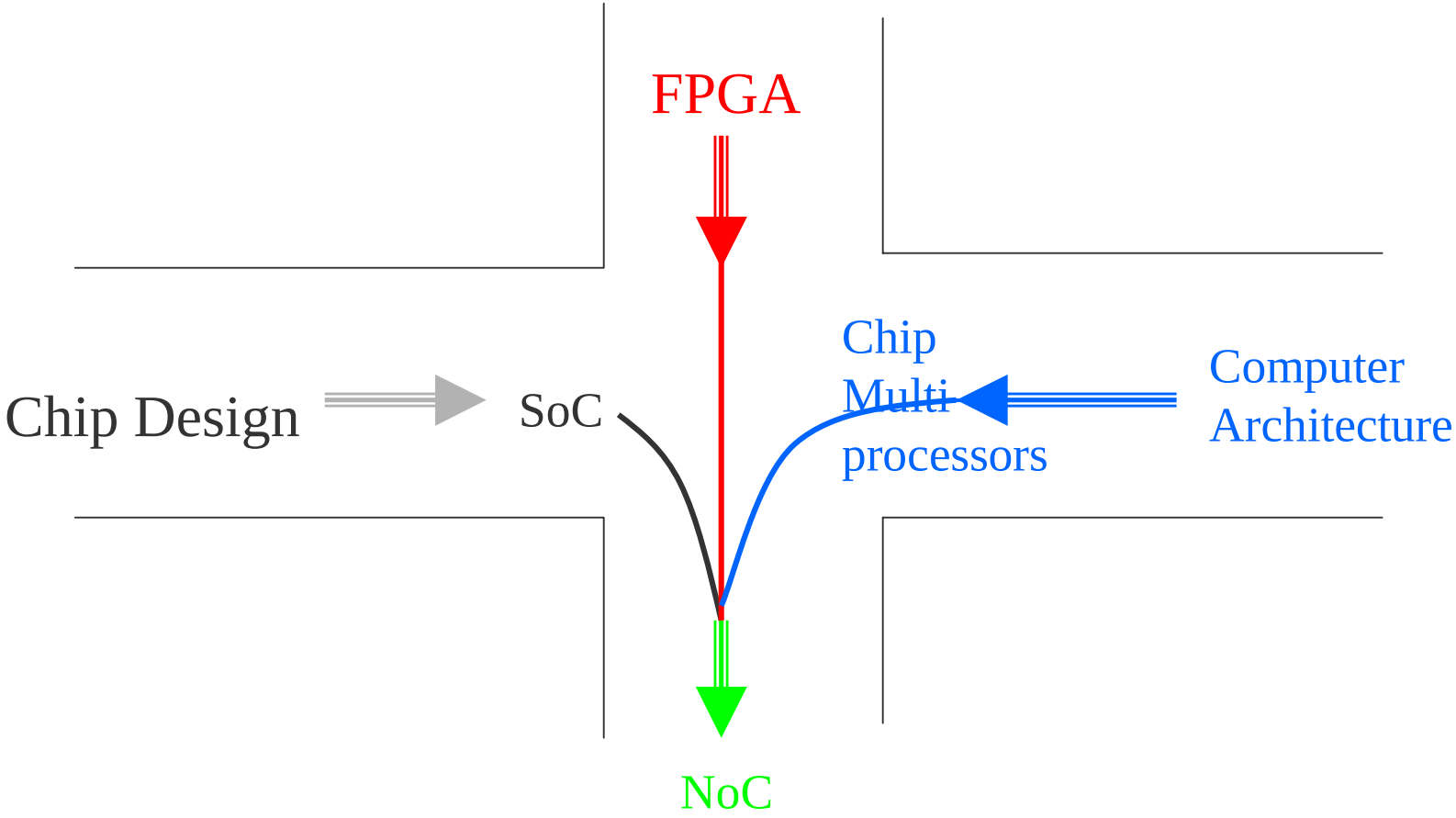
Outline

- Background and Introduction
- NOC Architecture: Basic features
  - Physical Level_Architectural Level Design Integration
  - Packets switched communication rather than wires
  - Region
- Evaluation of NOC
- A Methodology for NOC design
- Conclusions

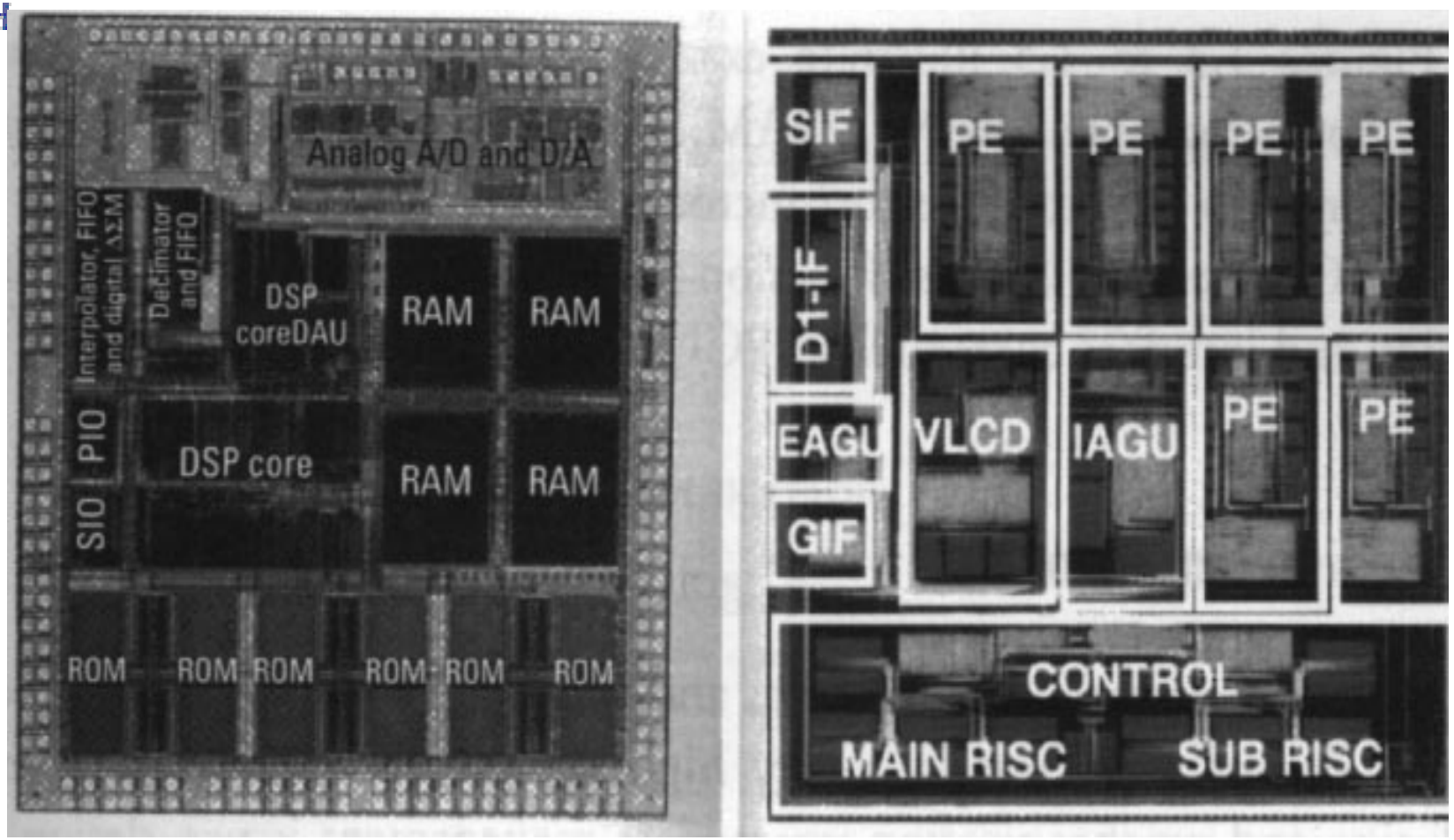
An Interesting Cross-road



An Interesting Cross-road



SoCs Today


Analog A/D and D/A
Interpolator, FIFO and digital ΣΔM
Decimator and FIFO
DSP coreDAU
RAM
RAM
PIO
SIO
DSP core
RAM
RAM
ROM
ROM
ROM
ROM
ROM
ROM
SIF
PE
PE
PE
PE
D1-IF
EAGU
VLCD
IAGU
PE
PE
GIF
CONTROL
MAIN RISC
SUB RISC

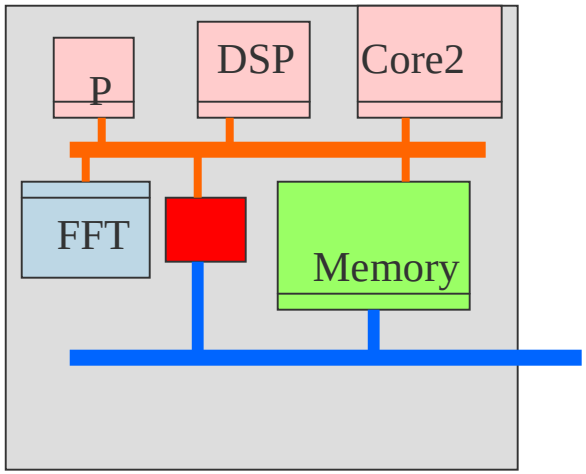
Challenges

- How to use available capacity of the chip?
  - 1 Billion gates by 2008
- Developing efficient and scalable architectures for connecting a large number of cores
- Fast time to market
  - Reuse as much as possible: Architecture, Components, Software, O.S.
- Small development cost for a new product
  - Programmable, Configurable and Up-gradable platform
- Low power consumption

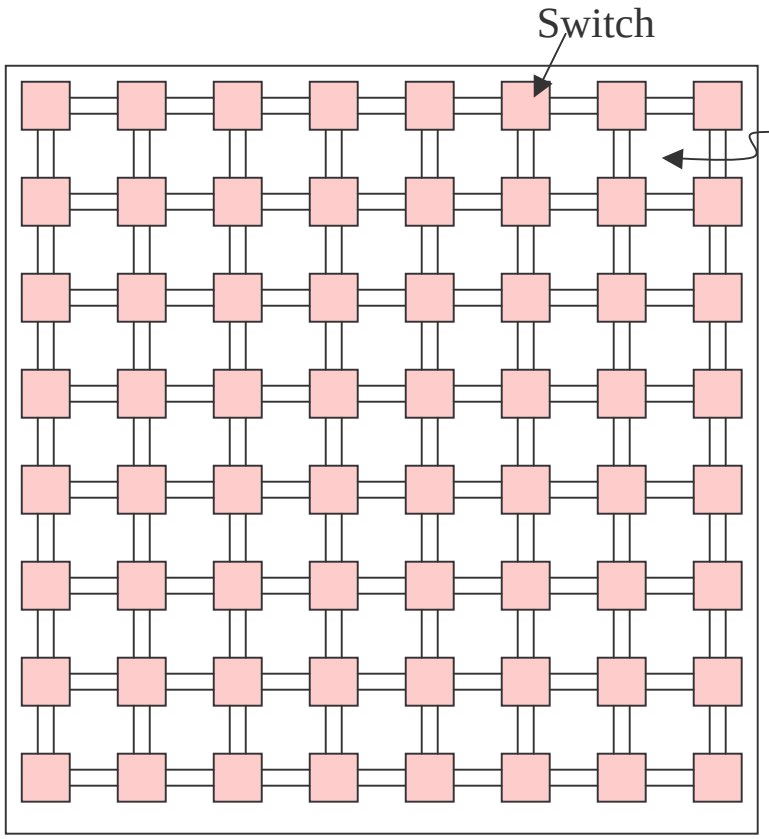
Platform Based Design

Fixed interconnection infrastructure

- Time-share the resources
- Bus based platform is not scalable

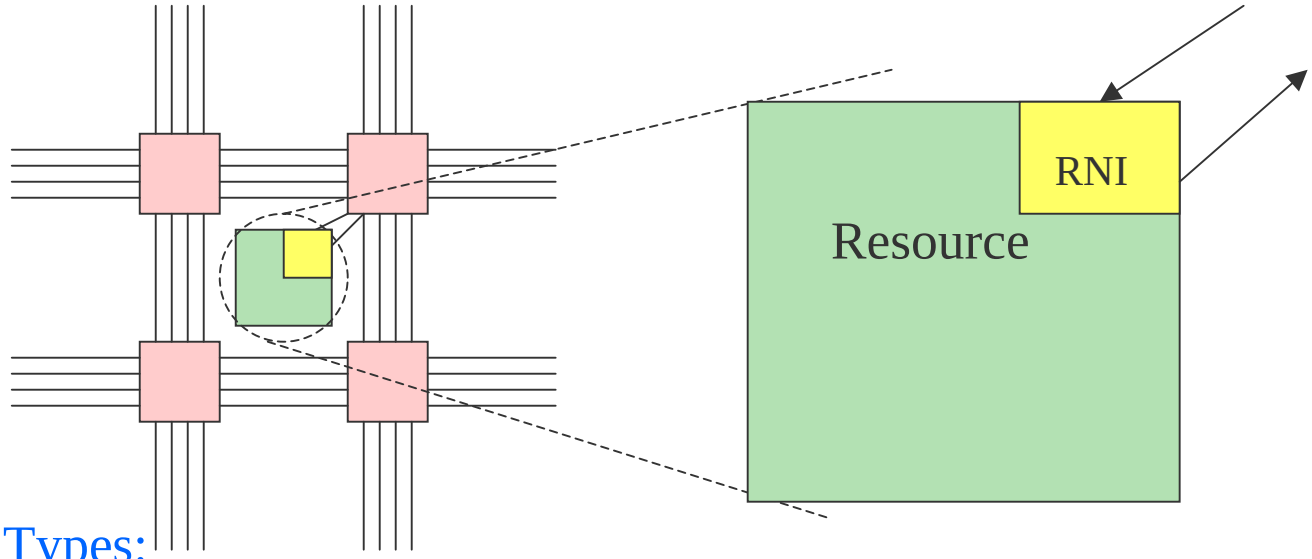


NoC Architecture Overview



- Scalable packet switched communication infrastructure
- Physical-Architectural Level design integration:
  - o A Resource must fit in the slot
  - o Layout same as topology
    - -Predictable electrical properties

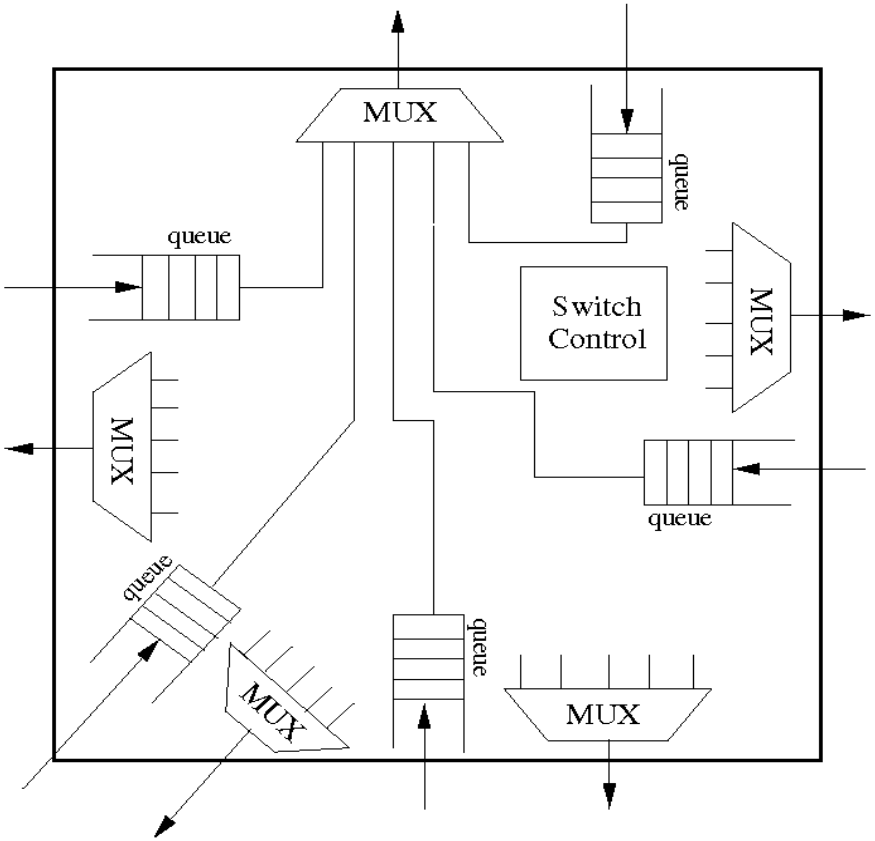
Resource-Network Interface



Resource Types:

- Processor of any type with/without local memory
- Memory
- IP Functional Cores
- FPGAs
- Dedicated Hardware block

NoC Switch


MUX
queue
queue
Switch
Control
MUX
MUX
queue
queue
queue
MUX
MUX

NoC layout: Square Switch

-Technology: 60 nm

-22 mm X 22 mm

-Switch:

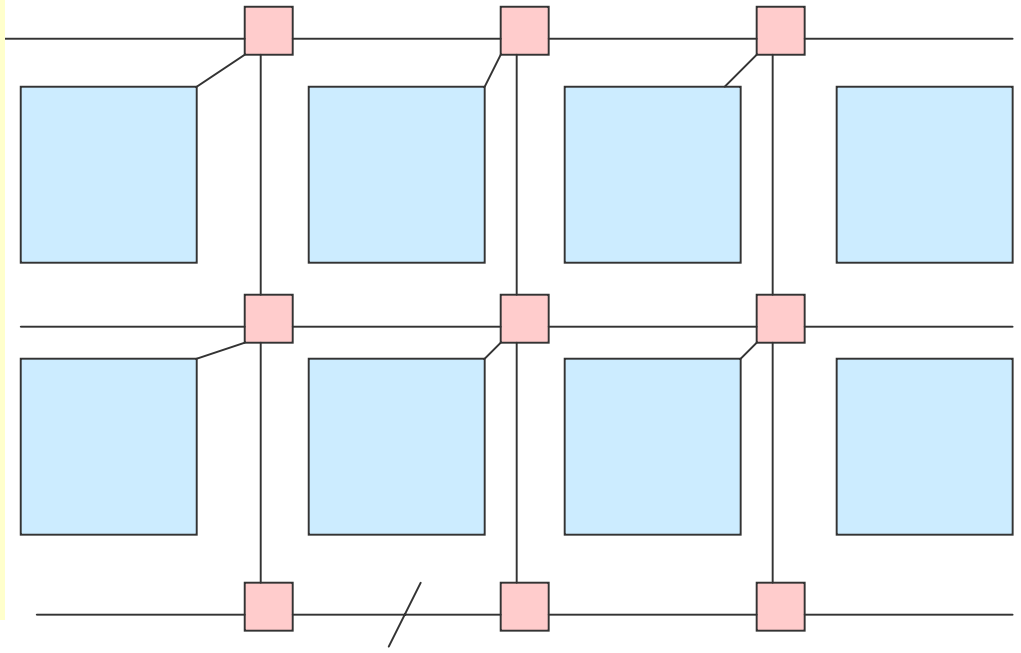
0.2mm X 0.2mm

Resource Slot:

2mm X 2mm

-100 resources

-256 wires in each direction

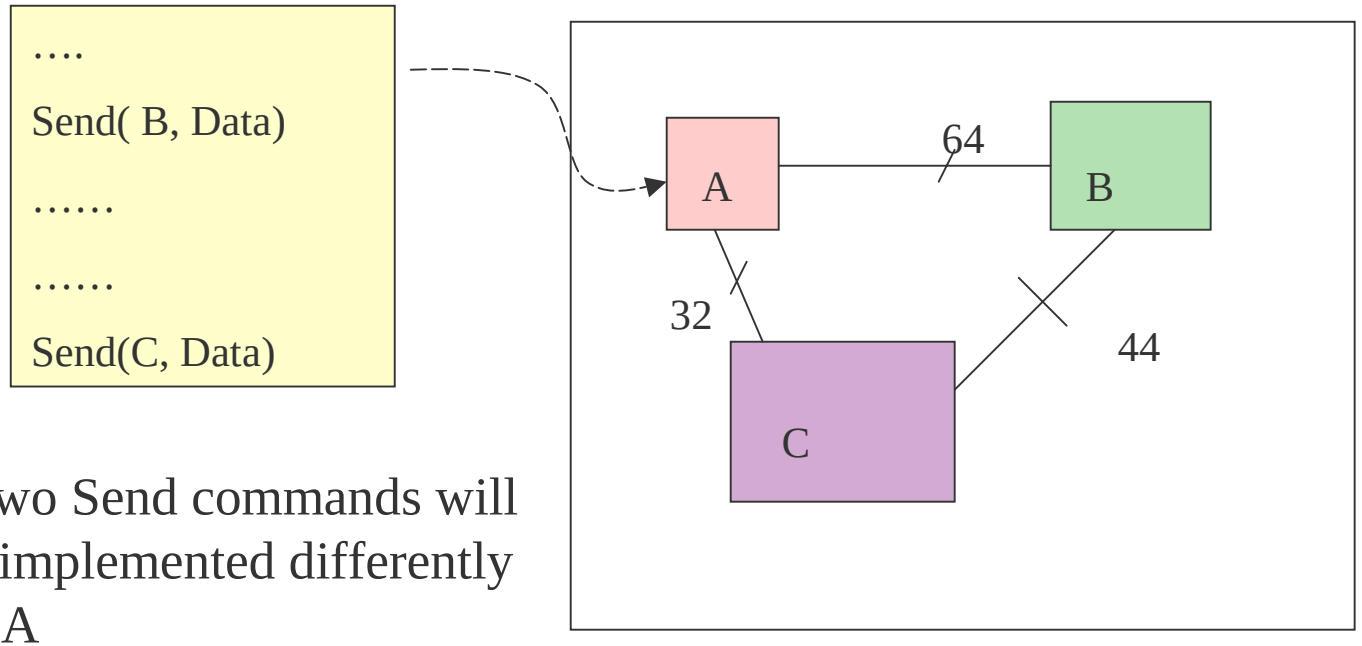


256

Communication in NoC: Layered Communication

- Standard and uniform interfaces
- Standard layered communication protocols adapted from OSI
  - Physical level : Number of wires, control signals, clock signals for every connection(S-S, S-R), electrical levels, ……
  - Data-Link Level: Word from one switch to its neighbor, Number of bits per word, Error detection and correction mechanism, encoding,…….
  - Network Layer: Packet from a resource to any other resource, routing algorithm, addressing resources, packet buffering, …
  - Application Level: Message vs. packet size

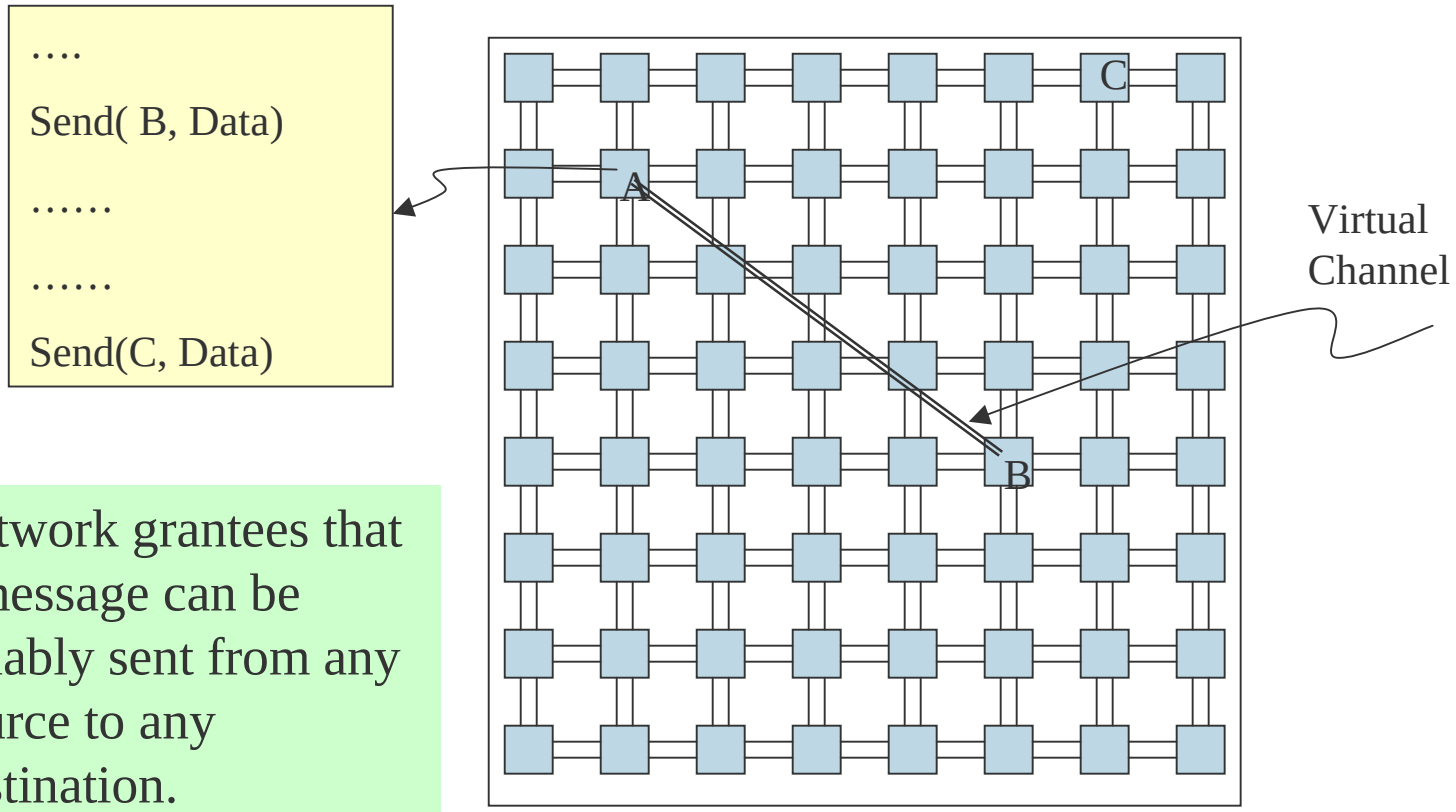
Comparison with communication in core based SoC



- Two Send commands will be implemented differently by A

- Interfaces A-B and A-C may use different protocols

Application Layer in NoC Architecture

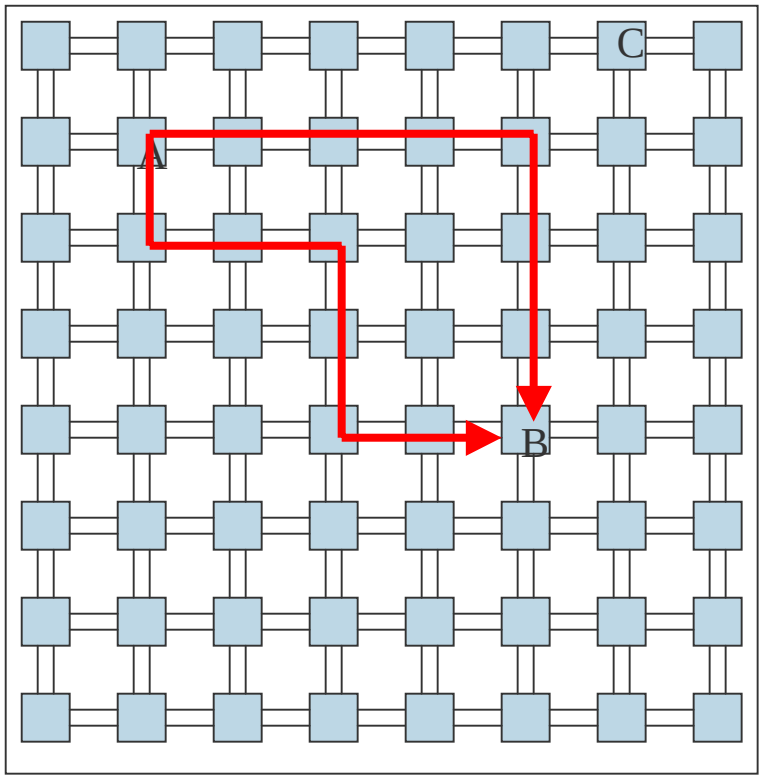


Network grantees that a message can be reliably sent from any source to any destination.

Network Layer in NoC Architecture

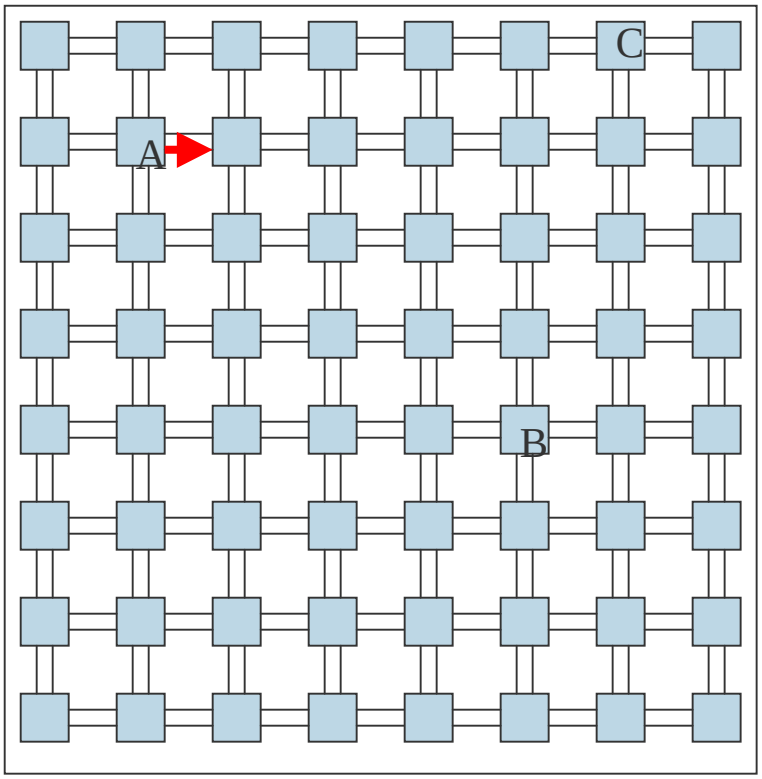
- Packet size vs. word size
- Different packets may get routed independently
- Routing algorithm

  Static vs. dynamic
- Priority classes
- Buffer in switch



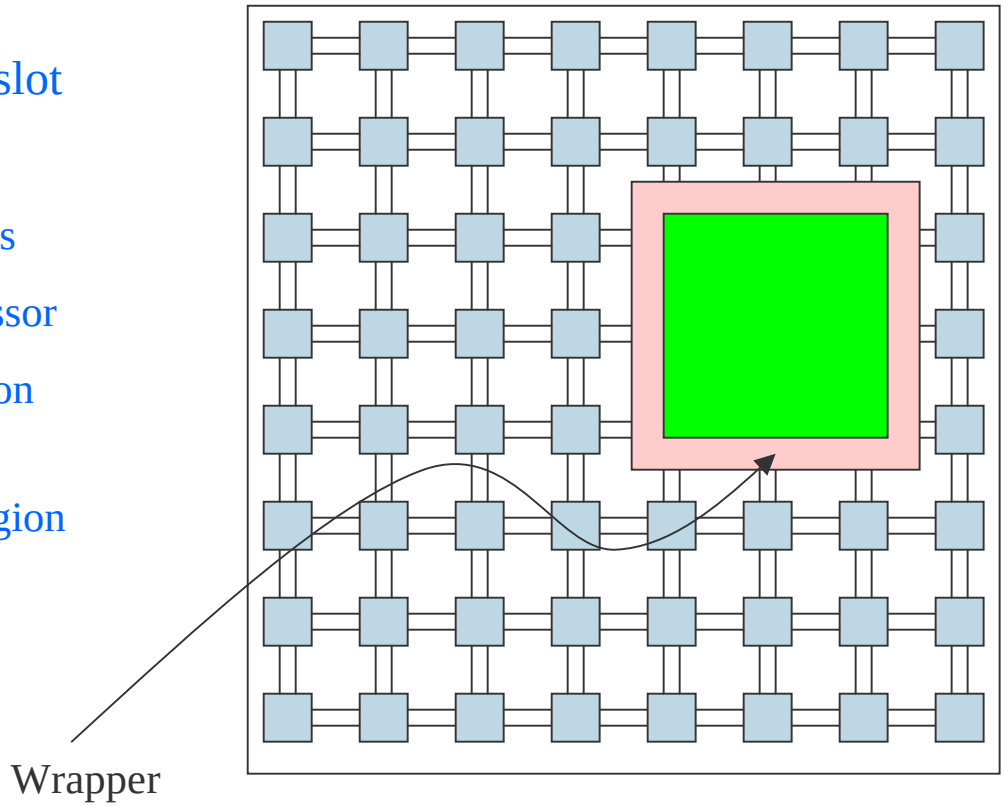
Data-link layer

- Moving a word from one switch to a neighboring switch using interconnection resources
- Error detection and correction
- Encoding for efficiency



Concept of Region

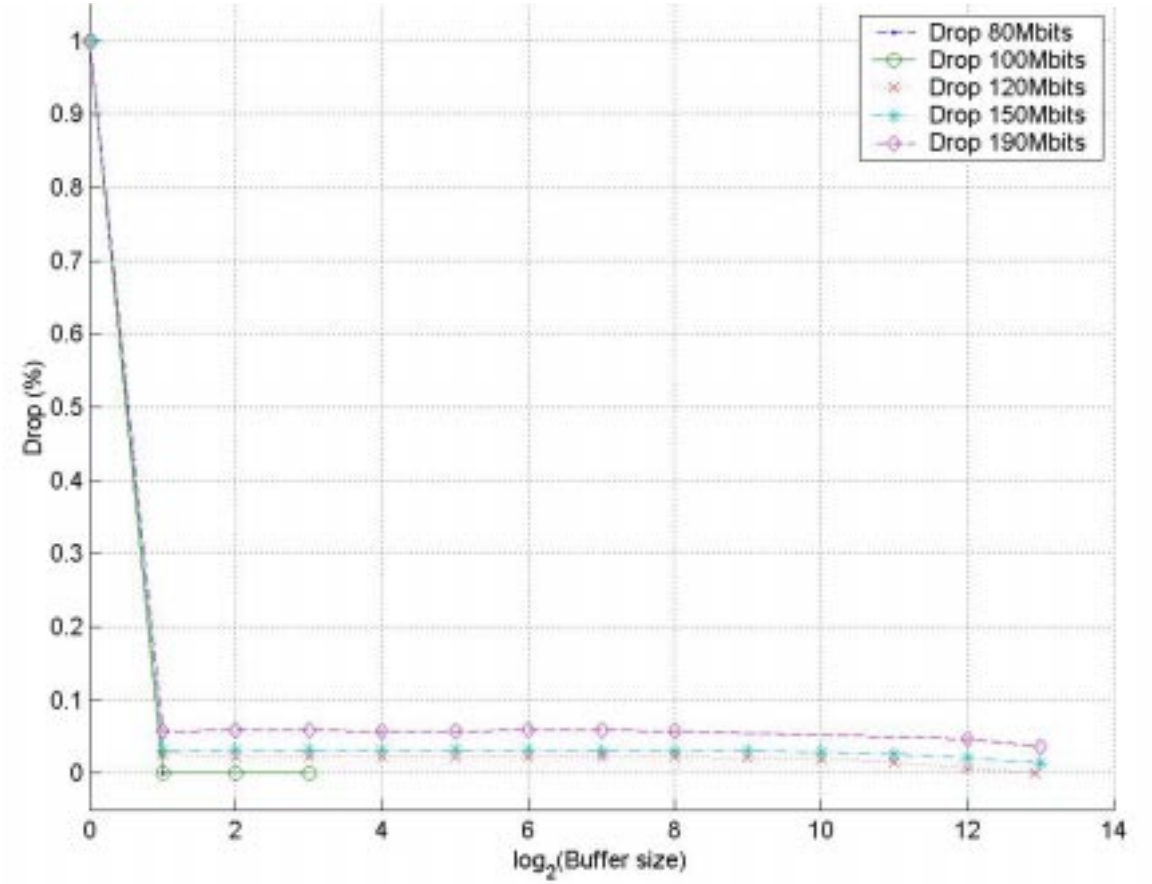
- Resources larger than a slot
  - FPGA
  - Shared Memory blocks
  - Special parallel processor
- Wrapper will make the region transparent to outside traffic
- Communication within a region could happen differently than outside



NoC Simulation using ns-2

- ns-2 is a network simulator from Univ. of Berkeley
  - Has been extensively been used for research and teaching of computer networks
- Architectural Parameters
  - Topology: 5 X 5 NoC
  - Protocol: UDP(no acknowledgement)
  - Link Bandwidth: 200 Mbits/sec
  - Routing algorithm: Static-shortest distance to destination
- Application Parameters
  - Random bursty traffic with strong bias for locality
- Performance Experiments
  - Packet delay vs. buffer size
  - Drop probability vs. buffer size
  - Packet delay vs. network load
  - Drop probability vs. network load

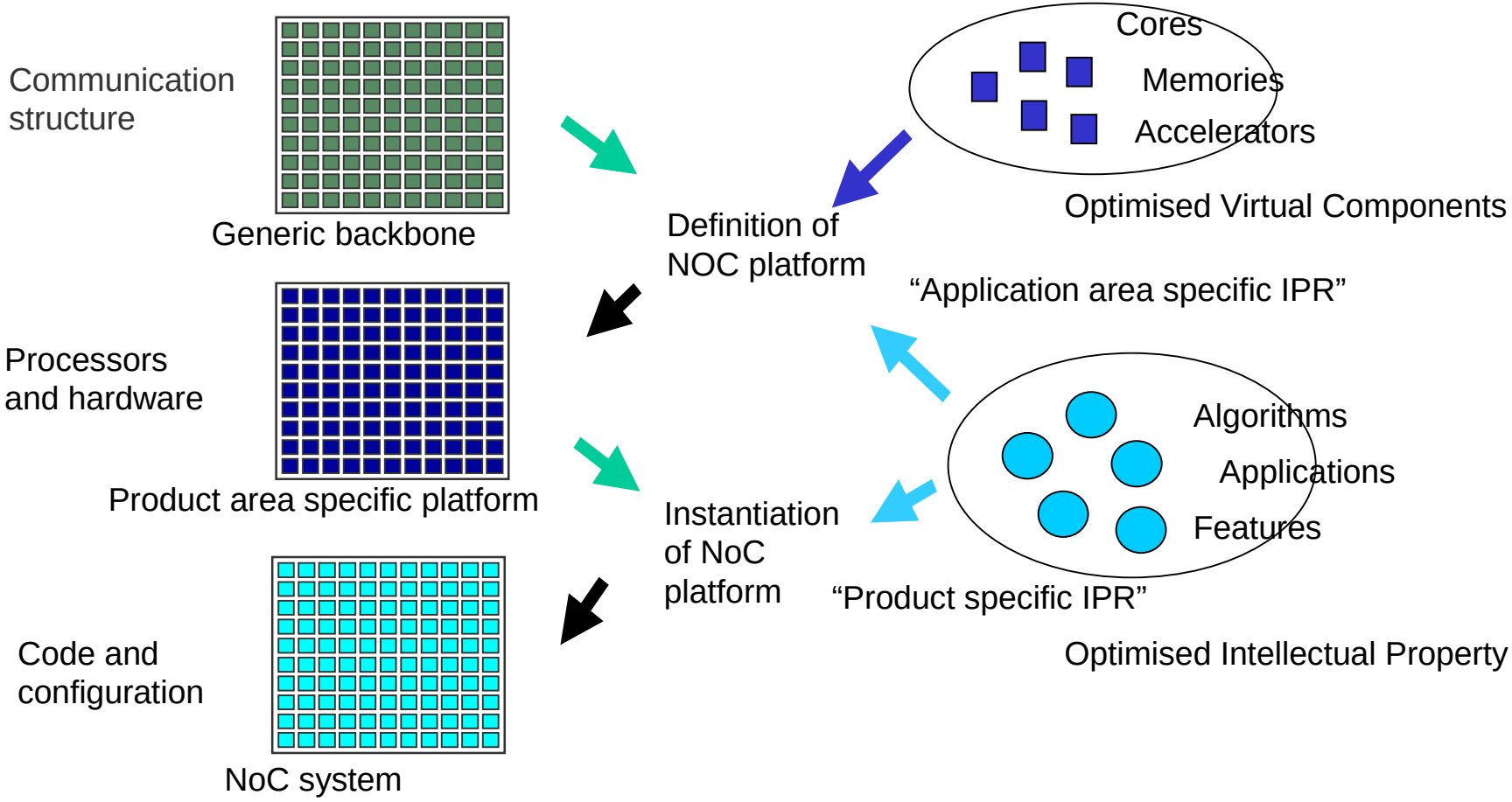
Drop probability *vs.* Buffer size



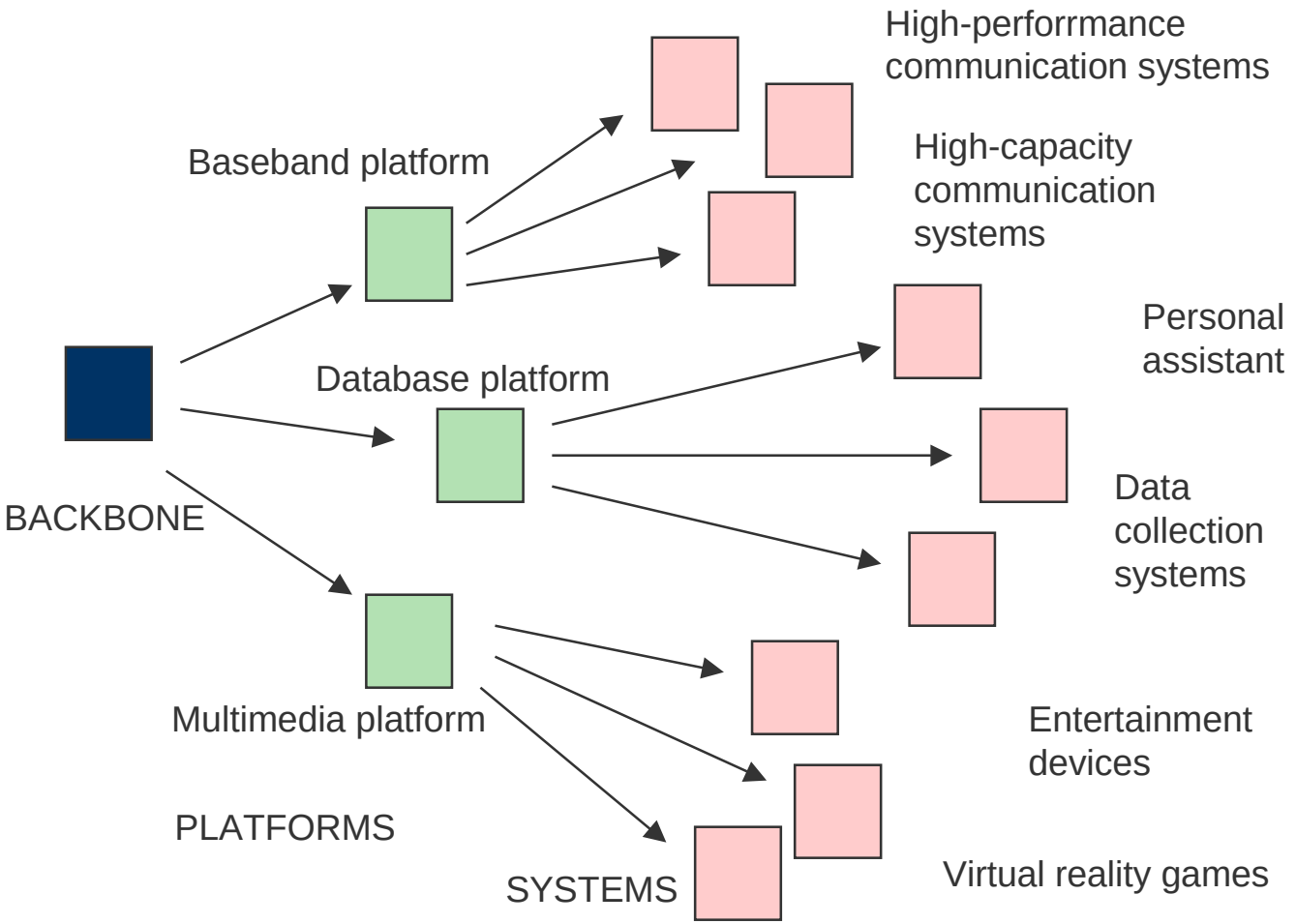
Basic requirements for NOC design methodology

- Reuse of intellectual property blocks
  - best performance/energy ratio
  - best mapping to application characteristics
- Reuse of hardware (and architecture)
  - best complexity/cost and performance/cost ratio
  - only way to even dream of achieving time-to-profit requirements
- Reuse of design methods and tools
  - only way to deal with heterogenuous application set
- Partitioning of problems
  - by encapsulation and hiding of the complexity of the overall system

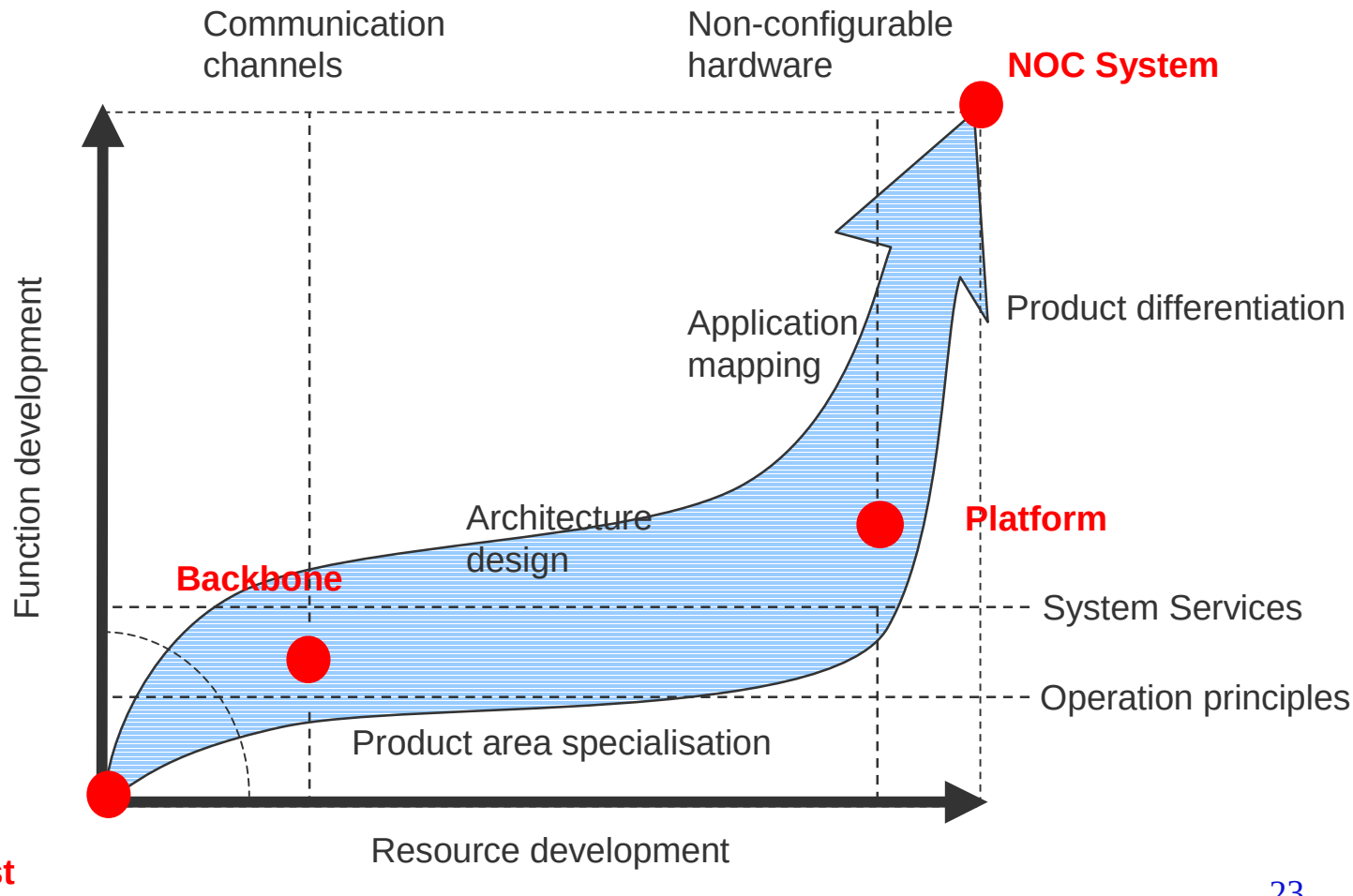
NOC Design Methodology



Development of NOC based systems



Network-on-a-Chip Design Space



Conclusions

- NoC architecture provides a SoC development platform which allows reuse at many levels
  - Reduces time to design
  - Reduces time to test
- NoC design has a lot in common with Distributed System design
- For NoC approach to become usable we require to develop new tools for
  - Evaluation of NoC architecture and estimation of performance
  - NoC Specialization
    - Resource Selection and allocation
    - Protocol specialization
  - Mapping of applications to NoC
    - Application partitioning and scheduling