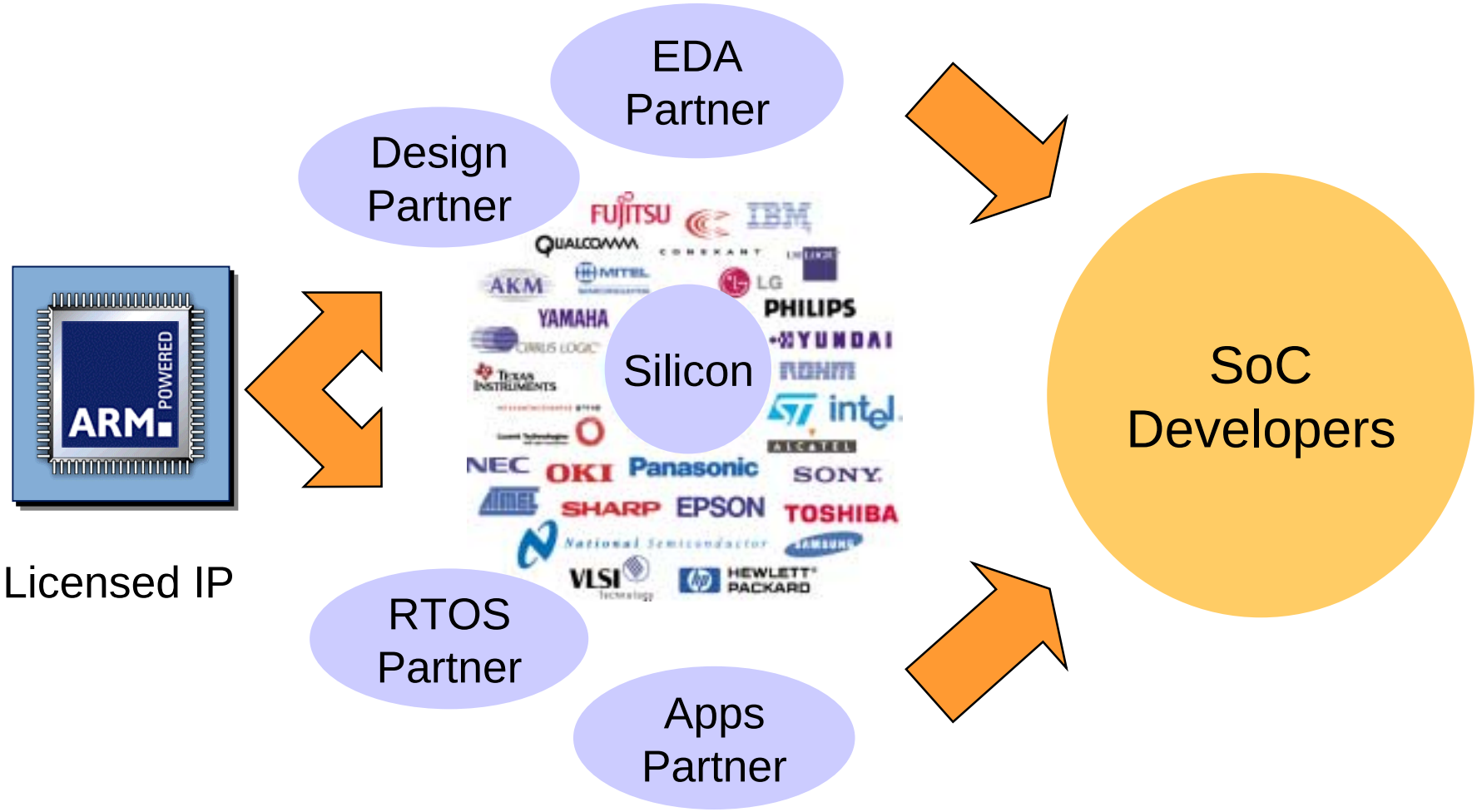
Open SystemC Initiative

SystemC Organization Perspective

Agenda

- The System Design Problem
- What is SystemC ?
- Expanding the Initiative
- Synopsys System-Level Solutions

IP Licensing Model & Challenge



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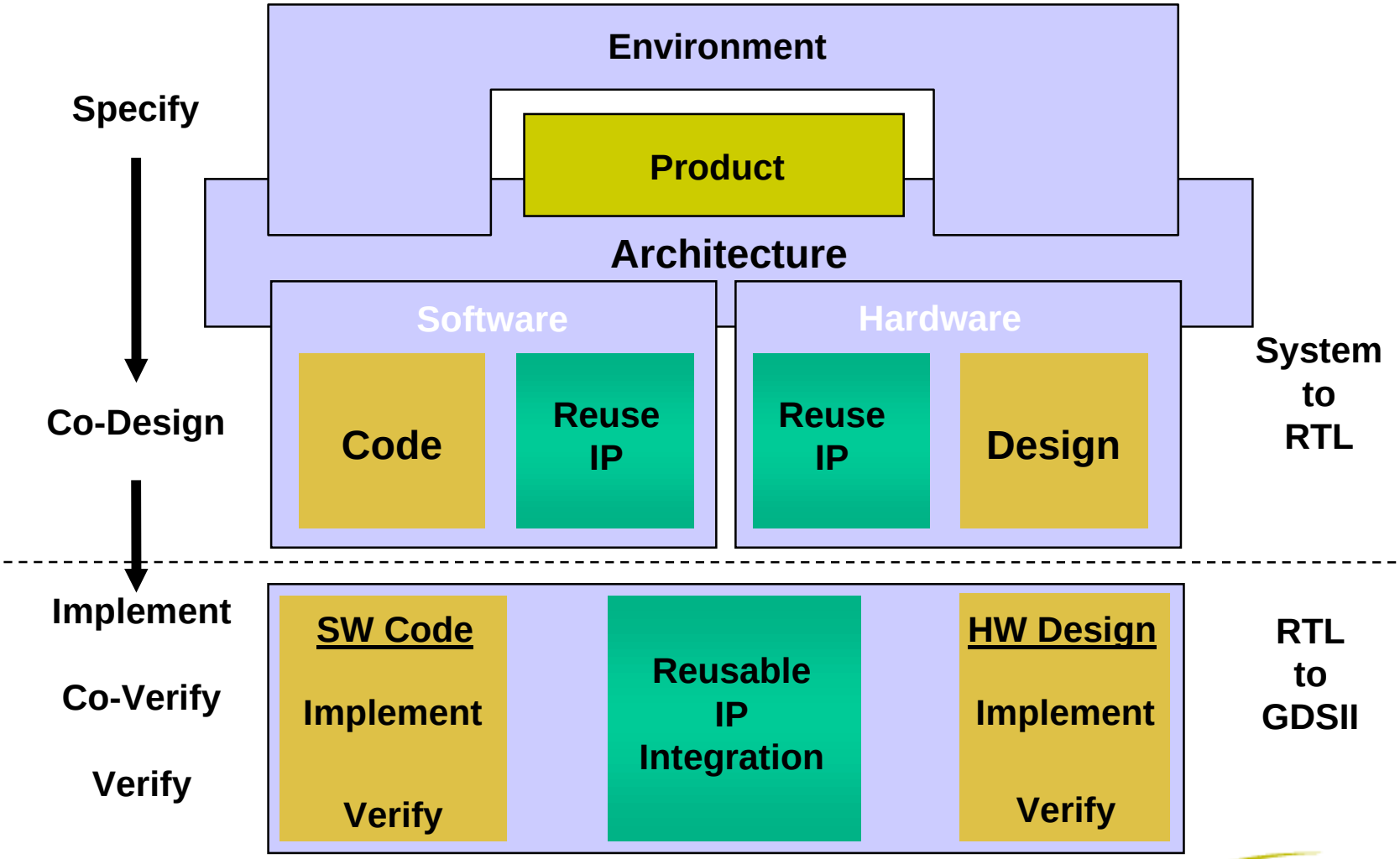
System-on-Chip Design Flow



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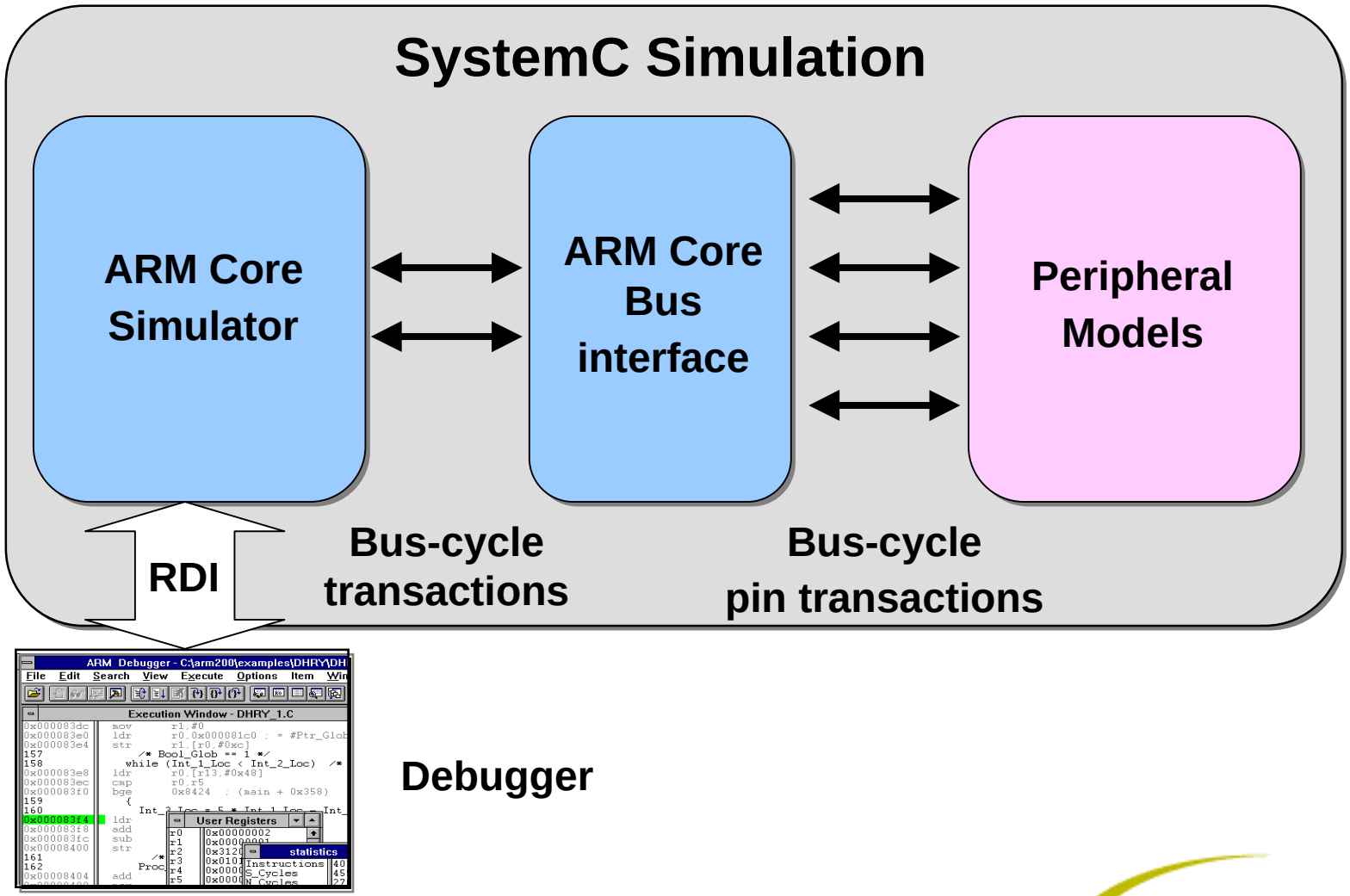
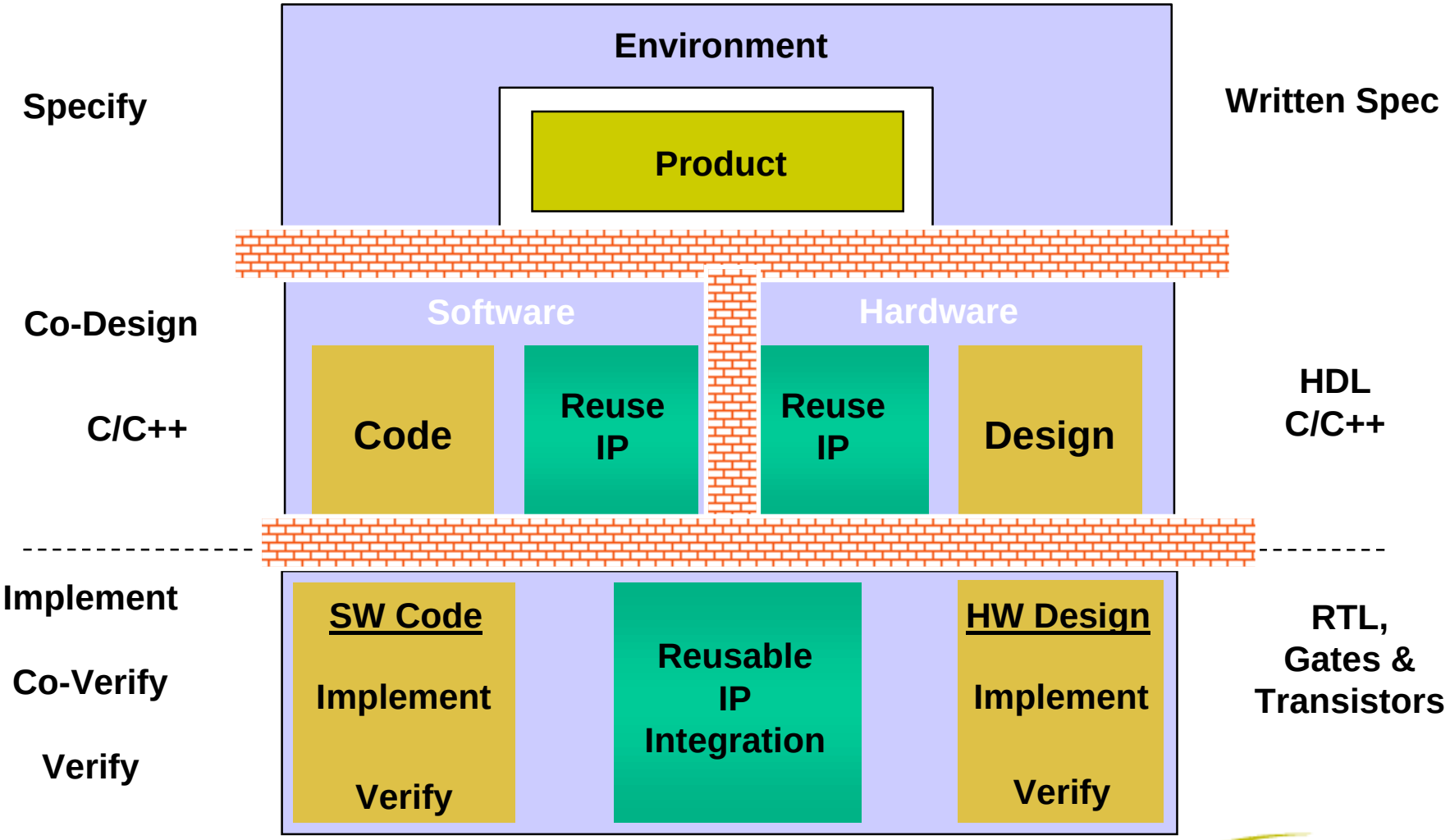
What's the Issue

- **Requirement**
  - Fast system simulation containing multiple source components
  - Capture once for multiple abstraction levels, multiple users, multiple purposes
- **Problem**
  - No common format for describing components and surrounding environment
  - Verilog or VHDL don't offer sufficient capabilities or performance for abstraction levels above RTL
- **Solution**
  - Promote a standard language at system-level (C++), that is, SystemC!

ARM SystemC Model



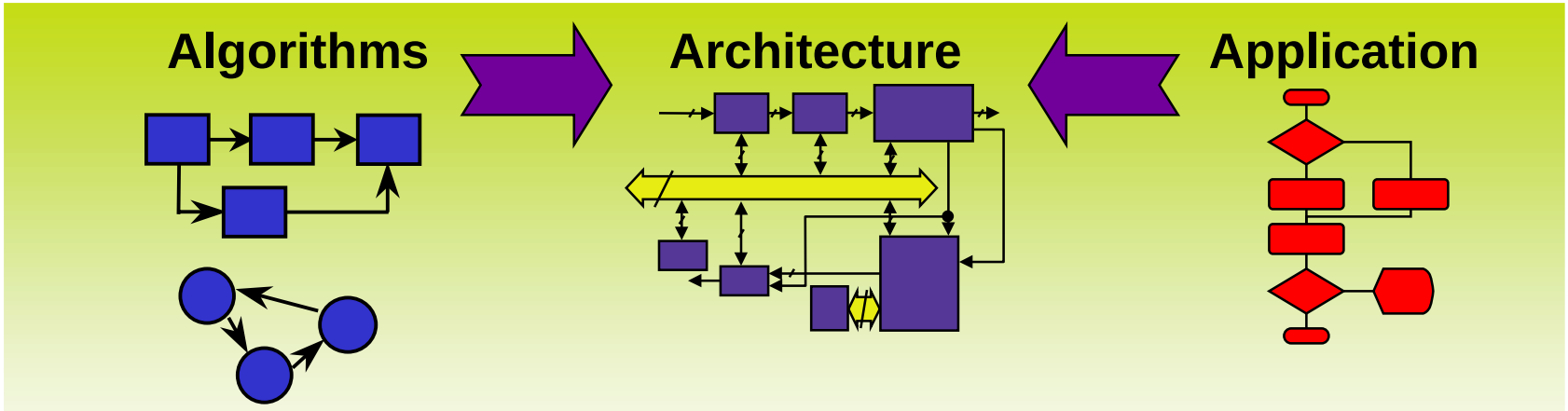
Challenge - Design Hand-off Walls



What's the Issue

- **Requirement**
  - Smooth handoffs between specification, co-design and implementation of a system
  - Capture once for multiple abstraction levels, multiple users, multiple purposes
- **Problem**
  - No common format, even within a single company, for system design methodology
- **Solution**
  - Promote a standard language and tools that can be used throughout the system-level to implementation flow

Need for Common C/C++ Approach



Common Dialect to Unify the Industry

- to model/exchange system level IP

- to build interoperable tools infrastructure

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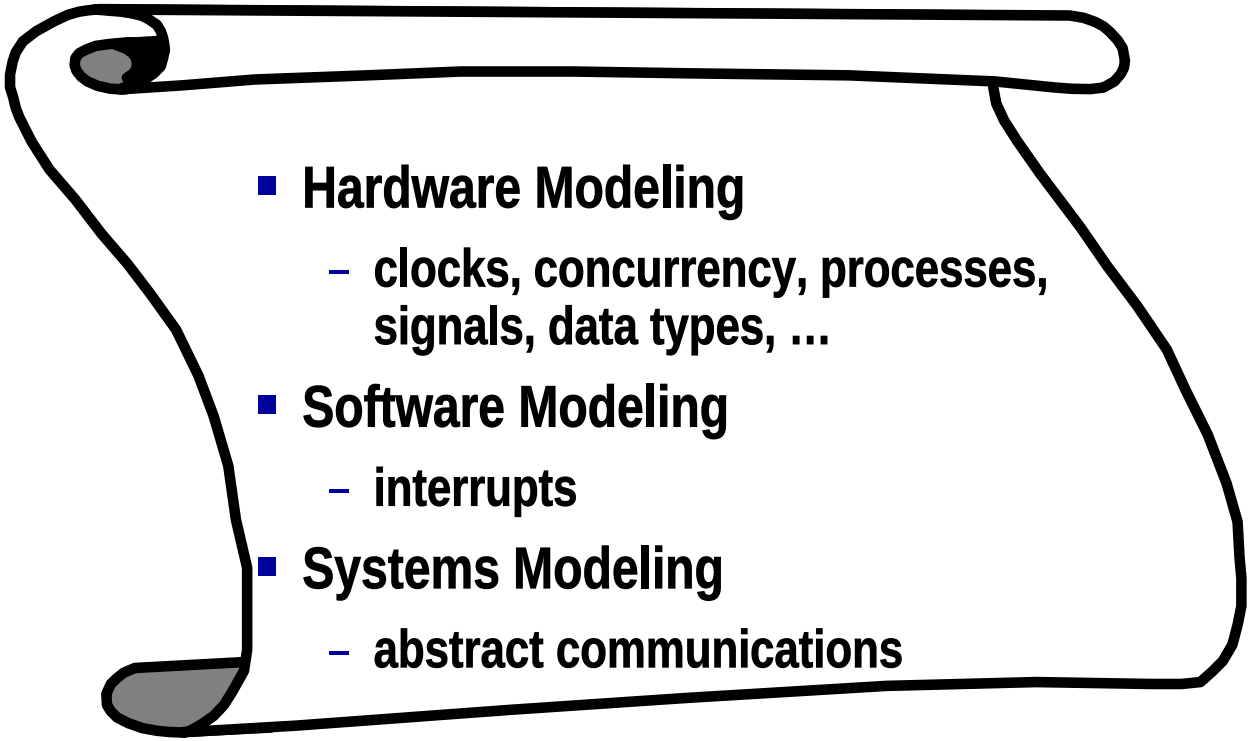
An Opportunity To Do It Right !

What is SystemC ?

SystemC: The Open Modeling Platform

Defines C++ Class Library & Simulation Kernel For:



Build and Simulate Using an ANSI C++ Compiler

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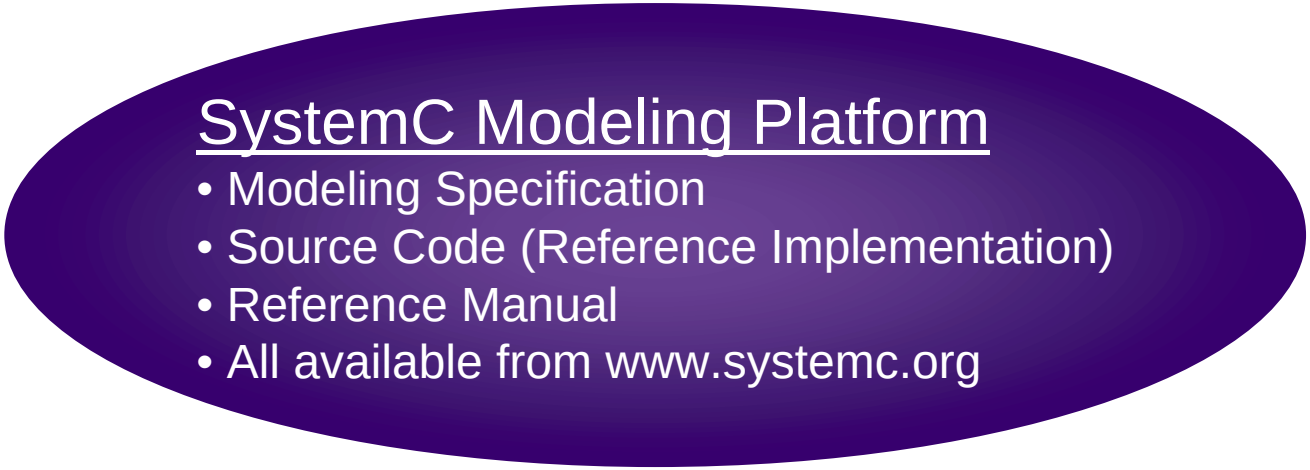
SystemC Modeling Platform



- **Mechanism for Evolution**
  - **Community members have the right and responsibility to contribute enhancements**
  - **Steering Group will drive convergence and interoperability**
- **Open Community Licensing**
  - **Ensures interoperability**
  - **Structured innovation**

What is SystemC

- A library of C++ classes
  - Processes (for concurrency)
  - Clocks (for time)
  - Hardware data types (bit vectors, 4-valued logic, fixed-point types, arbitrary precision integers)
  - Waiting and watching (for reactivity)
  - Modules, ports, signals (for hierarchy)
  - Abstract ports and protocols (abstract communications)
- A light-weight simulation kernel

SystemC Classes - Processes

- **Processes**
  - Functionality is described in a process
  - Processes run concurrently
  - Code inside a process is sequential
  - Methods as well as threads supported as processes
    - SC_METHOD
    - SC_THREAD
    - SC_CTHREAD

SystemC Simulation Kernel

- Ultra light-weight for simulation efficiency
- Cycle-based

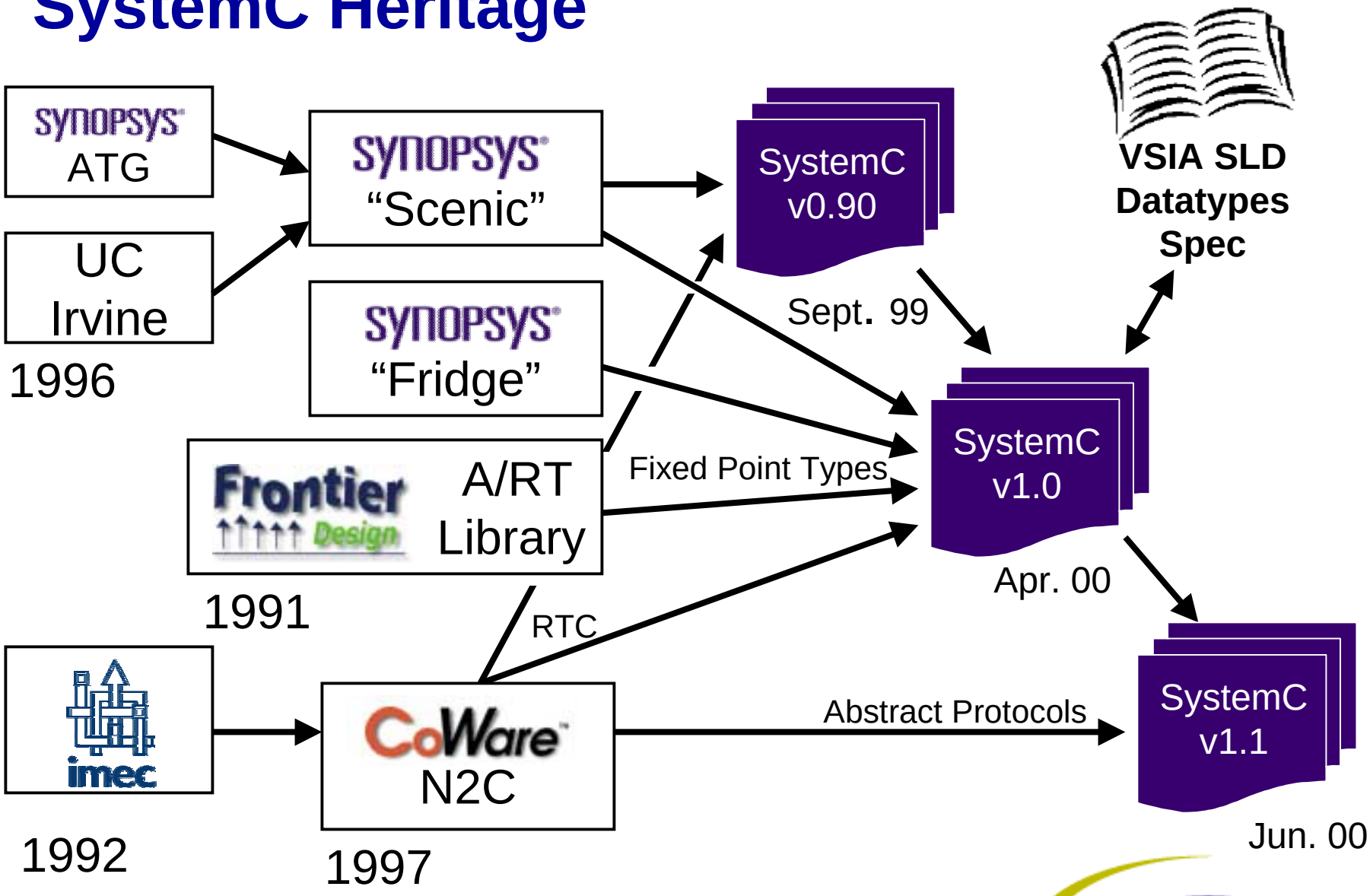
SystemC Simulation Semantics

- **Evaluate - update paradigm is used**
  - **All processes that have events at their inputs are run**
  - **When a process writes to an output signal, the value is not immediately available on the signal**
  - **After all processes have executed, all signal values are updated**
  - **Process execution order does not determine result of simulation**
  - **Each evaluate-update cycle is called a DELTA cycle**

Other Capabilities of SystemC

- Post-processing waveform visualization
  - VCD
  - WIF
  - ISDB
- Run-time error checking
  - Improper port connection
  - Array bounds violation
  - Type conversion violation

SystemC Heritage



Plus the SystemC User Community !

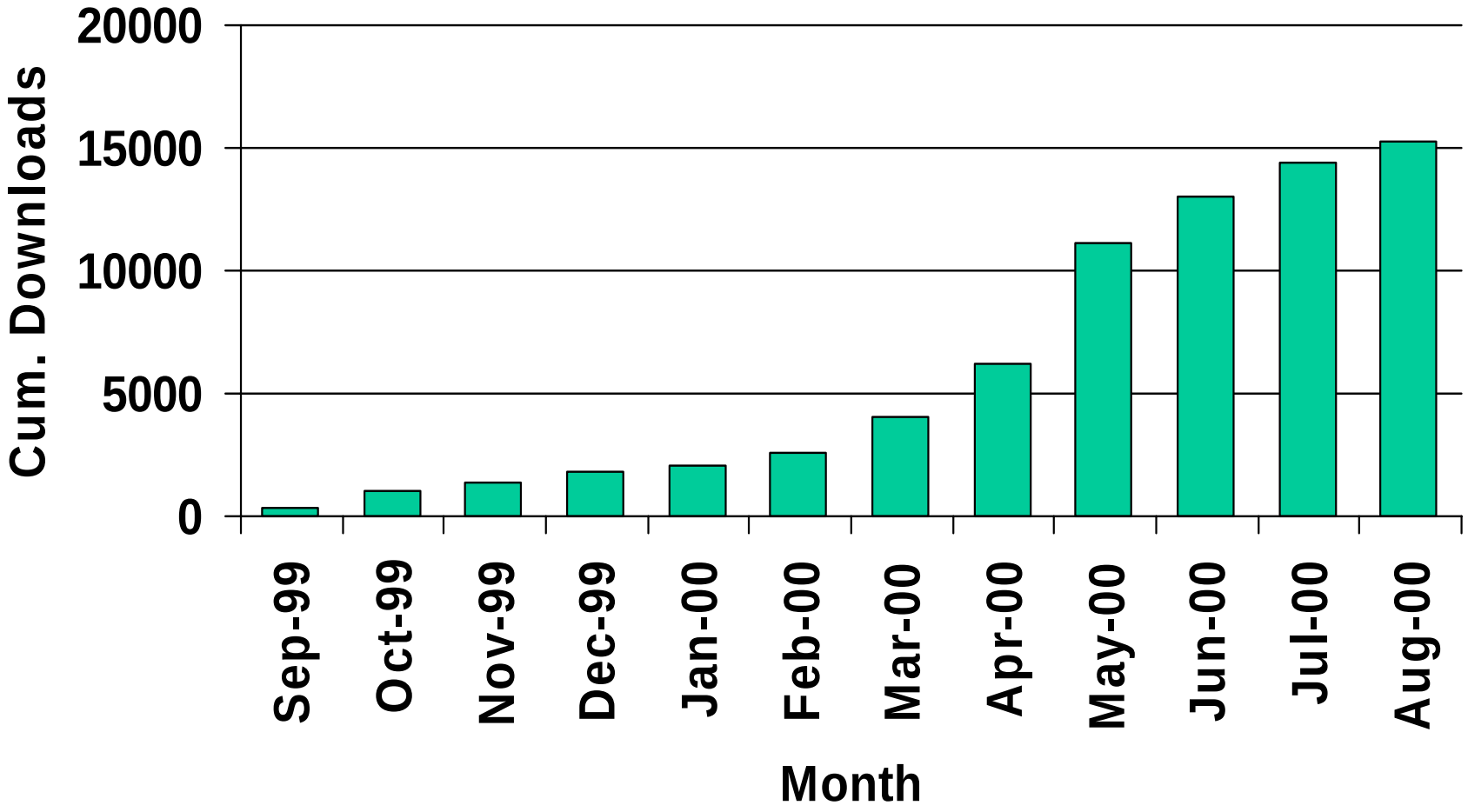
- **Thank you all for your feedback and guidance**
  - **Infineon**
  - **STMicroelectronics**
  - **Willamette HDL**
  - **Motorola**
  - **Ericsson**
  - **NEC**
  - **Red Hat**

and many more ...

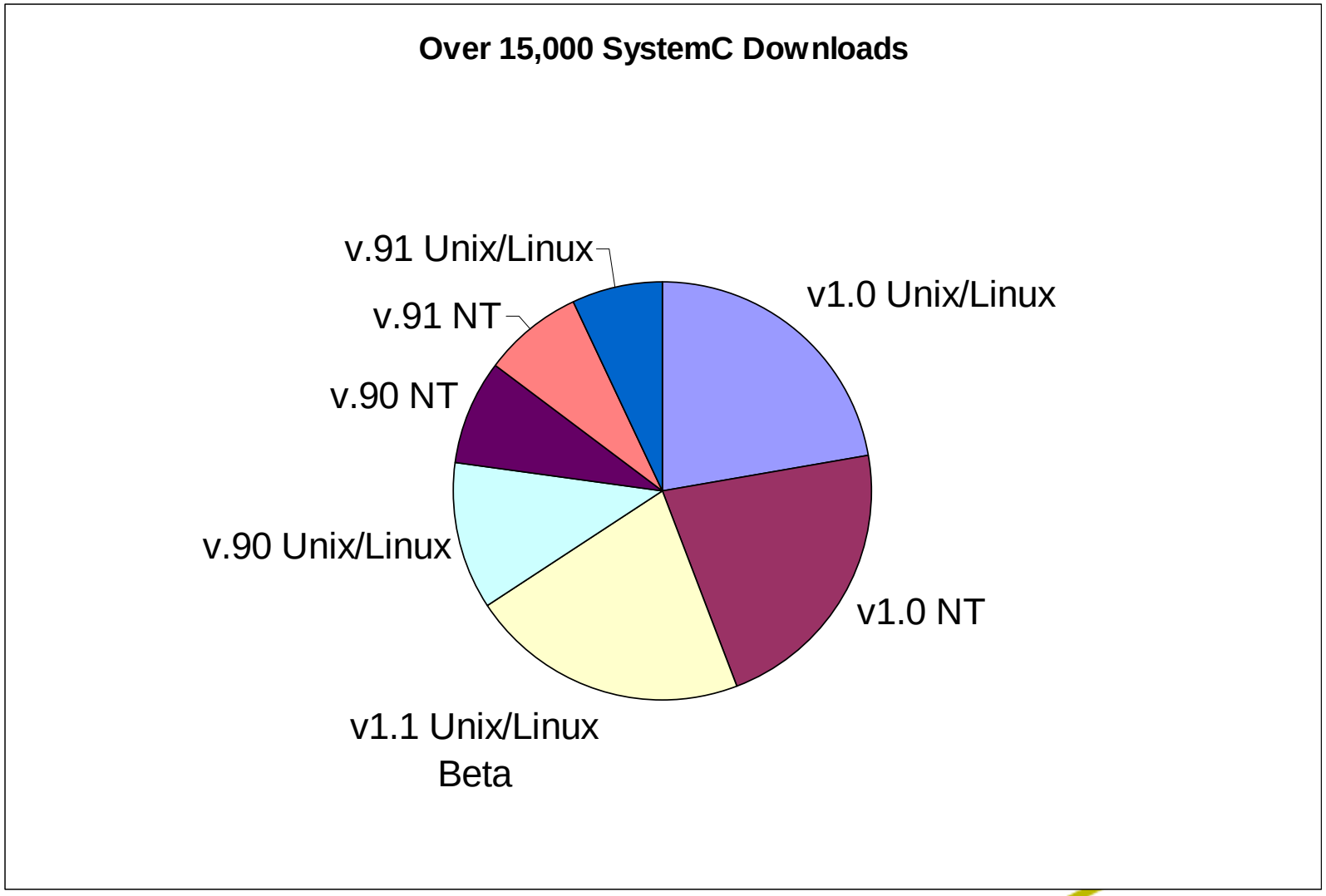
The Proof Today

- Over 5,500 registered licensees at over 500 companies
- Over 15,000 downloads through Aug 2000
- Over 20 EDA/IP products happening now !
  - Synopsys - CoCentric Family - System Studio, Fixed Point Designer, & SystemC Compiler, plus Vera, VCS, Scirocco, VMC, VhMC, & CMC
  - CoWare - CoWare N2C
  - Frontier - A/RT Designer
  - TransModeling - SystemModeler, CoDesign - SystemSim
  - Innoveda, Denali, Virtio, Blue Pacific, Veritools, Willamette HDL, C-Level Design, Dynalith, Tenison Tech, Tops-sld
  - Training - WHDL, Blue Pacific, FhG (Germany), NSKK (Japan), Doulos
  - IP - ARM, CSELT
- Aligned with VSIA SLD datatypes

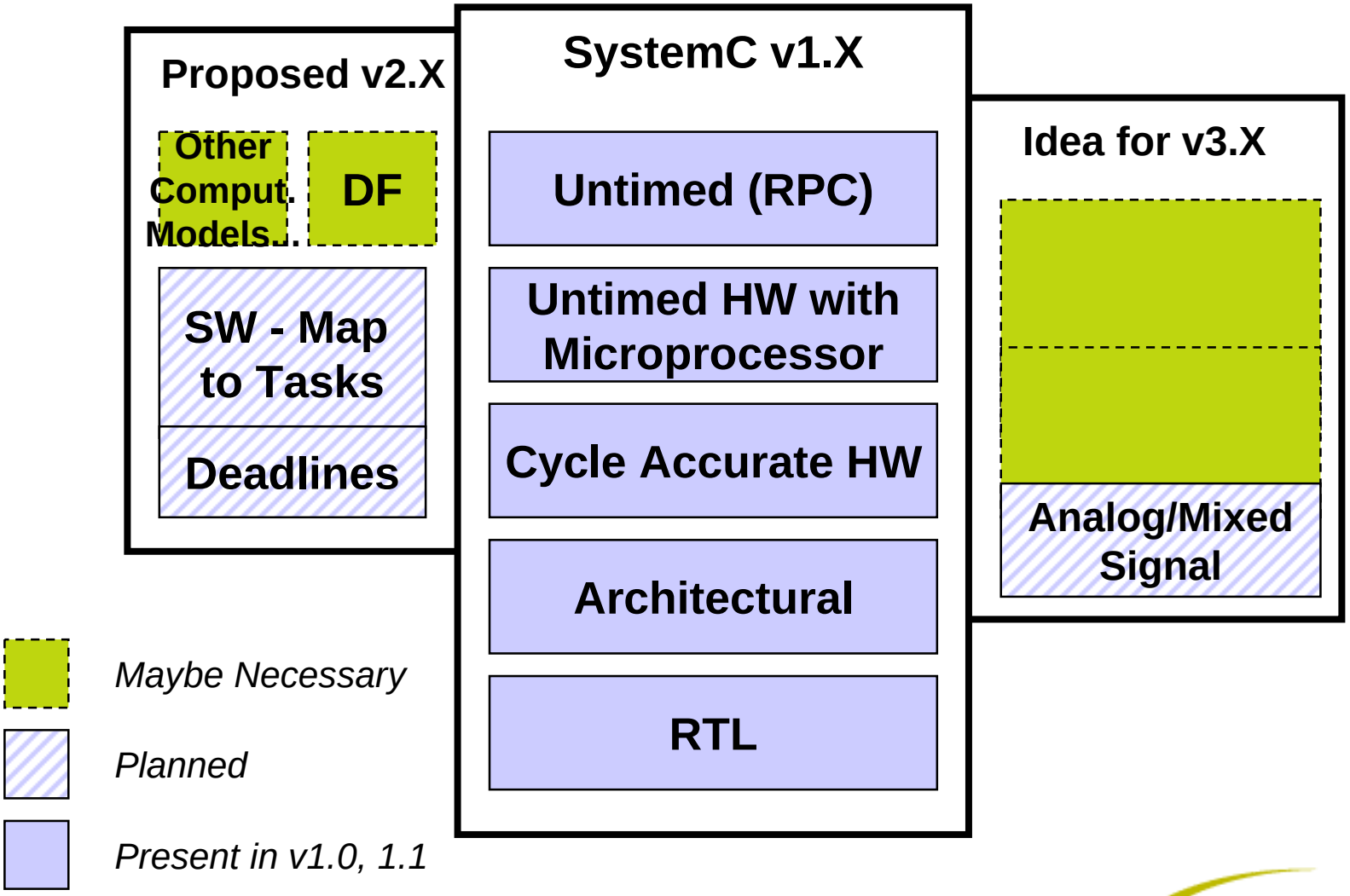
SystemC Adoption - Over 15,000 downloads



V1.0 and v1.1beta Enjoying Success



v1.X - A Complete Range of Abstraction

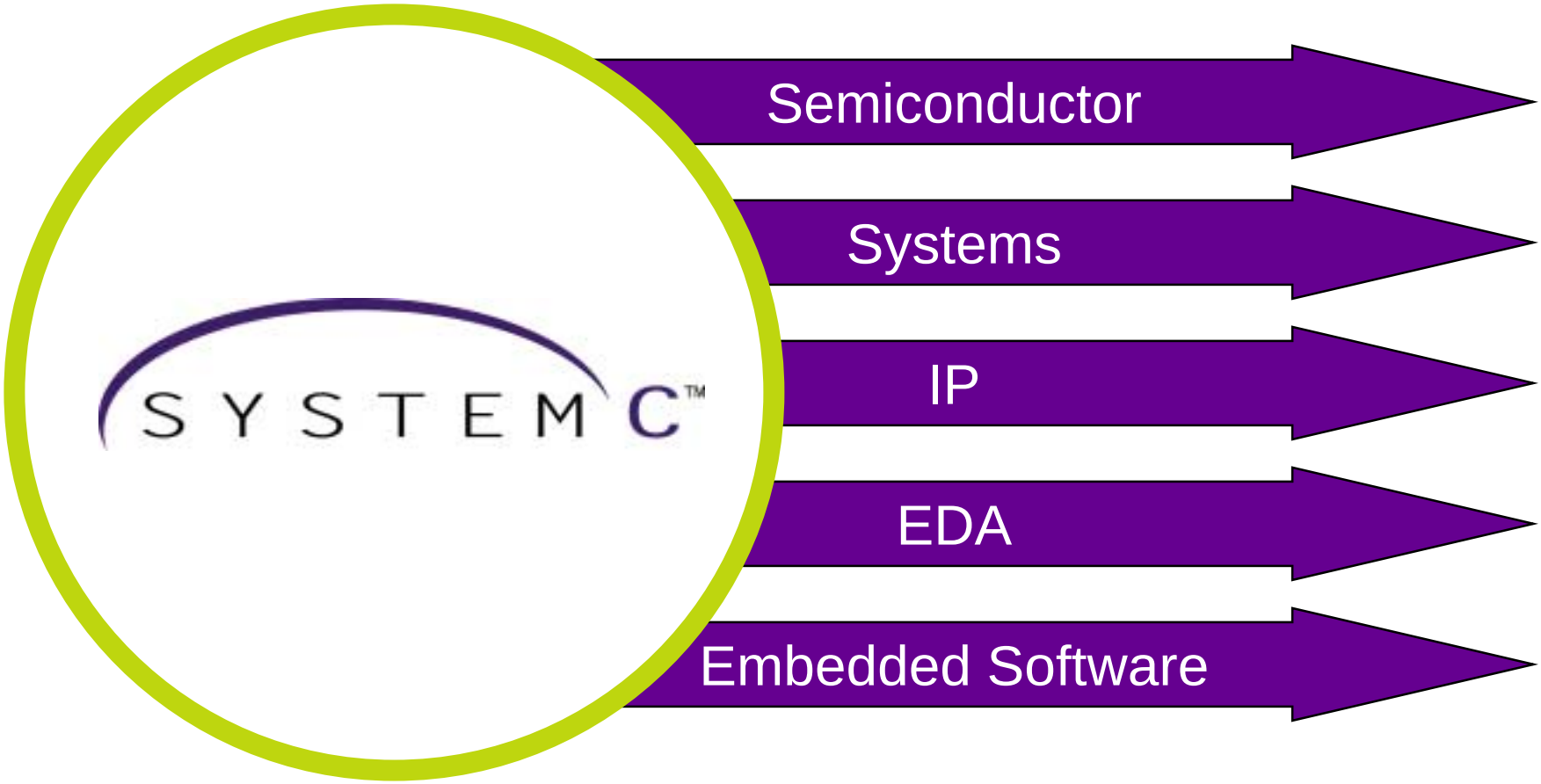


Industry Initiative

Cadence Joins SystemC Initiative

- **Cadence to use System-Level Modeling and Methodology Expertise in Conjunction with Industry Leaders to Produce High-Level Modeling Language**
- **SAN JOSE, Calif.--(BUSINESS WIRE)--June 5, 2000-- Cadence Design Systems, Inc. (NYSE:CDN - news), the world's leading supplier of electronic design products and services, today announced that it will join the Open SystemC Initiative.**

Industry Alignment Required



Feedback from the Industry

- **Open Community Source Model is Great**
  - **Fast Evolution**
  - **Open Access, Support and Contribution via web**
  - **Ensures interoperability**

  => Keep this process going !

- **Community benefits from Cadence and Mentor fully onboard**
  - **SystemC "language" needs to be open for use without any licensing restrictions**
  - **Language direction and growth needs to be in the hands of independent organization of SystemC users**

  => Formalize and fund Steering Group and OSCI membership as an independent organization

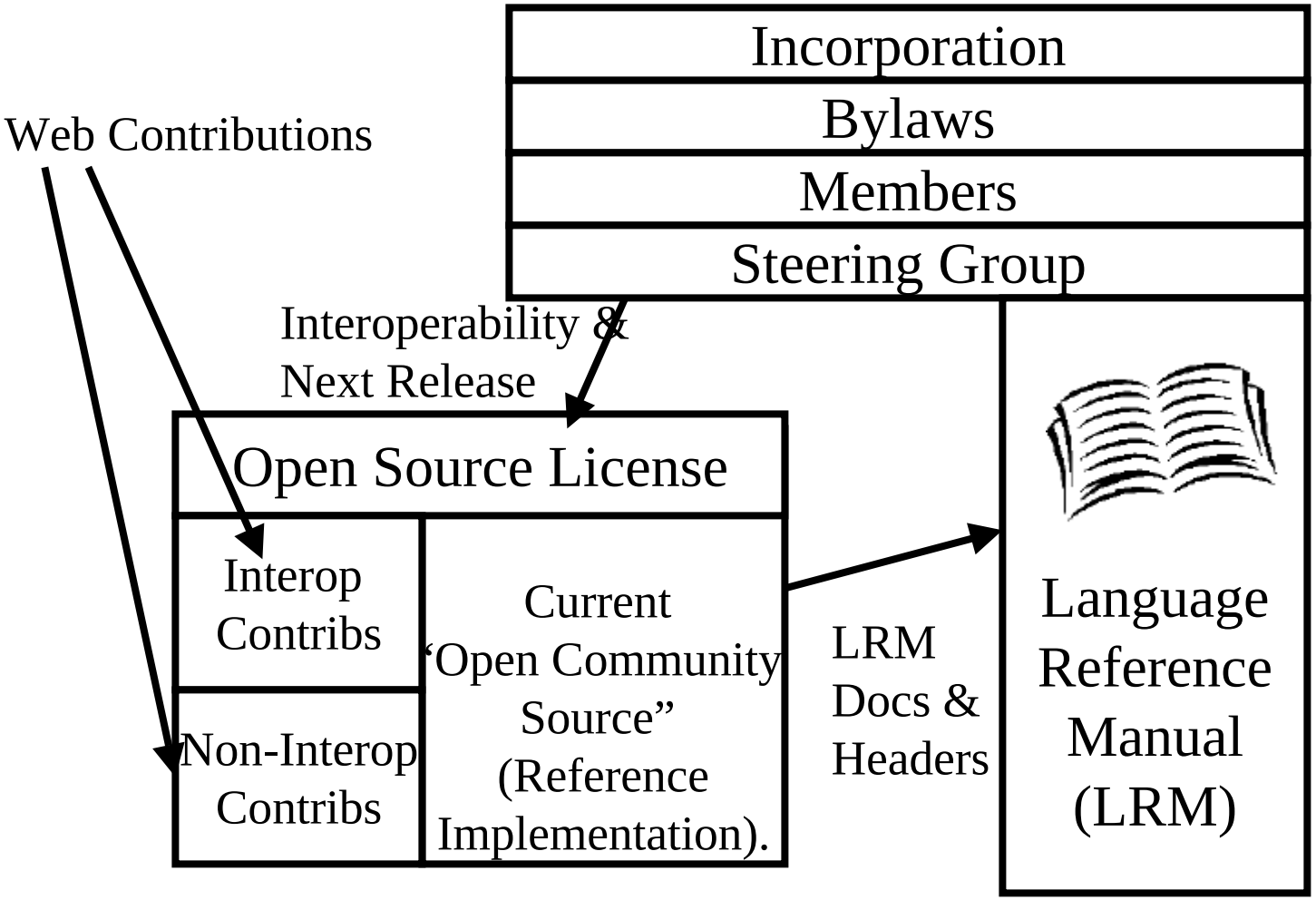
Introducing OSCI Organization

- Independent organization
  - Independently funded and incorporated
  - Steering Group developed bylaws
  - Headed by elected 13 company Steering Group

... that guides future of SystemC

  - Owns and publishes LRM
  - Drives ongoing releases of SystemC
    - Selects contributions for inclusion in reference implementation
    - Sets vision and key requirements for future additions

OSCI - Independent Organization



SYSTEMC™

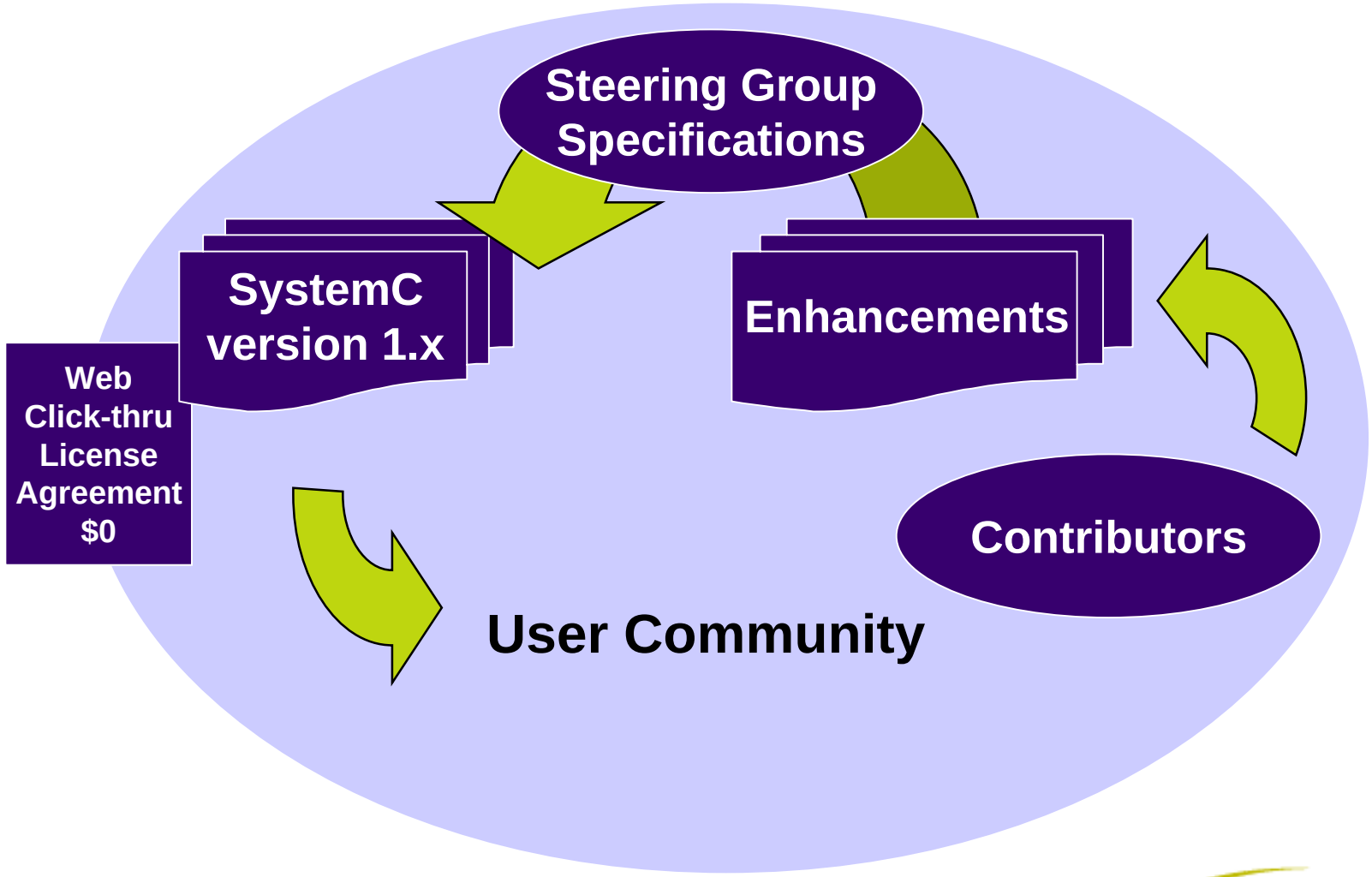
We're Headed for Success !

- The industry wants a single open solution
- SystemC has all the right Success Factors
  - Community support
    - Huge registered user base - de facto standard !
    - IP & EDA Tool Support available now !
  - Fast Evolution
  - Open Technology
- SystemC and tools solve system level design problems
  - System level modeling and analysis with IP
  - Smooth flow from spec to implementation
- Join us !

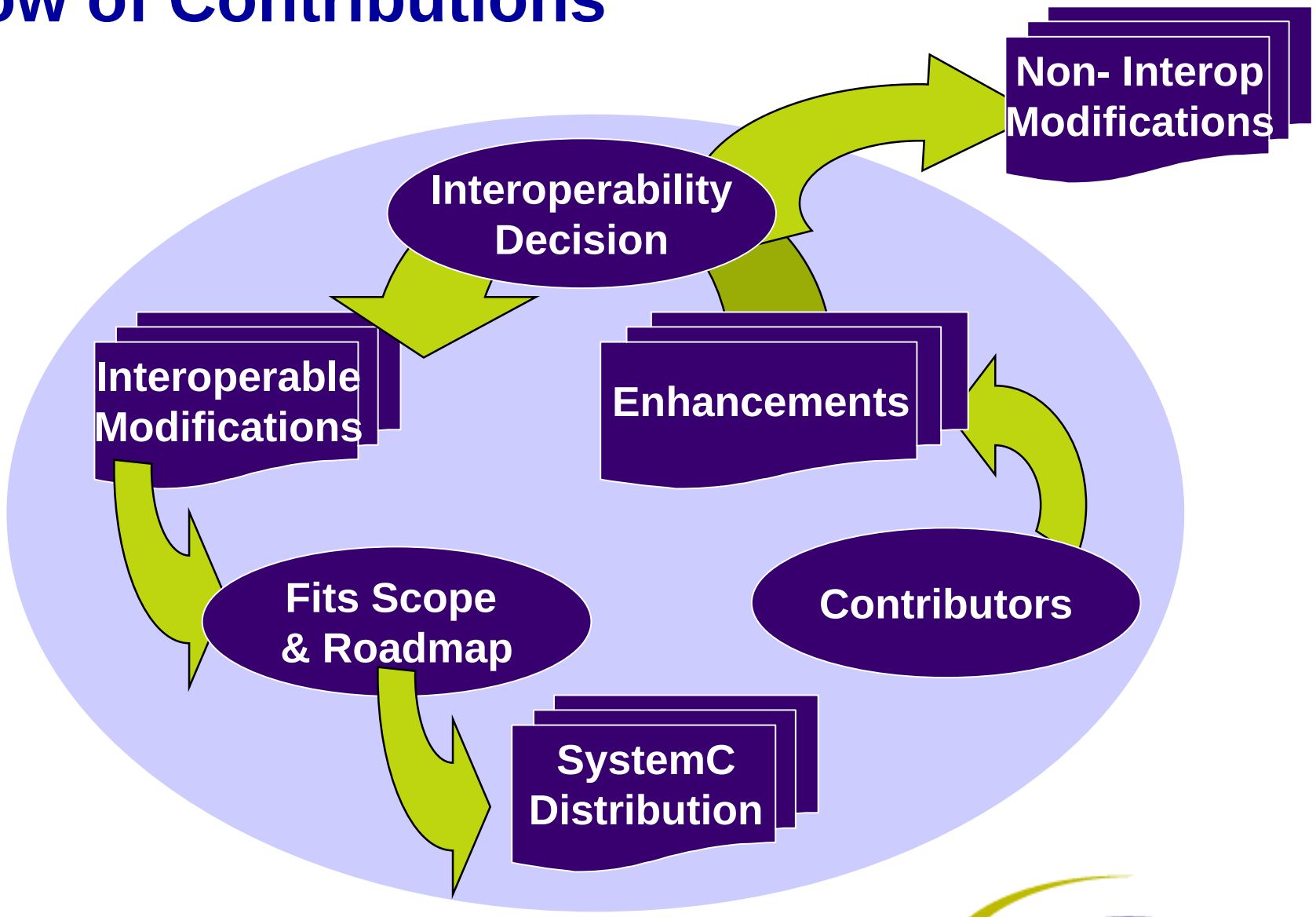
SYSTEMC™

Appendix

Open Community Licensing: Interoperability and Structured Innovation



Flow of Contributions



SystemC Product Briefs

All product claims contained within are provided by the respective supplying company.

ARM SystemC Model

- ARM SystemC Model
- SystemC enabled model for system design
- Product is still in pre-announce stage

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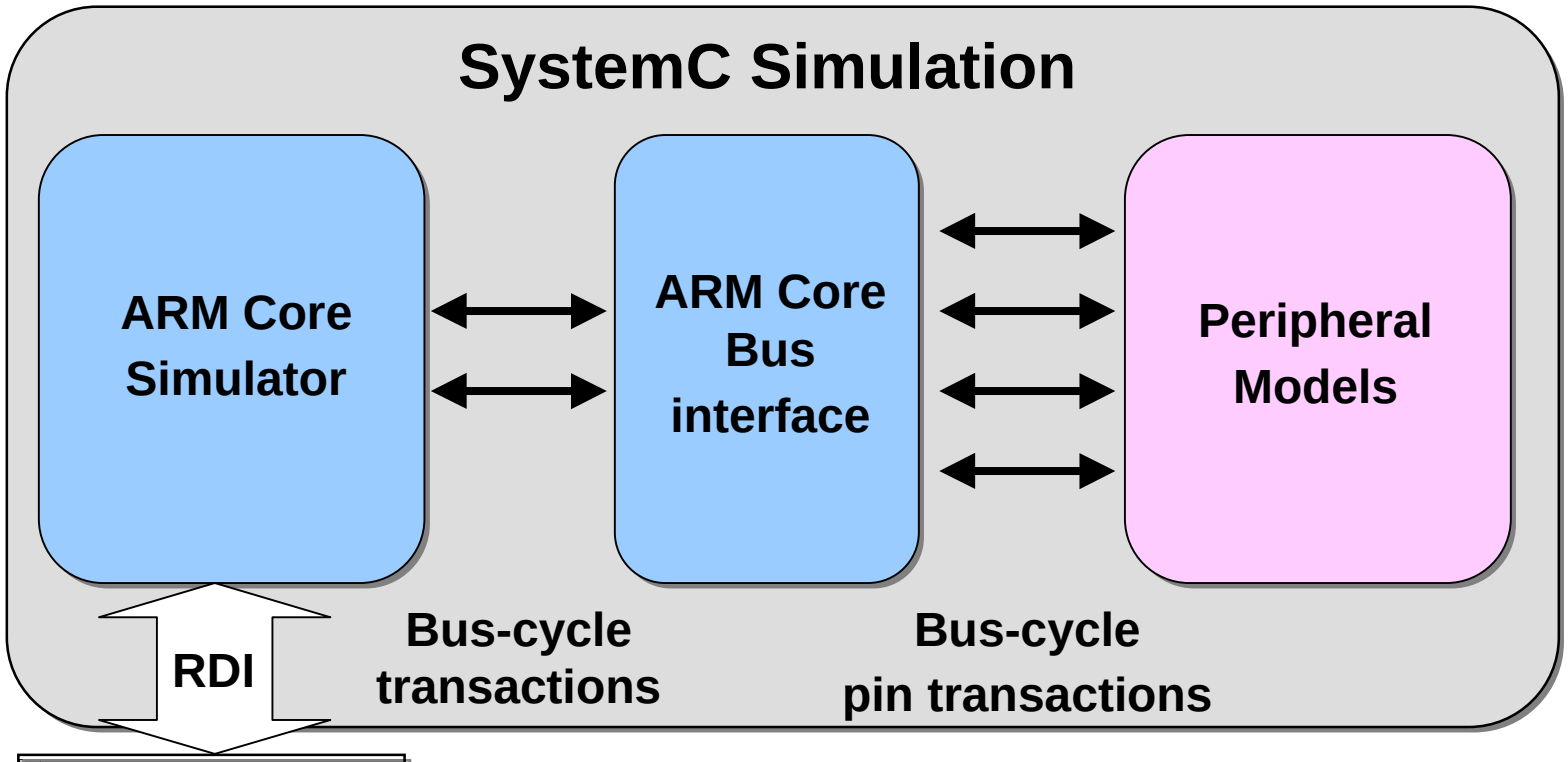
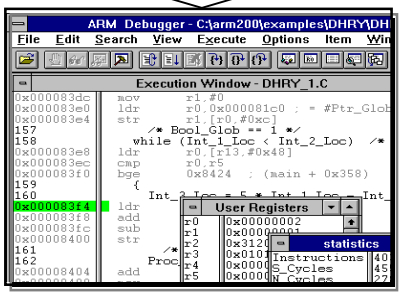
ARM SystemC Model





Debugger

Blue Pacific Computing BlueWave

- Blue Pacific's BlueWave is a simulation GUI, including waveform viewer that can be used to view and analyze VCD results on Linux, Unix, Windows, including SystemC outputs. BlueWave Student version is free.

- Enables visualization and analysis of SystemC modeling

- Contact Blue Pacific at: info@bluepc.com of find us on the web at www.bluepc.com, phone: (858) 484-7500

Blue Pacific Computing

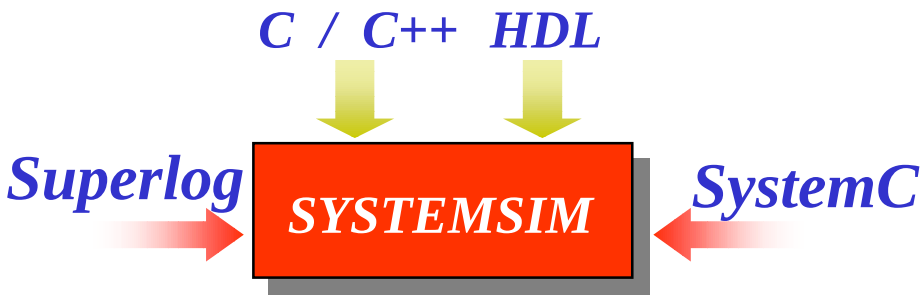
SystemC Classes

- Three-day SystemC On-Site Classes focussing on SystemC for VHDL and Verilog Designer with additional two-day foundational course on C and C++
- Teaches SystemC modeling and simulation to people with traditional Verilog or VHDL background.
- Contact Blue Pacific at info@bluepc.com or find us on the web at www.bluepc.com, phone: (858) 484-7500

SYSTEMC™

SYSTEMSIM™

- Multilingual simulator, supporting Verilog, Superlog, C, C++ and SystemC, without interfaces or co-simulation

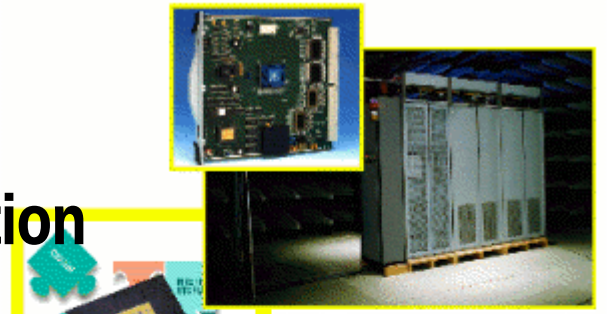


- Allows SystemC models to be called from alternative language constructs to provide a fast, usable method to solve alternative language IP and legacy code issues
- Contact Co-Design Automation, Inc, www.co-design.com, info@co-design.com

Telecom Italia Group

Vip library™

- **Vip Library: a wide set of customizable and flexible system level Intellectual Property Soft Cores to answer Information and Communication Technologies Product requirements**



- **Availability of SystemC Core description to stress architectural exploration before HW/SW partitioning is performed.**

- **Contact CSELT S.p.A, *viplibrary@cselt.it,***

  Visit Booth 4653 at DAC 2000.

SYSTEMC™

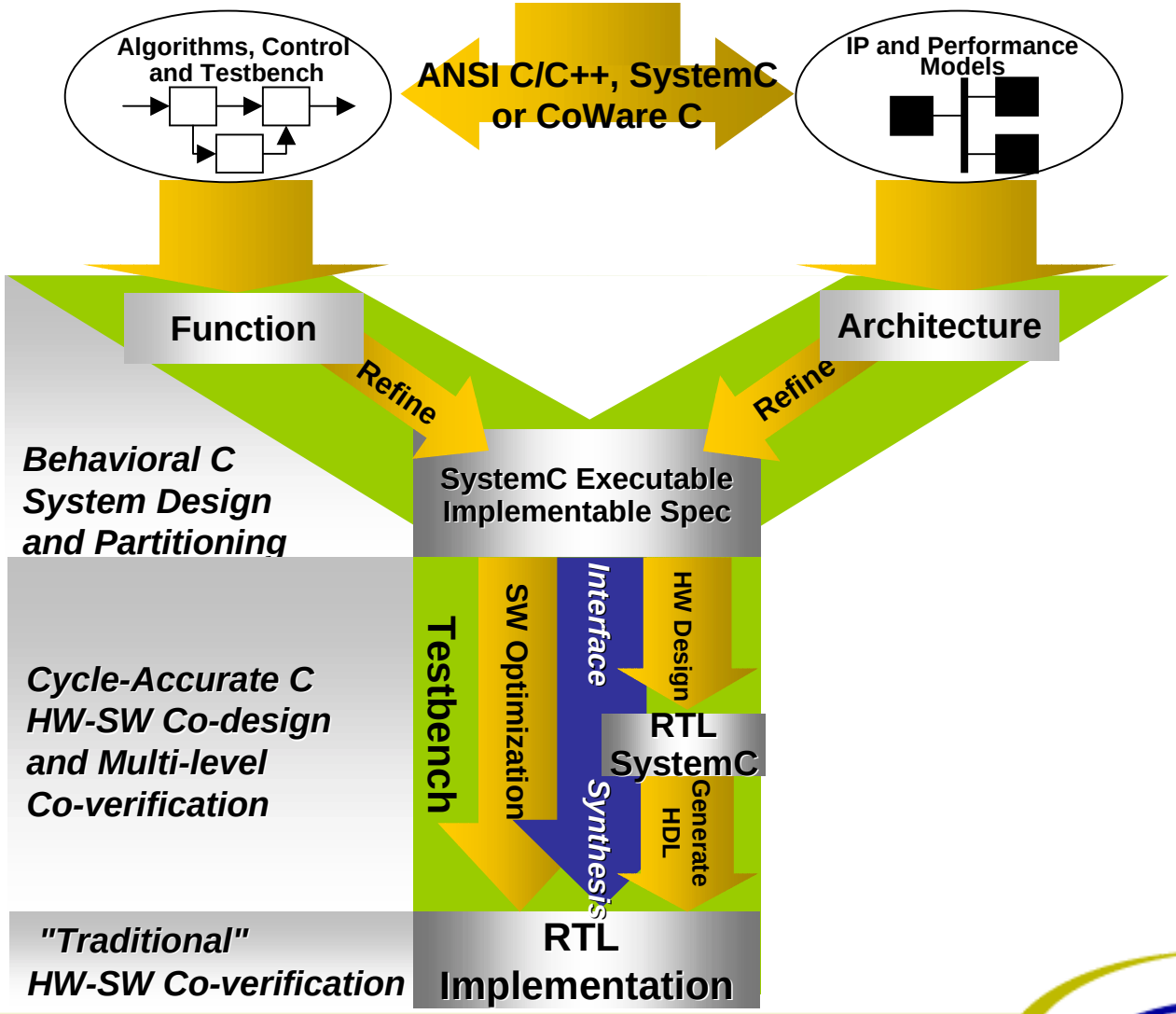
CoWare N2C™

- **CoWare N2C - Napkin to Chip in Half the Time. Full SystemC Co-Design Environment featuring:**
  - **Specification**
  - **Partitioning**
  - **Co-implementation**
  - **Co-verification**

  } **Analysis at every stage**
- **Read in and write out SystemC from CoWare N2C**
  - **CoWareC or SystemC in**
  - **CoWareC, SystemC, VHDL and Verilog out**
- **Visit DAC booth #4745 or www.CoWare.com**

SYSTEMC™

CoWare N2C System-Level Design Flow



Databahn Memory Subsystem Generator

- Databahn, an on-line tool, generates synthesizable memory controller cores and automatically produces all C-level verification support for the associated memory subsystem
- Produces SystemC models of these cores
- Contact: Steven Shrader (208) 376-6030, steven@denalisoft.com or visit our website at www.denalisoft.com

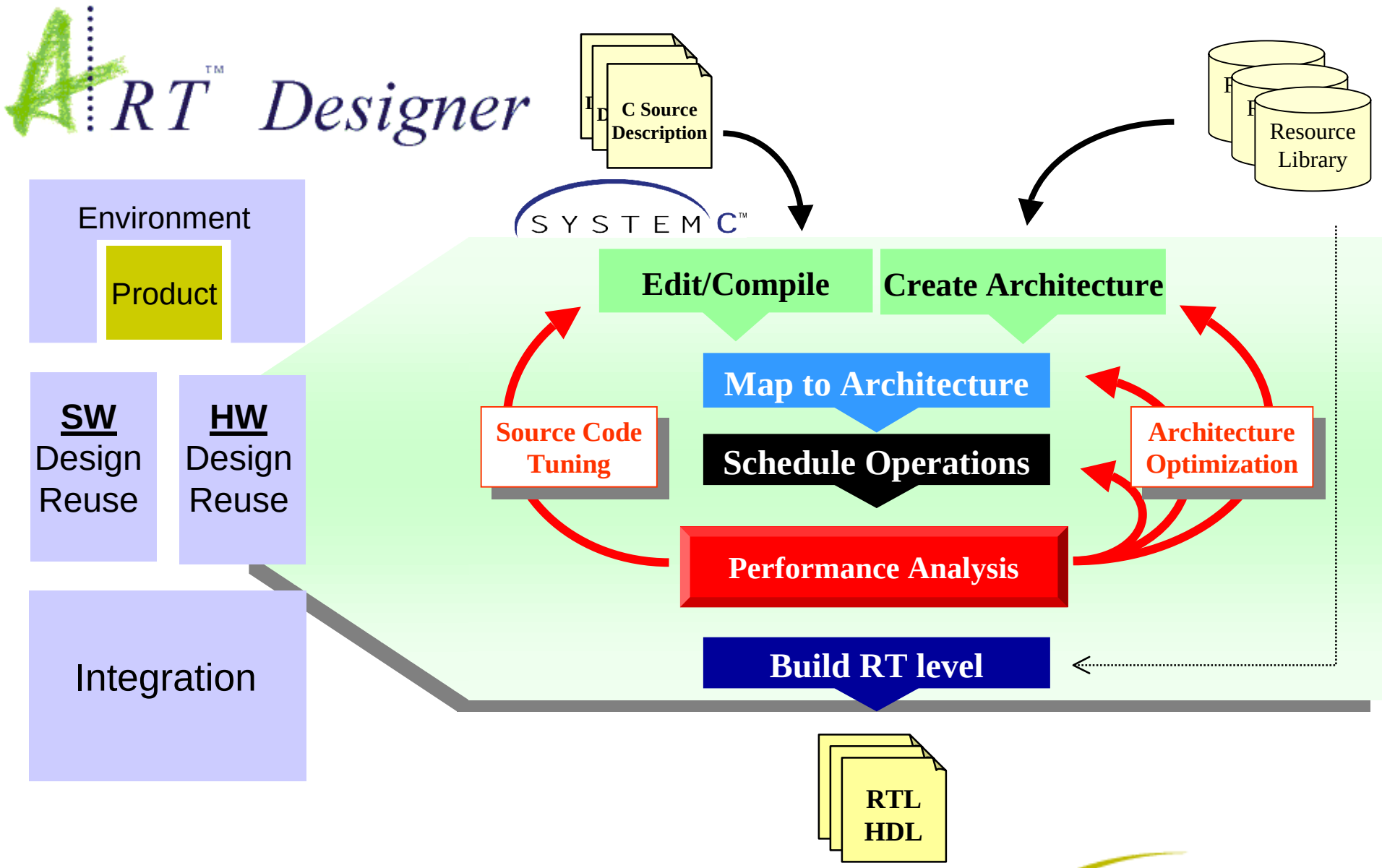
SYSTEMC™

Frontier Design

ART™ Designer

- **Architectural Synthesis using ANSI C or SystemC input:**
  - State-of-the-art Data-flow Analysis
  - Resource Allocation and Assignment
  - Automatic Scheduling and Controller Generation
  - Detailed Performance-analysis Functions
  - Pipelined VLIW Controller Architecture
  - ASIC and FPGA Implementation Paths to VHDL and Verilog
- **Performs SystemC-based architectural synthesis**
- **Contact marc_vancanneyt@frontierd.com (Europe), doug_johnson@frontierd.com (US) or visit www.frontierd.com for more information**

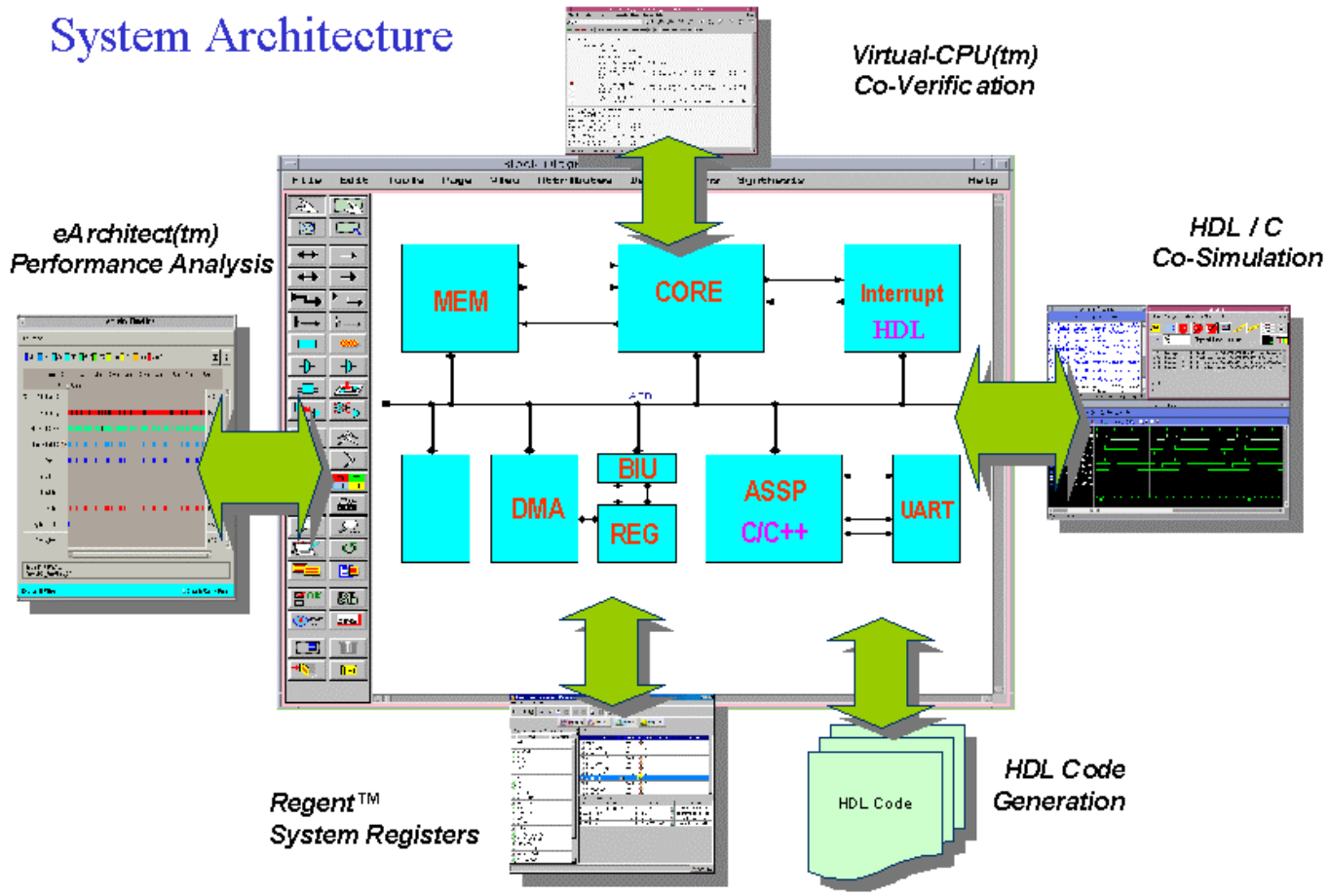
SYSTEMC™


ART™ Designer
C Source Description
Resource Library
SYSTEMC™
Environment
Product
SW Design Reuse
HW Design Reuse
Integration
Edit/Compile
Create Architecture
Map to Architecture
Source Code Tuning
Schedule Operations
Architecture Optimization
Performance Analysis
Build RT level
RTL HDL

- Systems-Level Design environment for defining and verifying system architecture, Hardware/Software co-verification, Register Definition. Includes Embedded Systems support, Complete code-coverage debug and analysis. Built upon the strongest graphic entry tool in the industry, Visual HDL. Truth-table, flowchart, Finite-State Machine, Block Diagram
- Language design via SystemC, C/C++, Verilog, VHDL

- Come see Innoveda at booth (3101), www.innoveda.com, or (800) 223-8439

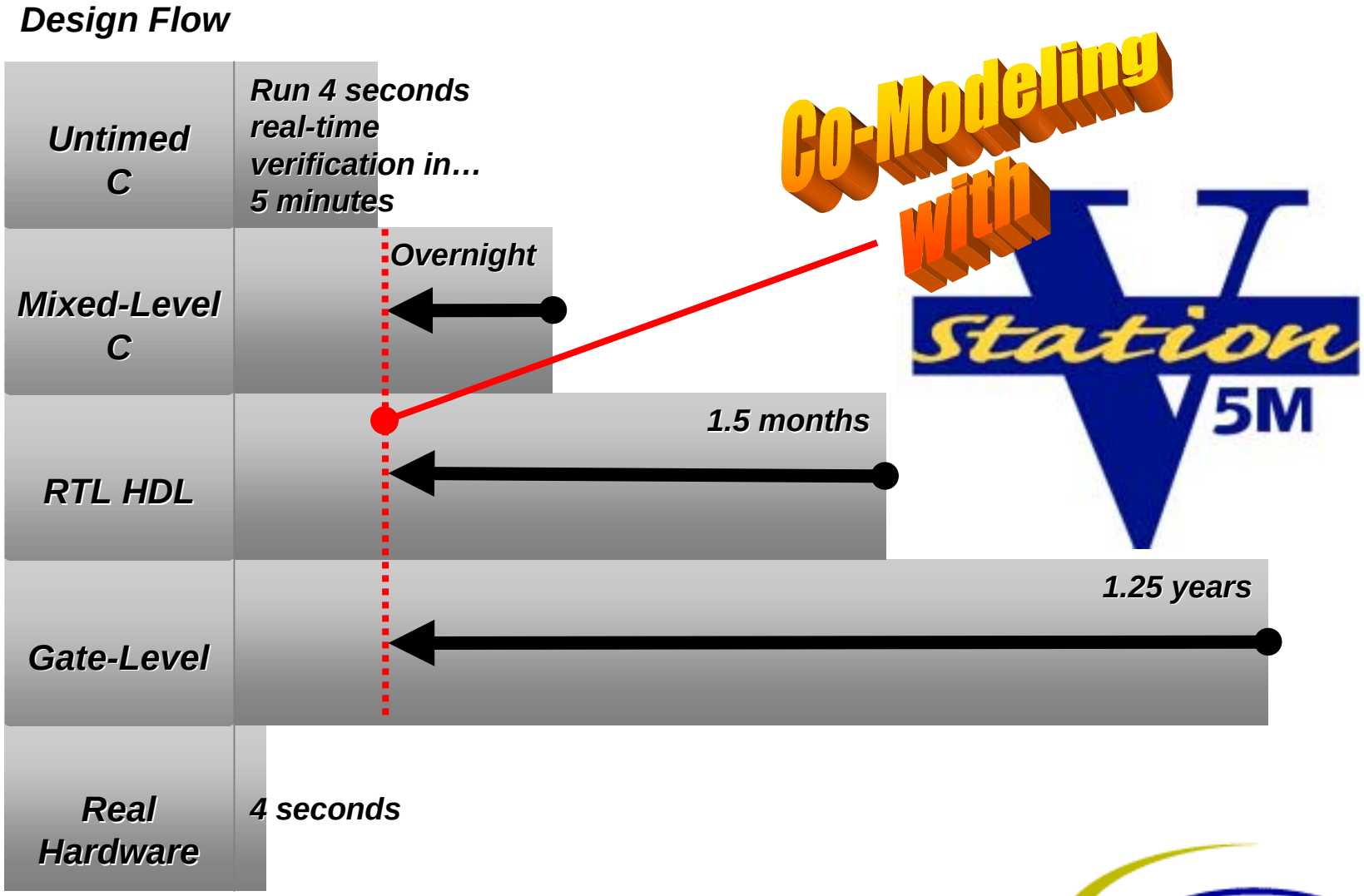
Visual SLD


System Architecture
Virtual-CPU(tm)
Co-Verification
eArchitect(tm)
Performance Analysis
HDL / C
Co-Simulation
MEM
CORE
Interrupt
HDL
DMA
BIU
REG
ASSP
C/C++
UART
Regent™
System Registers
HDL Code
HDL Code
Generation

VStation Co-Modeling

- Ultra high performance Co-Modeling between a *model* running on a workstation and a *model* running in an IKOS Vstation, communicating using *transactions.* Based on the world's first high-performance transaction-oriented API (TAPI)
- Enables SystemC models to be used in conjunction with emulation speed
- For a demo visit IKOS or CoWare at DAC or contact your local IKOS representative http://www.ikos.com

Closing The Verification Productivity Gap



SYNOPSYS®

CoCentric™ System Studio

- An integrated solution for designing at a higher level of abstraction, creating and integrating reusable components, and building heterogeneous and multi-level blocks in an environment architected for co-design and co-verification.
- Enables entry, system design and functional validation using SystemC-based as well as other system level IP and building blocks.
- Contact chriscav@synopsys.com or visit the website at www.synopsys.com/products/cocentric_studio for more information

SYSTEMC™

SYNOPSYS®

CoCentric™ Fixed Point Designer

- Tool and environment that converts ANSI-C programs employing floating-point data types into a program using appropriate SystemC fixed-point data types. It enables a signal processing algorithms written in floating-point to be converted to an executable fixed-point reference specification for implementation and validation in hardware and software.
- Outputs ANSI C transformed to SystemC fixed point datatypes
- Contact chriscav@synopsys.com or visit the website at www.synopsys.com/products/cocentric_fixedpoint for more information

SYSTEMC™

SYNOPSYS®

CoCentric™ SystemC Compiler

- A tool for synthesis of hardware from SystemC models. It is ideal for those designers needing a fast and easy way to get from system level design descriptions coded in SystemC to a gate-level or RT-level hardware description in VHDL or Verilog.
- Synthesizes SystemC design descriptions to high quality gate or RT-Level implementation.
- Contact esmith@synopsys.com or visit the website at www.synopsys.com for more information

SYSTEMC™

SYNOPSYS®

SystemC VCS / MTI Co-Simulation I/F

- High performance co-simulation interface that enables co-verification of a system description in SystemC with existing Verilog/VCS or VHDL/MTI IP blocks or models. Facilitates mixing bottom-up and top-down system design, and simplifies verification for SystemC-based methodologies.
- Simulates SystemC together with Verilog and VHDL
- Contact esmith@synopsys.com or visit the website at www.synopsys.com for more information

SYSTEMC™

SYNOPSYS®

SystemC-VERA I/F

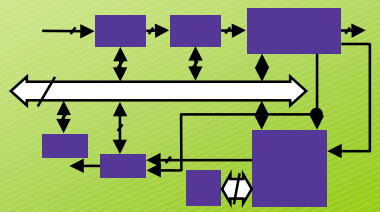
- High performance, direct kernel interface for integrating VERA with SystemC
- Uses the powerful, verification related features in VERA to verify system designs described in SystemC
- Contact swamiv@synopsys.com or visit the website at www.synopsys.com for more information

SYSTEMC™

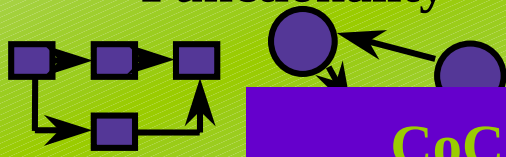
CoCentric™: Synopsys delivers SystemC based solutions

System

Architecture



Functionality



CoCentric System Studio

SystemC

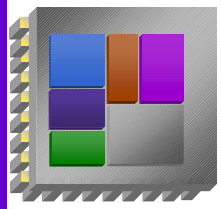
CoCentric Fixed-Point Designer

NEW: CoCentric SystemC Compiler

Chip

NEW VERA SysC I/F

NEW VCS and MTI Co-Sim



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a.out

SYSTEMC™

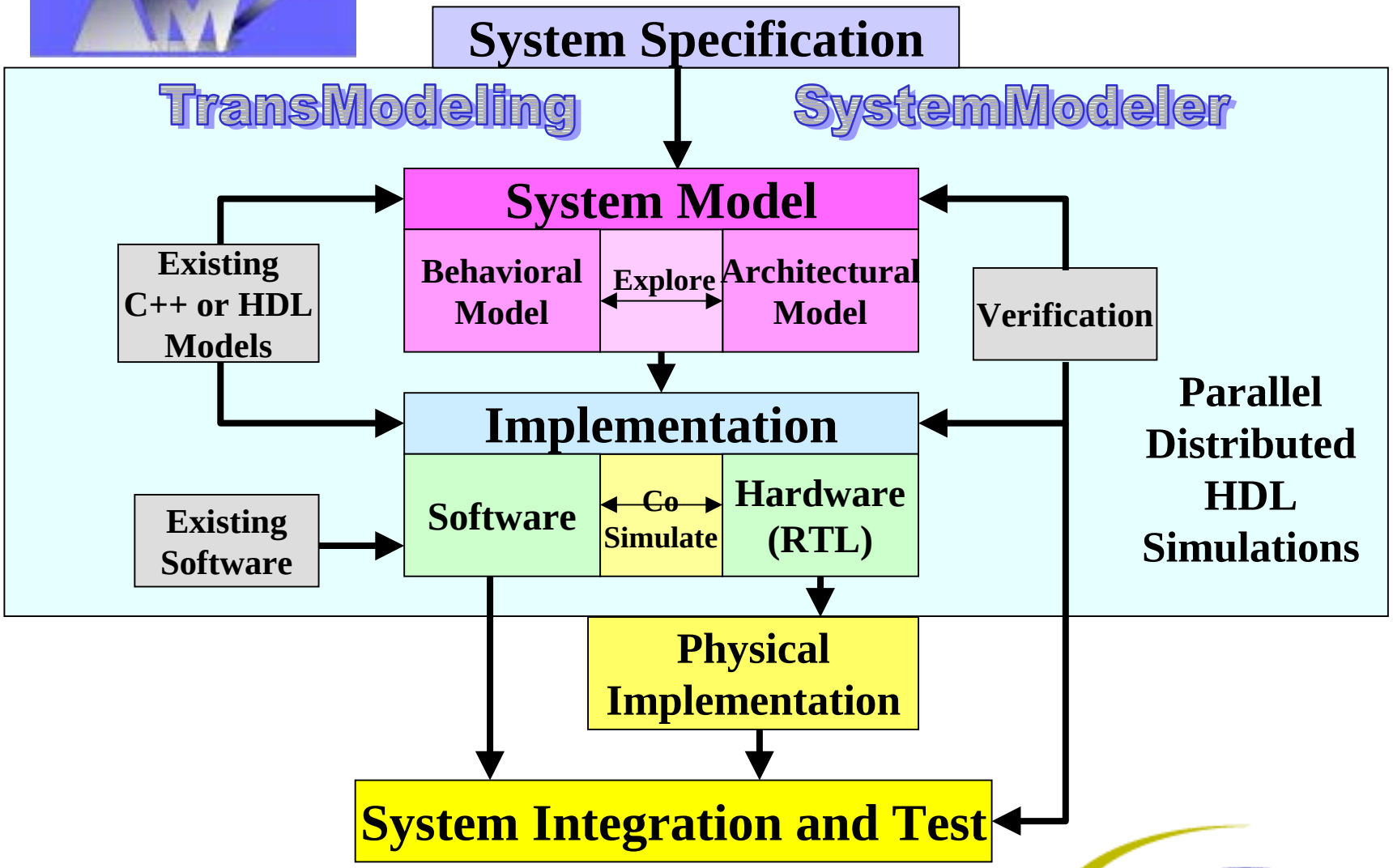
TransModeling, Inc

SystemModeler 2000

- **SystemModeler is a general-purpose system level design tool for developing high-speed C++ models and test benches. C++ and HDL models are easily interchanged for development and co-verification in the system level environment. SystemModeler's transparent parallel distributed HDL simulations speeds the verification of system level designs.**
- **SystemModeler outputs C++ code based on SystemC.**
- **Contact TransModeling at (480) 502-9381 or visit our website at www.TransModeling.com for more information.**

TransModeling, Inc

SystemModeler Design Flow



SYSTEMC™

Veritools

SuperC™

- A very fast SystemC Simulator that writes a highly compressed data format. This wave form data is compressed by 15-50X and can be displayed almost instantly by the Undertow waveform viewer regardless of file size.
- Veritools provides the SuperC™ C++ class compile library for the Veritools SuperC™ simulator
- Contact Veritools at inquiry@veritools.com or Robert Schopmeyer at schop@veritools.com

SYSTEMC™

Veritools

Undertow Suite

- A waveform viewer and Source Code debugging program for the SystemC/SuperC™ Simulator that reads the the highly compressed data format that is written directly by the SuperC™ simulator. This waveform data can be displayed almost instantly by the Undertow waveform viewer regardless of file size while providing linkage and synchronization with the SystemC source code.
- Undertow uses the highly compressed “Fast file” format from SuperC™ while providing Source Code debug facilities for SystemC Source Code.
- Contact Veritools at inquiry@veritools.com, or Robert Schopmeyer at schop@veritools.com

SYSTEMC™

Veritools

Undertow

- A very powerful waveform viewer for the SystemC/SuperC™ Simulator. This wave form data can be displayed almost instantly by the Undertow waveform viewer regardless of file data size
- Undertow uses the SystemC native waveform data or the highly compressed “Fast file” format from SuperC™
- Contact Veritools, Inc. at inquiry@veritools.com or Robert Schopmeyer at schop@veritools.com

SYSTEMC™

From Virtual Prototyping to SystemC

- Evaluate, experience, and design embedded IP platforms from your browser!
- Explore pre-configured embedded platforms, create high-level system models, and generate SystemC to link your designs to implementation.
- For more information contact info@virtio.com or visit our web site at www.virtio.com.

SYSTEMC™

Training: Modeling with SystemC

- Three day workshop provides introduction to modeling with C/C++ and the SystemC C++ class libraries. This course is a mix of lecture and exercises.
- Learn how to write, compile, execute, and debug system and hardware descriptions with SystemC.
- Contact Willamette HDL, *info@whdl.com*, for class schedule information.

SYSTEMC™

Language Rule Checker & Rule Generator

- Complete language rule checker and rule generator… product to be introduced in Q3, more details to follow.
- Performs syntax, netlist, and synthesis checks on your SystemC code.
- Contact Willamette HDL, *info@whdl.com*, or stop by their Suite #5365 for more information or to preview the product.