

Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
 - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTs)
 - Up to two IBM PowerPC™ RISC processor blocks
 - Based on Virtex-II™ Platform FPGA Technology
 - Flexible logic resources
 - SRAM-based in-system configuration
 - Active Interconnect technology
 - SelectRAM™+ memory hierarchy
 - Dedicated 18-bit x 18-bit multiplier blocks
 - High-performance clock management circuitry
 - SelectI/O™-Ultra technology
 - XCITE Digitally Controlled Impedance (DCI) I/O
- Virtex-II Pro / Virtex-II Pro X family members and resources are shown in [Table 1](#).

Table 1: Virtex-II Pro / Virtex-II Pro X FPGA Family Members

Device ⁽¹⁾	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells ⁽²⁾	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8 ⁽⁴⁾	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0 ⁽³⁾ , 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0 ⁽³⁾ or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20 ⁽⁴⁾	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0 ⁽³⁾ or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:

1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell = (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See [Table 3](#) for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable Speed Full-Duplex Transceiver, Allowing 2.488 Gb/s to 10.3125 Gb/s Baud Transfer Rates.
 - Includes specific baud rates used by various standards, as listed in [Table 4, Module 2](#).
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
 - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
 - 200 mV to 1600 mV, peak-peak
 - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
 - "x8" and "x10" clocking/data paths
 - 64B/66B clocking support
- Programmable Receiver Equalization

Virtex-II Pro⁽¹⁾ Array Functional Description

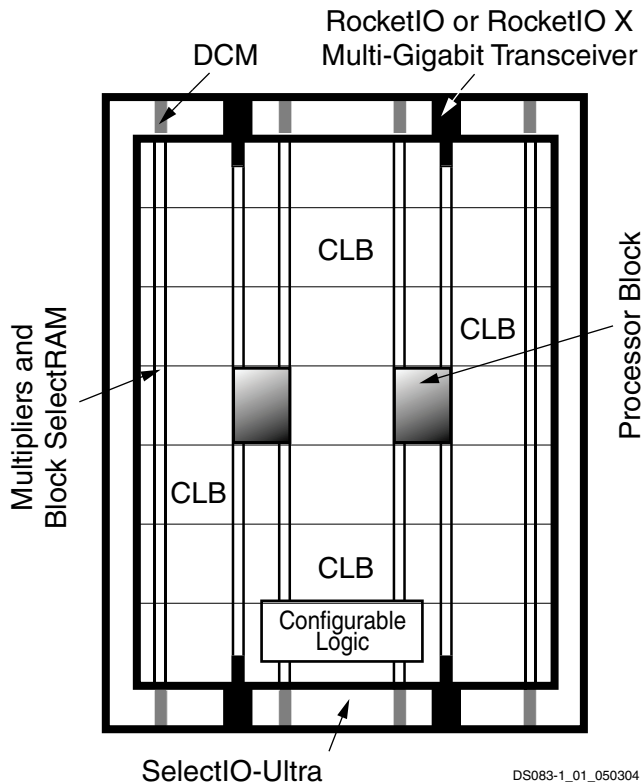


Figure 1: Virtex-II Pro Generic Architecture Overview

This module describes the following Virtex-II Pro functional components, as shown in Figure 1:

- Embedded RocketIO™ (up to 3.125 Gb/s) or RocketIO X (up to 10.3125 Gb/s) Multi-Gigabit Transceivers (MGTs)
- Processor blocks with embedded IBM PowerPC™ 405 RISC CPU core (PPC405) and integration circuitry.
- FPGA fabric based on Virtex-II architecture.

Virtex-II Pro User Guides

Virtex-II Pro User Guides cover theory of operation in more detail, and include implementation details, primitives and attributes, command/instruction sets, and many HDL code examples where appropriate. All parameter specifications are given only in **Module 3** of this Data Sheet.

These User Guides are available:

- For a description of PPC405 embedded core

programming models and internal core operations, refer to [PowerPC Processor Reference Guide](#) and [PowerPC 405 Processor Block Reference Guide](#).

- For detailed RocketIO transceiver digital/analog design considerations, refer to [RocketIO Transceiver User Guide](#).
- For detailed RocketIO X transceiver digital/analog design considerations, refer to [RocketIO X Transceiver User Guide](#).
- For a detailed description of the FPGA fabric (CLB, IOB, DCM, etc.), refer to [Virtex-II Pro Platform FPGA User Guide](#).

All of the documents above, as well as a complete listing and description of Xilinx-developed Intellectual Property cores for Virtex-II Pro, are available on the Xilinx website.

Contents of This Module

- [Functional Description: RocketIO X Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: RocketIO Multi-Gigabit Transceiver \(MGT\)](#)
- [Functional Description: Processor Block](#)
- [Functional Description: Embedded PowerPC 405 Core](#)
- [Functional Description: FPGA](#)
- [Revision History](#)

Virtex-II Pro Compared to Virtex-II Devices

Virtex-II Pro devices are built on the Virtex-II FPGA architecture. Most FPGA features are identical to Virtex-II devices. Major differences are described below:

- The Virtex-II Pro FPGA family is the first to incorporate embedded PPC405 and RocketIO/RocketIO X cores.
- V_{CCAUX} , the auxiliary supply voltage, is 2.5V instead of 3.3V as for Virtex-II devices. Advanced processing at 0.13 μm has resulted in a smaller die, faster speed, and lower power consumption.
- Virtex-II Pro devices are neither bitstream-compatible nor pin-compatible with Virtex-II devices. However, Virtex-II designs can be compiled into Virtex-II Pro devices.
- On-chip input LVDS differential termination is available.
- SSTL3, AGP-2X/AGP, LVPECL_33, LVDS_33, and LVDS_33 standards are not supported.
- The open-drain output pin TDO does not have an internal pull-up resistor.

1. Unless otherwise noted, "Virtex-II Pro" refers to members of the Virtex-II Pro and/or Virtex-II Pro X families.

Functional Description: Processor Block

This section briefly describes the interfaces and components of the Processor Block. The subsequent section, [Functional Description: Embedded PowerPC 405 Core](#) beginning on [page 20](#), offers a summary of major PPC405 core features. For an in-depth discussion on both the Processor Block and PPC405, see the [PowerPC Processor Reference Guide](#) and the [PowerPC 405 Processor Block Reference Guide](#) available on the Xilinx website at <http://www.xilinx.com>.

Processor Block Overview

Figure 14 shows the internal architecture of the Processor Block.

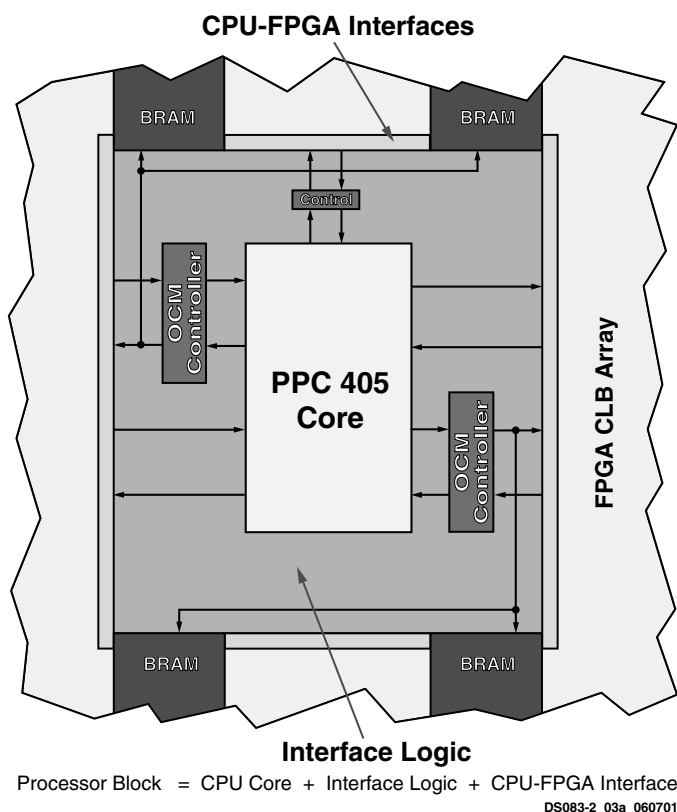


Figure 14: Processor Block Architecture

Within the Virtex-II Pro Processor Block, there are four components:

- Embedded IBM PowerPC 405-D5 RISC CPU core
- On-Chip Memory (OCM) controllers and interfaces
- Clock/control interface logic
- CPU-FPGA Interfaces

Embedded PowerPC 405 RISC Core

The PowerPC 405D5 core is a 0.13 μm implementation of the IBM PowerPC 405D4 core. The advanced process technology enables the embedded PowerPC 405 (PPC405)

core to operate at 300+ MHz while maintaining low power consumption. Specially designed interface logic integrates the core with the surrounding CLBs, block RAMs, and general routing resources. Up to four Processor Blocks can be available in a single Virtex-II Pro device.

The embedded PPC405 core implements the PowerPC User Instruction Set Architecture (UISA), user-level registers, programming model, data types, and addressing modes for 32-bit fixed-point operations. 64-bit operations, auxiliary processor operations, and floating-point operations are trapped and can be emulated in software.

Most of the PPC405 core features are compatible with the specifications for the PowerPC Virtual Environment Architecture (VEA) and Operating Environment Architecture (OEA). They also provide a number of optimizations and extensions to the lower layers of the PowerPC Architecture. The full architecture of the PPC405 is defined by the PowerPC Embedded Environment and PowerPC UISA documentation, available from IBM.

On-Chip Memory (OCM) Controllers

Introduction

The OCM controllers serve as dedicated interfaces between the block RAMs in the FPGA fabric (see [18 Kb Block SelectRAM+ Resources](#), [page 44](#)) and OCM signals available on the embedded PPC405 core. The OCM signals on the PPC405 core are designed to provide very quick access to a fixed amount of instruction and data memory space. The OCM controller provides an interface to both the 64-bit Instruction-Side Block RAM (ISBRAM) and the 32-bit Data-Side Block RAM (DSBRAM). The designer can choose to implement:

- ISBRAM only
- DSBRAM only
- Both ISBRAM and DSBRAM
- No ISBRAM and no DSBRAM

One of OCM's primary advantages is that it guarantees a fixed latency of execution for a higher level of determinism. Additionally, it reduces cache pollution and thrashing, since the cache remains available for caching code from other memory resources.

Typical applications for DSOCM include scratch-pad memory, as well as use of the dual-port feature of block RAM to enable bidirectional data transfer between processor and FPGA. Typical applications for ISOCM include storage of interrupt service routines.

Functional Features

Common Features

- Separate Instruction and Data memory interface between processor core and BRAMs in FPGA
- Dedicated interface to Device Control Register (DCR) bus for ISOCM and DSOCM

- Single-cycle and multi-cycle mode option for I-side and D-side interfaces
- Single cycle = one CPU clock cycle; multi-cycle = minimum of two and maximum of eight CPU clock cycles
- FPGA configurable DCR addresses within DSOCM and ISOCM.
- Independent 16 MB logical memory space available within PPC405 memory map for each of the DSOCM and ISOCM. The number of block RAMs in the device might limit the maximum amount of OCM supported.
- Maximum of 64K and 128K bytes addressable from DSOCM and ISOCM interfaces, respectively, using address outputs from OCM directly without additional decoding logic.

Data-Side OCM (DSOCM)

- 32-bit Data Read bus and 32-bit Data Write bus
- Byte write access to DSBRAM support
- Second port of dual port DSBRAM is available to read/write from an FPGA interface
- 22-bit address to DSBRAM port
- 8-bit DCR Registers: DSCNTL, DSARC
- Three alternatives to write into DSBRAM: BRAM initialization, CPU, FPGA H/W using second port

Instruction-Side OCM (ISOCM)

The ISOCM interface contains a 64-bit read only port, for instruction fetches, and a 32-bit write only port, to initialize or test the ISBRAM. When implementing the read only port, the user must deassert the write port inputs. The preferred method of initializing the ISBRAM is through the configuration bitstream.

- 64-bit Data Read Only bus (two instructions per cycle)
- 32-bit Data Write Only bus (through DCR)
- Separate 21-bit address to ISBRAM
- 8-bit DCR Registers: ISCNTL, ISARC
- 32-bit DCR Registers: ISINIT, ISFILL
- Two alternatives to write into ISBRAM: BRAM initialization, DCR and write instruction

Clock/Control Interface Logic

The clock/control interface logic provides proper initialization and connections for PPC405 clock/power management, resets, PLB cycle control, and OCM interfaces. It also couples user signals between the FPGA fabric and the embedded PPC405 CPU core.

The processor clock connectivity is similar to CLB clock pins. It can connect either to global clock nets or general routing resources. Therefore the processor clock source can come from DCM, CLB, or user package pin.

CPU-FPGA Interfaces

All Processor Block user pins link up with the general FPGA routing resources through the CPU-FPGA interface. Therefore processor signals have the same routability as other

non-Processor Block user signals. Longlines and hex lines travel across the Processor Block both vertically and horizontally, allowing signals to route through the Processor Block.

Processor Local Bus (PLB) Interfaces

The PPC405 core accesses high-speed system resources through PLB interfaces on the instruction and data cache controllers. The PLB interfaces provide separate 32-bit address/64-bit data buses for the instruction and data sides.

The cache controllers are both PLB masters. PLB arbiters are implemented in the FPGA fabric and are available as soft IP cores.

Device Control Register (DCR) Bus Interface

The device control register (DCR) bus has 10 bits of address space for components external to the PPC405 core. Using the DCR bus to manage status and configuration registers reduces PLB traffic and improves system integrity. System resources on the DCR bus are protected or isolated from wayward code since the DCR bus is not part of the system memory map.

External Interrupt Controller (EIC) Interface

Two level-sensitive user interrupt pins (critical and non-critical) are available. They can be either driven by user defined logic or Xilinx soft interrupt controller IP core outside the Processor Block.

Clock/Power Management (CPM) Interface

The CPM interface supports several methods of clock distribution and power management. Three modes of operation that reduce power consumption below the normal operational level are available.

Reset Interface

There are three user reset input pins (core, chip, and system) and three user reset output pins for different levels of reset, if required.

Debug Interface

Debugging interfaces on the embedded PPC405 core, consisting of the JTAG and Trace ports, offer access to resources internal to the core and assist in software development. The JTAG port provides basic JTAG chip testing functionality as well as the ability for external debug tools to gain control of the processor for debug purposes. The Trace port furnishes programmers with a mechanism for acquiring instruction execution traces.

The JTAG port complies with IEEE Std 1149.1, which defines a test access port (TAP) and boundary scan architecture. Extensions to the JTAG interface provide debuggers with processor control that includes stopping, starting, and stepping the PPC405 core. These extensions are compliant with the IEEE 1149.1 specifications for vendor-specific extensions.

The Trace port provides instruction execution trace information to an external trace tool. The PPC405 core is capable of back trace and forward trace. Back trace is the tracing of instructions prior to a debug event while forward trace is the tracing of instructions after a debug event.

The processor JTAG port and the FPGA JTAG port can be accessed independently, or the two can be programmatically linked together and accessed via the dedicated FPGA JTAG pins.

For detailed information on the PPC405 JTAG interface, please refer to the "JTAG Interface" section of the [PowerPC 405 Processor Block Reference Guide](#)

CoreConnect™ Bus Architecture

The Processor Block is compatible with the CoreConnect™ bus architecture. Any CoreConnect compliant cores including Xilinx soft IP can integrate with the Processor Block through this high-performance bus architecture implemented on FPGA fabric.

The CoreConnect architecture provides three buses for interconnecting Processor Blocks, Xilinx soft IP, third party IP, and custom logic, as shown in [Figure 15](#):

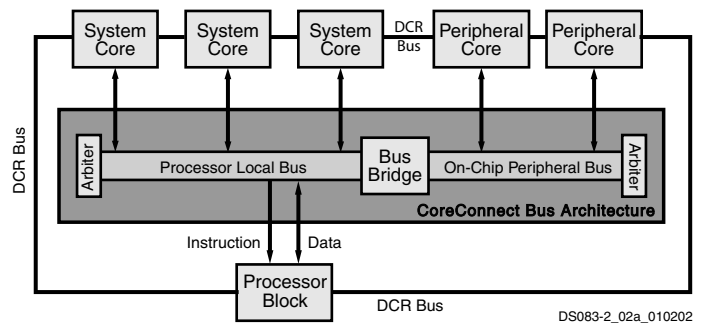


Figure 15: CoreConnect Block Diagram

- Processor Local Bus (PLB)
- On-Chip Peripheral Bus (OPB)
- Device Control Register (DCR) bus

High-performance peripherals connect to the high-bandwidth, low-latency PLB. Slower peripheral cores connect to the OPB, which reduces traffic on the PLB, resulting in greater overall system performance.

For more information, refer to:

http://www-3.ibm.com/chips/techlib/techlib.nfs/product/families/CoreConnect_Bus_Architecture/

Functional Description: Embedded PowerPC 405 Core

This section offers a brief overview of the various functional blocks shown in [Figure 16](#).

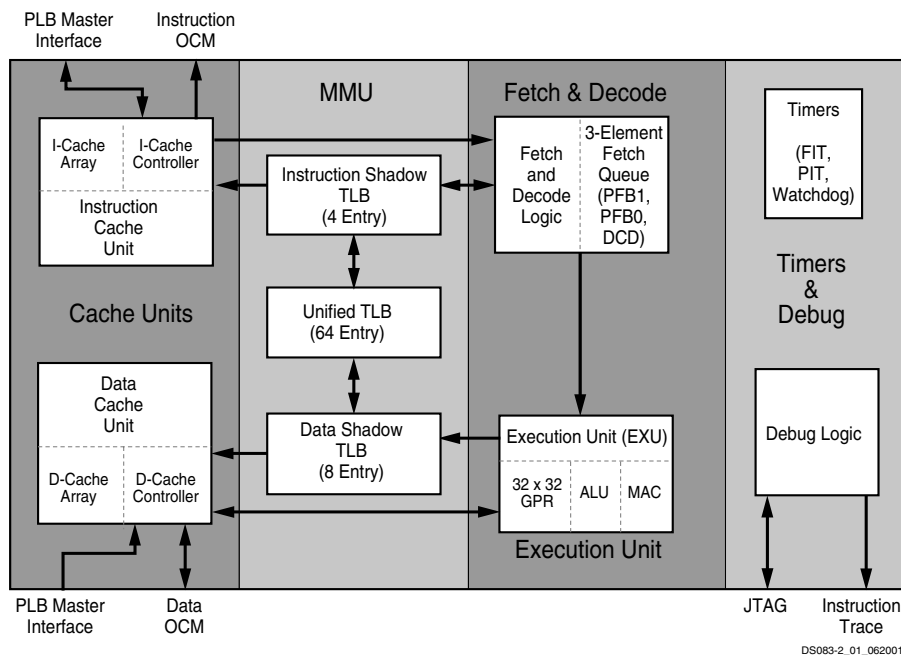


Figure 16: Embedded PPC405 Core Block Diagram

Embedded PPC405 Core

The embedded PPC405 core is a 32-bit Harvard architecture processor. [Figure 16](#) illustrates its functional blocks:

- Cache units
- Memory Management unit
- Fetch Decode unit

Configurable Logic Blocks (CLBs)

The Virtex-II Pro configurable logic blocks (CLB) are organized in an array and are used to build combinatorial and synchronous logic designs. Each CLB element is tied to a switch matrix to access the general routing matrix, as shown in Figure 32.

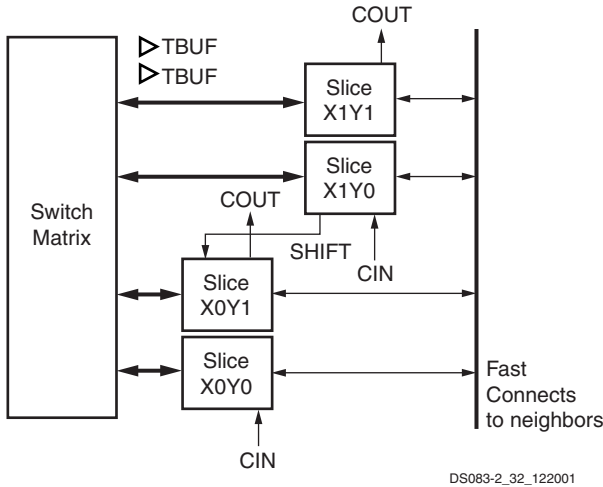


Figure 32: Virtex-II Pro CLB Element

DS083-2_32_122001

A CLB element comprises 4 similar slices, with fast local feedback within the CLB. The four slices are split in two columns of two slices with two independent carry logic chains and one common shift chain.

Slice Description

Each slice includes two 4-input function generators, carry logic, arithmetic logic gates, wide function multiplexers and two storage elements. As shown in Figure 33, each 4-input function generator is programmable as a 4-input LUT, 16 bits of distributed SelectRAM+ memory, or a 16-bit variable-tap shift register element.

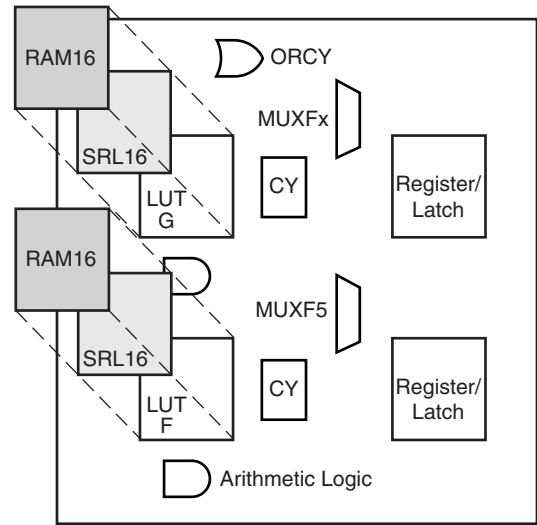
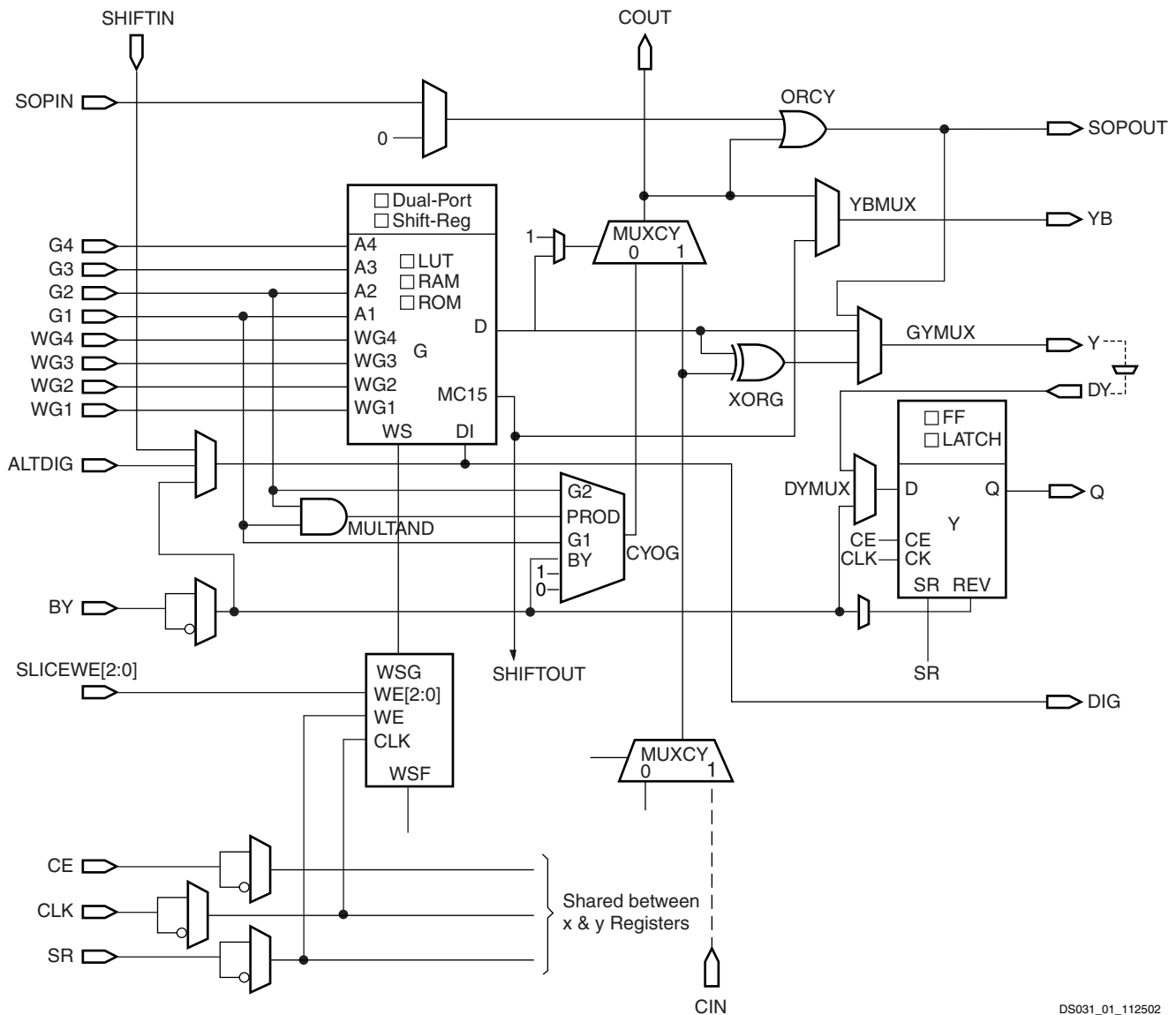


Figure 33: Virtex-II Pro Slice Configuration

DS083-2_31_122001

The output from the function generator in each slice drives both the slice output and the D input of the storage element. **Figure 34** shows a more detailed view of a single slice.



DS031_01_112502

Figure 34: Virtex-II Pro Slice (Top Half)

Configurations

Look-Up Table

Virtex-II Pro function generators are implemented as 4-input look-up tables (LUTs). Four independent inputs are provided to each of the two function generators in a slice (F and G). These function generators are each capable of implementing any arbitrarily defined boolean function of four inputs. The propagation delay is therefore independent of the function implemented. Signals from the function generators can exit the slice (X or Y output), can input the XOR dedicated gate (see arithmetic logic), or input the carry-logic multiplexer (see fast look-ahead carry logic), or feed the D input of the storage element, or go to the MUXF5 (not shown in **Figure 34**).

In addition to the basic LUTs, the Virtex-II Pro slice contains logic (MUXF5 and MUXFX multiplexers) that combines function generators to provide any function of five, six, seven, or eight inputs. The MUXFX is either MUXF6, MUXF7, or MUXF8 according to the slice considered in the CLB. Selected functions up to nine inputs (MUXF5 multiplexer) can be implemented in one slice. The MUXFX can also be a MUXF6, MUXF7, or MUXF8 multiplexer to map any function of six, seven, or eight inputs and selected wide logic functions.

Register/Latch

The storage elements in a Virtex-II Pro slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D input can be directly driven by