First Encounter Workshop 3

What you will learn - Running Power Analysis in the Floorplan Mode

- **Importing a design**
- **Loading a top level floor plan**
- **Creating power mesh/grid**
- **Running statistical mode power analysis**
- **Viewing the created power graph**
- **Displaying the IR drop**
- **Displaying the macros/blocks current sources**
- **Displaying the EM segements**

1. TESTCASE INFORMATION

The testcase is the same one used in Workshop 1. The netlist format is hierarchical Verilog, and the process is 5 layers of metal. It has one clock source, `MCK`.

2. DESIGN IMPORT

Start new First Encounter session for this Workshop and use the same work directory.

Open the *Design -> Design Import…* form and load in the configuration file, `train.power.conf`. Examine the entries in the Design Import form. Click *Ok* when ready to import.

3. LOAD FLOOR PLAN AND CREATE POWER MESH

You have two choices of 1) load the class floor plan file, or 2) create your own power ring and power mesh.

For choice 1), load the floor plan file, `train.power.fp.`

Creating power rings

For choice 2), first load the floor plan file, `train.power.fp0.` Then use the *FloorPlan -> Power Planning -> Add Rings…* form to create power rings around the core design area. The power net names, `vdd` and `gnd` are already there from the entries in the Power page of Design Import form. In the *Type* section, choose the type of core ring you want or use the default setting.

In the *Ring Configuration* section, select the metal layer *Metal5* for the *Top* and *Bottom* segments, and choose metal layer *Metal4* for the *Left* and *Right* segments. Now, change the default values for *Width* to `10.0` and *Spacing* to `6.0` for both metal layers, and the *Offset* applies depending upon your *Type* section. Click *Apply* button when ready. This ring is optional but it will connect all the power stripes that are created next. If you do not like the created power routes, type the FE command, `undo`, in the Encounter console to undo the last Apply.

Zoom-in to one of the corners of the rings to view the vdd / gnd power routes and look for the vias.

Creating power stripes

Create the power stripes by using the *FloorPlan -> Power Planning -> Add Stripes…* form. The power nets, `vdd` and `gnd`, should display. In the *Set Configuration* section, choose metal layer *Metal4* for *Vertical* stripes. Change the values for *Width* to `10.0` and for *Spacing* to `6.0`.

For the *Set Pattern* section, enter `700` for *Set-to-set distance*.

For the *Limits* section, choose *Absolute locations* and click the *Point…* button to mark the boundary of the sets of stripes to be created. Or you can enter `1400.0` for *Start (X)* and `6500.0` for *Stop (X).* Now click the *Apply* button to create the vertical stripes.

For the horizontal stripes, choose *Horizontal* and choose *Metal5*. In the *Limits* section, click the *Point…* button to mark the boundary of the sets of stripes to be created. Or you can enter `1300.0` for *Start (Y)* and `7000.0` for *Stop (Y).* Click the *Apply* button to create the horizontal stripes.

In the *Advanced* page, there are many options to control the creating of power stripes but for this workshop, the default settings are used.

The created power stripes should now crisscross the entire core design area.

4. RUN AMOEBA PLACEMENT AND TRIAL ROUTE

Run placement and trial route with the *Medium Effort* option, and this is done by opening the *Place -> Place* form. Next, to run trial route, you can either use the *Route -> Trial Route* form, or enter the FE command, `trialroute`, in the console while placement program is running.

5. RUN EXTRACT RC

First, choose the process model by using the *Timing -> Specify Operating Condition* form and select *BEST* process model. Then extract RC using the *Timing -> Extract RC* form (you can deselect *Save Cap to* if you want) or enter the FE command `extractrc` in the console. Now the Power menu is activated.

6. PREPARE TO RUN POWER ANALYSIS FOR VDD

First, power reference point must be created on the power rings around the core design area. Make sure you are in the *Placement View* and then, open the *Power -> Edit Pad Location* form. Also, click on the *Auto Query* (question mark at bottom of the FE form) button to help you in the next step.

Zoom in to the power ring area where a vdd pad is to be added. To add the vdd pad, this can be easily done by first clicking the *Get Coord* button, second, click on the location on the vdd ring where a pad is desired, and then click the *Add* button. Now you should see a yellow colored circle representing the vdd pad. Complete adding vdd pads by adding at least one vdd pad per side.

Or you can click the *Load* button to load the vdd pad file, `vdd.pp`. You should see the yellow colored circle pads in the Placement View.

7. RUN STATISTICAL POWER ANALYSIS

Open the *Power -> Power Analysis -> Statistical Mode* form. Enter `vdd` for the *Net Name*. Leave the *Net Toggle Probability* to 0.2, which is 20 percent. Change the *Clock Rate* to `83.3` MHz since the timing constraints file has the clock period at 12 Ns. *Select the Pad Location File*, `vdd.pp`, which was created in the last step and select *Floorplan* mode before clicking *Ok*. Now

8. VIEW POWER ANALYSIS RESULTS

power analysis will run.

First, view the `vdd.report` file or view the console messages to see the average power dissipation and worst IR drop in the design plus other items.

Next, to view the created power graph in the *Placement View*, open the *Color Preference* form by clicking the *More* button in the *Colors* area, and select *Power Graph* and the created power graph is ready to be displayed. For a better view of the power graph, you have to deselect *Net*, *Power Trunk/Rail,* and *Instance*. Now, zoom-in to see the details of the power graph.

To display the IR drop, open the *Power -> Display IR Drop* form. Enter `vdd` for the *Net Name* and enter the worst IR drop value from the report for the *Threshold* value. The default Threshold value is 10 per cent of the power supply, which is 0.28 Volts. Now, the color code IR drop displays. To get a more detailed and colorful display of the IR drop, you may have to change the *Threshold* value (eg, 0.05) that is closer to reported worst IR drop value, and them you will start to see the area(s) with the worst IR drop. The color-coding can be changed by clicking the *More* button in the *Tools* area. This opens the *Color Preference* form.

To display the Macro Current Source location, open the *Power -> Macro I Source Location* form. Enter `vdd` for the *Net Name* and click *Ok*. Now the white colored circle shaped current sources for the blocks are displayed. These sources represents distributed current sink points for the blocks. Note that some current source points are outside the actual block area. This because the power analysis in the Floorplan mode creates grids and then the blocks are divided into grids. Macro Current Source location has more meaning with power analysis run in the Layout mode since the current source point are actually where the power graph connects to the block's power pins.

9. VIEW EM VIOLATIONS

To display electromigration violations on power route segments, open the *Power -> Display EM* form and note the default current limit values(mA per width in Micron) and mA per via). Click OK to display the power route segments that exceed the current density limits. The color code scheme is the same for IR drop, where the color red indicates that a segment exceeds the current limit or via current limit.

10. PREPARE TO RUN POWER ANALYSIS FOR GND

Go back to step, "Prepare to Run Power Analysis for VDD" and follow the same steps substituting gnd for vdd.

11. OTHER POWER ANALYSIS THAT CAN BE RUN

A more realistic power analysis of this design is setting a net toggle value differently to each clock domain which are defined in the timing constraint file.

In the *Power -> Power Analysis -> Statistical Mode* form, make the selections *Pre-CTS Clock* and *Net Toggle Probability File*. Next, open the *Power -> Net Toggle Probability File* form and click the *Get Clock* button and note that clock, MCK, appears. You can add MCK toggle probability by clicking the *Edit* button. *Add* your edits and *Save* it to a file. Now, go back to the *Statistical Mode* form and enter the save file name for the *Net Toggle Probability File.* Click *Ok* to run power analysis.

This ends the work for Workshop 3.