Announcements

• SAIS
  - https://utk.campuslabs.com/courseeval/
  - 5% EC on final if 100% completion rate
    ▪ 78% in 481
    ▪ 67% in 599
    ▪ Ends 12/6 (Wednesday)

Simulation Example

• AWG#30 copper wire
  • Diameter $d = 0.294$ mm
  • $d = \delta$ at around 50 kHz
• 1:1 transformer
  • Primary and secondary are the same, 30 turns in 3 layers
• Sinusoidal currents,
  $$I_{1\text{rms}} = I_{2\text{rms}} = 1 \text{ A}$$

Numerical field and current density solutions using EEMM (Finite Element Method Magnetics), a free 2D solver,
http://www.femm.info/wiki/HomePage
Frequency: 1 kHz
**Frequency: 100 kHz**

Total copper losses 1.8 larger than at 1 kHz

**Frequency: 1 MHz**

Total copper losses 20 times larger than at 1 kHz
Frequency: 10 MHz

Flux density

Current Density

Very significant proximity effect
Total copper losses = 65 times larger than at 1 KHz

Fringing Flux
Fringing Flux Simulation

Litz Wire

- A way to increase conductor area while maintaining low proximity losses
- Many strands of small-gauge wire are bundled together and are externally connected in parallel
- Strands are twisted, or transposed, so that each strand passes equally through each position on inside and outside of bundle. This prevents circulation of currents between strands.
- Strand diameter should be sufficiently smaller than skin depth
- The Litz wire bundle itself is composed of multiple layers
- Advantage: when properly sized, can significantly reduce proximity loss
- Disadvantage: increased cost and decreased amount of copper within core window
Chapter 15: Transformer Design

15.1 Transformer design: Basic constraints
15.2 A step-by-step transformer design procedure
15.3 Examples
15.4 AC inductor design
15.5 Summary

Transformer Design Constraints

1. Obtain turns ratio \( n_1 : n_2 \)
2. Minimize losses
   \[ P_{\text{tot}} = P_{\text{cu,dc}} + P_{\text{core}} \]
   \[ P_{\text{cu,dc}} = \sum_{i=1}^{m} \rho_{i} \frac{A_{i}}{A_{w}} \]
   \[ A_{i} = \frac{w_{i} d_{i}}{n_{i}} \]
   \[ \rightarrow P_{\text{cu,dc}} \propto n^2 \]
   \[ P_{\text{core}} = K_a (f_{L})^a ( \Delta B )^b V_e \]
   \[ \Delta B = \frac{1}{2 \mu_{c}} \int_{0}^{50} V_{i} d t \]

3. Make sure winding fit in window

\( \beta > 1 \)
Minimizing Total Loss

There is a value of $\Delta B$ that minimizes the total power loss.

\[ P_{\text{tot}} = P_{fe} + P_{cu} \]

\[ P_{fe} = K_{fe}(\Delta B)^\beta A_c \ell_m \]

\[ P_{cu} = \left( \frac{\rho \lambda^2 I^2_{\text{tot}}}{4K_n} \right) \left( \frac{(\text{MLT})}{W_A A_c^2} \right) \left( \frac{1}{\Delta B} \right)^2 \]

Calculation of Total Loss

Substitute optimum $\Delta B$ into expressions for $P_{cu}$ and $P_{fe}$. The total loss is:

\[ P_{\text{tot}} = \left[ A_c \ell_m K_{fe} \right] \left( \frac{2}{\beta + 2} \right) \left[ \frac{\rho \lambda^2 I^2_{\text{tot}}}{4K_n} \right] \left( \frac{(\text{MLT})}{W_A A_c^2} \right) \left( \frac{\beta}{\beta + 2} \right) + \left( \frac{\beta}{\beta + 2} \right)^2 \]

Rearrange as follows:

\[ \frac{W_A (A_c) (2\beta - 1)\beta}{(\text{MLT}) \ell_m (2\beta)} \left[ \left( \frac{\beta}{2} \right) \left( \frac{\beta}{\beta + 2} \right) + \left( \frac{\beta}{2} \right)^{2} \right] = \frac{\rho \lambda^2 I^2_{\text{tot}} K_{fe}^{2(\beta)}}{4K_n (P_{\text{tot}})^{((\beta + 2)\beta)}} \]

Left side: terms depend on core geometry

Right side: terms depend on specifications of the application
The $K_{gfe}$ Method

Define

$$K_{gfe} = \frac{W_A(A_c)^{(2\beta-1)/\beta}}{(MLT)m_c^{2/\beta}} \left( \frac{\beta}{2} \right)^{-\frac{\beta}{\beta+2}} + \left( \frac{\beta}{2} \right)^{\frac{2}{\beta+2}}$$

Design procedure: select a core that satisfies

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{2/\beta}}{4K_u(P_{tot})^{(\beta+2)/\beta}}$$

Appendix D lists the values of $K_{gfe}$ for common ferrite cores

$K_{gfe}$ is similar to the $K_g$ geometrical constant used in Chapter 14:

- $K_g$ is used when $B_{max}$ is specified
- $K_{gfe}$ is used when $\Delta B$ is to be chosen to minimize total loss

Verify $B_{max} < B_{sat}$
Switching Frequency Vs. XF Size

- As switching frequency is increased from 25 kHz to 250 kHz, core size is dramatically reduced.
- As switching frequency is increased from 400 kHz to 1 MHz, core size increases.

Fundamentals of Power Electronics

Chapter 15: Transformer design
Practical Issues in PE: Parasitics

Use loop analysis

switched input current $i_1(t)$ contains large high frequency harmonics
—hence inductance of input loop is critical
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI
the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc
—hence additional inductance is not a significant problem in the second loop
Decoupling

Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source

Real Switching Waveforms
Input Filter Design

- Filter can seriously degrade converter control system behavior
- Use extra element theorem to derive conditions which ensure that converter dynamics are not affected by input filter
- Must design input filter having adequate damping

Damped Input Filters

Design criteria derived via Extra Element theorem:

Two-section damped input filter design:

\[
\left| Z(j\omega) \right| \gg \left| Z_D(j\omega) \right|, \quad \left| Z(j\omega) \right| \gg \left| Z_D(j\omega) \right|
\]
Current Programmed Control

- Chapter 12
- A very popular method for controlling PWM converters
- Transistor turns off when its current $i_c(t)$ is equal to the control input $i_c(t)$
- Simpler dynamics, more robust compensator

Buck Converter With CPM

Comparison of control-to-output transfer functions

Averaged switch model used in PSPICE simulations
Digital Control of SMPS

- Digital Control can improve noise immunity, element variation, size/cost
- Advanced tuning algorithms can be included to change compensator dynamically or over lifetime
- Can model power stage without averaging assumptions
- Need to include sampling, delay, saturation, and quantization effects

Resonant and Soft-Switching Topologies

- Switch network
- Resonant tank network
- Switch network
- Low-pass filter network
- dc load

- Section V
Soft Switching Converters

Power Electronics Courses at UTK

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