Lecture 8: Flyback Example

ECE 481: Power Electronics
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6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors. Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.
- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.
Converters producing a unipolar output voltage

1. **Buck**
   \[ M(D) = D \]

   ![Buck Circuit Diagram]

2. **Boost**
   \[ M(D) = \frac{1}{1-D} \]

   ![Boost Circuit Diagram]

3. **Buck-boost**
   \[ M(D) = -\frac{D}{1-D} \]

   ![Buck-boost Circuit Diagram]

4. **Noninverting buck-boost**
   \[ M(D) = \frac{D}{1-D} \]

   ![Noninverting Buck-boost Circuit Diagram]
Converters producing a bipolar output voltage suitable as dc-ac inverters

5. Bridge

\[ M(\Delta) = \frac{2(1-D)}{1} \]

6. Watkins-Johnson

\[ M(\Delta) = \frac{2D-1}{D} \]

Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. Current fed bridge

\[ M(\Delta) = \frac{D}{2D-1} \]

8. Inverter of Watkins-Johnson

\[ M(\Delta) = \frac{D}{2D-1} \]
Several members of the class of two-inductor converters

1. Čuk
   \[ M(D) = -\frac{D}{1-D} \]

2. SEPIC
   \[ M(D) = \frac{D}{1-D} \]

3. Inverse of SEPIC
   \[ M(D) = \frac{D}{1-D} \]

4. Buck
   \[ M(D) = D^3 \]
6.3. Transformer isolation

Objectives:
- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed—use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits

A simple transformer model

Diagram of multiple winding transformer and equivalent circuit model.
The magnetizing inductance $L_M$

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltage
- Transformer saturates when magnetizing current $i_M$ is too large

Volt-second balance in $L_M$

The magnetizing inductance is a real inductor, obeying

$$v_i(t) = L_M \frac{di_M(t)}{dt}$$

Integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_i(\tau) d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_i) - i_M(0)$, and hence

$$0 = \frac{1}{L_M} \int_0^t v_i(t) dt$$
Transformer reset

- “Transformer reset” is the mechanism by which magnetizing inductance volt-second balance is obtained.
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters.
- To understand operation of transformer-isolated converters: replace transformer by equivalent circuit model containing magnetizing inductance.
- Analyze converter as usual, treating magnetizing inductance as any other inductor.
- Apply volt-sec balance to all converter inductors, including magnetizing inductance.

6.3.4. Flyback converter

* buck-boost converter:

* construct inductor winding using two parallel wires:
Derivation of flyback converter, cont.

Isolate inductor windings: the flyback converter

Flyback converter having a 1:n turns ratio and positive output:

The "flyback transformer"

- A two-winding inductor
- Symbol is same as transformer, but function differs significantly from ideal transformer
- Energy is stored in magnetizing inductance
- Magnetizing inductance is relatively small

- Current does not simultaneously flow in primary and secondary windings
- Instantaneous winding voltages follow turns ratio
- Instantaneous (and rms) winding currents do not follow turns ratio
- Model as (small) magnetizing inductance in parallel with ideal transformer
Flyback Converter Example

Equivalent Circuit Model

\[ \langle i_s \rangle = DI_{\text{in}} \]
\[ \langle v_{\text{in}} \rangle = 0 = DV_g - D \left( \frac{V}{n} \right) \]
\[ \langle i_{\text{co}} \rangle = 0 = D \cdot \frac{I_{\text{in}}}{n} \cdot \frac{V}{R} \]
Subinterval 1

$Q_1$ on, $D_1$ off

Transformer model

$V_s$ $L$ $C$ $R$ $i_c = i$ $v_L = V_s$ $i_c = -\frac{v}{R}$

CCM: small ripple approximation leads to

$Q_1$ off, $D_1$ on

Transformer model

$V_s$ $L$ $C$ $R$ $i_c = i$ $v_L = -\frac{v}{n}$ $i_c = \frac{i}{n} - \frac{v}{R}$ $i_s = 0$

CCM: small ripple approximation leads to
CCM Flyback waveforms and solution

Volt-second balance:
\[ \langle v_i \rangle = D \langle v_s \rangle + D \left( -\frac{V}{R} \right) = 0 \]

Conversion ratio is
\[ M(D) = \frac{V}{V_s} = n \frac{D}{1-D} \]

Charge balance:
\[ \langle i_c \rangle = D \left( -\frac{V}{R} \right) + D \left( 1 - \frac{V}{R} \right) = 0 \]

Dc component of magnetizing current is
\[ I = \frac{nV}{2nR} \]

Dc component of source current is
\[ I_s = \langle i_s \rangle = D(I) + D(0) \]

Equivalent circuit model: CCM Flyback

\[ \langle v_i \rangle = D \langle v_s \rangle + D \left( -\frac{V}{R} \right) = 0 \]

\[ \langle i_c \rangle = D \left( -\frac{V}{R} \right) + D \left( 1 - \frac{V}{R} \right) = 0 \]

\[ I_s = \langle i_s \rangle = D(I) + D(0) \]
Large Step Conversion Ratio

Boost Converter

Flyback, $n=100$

Flyback Semiconductor Waveforms
Flyback Switch Implementation

Flyback Reverse Recovery
Flyback Reverse Recovery

\[
\begin{align*}
\langle i_u \rangle &= D I_{\text{in}} + \frac{t_v}{T_s} I_{\text{in}} + \frac{Q_v}{T_s} \\
\langle i_c \rangle &= 0 = D I_{\text{in}} - \frac{V}{R} - \frac{t_v}{n T_s} I_{\text{in}} - \frac{Q_v}{n T_s} \\
\langle v_{\text{in}} \rangle &= 0 = D V_g - D \left( \frac{V}{n} \right)
\end{align*}
\]
Discussion: Flyback converter

- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies
- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design
6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress $S$

In a converter having $k$ active semiconductor devices, the total active switch stress $S$ is defined as

$$ S = \sum_{j=1}^{k} V_j I_j $$

where

- $V_j$ is the peak voltage applied to switch $j$,
- $I_j$ is the rms current applied to switch $j$ (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.
Active switch utilization $U$

It is desired to minimize the total active switch stress, while maximizing the output power $P_{\text{load}}$.

The active switch utilization $U$ is defined as

$$ U = \frac{P_{\text{load}}}{S} $$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of $S$

During subinterval 2, the transistor blocks voltage $V_{\text{Q2,pk}}$ equal to $V_s$ plus the reflected load voltage:

$$ V_{Q2,pk} = V_s + \frac{V}{n} = \frac{V_s}{D} $$

Transistor current coincides with $i_s(t)$. RMS value is

$$ I_{Q2,\text{rms}} = I \sqrt{D} = \frac{P_{\text{load}}}{V_s \sqrt{D}} $$

Switch stress $S$ is

$$ S = V_{Q2,pk} I_{Q2,\text{rms}} = \left( \frac{V_s}{D} + \frac{V}{n} \right) I \sqrt{D} $$

Conducting devices:
CCM flyback example: Determination of $U$

Express load power $P_{\text{load}}$ in terms of $V$ and $I$:

$$P_{\text{load}} = D V \frac{I}{D}$$

Previously-derived expression for $S$:

$$S = V_{Q_{1\text{rev}}} I_{Q_{1\text{rev}}} = \left( V + \frac{V}{D} \right) I (1 - D)$$

Hence switch utilization $U$ is:

$$U = \frac{P_{\text{load}}}{S} = D (1 - D)$$

Flyback example: switch utilization $U(D)$

For given $V$, $V_{\text{max}}$, $P_{\text{load}}$, the designer can arbitrarily choose $D$. The turns ratio $n$ must then be chosen according to:

$$n = \frac{V}{V_{\text{max}}} \frac{D}{1 - D}$$

Single operating point design: choose $D = 1/3$.

small $D$ leads to large transistor current
large $D$ leads to large transistor voltage
Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

<table>
<thead>
<tr>
<th>Converter</th>
<th>$U(I)$</th>
<th>max $U(I)$</th>
<th>max $U(I)$ occurs at $D =$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck</td>
<td>$D$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Boost</td>
<td>$D' $</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk</td>
<td>$\frac{D}{D'}$</td>
<td>$\frac{D}{D'} = 0.385$</td>
<td>$\frac{1}{3}$</td>
</tr>
<tr>
<td>Forward $n_1 = n_2$</td>
<td>$\frac{1}{2} D$</td>
<td>$\frac{1}{2} D = 0.353$</td>
<td>$\frac{1}{2}$</td>
</tr>
<tr>
<td>Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)</td>
<td>$\frac{D'}{2 D}$</td>
<td>$\frac{D'}{2 D} = 0.353$</td>
<td>1</td>
</tr>
<tr>
<td>Isolated boost-derived converters (full bridge, push-pull)</td>
<td>$\frac{D}{2 D + D}$</td>
<td>$\frac{D}{2 D + D} = 0.5$</td>
<td>0</td>
</tr>
</tbody>
</table>

Active semiconductor cost vs. switch utilization

\[
\text{Active semiconductor cost per kW output power} = \left( \frac{\text{semiconductor device cost per rated kVA}}{\text{voltage derating factor}} \right) \left( \text{current derating factor} \right) \left( \frac{\text{converter switch utilization}}{1} \right)
\]

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in $\$/kVA. Typical values are less than $1/kVA.

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: $1 - $10 per kW of output power.