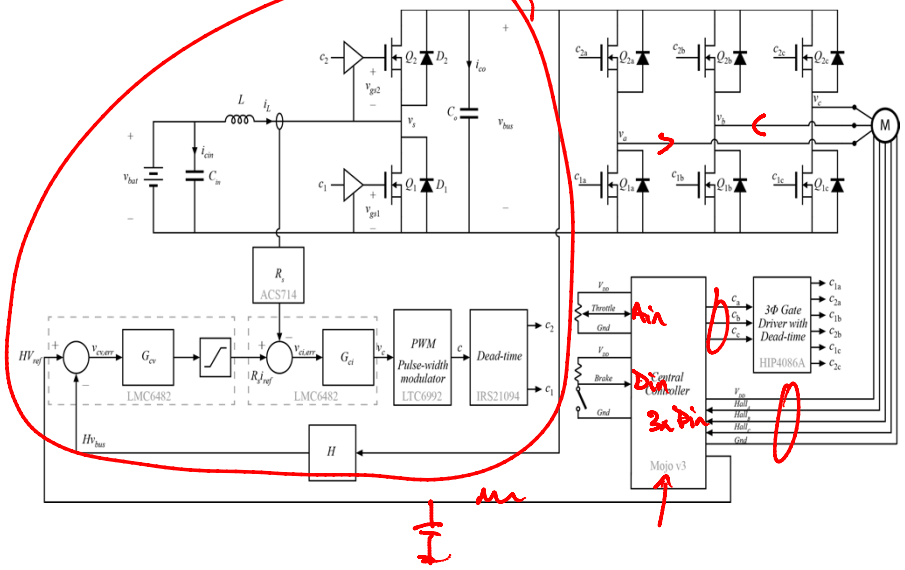
PCB Layout

ECE 482 Lecture 10
February 28, 2014

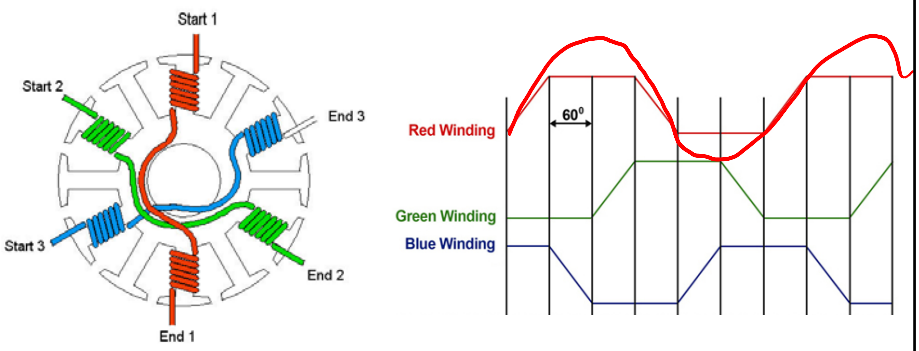
Announcements

- Prelab 4 due Friday
  - Decide on System Improvements
- Next week:
  - Demo closed-loop Voltage Regulation
  - Begin PCB Layout ASAP. Designs due Wed. Mar 12th.

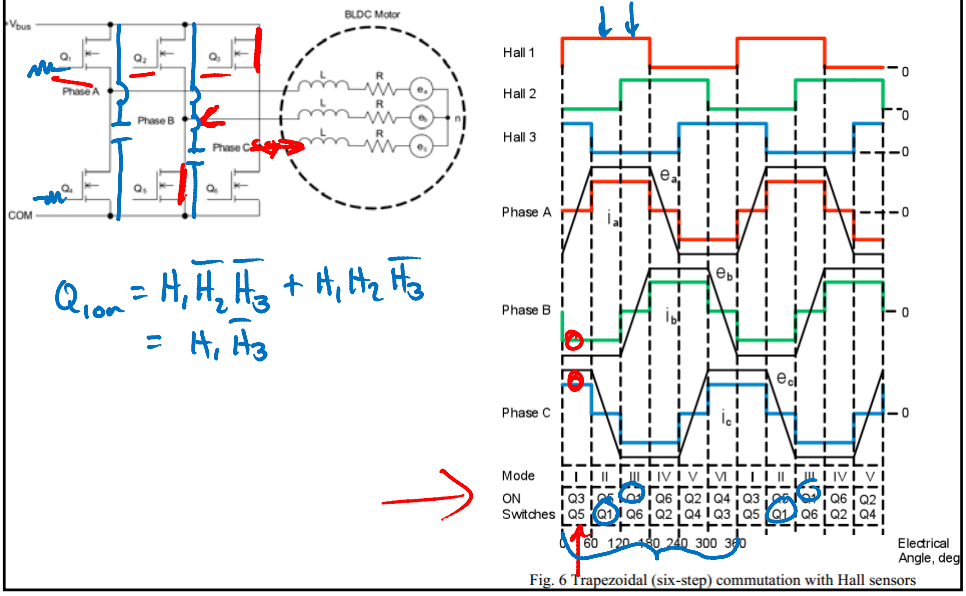
Lab 4: PCB Layout



6-step Trapezoidal Motor Control



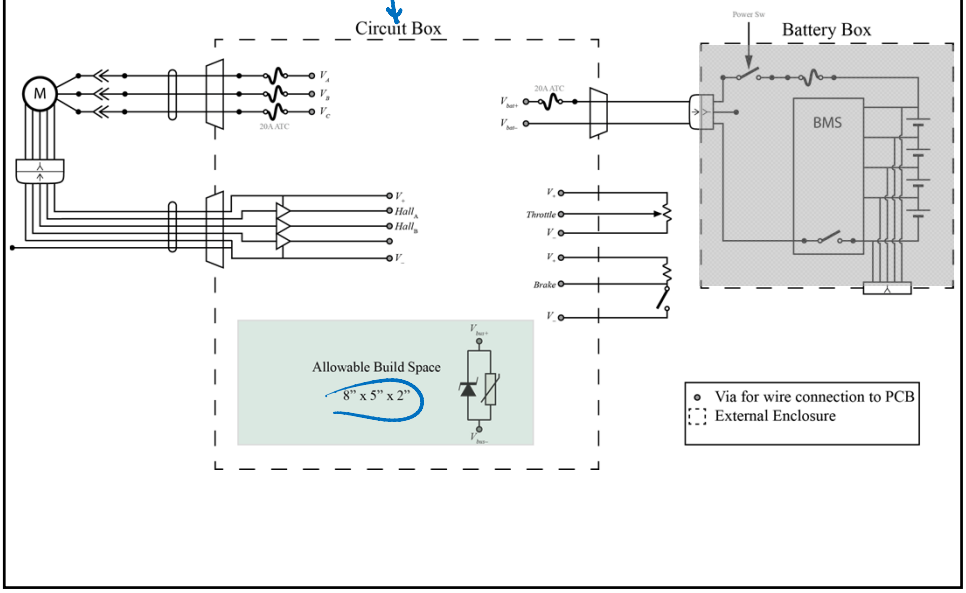
Trapezoidal Comm. Implementation

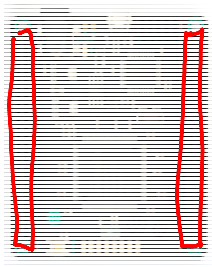


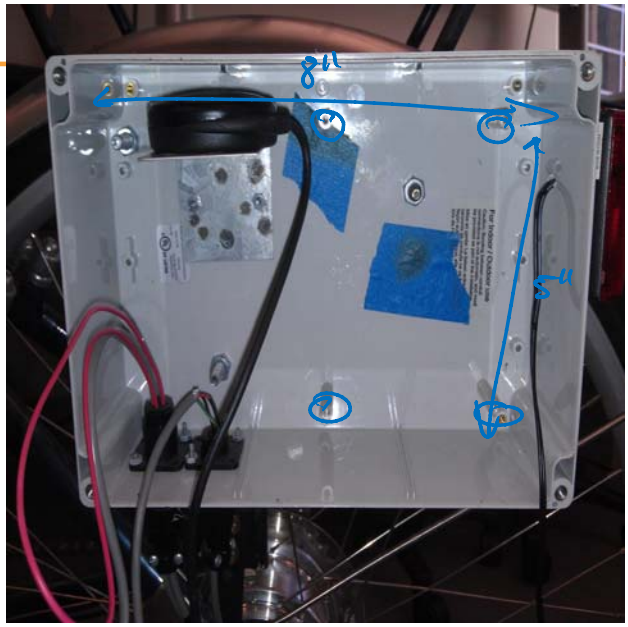
$Q_{1on} = H_1 \bar{H}_2 \bar{H}_3 + H_1 H_2 \bar{H}_3$
$= H_1 \bar{H}_3$

Fig. 6 Trapezoidal (six-step) commutation with Hall sensors

Circuit Connections







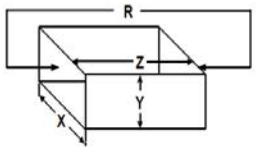
Basic PCB Layout Concepts

- Trace Resistances
- Kelvin Sensing
- Loop Inductances / Decoupling
- Ground Plane / Return Currents
- Partitioning

Trace Resistance

$$R = \frac{\rho Z}{XY}$$

ρ = RESISTIVITY



SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

$\rho = 1.724 \times 10^{-6}$ Ωcm; Y = 0.0036cm

$$R = 0.48 \frac{Z}{X} m\Omega$$

$\frac{Z}{X}$ = NUMBER OF SQUARES

R = SHEET RESISTANCE OF 1 SQUARE (Z=X)
= 0.48mΩ/SQUARE

Figure 12.2: *Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors*

Trace Sizing Rough Guidelines

2.2 *PCB Etch*

Table 1 is helpful to determine the current carrying capacity of PCB etches. The table assumes:

- 1oz/sq foot copper (0.035mm thickness).
- 10°C rise on outer layers, 20°C inner layers
- Groups of high current tracks are de-rated
- Tracks are not near or over heat sink areas

2-layer PCB

Table 1. Current Capacity PCB Etch

WIDTH	CURRENT CAPACITY
0.010"	0.8 A
0.015"	1.2 A
0.020"	1.5 A
0.050"	3.2 A
0.100"	6.0 A

2.3 *Vias or Feedthrus*

Vias limit the current and add inductance between the power supply and load. Layouts are usually done with 10-mil inner ring feedthrus. At this size, current capability is about 1 A per feedthru.

Kelvin Sensing

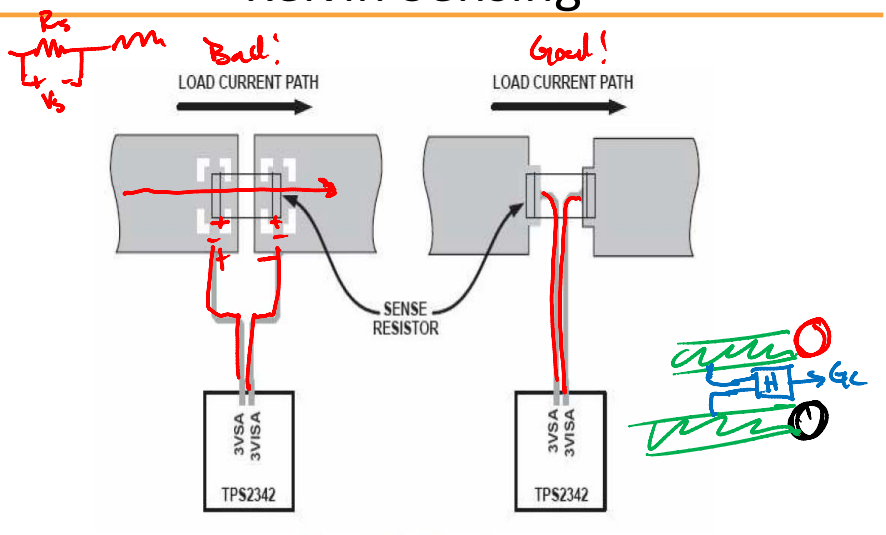
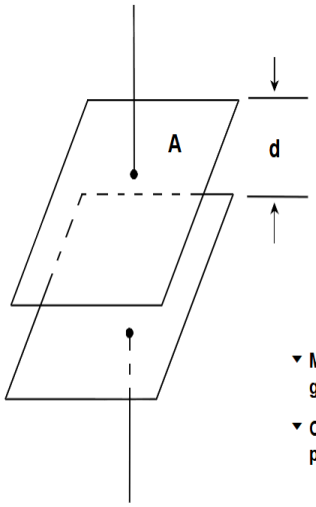


Figure 1. Kelvin Connection

Trace Capacitance



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

- Most common PCB type uses 1.5mm glass-fiber epoxy material with E_r = 4.7
- Capacitance of PC track over ground plane is roughly 2.8 pF/cm^2

Figure 12.24: *Capacitance of two parallel plates*

High Impedance Nodes and Capacitive Coupling

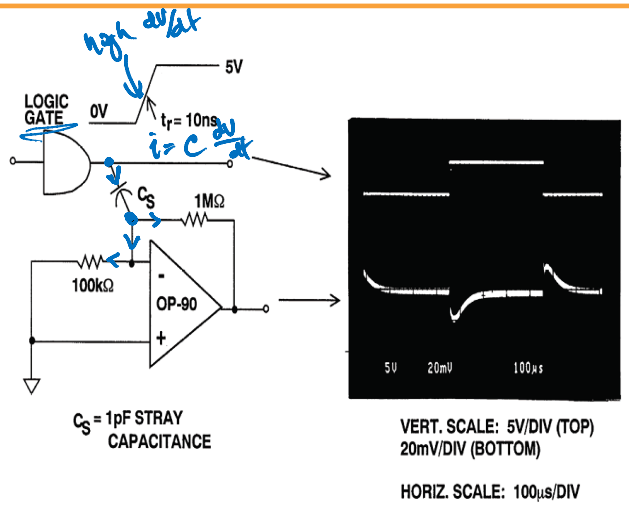


Figure 12.29 *High Circuit Impedances Increase Susceptibility to Noise Pickup*

Capacitive Shielding

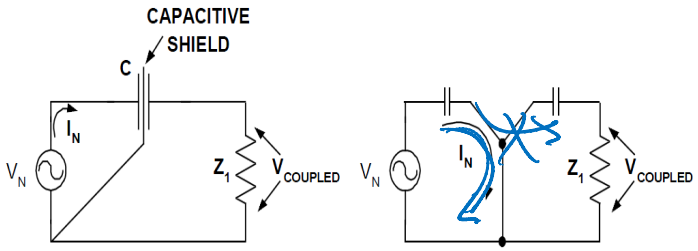
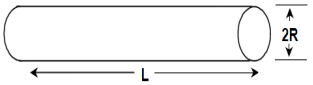


Figure 12.26: *An Operational Model of a Faraday Shield*

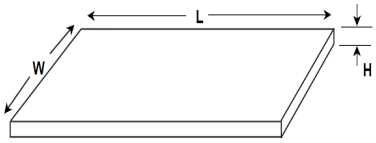
Trace Inductance



L, R in mm

WIRE INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\ \mu H$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)

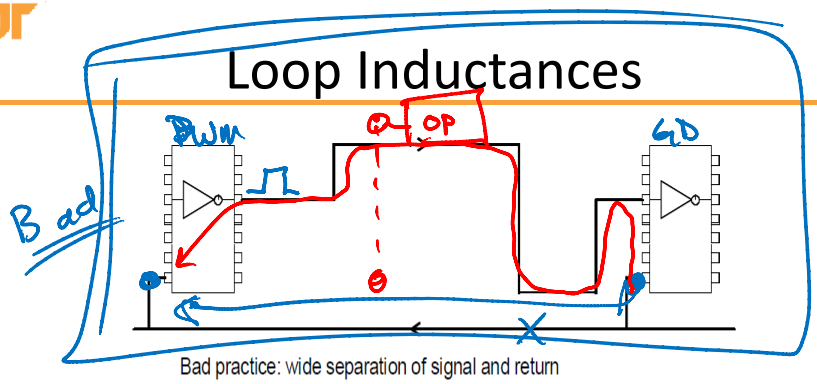


STRIP INDUCTANCE = $0.0002L\left[\ln\frac{2L}{(W+H)} + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H$

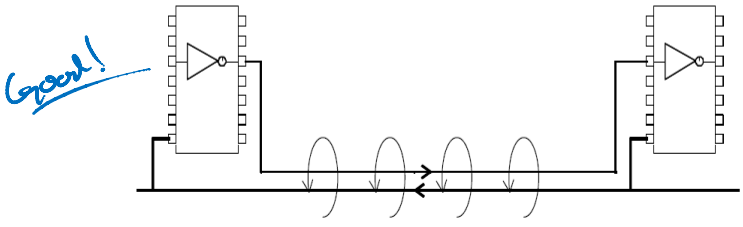
EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

Figure 12.18: *Wire and Strip Inductance Calculations*

Loop Inductances



Bad practice: wide separation of signal and return



Good practice: close coupling of signal and return

Loop Inductance: Experiment

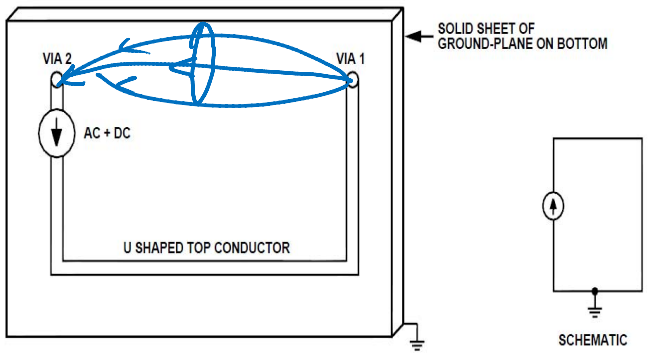


Figure 12.60: *Schematic and Layout of Current Source with U-shaped Trace on PC Board and Return through Ground Plane.*

Loop Inductance: Experiment

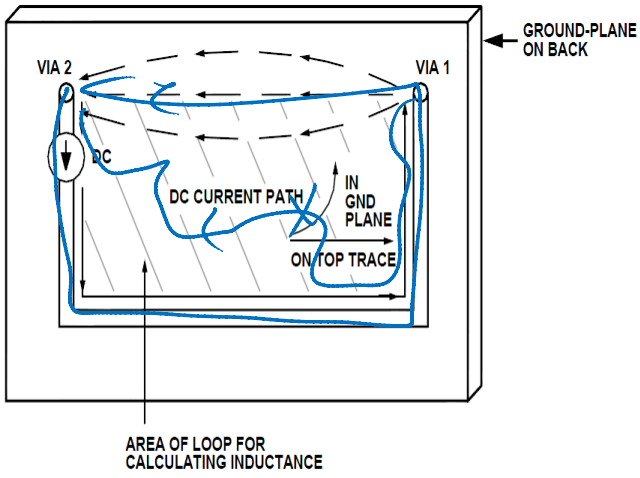


Figure 12.61: *DC Current Flow for Figure 12.60*

Loop Inductance: Experiment

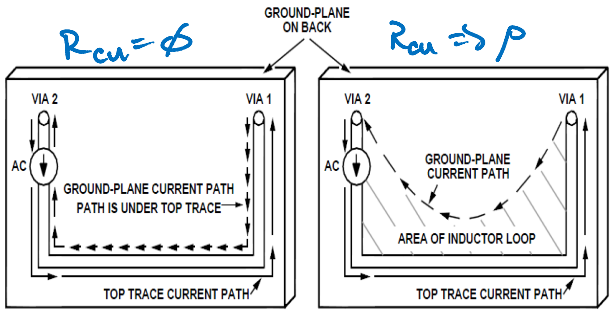
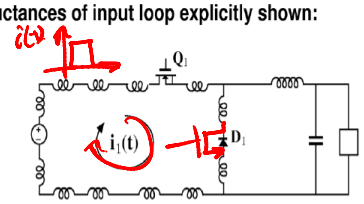
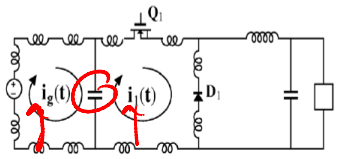


Figure 12.63: *AC Current Path Without (left) and with (right) Resistance in the Ground Plane*

Parasitic inductances of input loop explicitly shown:

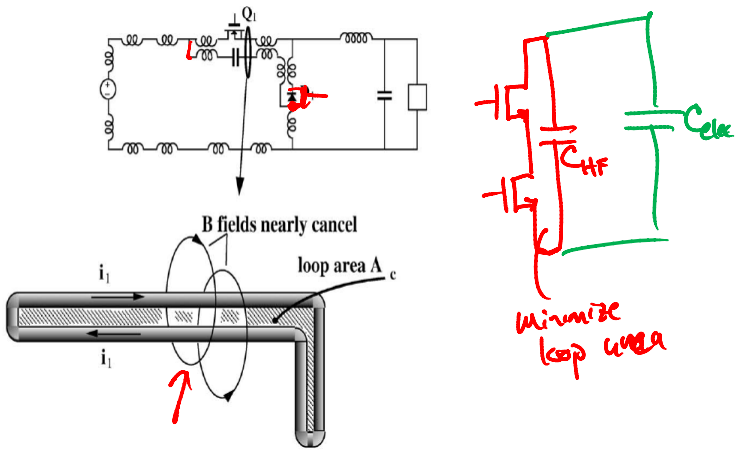


Addition of bypass capacitor confines the pulsating current to a smaller loop:

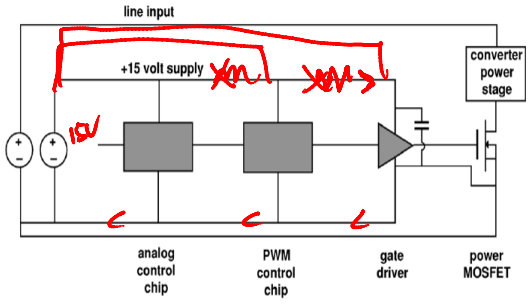


high frequency currents are shunted through capacitor instead of input source

Even better: minimize area of the high frequency loop, thereby minimizing its inductance



Solution: bypass capacitor and close coupling of gate and return leads



High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

Op-amp Pulsed Decoupling

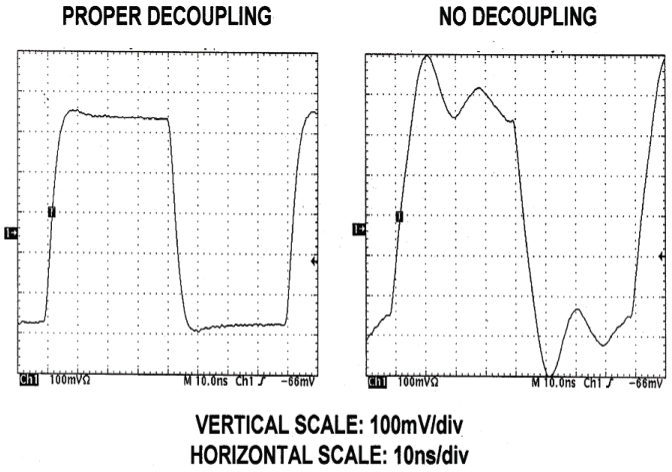


Figure 12.68: *Effects of Inadequate Decoupling on the Phase Response of the AD9631 Op Amp*

Star-Grounding Vs. Daisy Chain

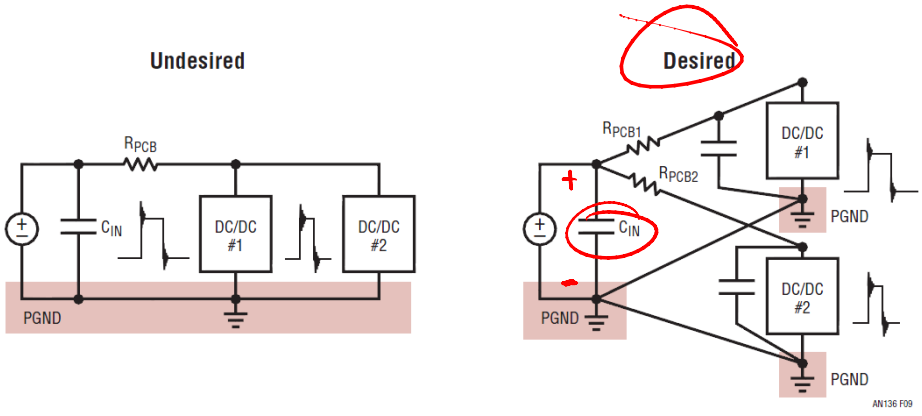


Figure 9. Separate the Input Current Paths Among Supplies

Gate Drive Signal Routing

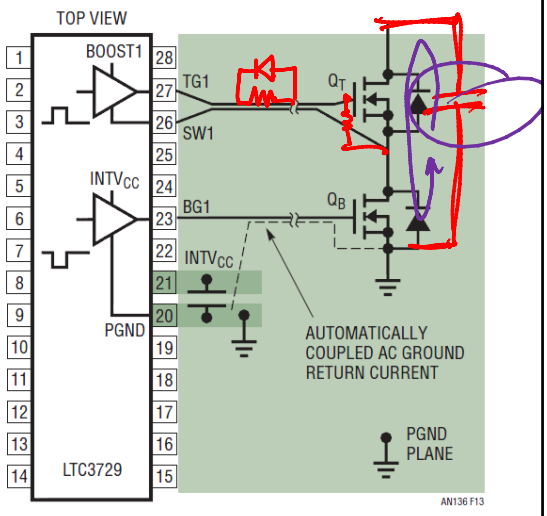


Figure 13. Gate Driver Trace Routing of the MOSFETs

Buck Example Bridge Layout

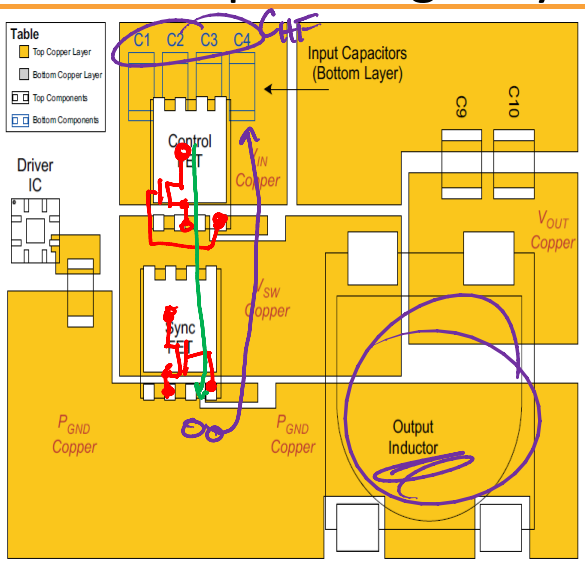


Figure 2. Typical Placement and PCB Layout of the Power Stage Components

Example Bridge Layout #2

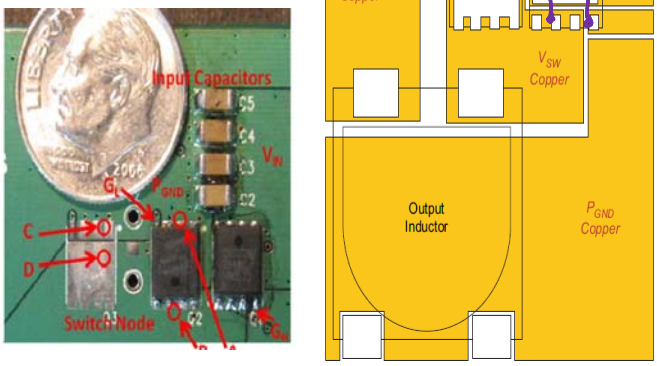


Figure 3. Optimized Placement and PCB Layout of Power Stage Components

Example Layout Experimental Results

Example Layout #1

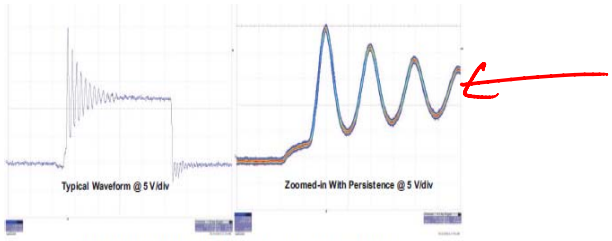


Figure 4. Switch Node (VSW) Voltage Ringing on Typical Layout

Example Layout #2

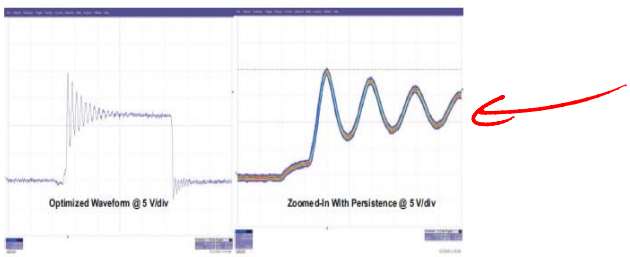


Figure 5. Switch Node (VSW) Voltage Ringing on Optimized Layout

Decoupling Capacitance

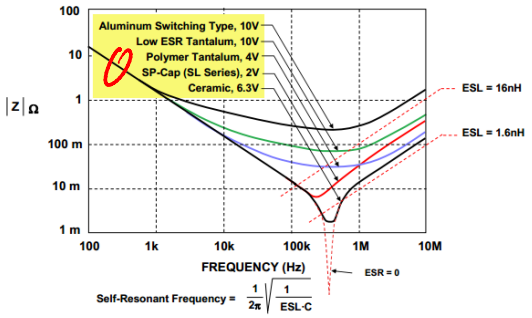
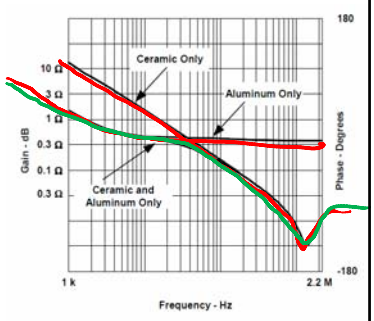


Figure 4: Impedance of Various 100µF Capacitors



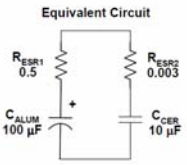


Fig. 8. Paralleled capacitors minimize impedance over frequency.

Capacitor Packaging

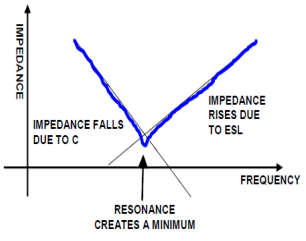


FIGURE 8. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL)

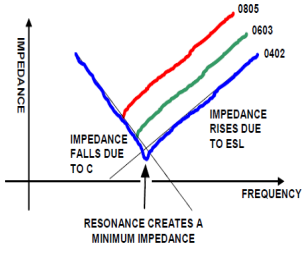


FIGURE 9. IMPEDANCE OF AN ACTUAL CAPACITOR (NON-IDEAL) IN DIFFERENT SURFACE-MOUNT PACKAGES

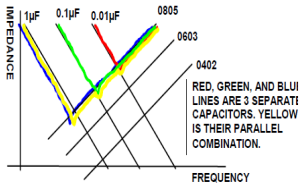


FIGURE 10. IMPEDANCE OF THREE CAPACITORS, THE SAME SURFACE-MOUNT PACKAGES

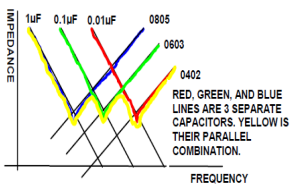
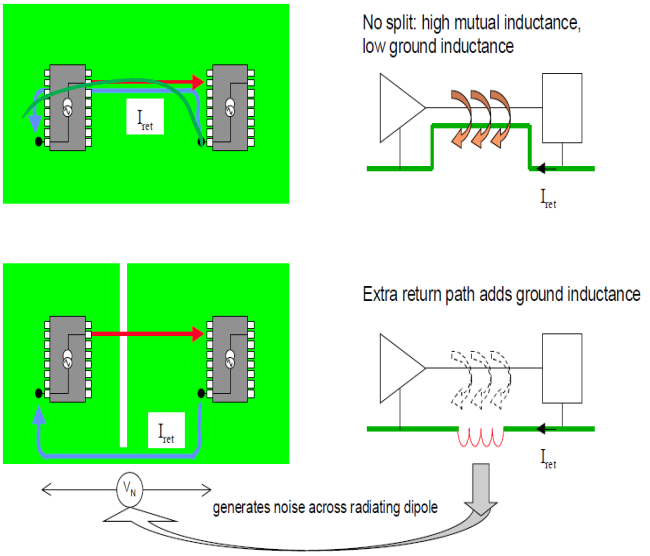


FIGURE 11. IMPEDANCE OF THREE CAPACITORS, SCALED SURFACE-MOUNT PACKAGES

Ground Plane

- Benefits:
  - Common reference voltage
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable

Ground Currents



Acceptable Cuts in Ground Plane

- Cuts that are necessary should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

Partitioning

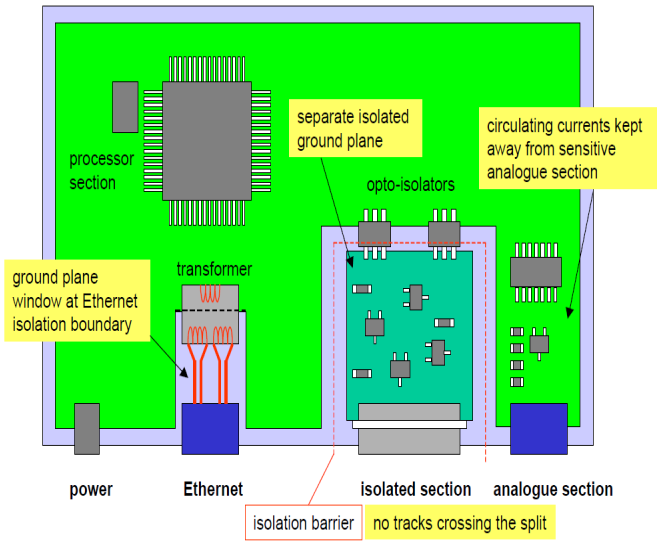


Figure 4 Uses of ground plane windows

Effective Ground Plane Cuts