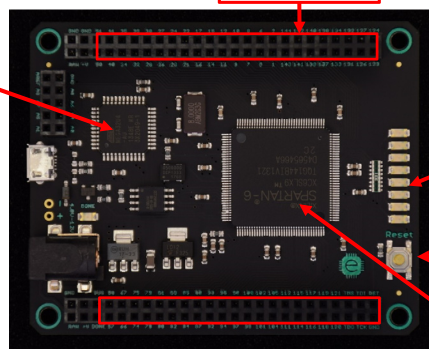
Converter Loss Analysis

ECE 482 Lecture 3
January 20, 2015

Announcements

- Finish Experiment 1: report due Tuesday, 1/27
- This week: Experiment 2
  - Intro to FPGA programming
- Next week: Experiment 3
  - Boost converter design and construction
  - Open-loop, steady-state efficiency analysis
- Component kits available in circuits store later this week
  - $100 *per group* for components for Labs 3 and after
  - Plan to spend additional ~$5.00 on resistors, etc.

Mojo v3 FPGA Development Board



Spartan-6 FPGA Feature Summary

Table 1: **Spartan-6 FPGA Feature Summary by Device**

Device	Logic Cells(1)	Configurable Logic Blocks (CLBs)			DSP48A1 Slices(3)	Block RAM Blocks		CMTs(5)	Memory Controller Blocks (Max)(6)	Endpoint Blocks for PCI Express	Maximum GTP Transceivers	Total I/O Banks	Max User I/O
		Slices(2)	Flip-Flops	Max Distributed RAM (Kb)		18 Kb(4)	Max (Kb)						
XC6SLX4	3,840	600	4,800	75	8	12	216	2	0	0	0	4	132
XC6SLX9	9,152	1,430	11,440	90	16	32	576	2	2	0	0	4	200
XC6SLX16	14,579	2,278	18,224	136	32	32	576	2	2	0	0	4	232

Words of Caution

- Very easy to blow pins on FPGA
  - 4V maximum!
    - Use resistor dividers when necessary
  - Double- and Triple-check I/O and connections before operating device

Basics of FPGA programming

- **Microcontroller**
  - Processor, ram, etc.
  - Code is instruction set; executed sequentially
- **FPGA**
  - Application specific circuitry
  - Code is hardware design language; all in parallel

Technology	Performance/Cost	Time until running	Time to high performance	Time to change code functionality
ASIC	Very High	Very Long	Very Long	Impossible
Custom Processor/ DSP	Medium	Long	Long	Long
FPGA	Low-Medium	Short	Short	Short
Generic	Low-Medium	Short	Not Attainable	Short

Speed ↑ Flexibility ↓

WP213_12_061104

Figure 12: **Design Choices**[4]

http://www.xilinx.com/support/documentation/white_papers/wp213.pdf

Configurable Logic Block

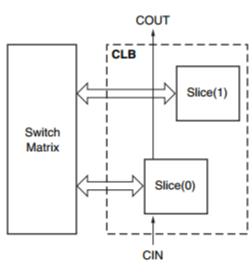


Figure 1: **Arrangement of Slices within the CLB**

Slice

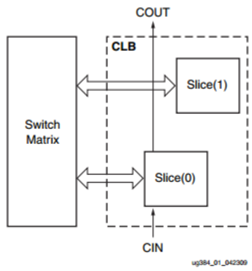


Figure 1: **Arrangement of Slices within the CLB**

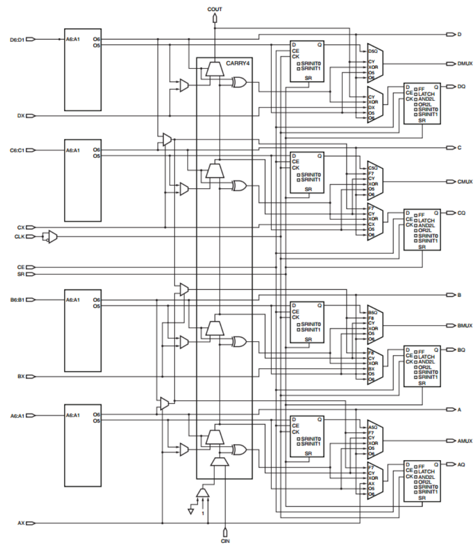


Figure 4: **Diagram of SLICEL**

Getting Started with Mojo v3

- Resources from board developer:
  - Tutorials
    - https://embeddedmicro.com/tutorials/mojo
  - Base Project
    - https://github.com/embmicro/mojo-base-project/archive/master.zip
- Will be coding in Xilinx ISE
- Mojo Loader used to write .bit file to on-board RAM/Flash

Base Project

```
module mojo_top(
    // 50MHz clock input
    input clk,
    // Input from reset button (active low)
    input rst_n,
    // cclk input from AVR, high when AVR is ready
    input cclk,
    // Outputs to the 8 onboard LEDs
    output[7:0]led,
    // AVR SPI connections
    output spi_miso,
    input spi_ss,
    input spi_mosi,
    input spi_sck,
    // AVR ADC channel select
    output [3:0] spi_channel,
    // Serial connections
    input avr_tx, // AVR Tx => FPGA Rx
    output avr_rx, // AVR Rx => FPGA Tx
    input avr_rx_busy // AVR Rx buffer full
    );

wire rst = ~rst_n; // make reset active high

// these signals should be high-z when not used
assign spi_miso = 1'bz;
assign avr_rx = 1'bz;
assign spi_channel = 4'bzzzz;

assign led = 8'b0;

endmodule
```

User Constraints File (.ucf)

```
#Created by Constraints Editor (xc6slx9-tqg144-3) - 2012/11/05
NET "clk" TNM_NET = clk;
TIMESPEC TS_clk = PERIOD "clk" 50 MHz HIGH 50%;

# PlanAhead Generated physical constraints
NET "clk" LOC = P56;
NET "rst_n" LOC = P38;

NET "cclk" LOC = P70;

NET "led<0>" LOC = P134;
NET "led<1>" LOC = P133;
NET "led<2>" LOC = P132;
NET "led<3>" LOC = P131;
NET "led<4>" LOC = P127;
NET "led<5>" LOC = P126;
NET "led<6>" LOC = P124;
NET "led<7>" LOC = P123;

NET "spi_mosi" LOC = P44;
NET "spi_miso" LOC = P45;
NET "spi_ss" LOC = P48;
NET "spi_sck" LOC = P43;
NET "spi_channel<0>" LOC = P46;
NET "spi_channel<1>" LOC = P61;
NET "spi_channel<2>" LOC = P62;
NET "spi_channel<3>" LOC = P65;

NET "avr_tx" LOC = P55;
NET "avr_rx" LOC = P59;
NET "avr_rx_busy" LOC = P39;
```

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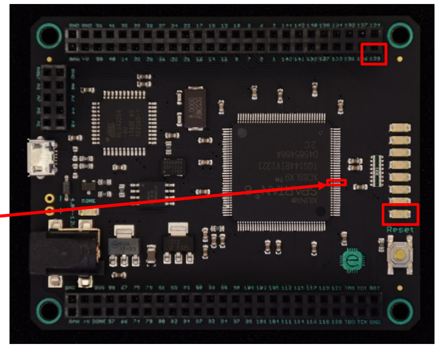
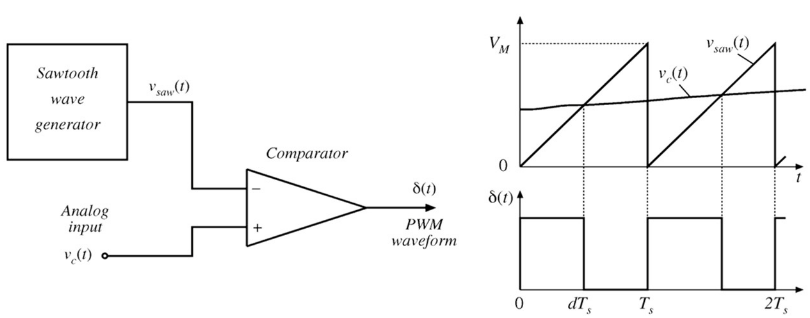


A Simple PWM

- Note: separate example given in Mojo tutorials on website



Digital Implementation

Verilog Code

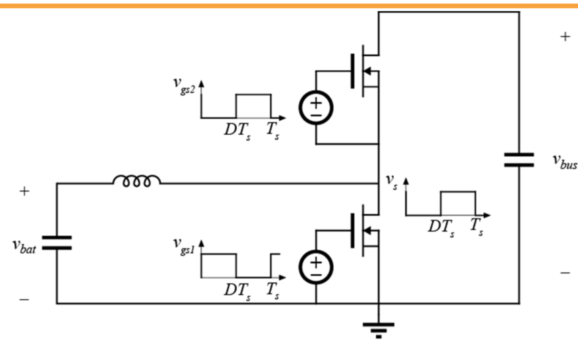
```
`define MAX_MOD_VALUE  198    // Modulator # of periods -1
`define MOD_SIZE  8           // Modulator Length, must be large enough to store MAX_MOD_VALUE

`define MSB_MOD  (`MOD_SIZE - 1)             //7:0


module modulator(
    input [`MSB_MOD:0] dutycycle,
    input rst,
    input clk,
    output DPWM,
    output dsample
    );

   reg [`MSB_MOD:0] duty_Mod;                //Modulator Duty Cycle
   reg dsample;
   reg [`MSB_MOD:0] mod_value;

   always @ (posedge clk or posedge rst)
   //Modulator implementation
   begin
      if (rst == 1)
         mod_value <= 0;
      else
      begin
         mod_value <= (mod_value > `MAX_MOD_VALUE) ? 0 : mod_value+1;   //increment/loop modulator
         dsample <= (mod_value == `MAX_MOD_VALUE);                      //sample new duty cycle on overflow
      end
   end

   assign DPWM = mod_value < duty_Mod;

   always @ (negedge dsample)
   //duty cycle sampled at end of modulator period.
   begin
      duty_Mod[`MSB_MOD:0] <= dutycycle;
   end

endmodule

```

Converter Loss Modeling

Analytical Loss Modeling

- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
- Argue which losses need to be included, and which may be neglected

Boost Converter Loss Analysis



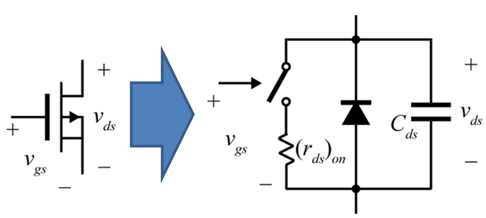
- Begin by solving important waveforms throughout converter assuming lossless operation

Power Stage Losses

	MOSFETS	IGBTs	Diodes	Inductor	Capacitors
Conduction Losses	• R_{on}	• r_{ce} • V_{ce}	• V_F • R_d	• R_{dc}	• ESR
Frequency-Dependent Losses	• C_{oss} • Overlap • P_g	• Current tailing	• C_d • Reverse-Recovery	• Skin Effect • Core Loss • Fringing • Proximity	• Dielectric Losses

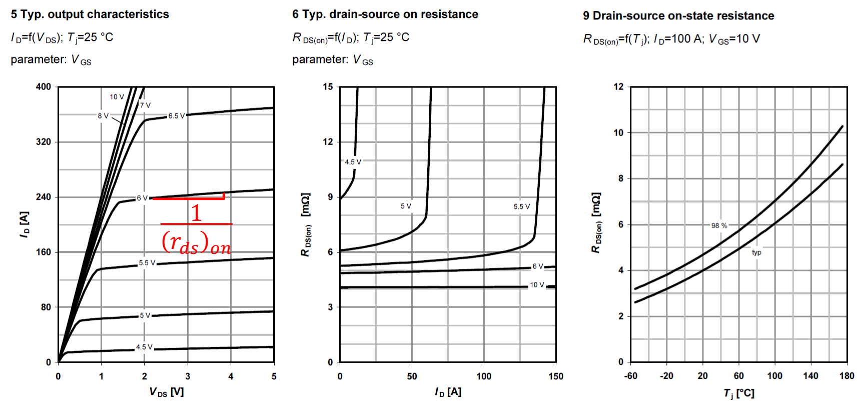
Conduction Loss Modeling

MOSFET Equivalent Circuit



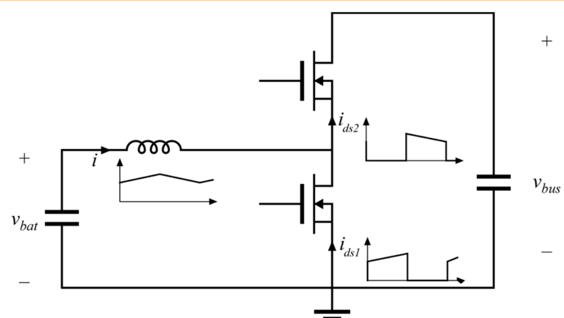
- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

MOSFET On Resistance



- On resistance extracted from datasheet waveforms
- Significantly dependent on V_{gs} amplitude, temperature

Boost Converter RMS Currents



- MOSFET conduction losses due to $(r_{ds})_{on}$ depend given as

$$P_{cond,FET} = I_{di,rms}{}^2 (r_{ds})_{on}$$

MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \qquad \text{(A.6)}$$

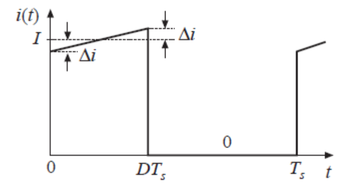
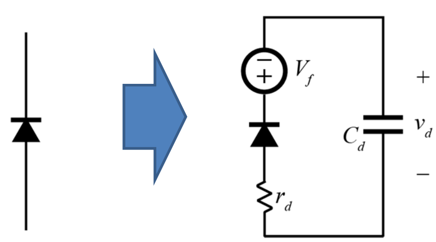


Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

Diode Loss Model



- Example loss model includes resistance and forward voltage drop extracted from datasheet

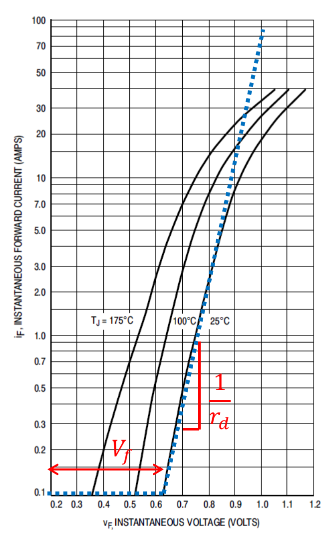
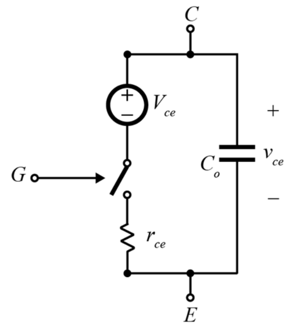
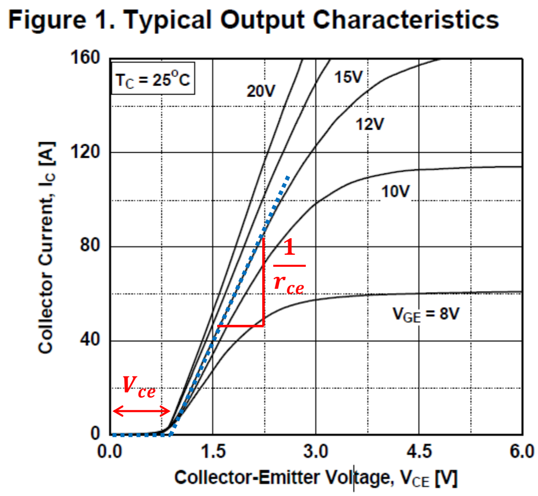


Figure 1. Typical Forward Voltage

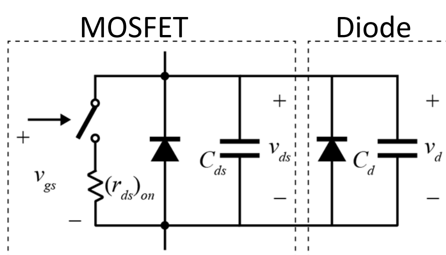
IGBT Loss Model



$$P_{cond} = I_{c,rms}{}^2 r_{ce} + V_{ce} I_{c,avg}$$



Semiconductor Switch Conduction Loss



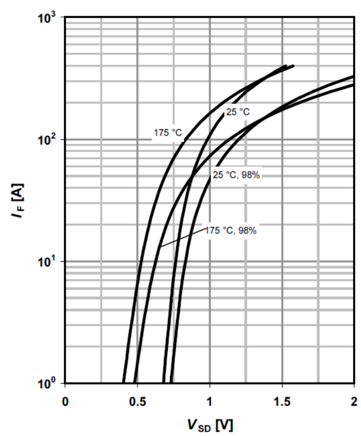
- Equivalent circuit of MOSFET with external antiparallel diode has two, non-ideal diodes
- Diodes, even when matched, will not share current equally, but $v_d = v_{ds}$ must remain true
- Silicon rectifier diodes are minority carrier devices
  - Concentration of minority carriers depends heavily on temperature

Diode Paralleling

12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

parameter: T_j



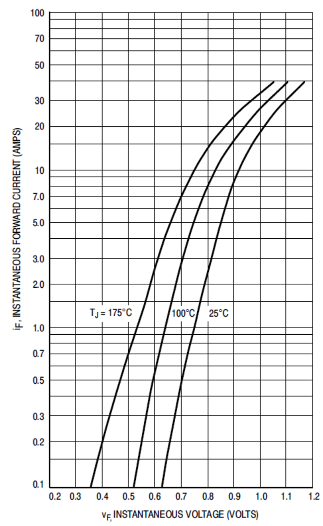
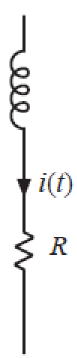


Figure 1. Typical Forward Voltage

DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

- At room temp, ρ = 1.724·10^{-6} Ω-cm
- At 100°C, ρ = 2.3·10^{-6} Ω-cm
- Losses due to DC current:

$$P_{cu,DC} = I_{L,rms}{}^2 R_{DC}$$

Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$rms = I\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \qquad \text{(A.2)}$$

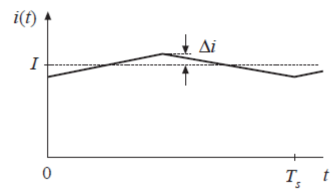
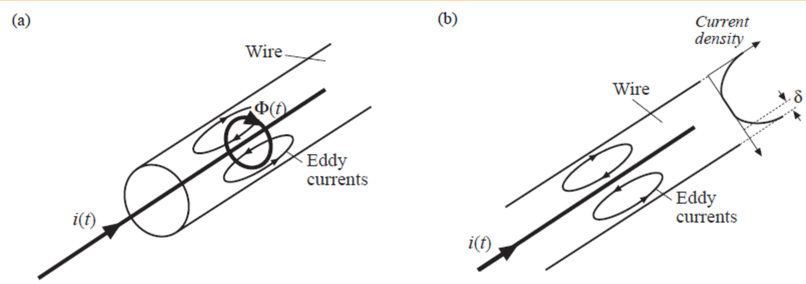


Fig. A.2

- Conduction losses dependent on RMS current through inductor

Skin Effect in Copper Wire



- Current profile at high frequency is exponential function of distance from center with characteristic length δ

Skin Depth

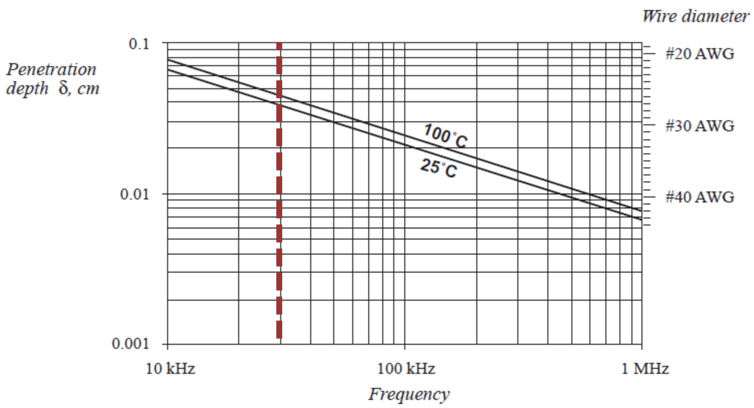
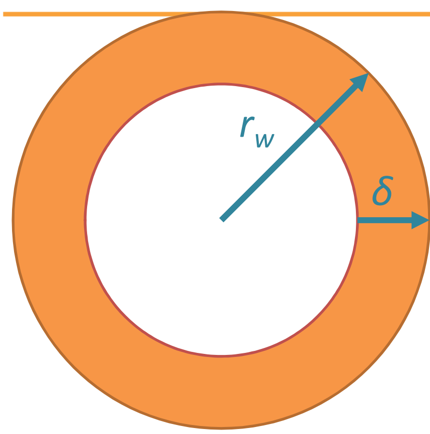


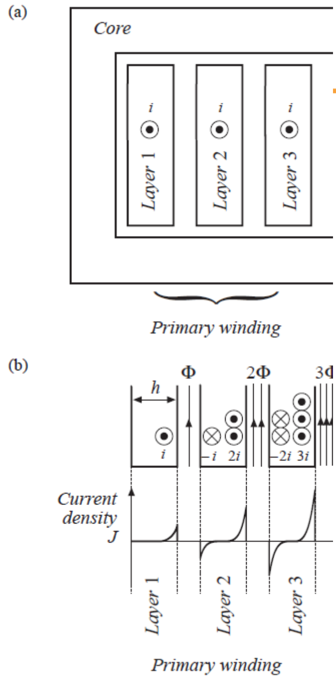
Fig. 13.23 Penetration depth δ, as a function of frequency *f*, for copper wire.

AC Resistance



$$A_{w,eff} = \pi {r_w}^2 - \pi(r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$



Proximity Effect

- In *foil* conductor closely spaced with *h* >> δ, flux between layers generates additional current according to Lentz's law.

$$P_1 = {I_{L,rms}}^2 R_{ac}$$

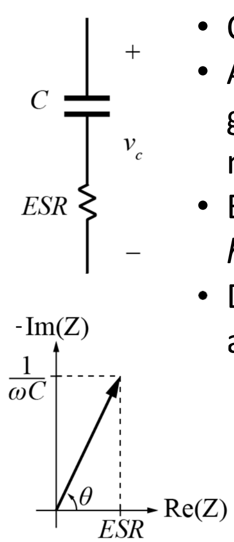
- Power loss in layer 2:

$$P_2 = {I_{L,rms}}^2 R_{ac} + (2I_{L,rms})^2 R_{ac}$$

$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

Capacitor Loss Model



- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:

$$\delta = \frac{\pi}{2} - \theta$$
$$D = \tan(\delta)$$

Capacitor ESR Extraction

WV (Vdc)	Cap (μF)	Case size ϕD×L(mm)	Impedance (Ωmax/100kHz)		Rated ripple current (mArms/ 105℃, 100kHz)	Part No.
			20℃	-10℃		
	6.8	5×11	1.4	5.6	125	EKZE101E□□6R8ME11D
	15	6.3×11	0.57	2.3	205	EKZE101E□□150MF11D
	27	8×11.5	0.36	1.4	355	EKZE101E□□270MHB5D
	39	8×15	0.25	1.0	450	EKZE101E□□390MH15D
	47	10×12.5	0.17	0.66	480	EKZE101E□□470MJC5S
	56	8×20	0.19	0.76	565	EKZE101E□□560MH20D
	68	10×16	0.11	0.47	600	EKZE101E□□680MJ16S
	82	10×20	0.084	0.34	800	EKZE101E□□820MJ20S
	100	12.5×16	0.11	0.34	750	EKZE101E□□101MK16S
	120	10×25	0.069	0.28	900	EKZE101E□□121MJ25S
	150	12.5×20	0.062	0.18	1,100	EKZE101E□□151MK20S
	220	12.5×25	0.047	0.14	1,250	EKZE101E□□221MK25S
100	220	16×20	0.048	0.15	1,350	EKZE101E□□221ML20S
	270	12.5×30	0.042	0.13	1,500	EKZE101E□□271MK30S

Dissipation Factor: 1% Max. (25 °C, 1kHz)

Dissipation Factor (tanδ)										
	Rated voltage (Vdc)	6.3V	10V	16V	25V	35V	50V	63V	80V	100V
	tanδ (Max.)	0.22	0.19	0.16	0.14	0.12	0.10	0.09	0.09	0.08
	When nominal capacitance exceeds 1,000μF, add 0.02 to the value above for each 1,000μF increase. (at 20℃, 120Hz)									

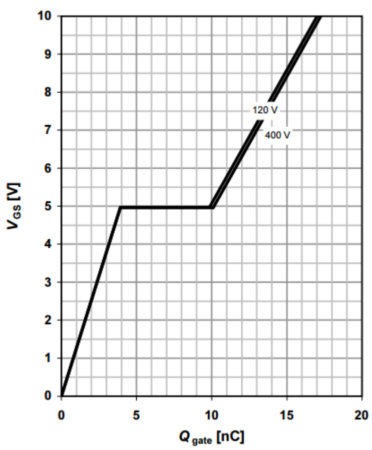
Switching Loss Modeling

Gate Charge Loss

9 Typ. gate charge

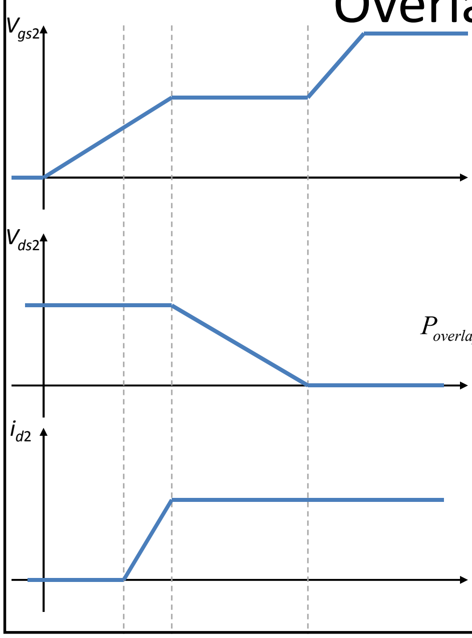
V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

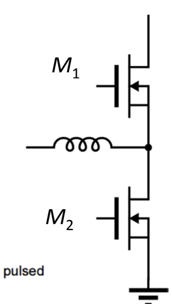
parameter: V_{DD}



$$P_g = Q_g V_{cc} f_s$$

Overlap Loss



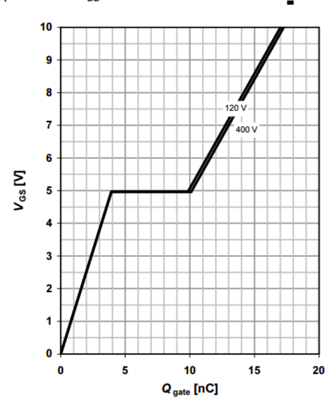


$$P_{overlap} = \frac{1}{2} I_L V \frac{t_{sw}}{T_s}$$

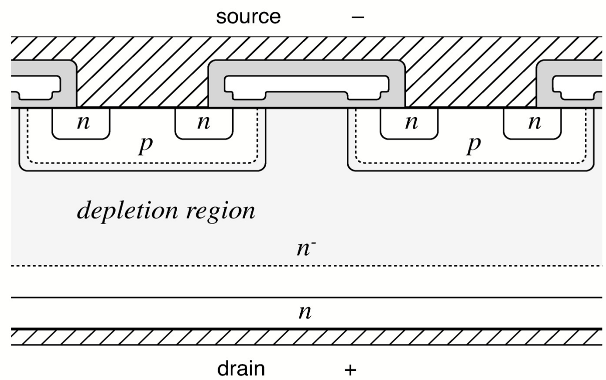
9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

parameter: V_{DD}

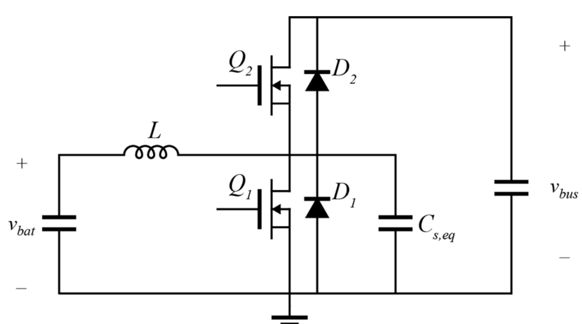


MOSFET Parasitic Capacitances



- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

Lump Switched Node Capacitance



- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices

Device Output Capacitances

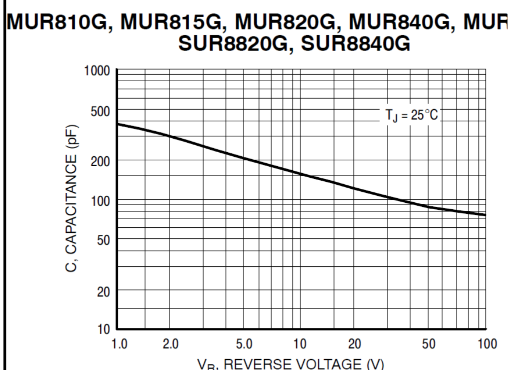
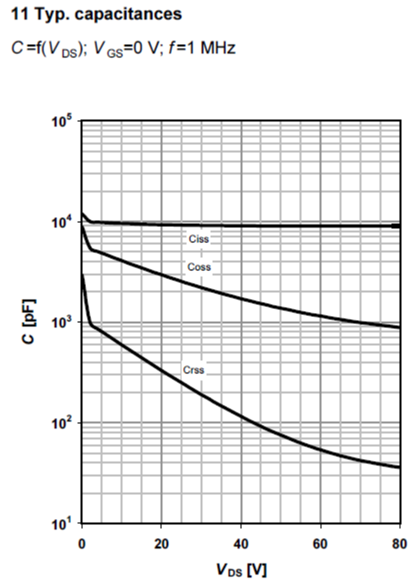
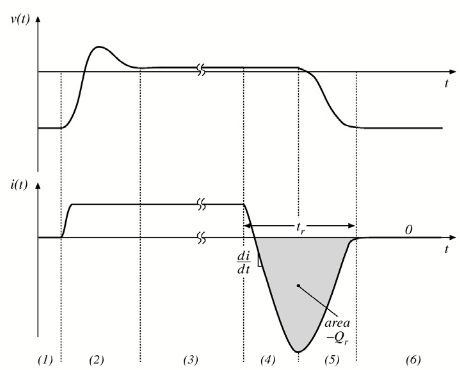


Figure 19. Typical Capacitance



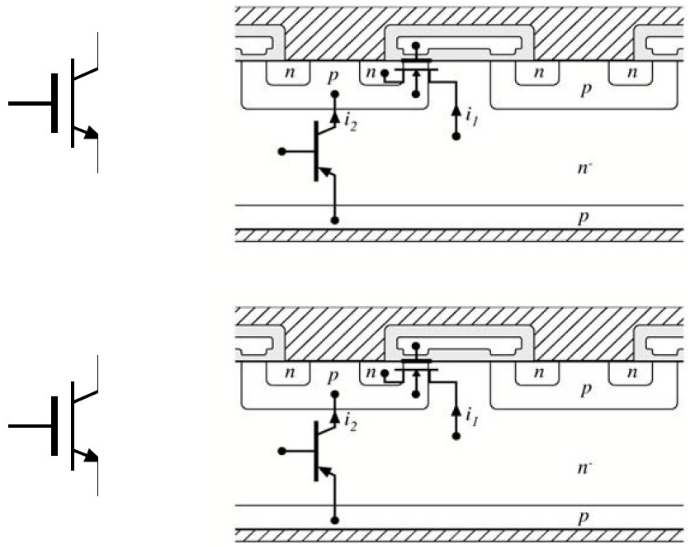
Diode Reverse Recovery

- Diodes will turn on during dead time intervals
- Significant reverse recovery possible on both body diode and external diode

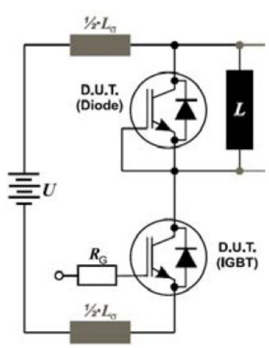


$$E_{on,rr} = ((I_L - \Delta i_L)t_{rr} + Q_{rr})V_{bus}$$

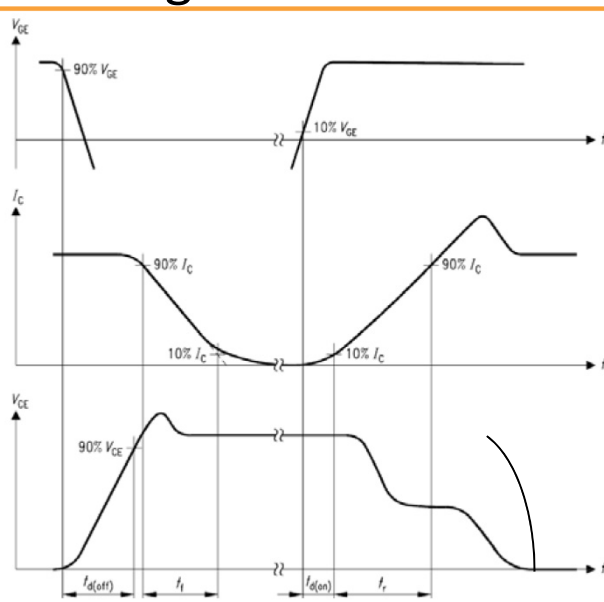
IGBT Switching



IGBT Switching Waveforms



Test circuit
(inductive switching)



Datasheet Reporting of IGBT Switching Loss

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 200 V, I_C = 20 A, R_G = 5 Ω, V_{GE} = 15 V, Resistive Load, T_C = 25°C	-	9	-	ns
t_r	Rise Time		-	33	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	32	-	ns
t_f	Fall Time		-	202	-	ns
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 200 V, I_C = 20 A, R_G = 5 Ω, V_{GE} = 15 V, Resistive Load, T_C = 125°C	-	9	-	ns
t_r	Rise Time		-	37	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33	-	ns
t_f	Fall Time		-	332	-	ns

Figure 15. Switching Loss vs. Gate Resistance

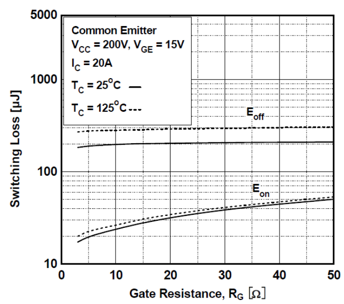
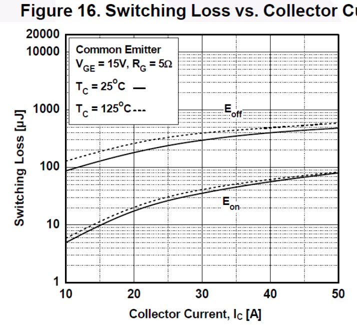


Figure 16. Switching Loss vs. Collector Current



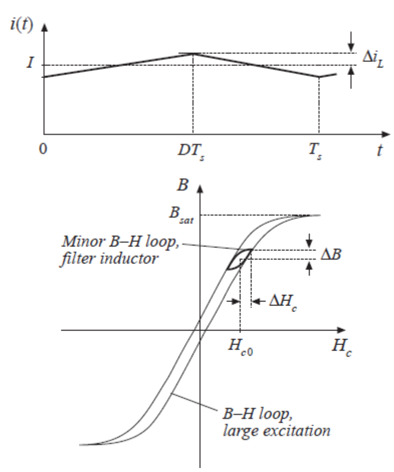
Inductor Core Loss

- Governed by Steinmetz Equation:

$$P_v = K_{fe} {f_s}^{\alpha} (\Delta B)^{\beta} \quad [\text{mW/cm}^3]$$

- Parameters K_{fe}, α, and β extracted from manufacturer data
- $\Delta B \propto \Delta i_L \rightarrow$ small losses with small ripple

$$P_{fe} = P_v A_c l_m \; [\text{mW}]$$



Steinmetz Parameter Extraction

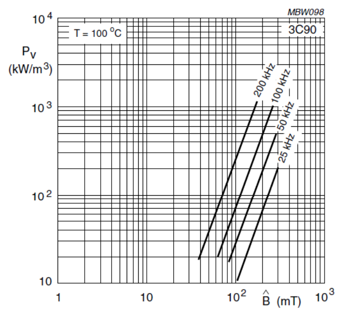


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

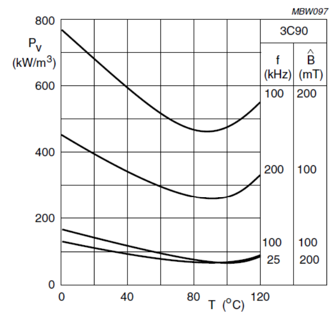


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B^y_{peak} \cdot (ct_0 - ct_1 T + ct_2 T^2) \qquad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B^y_{peak} \qquad [\text{mW/cm}^3]$$

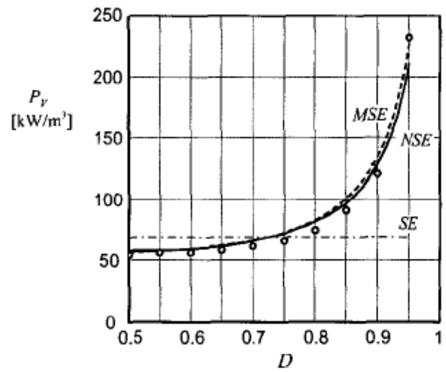
ferrite	f (kHz)	Cm	x	y	ct_2	ct_1	ct_0
3C30	20-100	$7.13.10^{-3}$	1.42	3.02	$3.65.10^{-4}$	$6.65.10^{-2}$	4
	100-200	$7.13.10^{-3}$	1.42	3.02	4.10^{-4}	$6.8\ .10^{-2}$	3.8
3C90	20-200	$3.2.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3C94	20-200	$2.37.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
	200-400	2.10^{-9}	2.6	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3F3	100-300	$0.25.10^{-3}$	1.63	2.45	$0.79.10^{-4}$	$1.05.10^{-2}$	1.26
	300-500	2.10^{-5}	1.8	2.5	$0.77.10^{-4}$	$1.05.10^{-2}$	1.28
	500-1000	$3.6.10^{-9}$	2.4	2.25	$0.67.10^{-4}$	$0.81.10^{-2}$	1.14
3F4	500-1000	12.10^{-4}	1.75	2.9	$0.95.10^{-4}$	$1.1.10^{-2}$	1.15
	1000-3000	$1.1.10^{-11}$	2.8	2.4	$0.34.10^{-4}$	$0.01.10^{-2}$	0.67

Table 1: Fit parameters to calculate the power loss density

NSE/iGSE

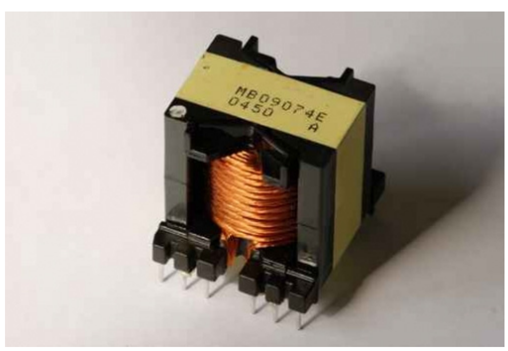
- More complex empirical loss models exist, and remain valid for non-sinusoidal waveforms
- NSE/iGSE:

$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt$$

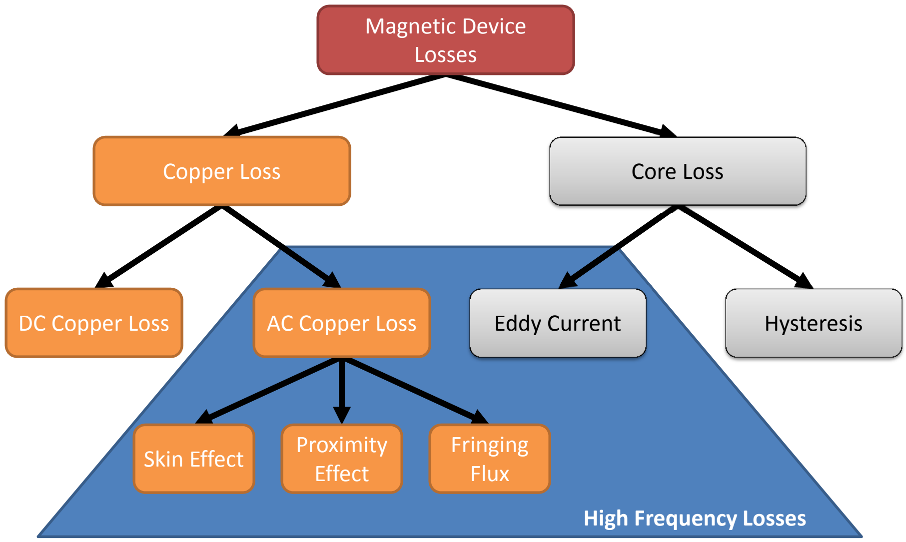


Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; , "Measurement and loss model of ferrites with non-sinusoidal waveforms," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* , vol.6, no., pp. 4814- 4818 Vol.6, 20-25 June 2004 doi: 10.1109/PESC.2004.1354851

Inductor Design

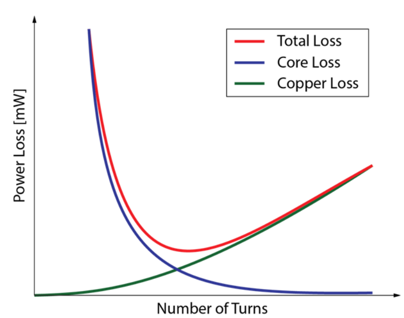


Magnetics Losses

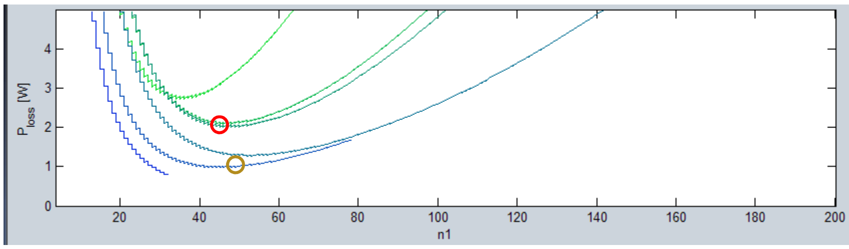


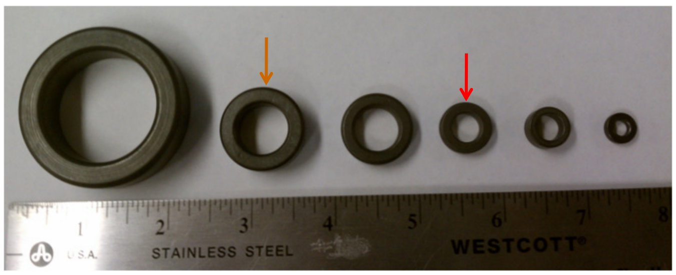
Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved for

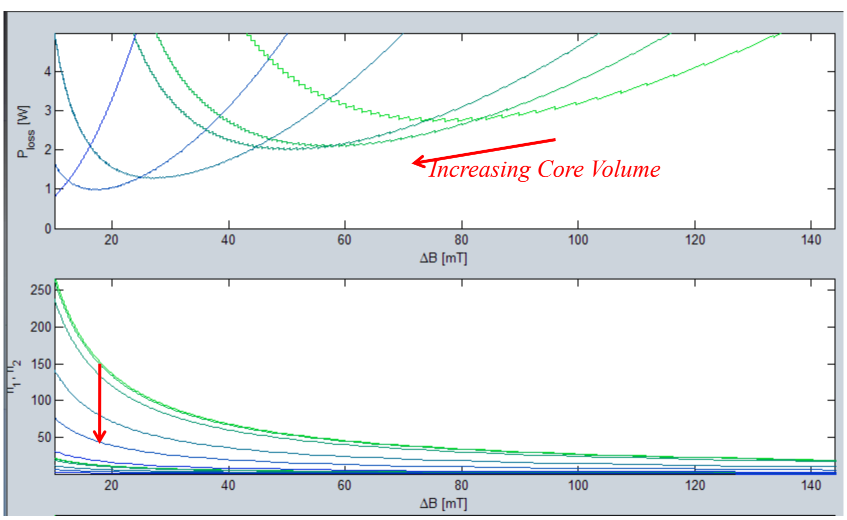


Matlab Example





Modified Core Loss Outputs



Spreadsheet Design

E5 — f_x =B6*B5/B4/B11*10^4

	A	B	C	D	E
1					
2	Design Params			Calculated Values	
3	Ku	0.5		Kg	3.34E-02
4	Bmax	0.25		lg	9.58E-04
5	Imax	5.5		n	34.64566929
6	L	2.00E-04		Aw	0.004098636
7	R	0.2		R	0.053774105
8	rho	1.72E-06			
9					
10	Core Geometry				
11	Ac	1.27E+00			
12	Wa	2.84E-01			
13	MLT	3.69E+00			
14					

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

K_g and K_{gfe} Methods

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

	K_g	K_{gfe}
Losses	DC Copper (specified)	DC Copper, SE Core Loss (optimized)
Saturation	Specified	Checked After
B_{max}	Specified	Optimized

K_g Method

- Method useful for filter inductors where ΔB is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired B_{max} is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website

The following quantities are specified, using the units

Wire resistivity	ρ	(Ω-cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Core maximum flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} 10^8 \quad (\text{cm}^5)$$

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad (\text{m})$$

$$n = \frac{L I_{max}}{B_{max} A_c} 10^4$$

$$A_W \leq \frac{K_u W_A}{n} \quad (\text{cm}^2)$$

$$R = \frac{\rho n\,(MLT)}{A_w} \quad (\Omega)$$

K_{gfe} Method

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized

K_{gfe} Procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω-cm)
Total rms winding current, ref to pri	I_{tot}	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	
Applied pri volt-sec	λ_1	(V-sec)
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm^{3}T$^\beta$)

Other quantities and their dimensions:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_e	(cm)
Wire areas	A_{w1}, …	(cm^2)
Peak ac flux density	ΔB	(T)

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4K_u (P_{tot})^{((\beta+2)/\beta)}} 10^8$$

$$\Delta B = \left[10^8 \frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \frac{(MLT)}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)}$$

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} 10^4 \qquad n_k = n_1 \frac{n_k}{n_1}$$

$$\alpha_k = \frac{n_k I_k}{n_1 I_{tot}} \qquad A_{wk} \leq \frac{\alpha_2 K_u W_A}{n_2}$$

Verify

K_{gfe} Method: Summary

- Method enforces an operating ΔB in which core and copper losses are minimized
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal
- Does not consider high frequency losses
- Step-by-step design procedure included on website