Experiment 3: Open Loop Boost

Power Converter Layout: Buck Example

Use loop analysis

Switched input current $i_1(t)$ contains large high frequency harmonics
- hence inductance of input loop is critical
  inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc
- hence additional inductance is not a significant problem in the second loop
Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

B fields nearly cancel

loop area $\Lambda_c$
Boost Converter RMS Currents

- MOSFET conduction losses due to \((r_{ds})_\text{on}\) depend given as

\[ P_{\text{cond,FET}} = I_{d,\text{rms}}^2 (r_{ds})_\text{on} \]

Driving a Power MOSFET Switch

- MOSFET is off when \(v_{gs} < V_{th} \approx 3\) V
- MOSFET fully on when \(v_{gs}\) is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when \(v_{gs} > 20\) V.
- Fast turn on or turn off (10’s of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability
Driving a Power MOSFET Switch

- MOSFET gate driver is used as a logic buffer with high output current (~1.8 A) capability
- The amplitude of the gate voltage equals the supply voltage VCC
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow dv/dt at switch node

Gate Driver Example

- Diagram showing line input, +15 volt supply, analog control chip, PWM control chip, gate driver, and power MOSFET with current waveform.
### Solution: bypass capacitor and close coupling of gate and return leads

High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large.

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### Half Bridge Gate Drive Waveforms

- Gate driver chip must implement $v_{gs}$ waveforms
- Sources will have pulsating currents and need decoupling
MOSFET Gate Charge

- Charge is supplied to both $C_{gs}$ and $C_{gd}$ in order to move gate voltage and switch MOSFET
- Would like to supply the charge in minimum time to quickly switch FET
- Results in high peak currents

Gate Drive Implementation

- Gate driver is cascades back half-bridges of decreasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections
Capacitor Sizing Notes

- Area of current pulse is total charge supplied to gate of capacitor
- All charge must be supplied from gate drive decoupling capacitor

\[ \frac{q_{gate}}{\Delta V_{DD}} = C \]

Gate Drive Losses

- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

\[ E_{loss} = q_{gate}V_{DD} \]
\[ P_{sw,g} = E_{loss}f_s \]
High Side Signal Ground

- Gate driver chip must implement $v_{gs}$ waveforms
- Issue: source of $Q_2$ is not grounded

Generating Floating Supply

- Isolated supplies sometimes used; Isolated DC-DC, batteries
- Bootstrap concept: capacitor can be charged when $V_s$ is low, then switched
### LM5104 Gate Driver

#### 8.2 Typical Application

![Diagram showing the typical application of LM5104 Gate Driver](image)

Figure 15. LM5104 Driving MOSFETs Connected in Synchronous Buck Configuration
Bootstrap Diode Loss

- Conduction losses due to pulsating currents are relatively small
- Switching losses are significant
- Diode capacitance and reverse recovery play a role

Figure 5. Diode Power Dissipation $V_{in} = 80V$