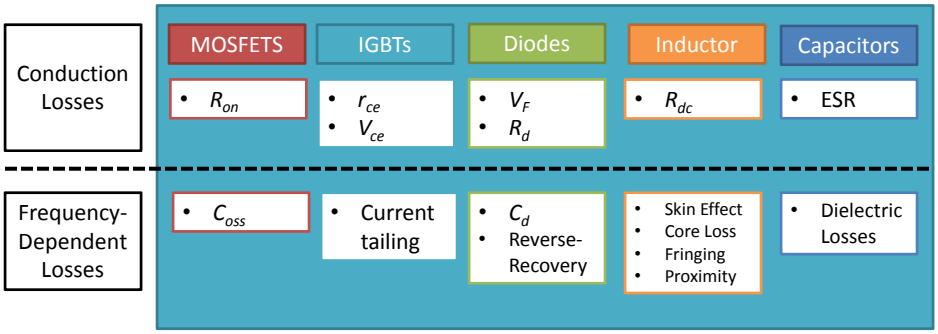
Power Stage Losses



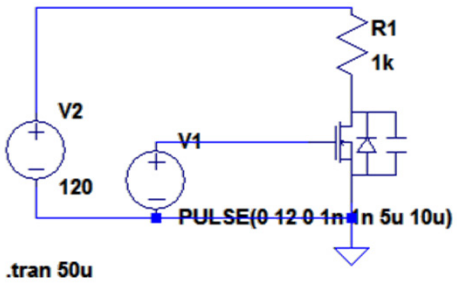
Simulation Modeling

4

Circuit Simulation

- Matlab, Simulink, LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)

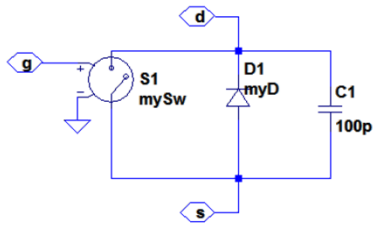
LTSpice Modeling Examples



- Example files added to course materials page

Custom Transistor Model

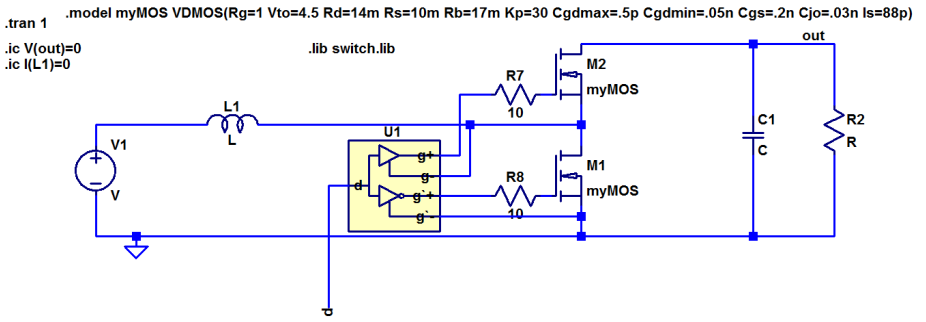
```
.model myD D(Ron=1m Roff=1G Vfwd=0.5)
.model mySw SW(Ron=10m Roff=1G Vt=0 Von=1 Voff = .5 )
```



Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately

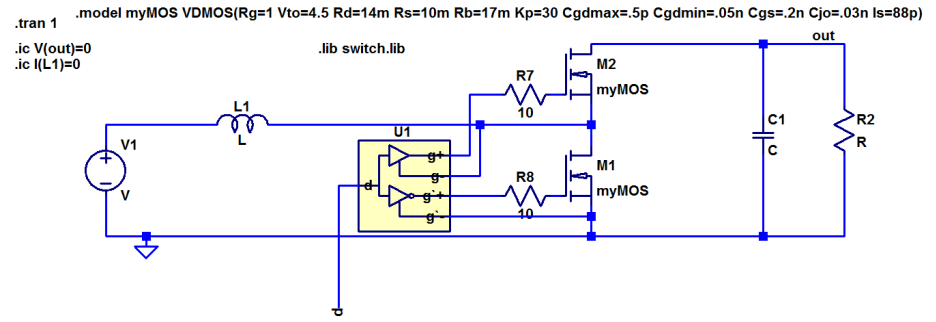
VDMOS SPICE Model



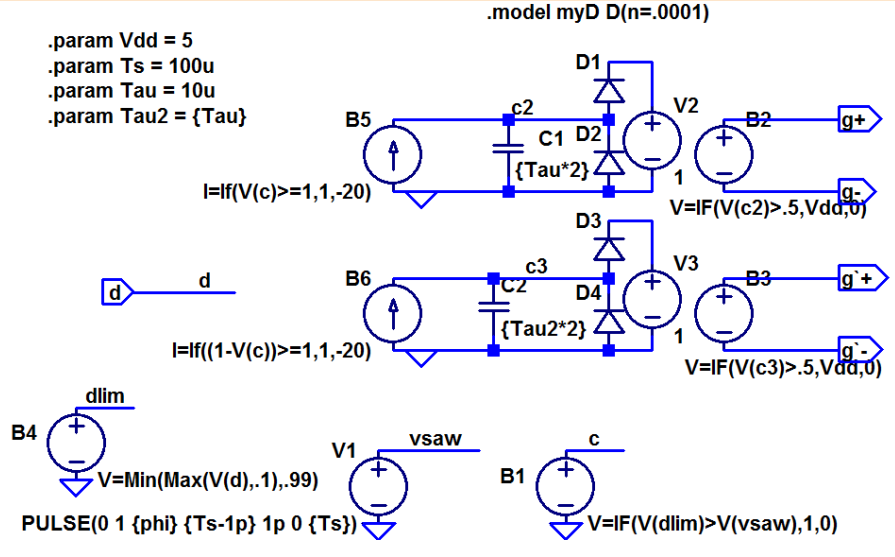
http://ltwiki.org/index.php?title=MOSFET_Model

Name	Description	Units	Default	Example
Vto	Threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V²	1.	.5
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation	1/V	0.	0.02
mtriode	Conductance multiplier in triode region(allows independent fit of triode and saturation regions	-	1.	2.
subtreas	Current(per volt Vds) to switch from square law to exponential subthreshold conduction	A/V	0.	1n
BV	Vds breakdown voltage	V	Infin.	40
IBV	Current at Vds=BV	A	100pA	1u
NBV	Vds breakdown emission coefficient	-	1.	10
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Rg	Gate ohmic resistance	Ω	0.	2.
Rds	Drain-source shunt resistance	Ω	Infin.	10Meg
Rb	Body diode ohmicresistance	Ω	0.	.5
Cjo	Zero-bias body diode junction capacitance	F	0.	1n
Cgs	Gate-source capacitance	F	0.	500p
Cgdmin	Minimum non-linear G-D capacitance	F	0.	300p
Cgdmax	Maximum non-linear G-D capacitance	F	0.	1000p
A	Non-linear Cgd capacitance parameter	-	1.	.5
Is	Body diode saturation current	A	1e-14	1e-15
N	Bulk diode emission coefficient	-	1.	
Vj	Body diode junction potential	V	1.	0.87
M	Body diode grading coefficient	-	0.5	0.5
Fc	Body diode coefficient for forward-bias depletion capacitance formula	-	0.5	
tt	Body diode transit time	sec	0.	10n
Eg	Body diode activation energy for temperature effect on Is	eV	1.11	
Xti	Body diode saturation current temperature exponent	-	3.	
L	Length scaling	-	1.	
W	Width scaling	-	1.	
Kf	Flicker noise coefficient	-	0.	
Af	Flicker noise exponent	-	1.	
nchan[*]	N-channel VDMOS	-	(true)	-
pchan[*]	P-channel VDMOS	-	(false)	-
Tnom	Parameter measurement temperature	°C	27	50

Full Switching Simulation

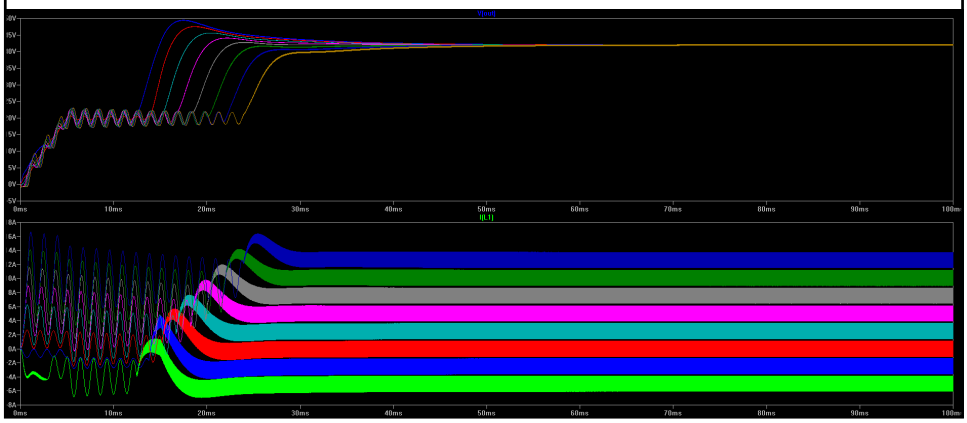


Functional Gate Driver Model



Switching Model Simulation Results

- Simulation Time ≈ 15 minutes



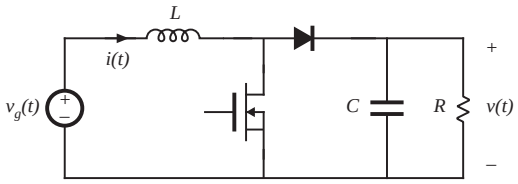
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

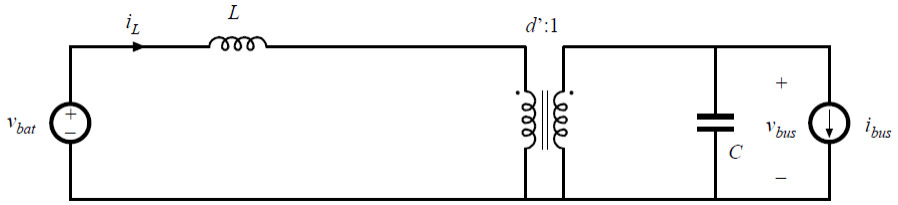
Averaged Switch Modeling: Motivation

- A *large-signal, nonlinear* model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an *averaged* model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

Nonlinear, Large-Signal Equations



Nonlinear, Averaged Circuit



$$L\frac{d\langle i_L\rangle}{dt} = \langle v_{bat}\rangle - (1-d)\langle v_{bus}\rangle$$

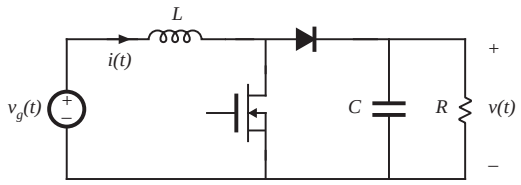
$$C\frac{d\langle v_{bus}\rangle}{dt} = (1-d)\langle i_L\rangle - \langle i_{bus}\rangle$$

Circuit Averaging and Averaged Switch Modeling

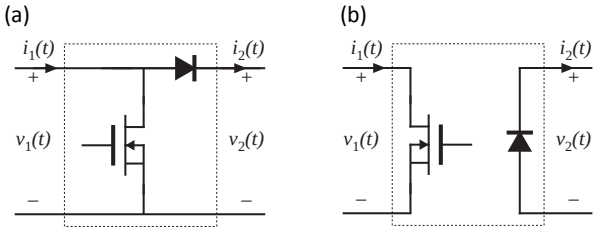
- Historically, circuit averaging was the first method known for modeling the small-signal ac behavior of CCM PWM converters
- It was originally thought to be difficult to apply in some cases
- There has been renewed interest in circuit averaging and its corrolary, averaged switch modeling, in the last two decades
- Can be applied to a wide variety of converters
  - We will use it to model DCM, CPM, and resonant converters
  - Also useful for incorporating switching loss into ac model of CCM converters
  - Applicable to 3ø PWM inverters and rectifiers
  - Can be applied to phase-controlled rectifiers
- Rather than averaging and linearizing the converter state equations, the averaging and linearization operations are performed directly on the converter circuit

Boost converter example

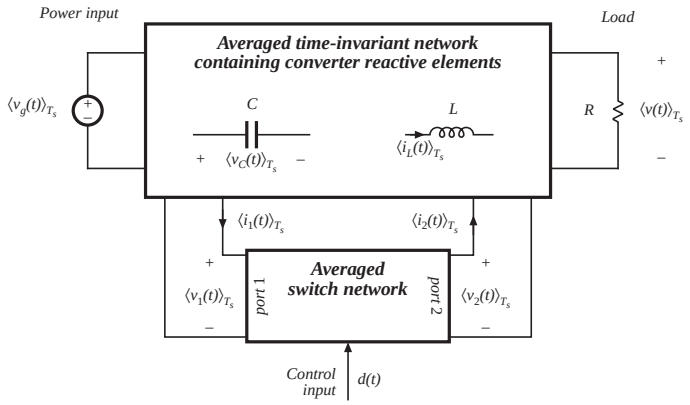
Ideal boost converter example



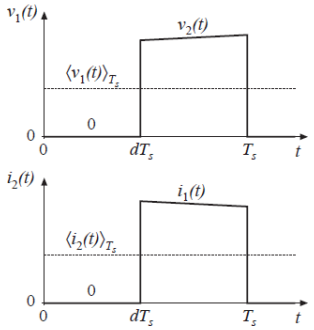
Two ways to define the switch network



Circuit Averaging



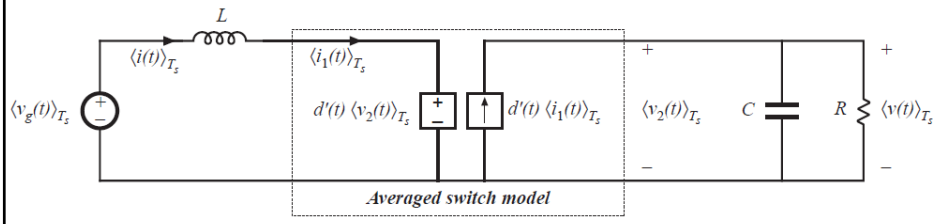
Compute average values of dependent sources



Average the waveforms of the dependent sources:

$$\left\langle v_1(t)\right\rangle_{T_s} = d'(t)\left\langle v_2(t)\right\rangle_{T_s}$$

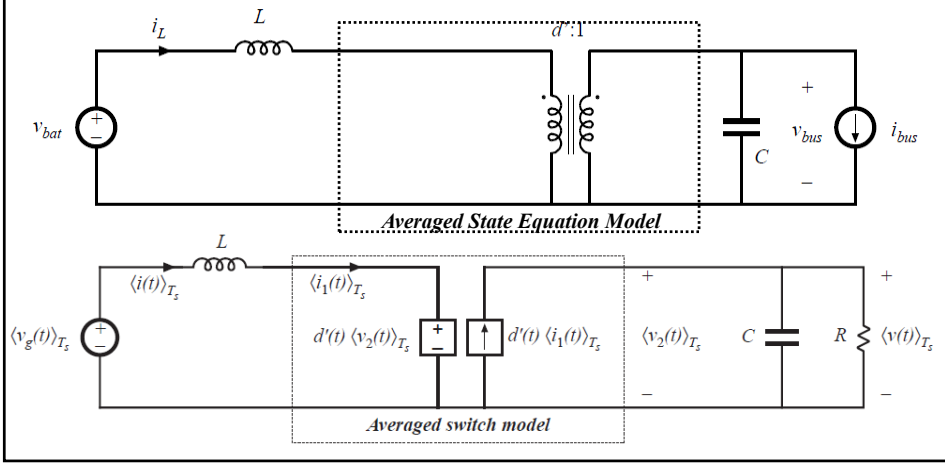
$$\left\langle i_2(t)\right\rangle_{T_s} = d'(t)\left\langle i_1(t)\right\rangle_{T_s}$$



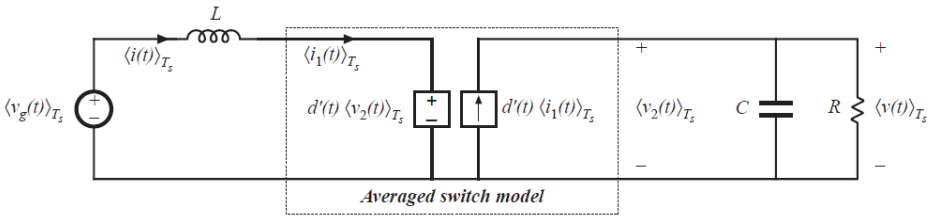
Summary: Circuit averaging method

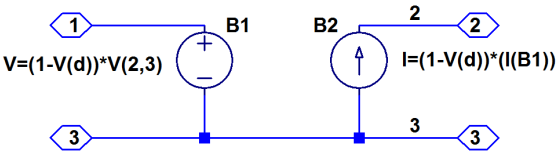
Model the switch network with equivalent voltage and current sources, such that an equivalent time-invariant network is obtained

Average converter waveforms over one switching period, to remove the switching harmonics

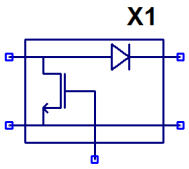


Implementation in LTSpice

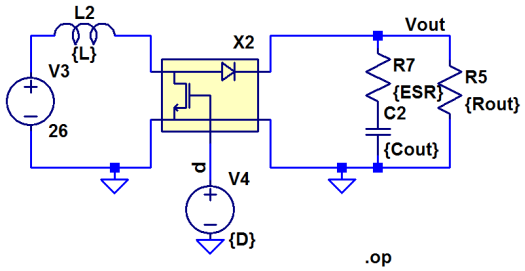




$$\left\langle v_1(t)\right\rangle_{T_s} = d'(t)\left\langle v_2(t)\right\rangle_{T_s}$$
$$\left\langle i_2(t)\right\rangle_{T_s} = d'(t)\left\langle i_1(t)\right\rangle_{T_s}$$

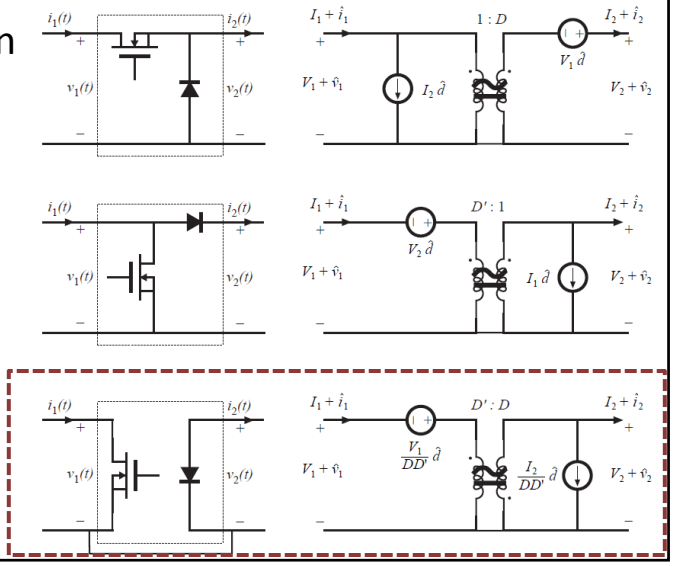


Averaged Switch Model



Three Basic Switch Cells

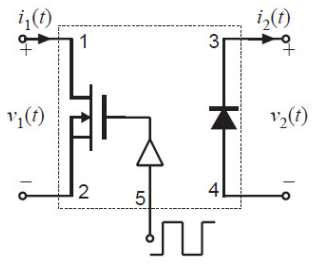
- Can perturb an linearize as normal for linear SSM
- Most general switch cell is included in library file, switch.lib



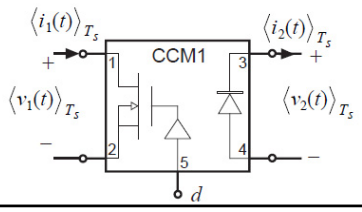
Switch.lib CCM1 Model

Generalized Equations: $\langle v_1(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle v_2(t) \rangle_{T_s}$ $\langle i_2(t) \rangle_{T_s} = \frac{d'(t)}{d(t)} \langle i_1(t) \rangle_{T_s}$

(a)



(b)



(c)

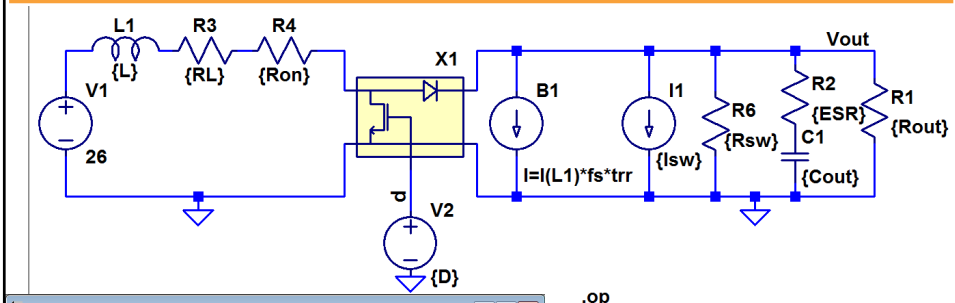
```
**********************************************************
* Subcircuit: CCM1
* Application: two-switch PWM converters
* Limitations: ideal switches, CCM only, no transformer
**********************************************************
* Parameters: none
**********************************************************
* Nodes:
* 1: transistor positive (drain for an n-channel MOS)
* 2: transistor negative  (source for an n-channel MOS)
* 3: diode cathode
* 4: diode anode
* 5: duty cycle control input
**********************************************************
.subckt CCM1 1  2  3  4  5
Et 1 2 value={(1-v(5))*v(3,4)/v(5)}
Gd 4 3 value={(1-v(5))*i(Et)/v(5)}
.ends
**********************************************************
```

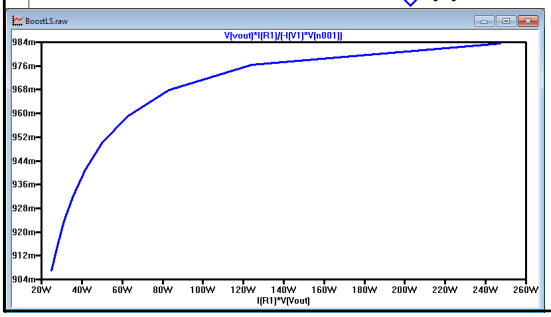
Fig. B.1 Averaged switch model CCM1: (a) the general two-switch network: (b) symbol for the averaged switch subcircuit model; (c) PSpice netlist of the subcircuit.

Averaged Switch Modeling: Further Comments

- Model is slightly different but can be produced in same manner for
  - Inclusion of loss models
  - Transformer isolated converters
  - Converters in DCM
- See book appendix B.2 for further notes

Averaged Model With Losses






```
.op
.param Rout = 10
.step param Rout 10 100 10
```

What known error will be present in loss predictions with this model?

Cross-Conduction