PCB Layout

ECE 482 Lecture 7
March 10, 2015

Announcements

• Prelab 5 due Thursday
  − Decide on System Improvements

• Experiment 4 report moved to Thurs. 3/26

• Midterm after spring break
  − Open note, book, instructor

• Today: Experiment 5
  − No report; deliverables are layout files
Lab 5: PCB Layout

Trapezoidal Comm. Implementation

Fig. 6 Trapezoidal (six-step) commutation with Hall sensors
Basic PCB Layout Concepts

- Trace Parasitics
- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances
- Ground Plane / Return Currents
- Partitioning

Kester, W. “Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects”
Trace Sizing Rough Guidelines

2.2 PCB Etch
Table 1 is helpful to determine the current carrying capacity of PCB etches. The table assumes:
- 1oz/sq foot copper (0.035mm thickness).
- 10°C rise on outer layers, 20°C inner layers
- Groups of high current tracks are de-rated
- Tracks are not near or over heat sink areas

<table>
<thead>
<tr>
<th>WIDTH</th>
<th>CURRENT CAPACITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.010&quot;</td>
<td>0.8 A</td>
</tr>
<tr>
<td>0.015&quot;</td>
<td>1.2 A</td>
</tr>
<tr>
<td>0.020&quot;</td>
<td>1.5 A</td>
</tr>
<tr>
<td>0.050&quot;</td>
<td>3.2 A</td>
</tr>
<tr>
<td>0.100&quot;</td>
<td>6.0 A</td>
</tr>
</tbody>
</table>

2.3 Vias or Feedthrus
Vias limit the current and add inductance between the power supply and load. Layouts are usually done with 10-mil inner ring feedthrus. At this size, current capability is about 1 A per feedthru.

Kester, W. “Tips about printed circuit board design: Part 1 – Dealing with harmful PCB effects”

Kelvin Connection

Texas Instruments, “LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers”
Persson E., “What really limits MOSFET performance: silicon, package, driver or circuit board?”
High Impedance Nodes and Capacitive Coupling

Analog Devices, "Decoupling Techniques," MT-101

Capacitive Shielding

Analog Devices, "Decoupling Techniques," MT-101
Supply Decoupling

High frequency components of gate drive current are confined to a small loop.

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large.

Pulsed Circuit Decoupling

VERTICAL SCALE: 100mV/div
HORIZONTAL SCALE: 10ns/div

Figure 12.68: Effects of Inadequate Decoupling on the Phase Response of the AD9631 Op Amp
Decoupling Capacitance

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt
Loop Inductances

Bad practice: wide separation of signal and return

Good practice: close coupling of signal and return

Loop Inductance: Experiment

Figure 12.60: Schematic and Layout of Current Source with U-shaped Trace on PC Board and Return through Ground Plane.
Loop Inductance: Experiment

- Current Return at DC
- Current Return at High Frequency AC

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

Addition of bypass capacitor confines the pulsating current to a smaller loop:

High frequency currents are shunted through capacitor instead of input source
Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize
Buck Example Bridge Layout

Figure 2. Typical Placement and PCB Layout of the Power Stage Components

Example Bridge Layout #2

Figure 1. Optimized Placement and PCB Layout of Power Stage Components
Example Layout Experimental Results

Example Layout #1

Example Layout #2

Star-Grounding Vs. Daisy Chain

Undesired

Desired

Figure 9. Separate the Input Current Paths Among Supplies
Another View

Adding a Ground Plane

Kester, W. “Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects”
Ground Plane

- Benefits:
  - Common reference voltage
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)

- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable
Cuts in Ground Plane

- Goals:
  - minimize inductance/loops
  - Minimize ground interference
- Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)
Effective Ground Plane Cuts

Experiment 5: Starting Files