PCB Layout

ECE 482 Lecture 7
March 10, 2015

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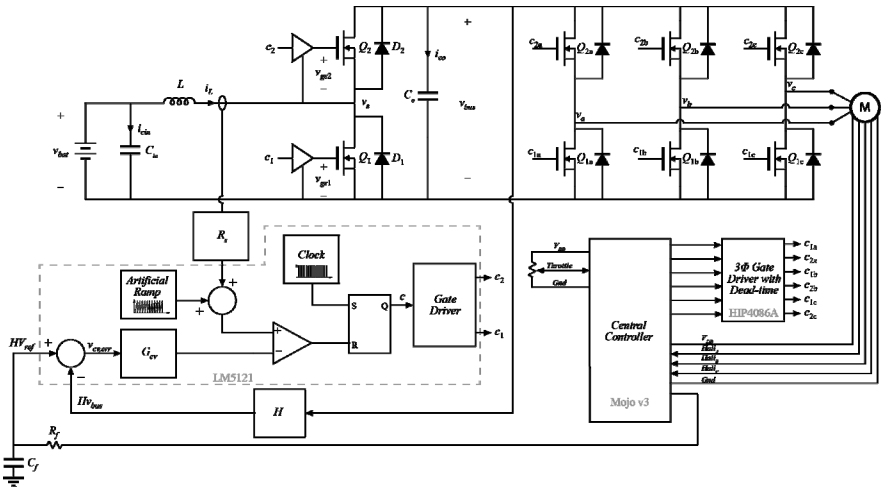
Announcements

- Prelab 5 due Thursday
  - Decide on System Improvements
- Experiment 4 report moved to Thurs. 3/26
- Midterm after spring break
  - Open note, book, instructor
- Today: Experiment 5
  - No report; deliverables are layout files

Lab 5: PCB Layout



Trapezoidal Comm. Implementation

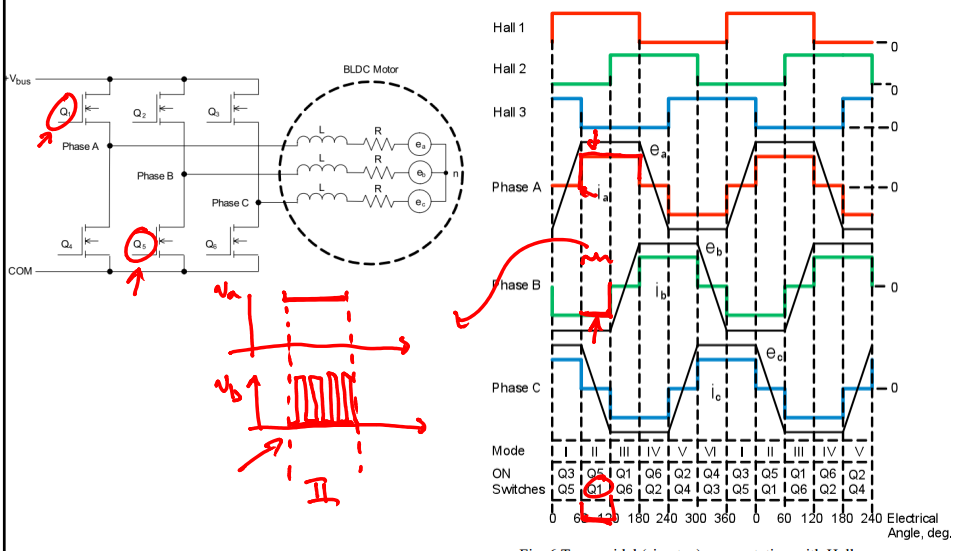
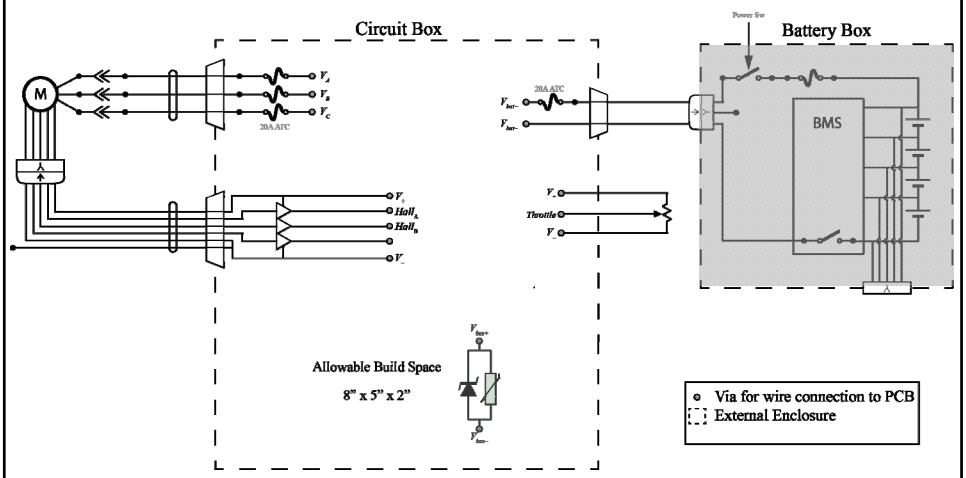


Fig. 6 Trapezoidal (six-step) commutation with Hall sensors

Circuit Connections



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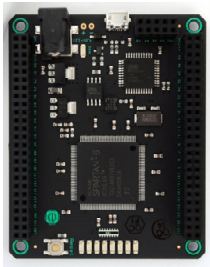

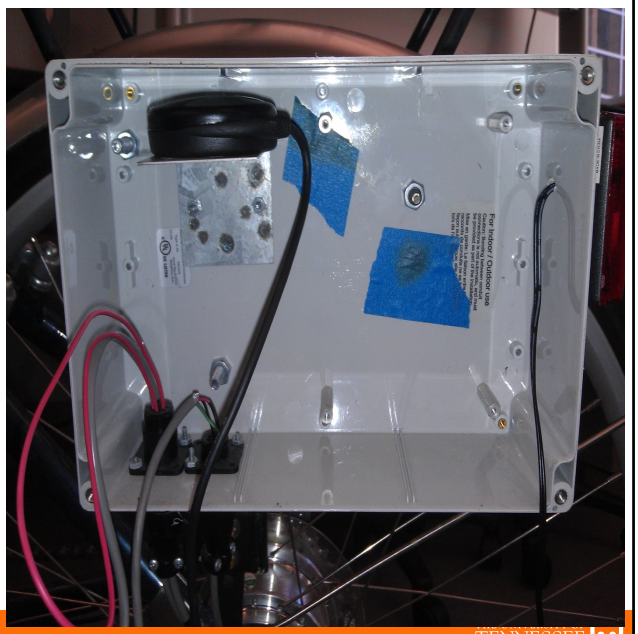

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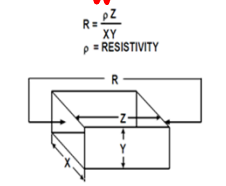
Basic PCB Layout Concepts

- Trace Parasitics
- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances
- Ground Plane / Return Currents
- Partitioning

Trace Parasitics



SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:

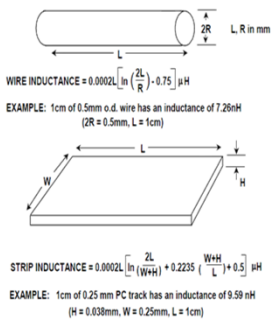
ρ = 1.724 X 10-6 Ωcm, Y = 0.0036cm

R = 0.48 Z/X mΩ

Z/X = NUMBER OF SQUARES

R = SHEET RESISTANCE OF 1 SQUARE (Z=X) = 0.48mΩ/SQUARE

Figure 12.2: Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors



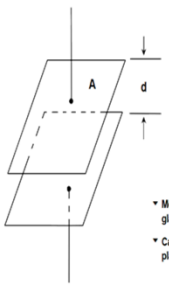
WIRE INDUCTANCE = 0.0002L [ln (2L/R) - 0.75] μH

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH (2R = 0.5mm, L = 1cm)

STRIP INDUCTANCE = 0.0002L [ln 2L/(W+H) + 0.2235 (W+H)/L + 0.5] μH

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH (H = 0.038mm, W = 0.25mm, L = 1cm)

Figure 12.18: Wire and Strip Inductance Calculations



C = 0.00885 E_r A/d pF

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

- Most common PCB type uses 1.5mm glass-fiber epoxy material with E_r = 4.7
- Capacitance of PC track over ground plane is roughly 2.8 pF/cm^2

Figure 12.24: Capacitance of two parallel plates

wide traces
high current carrying

short traces small loops
high di/dt loops

small parallel area
high dv/dt
high-Z nodes

Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

Trace Sizing Rough Guidelines

2.2 PCB Etch

Table 1 is helpful to determine the current carrying capacity of PCB etches. The table assumes:

- 1oz/sq foot copper (0.035mm thickness).
- 10°C rise on outer layers, 20°C inner layers
- Groups of high current tracks are de-rated
- Tracks are not near or over heat sink areas

Table 1. Current Capacity PCB Etch

WIDTH	CURRENT CAPACITY
0.010"	0.8 A
0.015"	1.2 A
0.020"	1.5 A
0.050"	3.2 A
0.100"	6.0 A

2.3 Vias or Feedthrus

Vias limit the current and add inductance between the power supply and load. Layouts are usually done with 10-mil inner ring feedthrus. At this size, current capability is about 1 A per feedthru.

Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

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Kelvin Connection

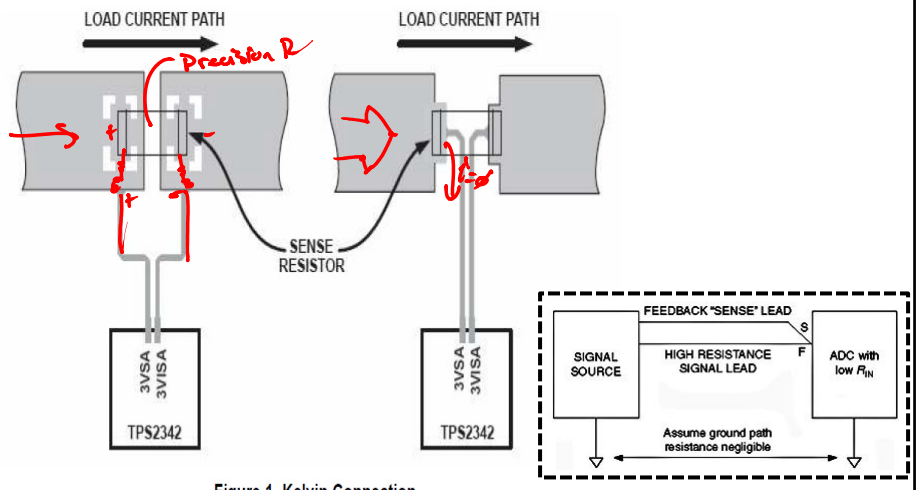

Figure 1. Kelvin Connection

Texas Instruments, "LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers"

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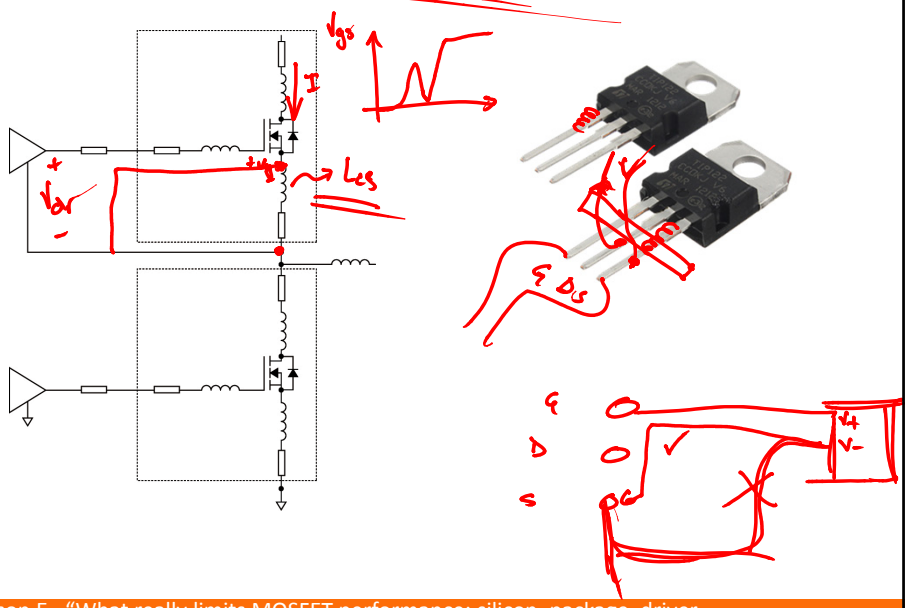
Common Source Inductance



Persson E., "What really limits MOSFET performance: silicon, package, driver or circuit board?"

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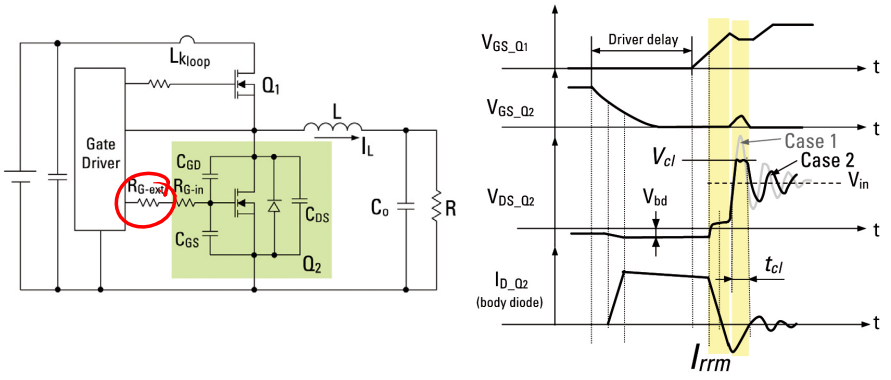
Gate-Drain Capacitance



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High Impedance Nodes and Capacitive Coupling

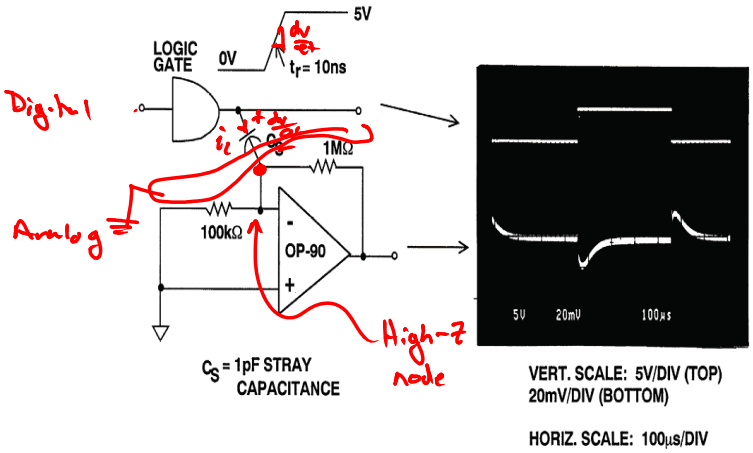


Figure 12.29 *High Circuit Impedances Increase Susceptibility to Noise Pickup*

Capacitive Shielding

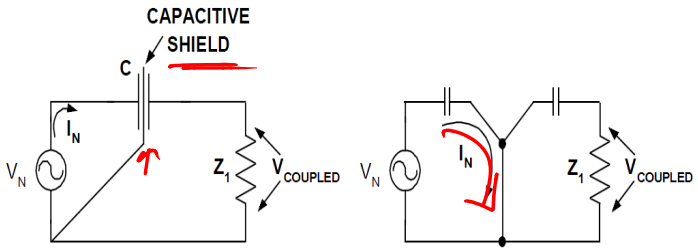
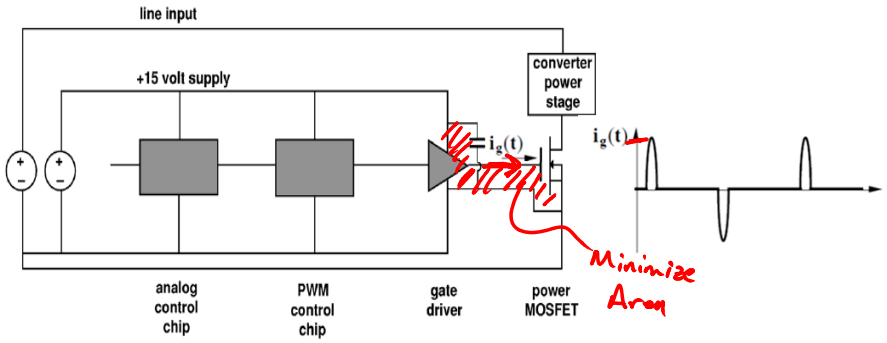


Figure 12.26: *An Operational Model of a Faraday Shield*

Supply Decoupling



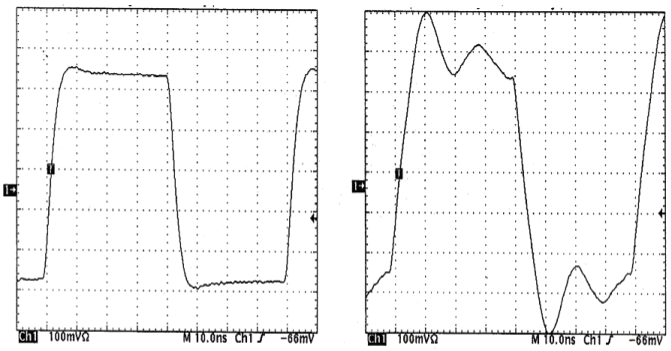
High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

Pulsed Circuit Decoupling

PROPER DECOUPLING

NO DECOUPLING



VERTICAL SCALE: 100mV/div
HORIZONTAL SCALE: 10ns/div

Figure 12.68: *Effects of Inadequate Decoupling on the Phase Response of the AD9631 Op Amp*

Analog Devices, "Decoupling Techniques," MT-101

Decoupling Capacitance

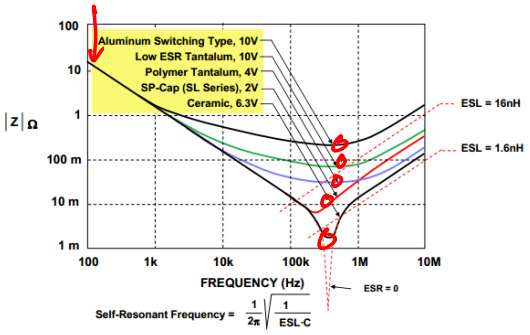


Figure 4: Impedance of Various 100µF Capacitors

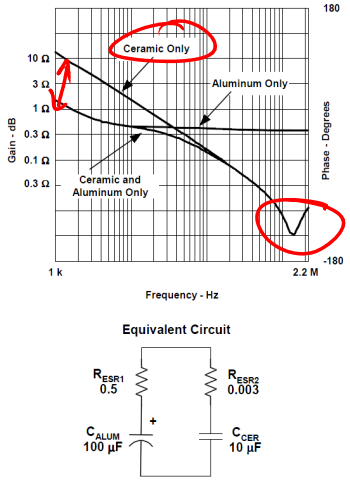


Fig. 8. Paralleled capacitors minimize impedance over frequency.

Analog Devices, "Decoupling Techniques," MT-101

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Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

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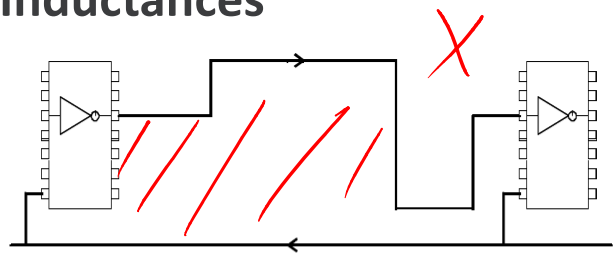
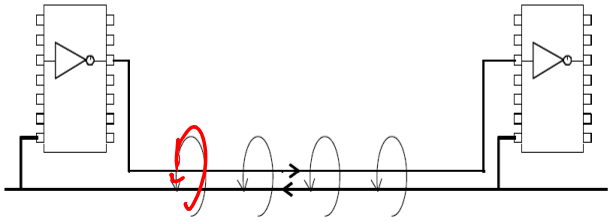
Loop Inductances



Bad practice: wide separation of signal and return



Good practice: close coupling of signal and return

Loop Inductance: Experiment

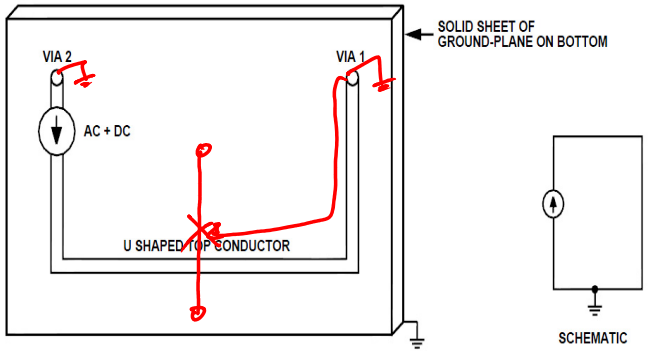
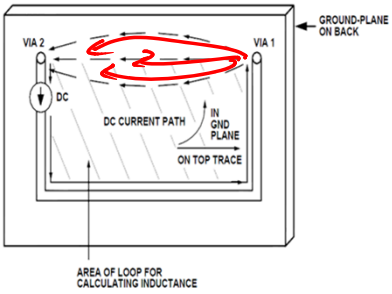
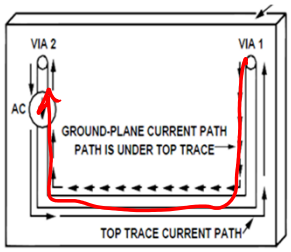


Figure 12.60: *Schematic and Layout of Current Source with U-shaped Trace on PC Board and Return through Ground Plane.*

Loop Inductance: Experiment



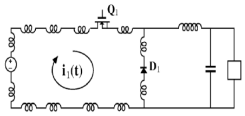
Current Return at DC



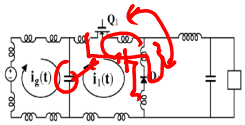
Current Return at High Frequency AC

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

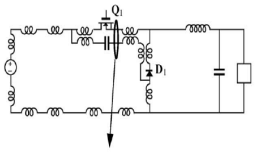


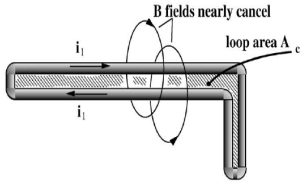
Addition of bypass capacitor confines the pulsating current to a smaller loop:



high frequency currents are shunted through capacitor instead of input source

Even better: minimize area of the high frequency loop, thereby minimizing its inductance





Gate Drive Signal Routing

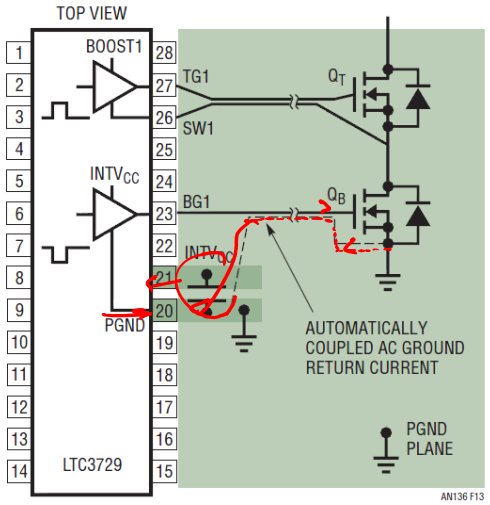


Figure 13. Gate Driver Trace Routing of the MOSFETs

Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize

Buck Example Bridge Layout

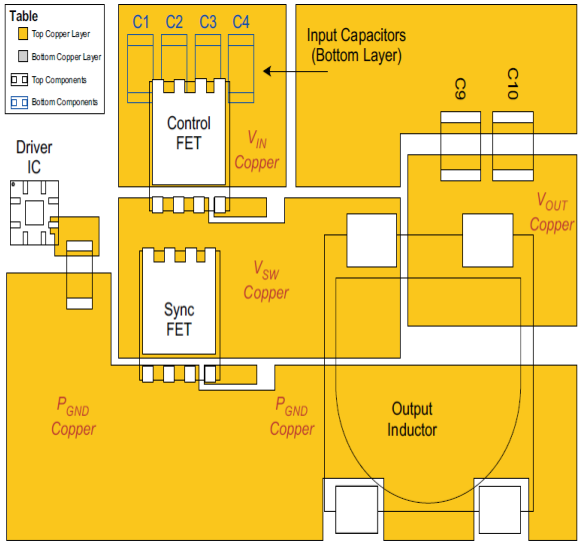


Figure 2. Typical Placement and PCB Layout of the Power Stage Components

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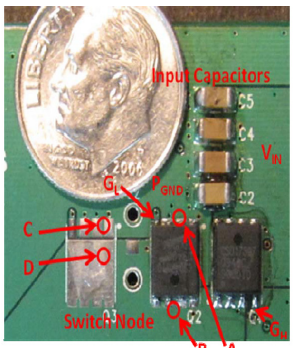
Example Bridge Layout #2



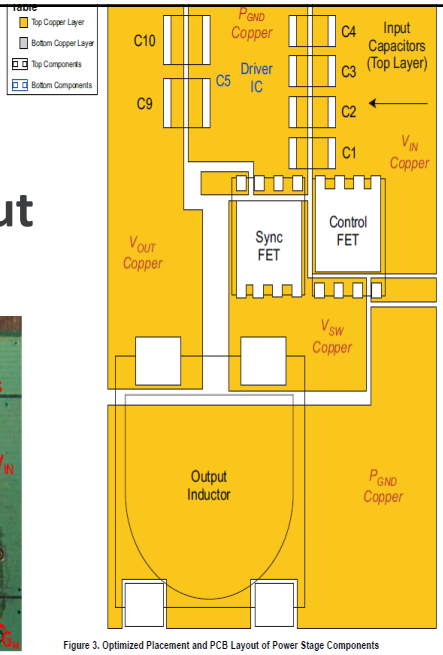


Figure 3. Optimized Placement and PCB Layout of Power Stage Components

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Example Layout Experimental Results

Example Layout #1

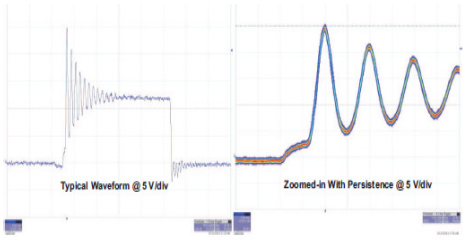


Figure 4. Switch Node (VSW) Voltage Ringing on Typical Layout

Example Layout #2

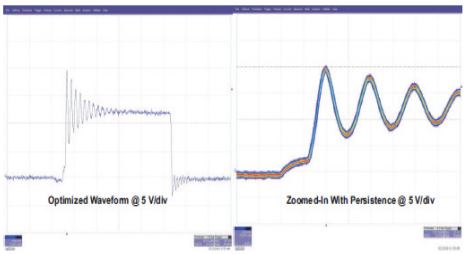


Figure 5. Switch Node (VSW) Voltage Ringing on Optimized Layout

Star-Grounding Vs. Daisy Chain

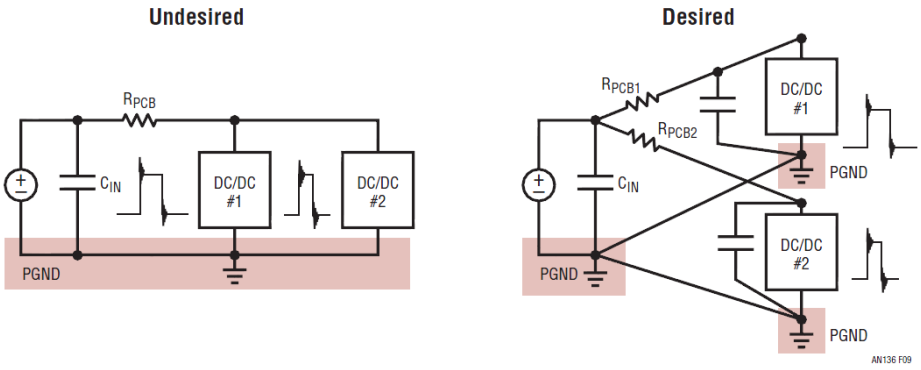
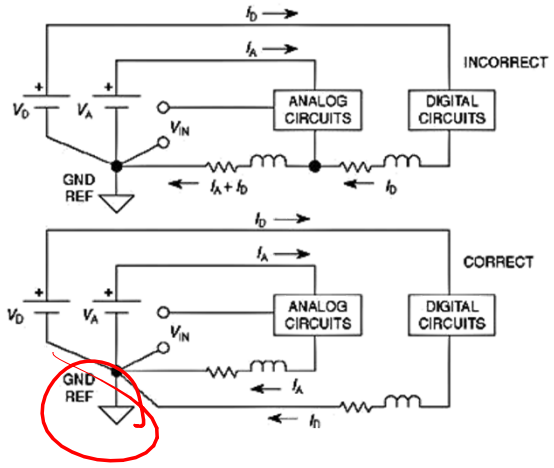


Figure 9. Separate the Input Current Paths Among Supplies

Another View



Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

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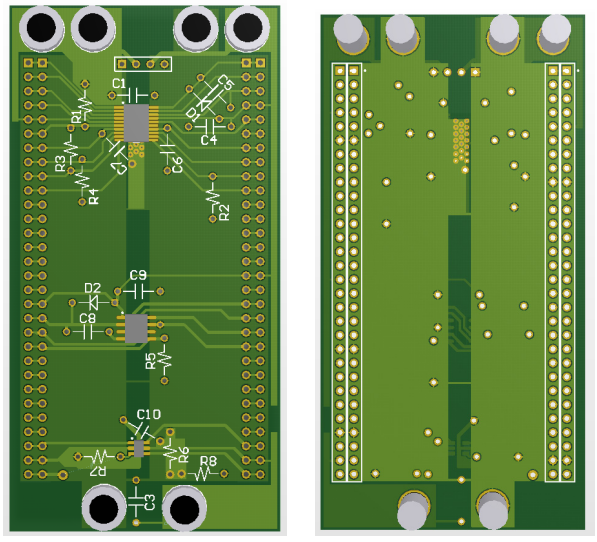
Adding a Ground Plane



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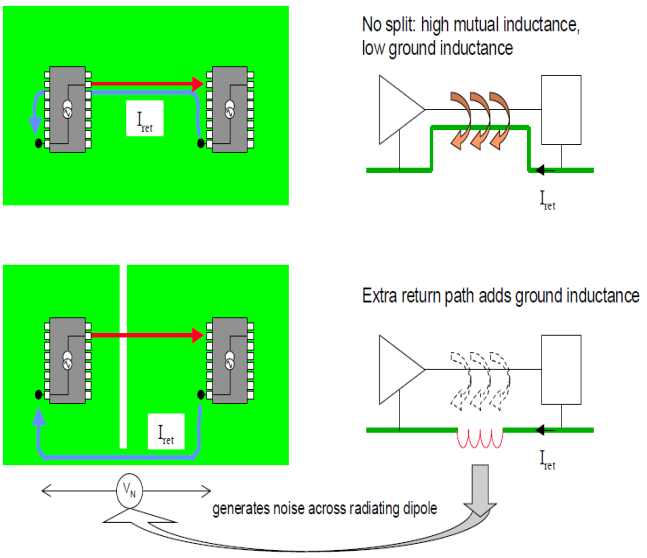
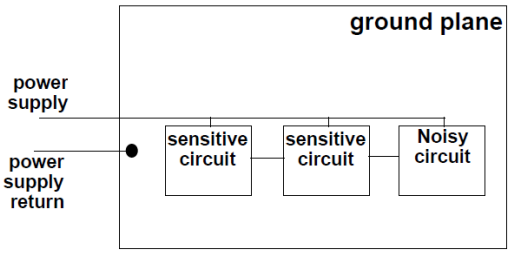
Ground Plane

- Benefits:
  - Common reference voltage
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable

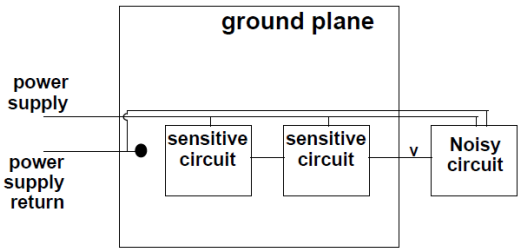
Ground Currents



A Poor Ground Plane Layout



Return current of noisy circuit runs underneath sensitive circuits, and can still corrupt their ground references



A solution is to remove the noisy circuit from the ground plane. One could then run a separate ground wire for the noisy circuit. The only drawback is that noise can be coupled into the input signal v.

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Cuts in Ground Plane

- Goals:
  - minimize inductance/loops
  - Minimize ground interference
- Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

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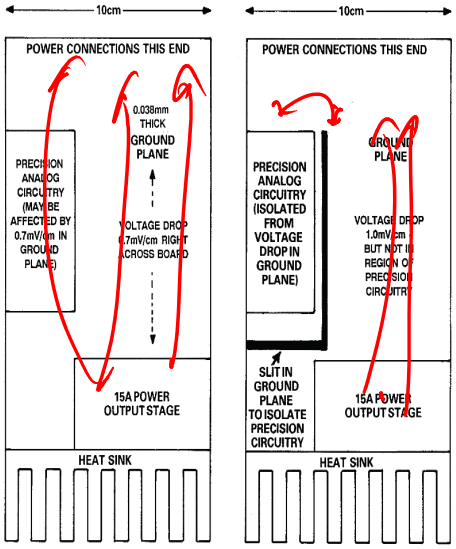
Effective Ground Plane Cuts



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Experiment 5: Starting Files

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