Power Electronics Circuits

Prof. Daniel Costinett

ECE 482 Lecture 4
February 15, 2016

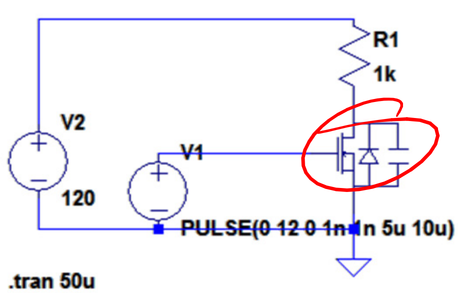
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Simulation Modeling

Circuit Simulation

- LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)

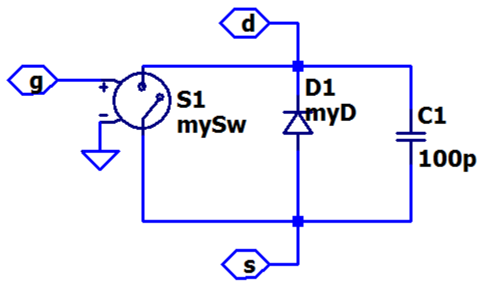
LTSpice Modeling Examples



- Example files added to course materials page

Custom Transistor Model

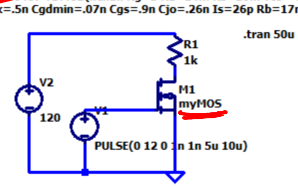
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Vt=0 Von=1 Voff = .5)



VDMOS Model

Name	Description	Units	Default	Example
Vto	Threshold voltage	V	0	1.0
Kp	Transconductance parameter	A/V^2	1.	.5
Phi	Surface inversion potential	V	0.6	0.65
Lambda	Channel-length modulation	1/V	0.	0.02
mtriode	Conductance multiplier in triode region(allows independent fit of triode and saturation regions	-	1.	2.
subthres	Current(per volt Vds) to switch from square law to exponential subthreshold conduction	A/V	0.	1n
BV	Vds breakdown voltage	V	Infin.	40
IBV	Current at Vds=BV	A	100pA	1u
NBV	Vds breakdown emission coefficient	-	1.	10
Rd	Drain ohmic resistance	Ω	0.	1.
Rs	Source ohmic resistance	Ω	0.	1.
Rg	Gate ohmic resistance	Ω	0.	2.
Rds	Drain-source shunt resistance	Ω	Infin.	10Meg
Rb	Body diode ohmic resistance	Ω	0.	.5
Cjo	Zero-bias body diode	F	0.	1n

myMOS
.model ~~AO6407~~ VDMOS(nchan Rg=3 Rd=14m Rs=10m Vto=-.8 Kp=32 Cgdmax=.5n Cgdmin=.07n Cgs=.9n Cjo=.26n Is=26p Rb=17m)

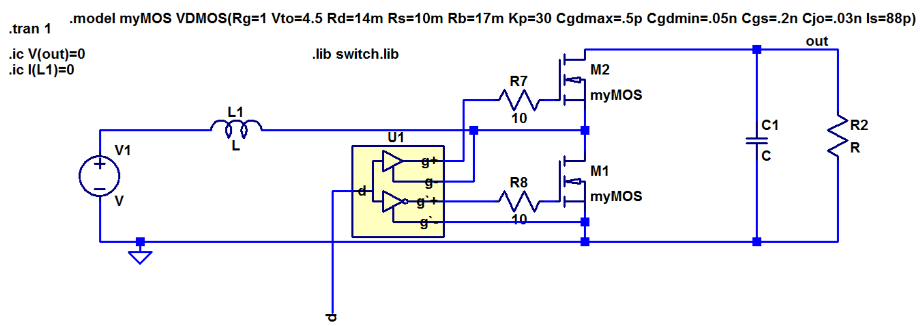


http://ltwiki.org/LTspiceHelp/LTspiceHelp/M_MOSFET.htm

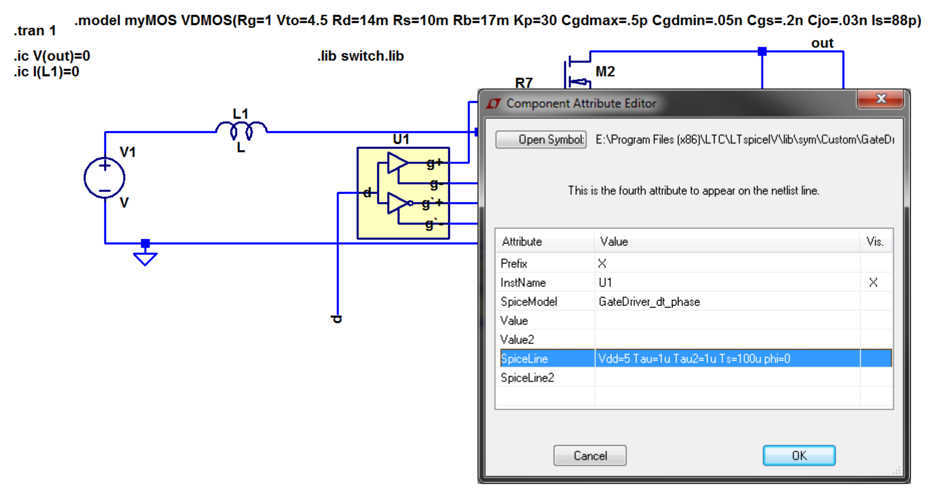
Manufacturer Device Model

- Text-only netlist model of device including additional parasitics and temperature effects
- May slow or stop simulation if timestep and accuracy are not adjusted appropriately

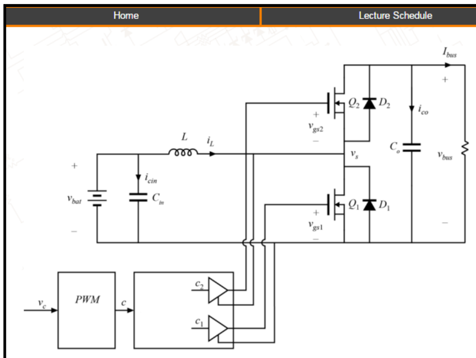
Full Switching Simulation



Full Switching Simulation



Home | Lecture Schedule | Materials



Available on Exp 3 Webpage

Experiment Procedure

- Prelab Assignment
- Experiment 3 Procedure

Experiment 3 Components

- Contents of the Experiment 3 Parts Kit
- Contents of the Magnetics Library
- Breakout Board Schematics and Layout

Reference Materials

- Power Converter Layout
- Reduction of Ringing in Power Converters (TI App. Note)
- RMS Values of Commonly Observed Waveforms

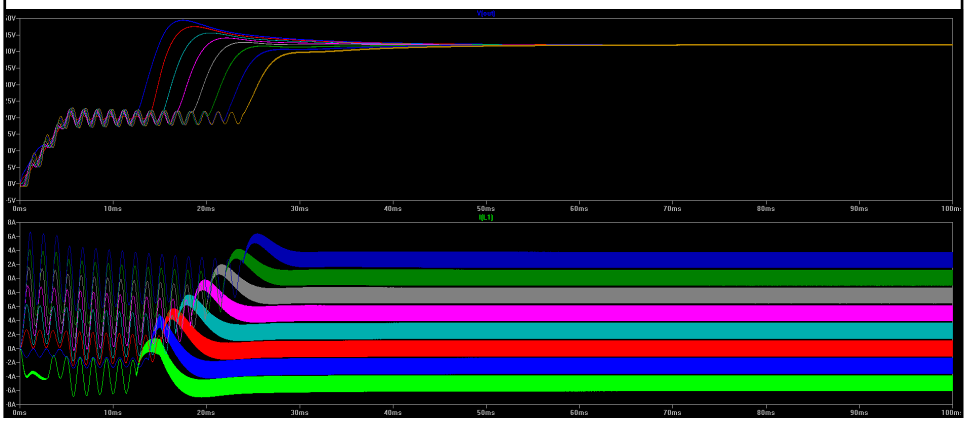
LTSpice Example Files

- **Examples of power semiconductor modeling using custom or manufacturer models**
- **Example Switching and Averaged Boost LTSpice Models**
- Additional materials on averaged-circuit modeling in SPICE simulators
- Example averaged, nonlinear boost converter model (Spring 2014)

- **Magnetics Design**

Switching Model Simulation Results

- Simulation Time ≈ 15 minutes



Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

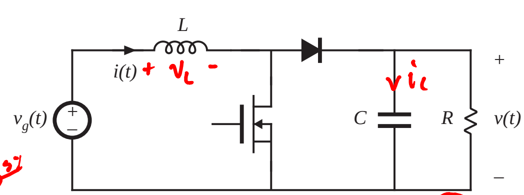
Averaged Switch Modeling: Motivation

- A *large-signal, nonlinear* model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an *averaged* model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Averaged, Nonlinear, Large-Signal Equations

ECE 481 Review:



Averaged eqs:

① $\langle v_L \rangle = \langle v_g \rangle - d'(t)\langle v \rangle$

↓ linearize

Avg. Linear AC + DC

DC: $\emptyset = V_g - D'V$

AC: $L\frac{d\hat{i}_L}{dt} = \hat{v}_g - D'\hat{v} + V\hat{d}$

② $\langle i_c \rangle = d'(t)\langle i_L \rangle - \frac{\langle v \rangle}{R}$

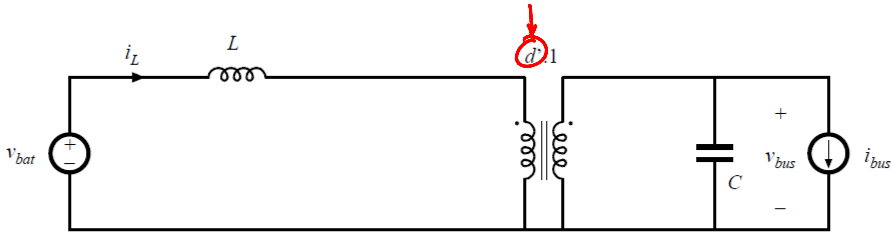
↓

DC: $\emptyset = D'I_L - \frac{V}{R}$

AC: $C\frac{d\hat{v}}{dt} = D'\hat{i}_L - I_L\hat{d} - \frac{\hat{v}}{R}$

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Nonlinear, Averaged Circuit



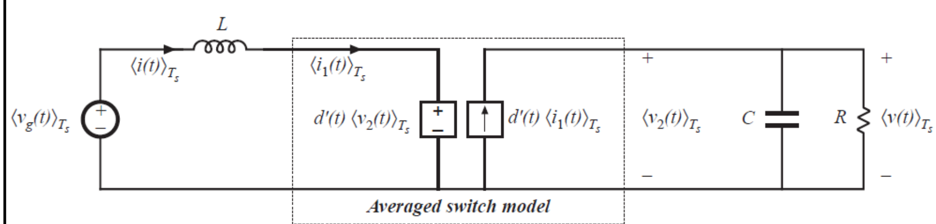
nonlinear

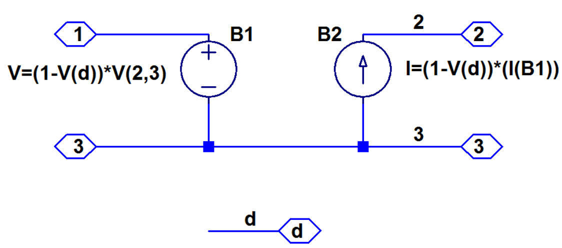
$$L\frac{d\langle i_L\rangle}{dt} = \langle v_{bat}\rangle - (1-d)\langle v_{bus}\rangle$$

$$C\frac{d\langle v_{bus}\rangle}{dt} = (1-d)\langle i_L\rangle - \langle i_{bus}\rangle$$

THE UNIVERSITY OF TENNESSEE KNOXVILLE

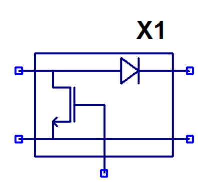
Implementation in LTSpice





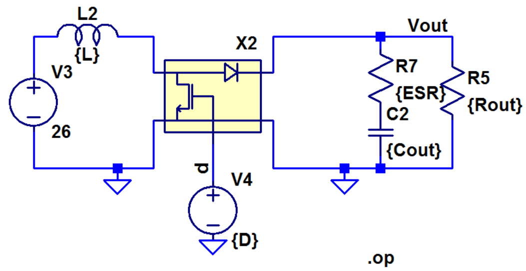
$$\langle v_1(t)\rangle_{T_s} = d'(t)\ \langle v_2(t)\rangle_{T_s}$$

$$\langle i_2(t)\rangle_{T_s} = d'(t)\ \langle i_1(t)\rangle_{T_s}$$

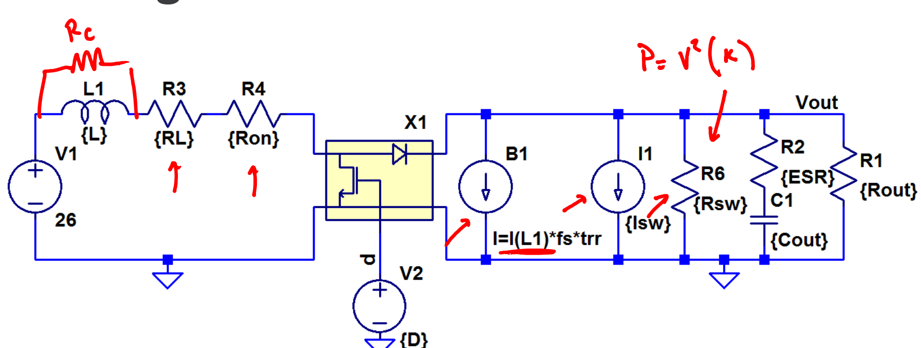


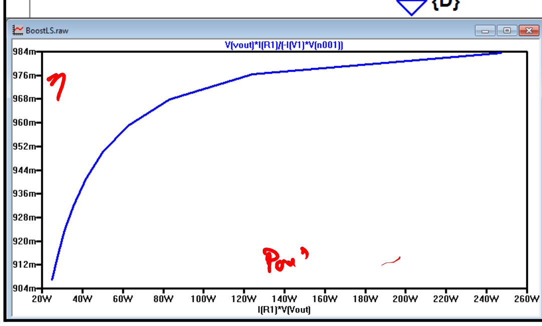
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Averaged Switch Model



Averaged Model With Losses





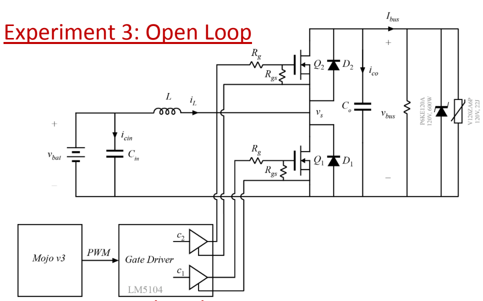
.op
.param Rout = 10
.step param Rout 10 100 10

What known error(s) will be present in loss predictions with this model?

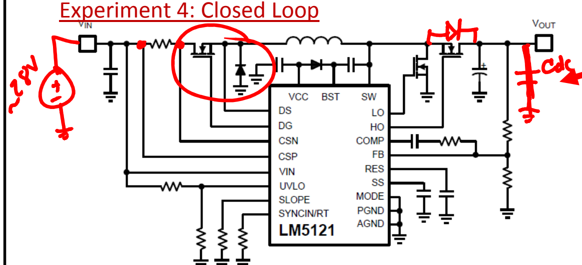
Experiment 4

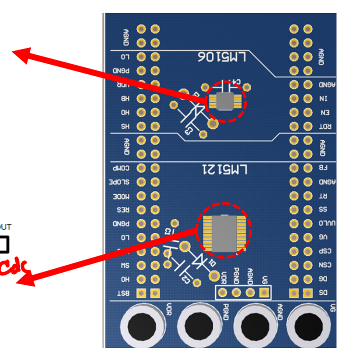
Experiment 4: Closed-Loop Boost

Experiment 3: Open Loop

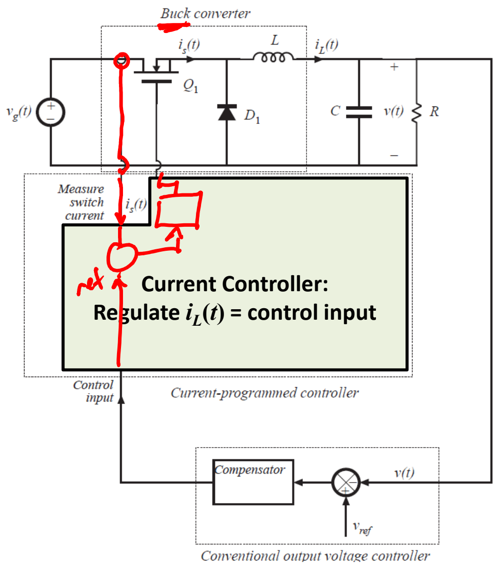


Experiment 4: Closed Loop

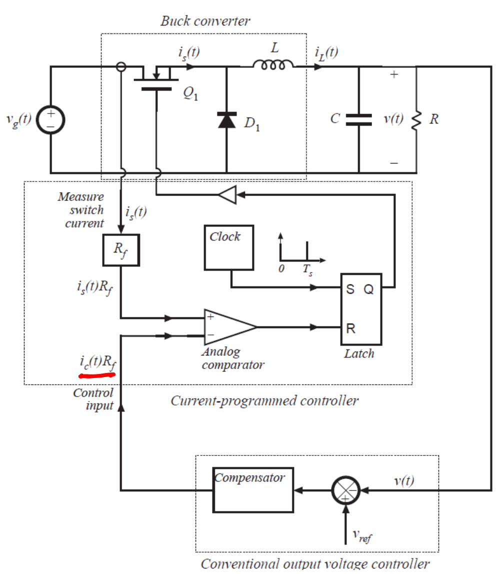




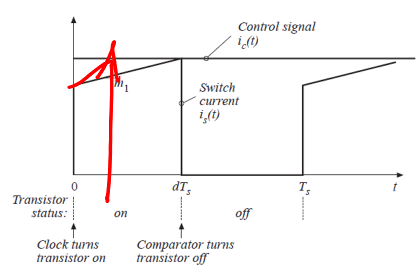
Current Control



Current Programmed Control (CPM)



The peak transistor current replaces the duty cycle as the converter control input.

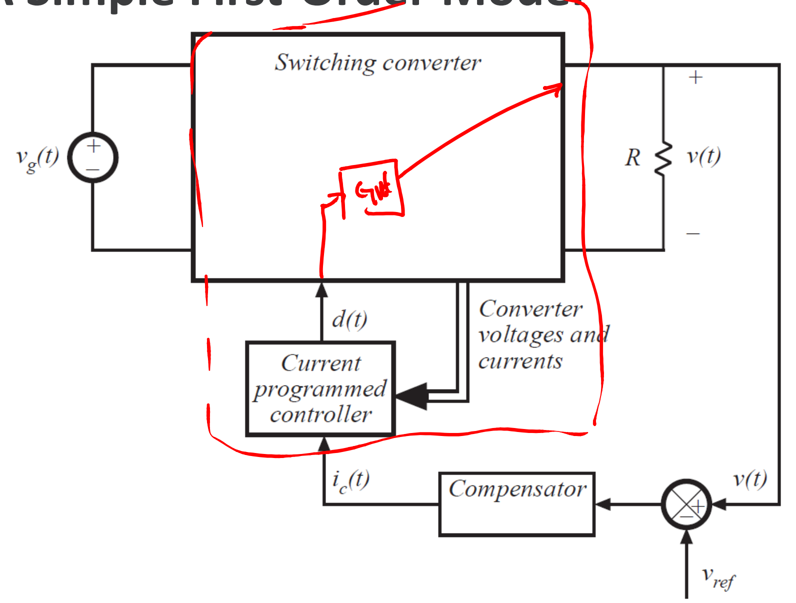


Current Programmed Control

- Covered in Ch. 12 of *Fundamentals of Power Electronics*
- Advantages of current programmed control:
  - Simpler dynamics —inductor pole is moved to high frequency
  - Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
  - It is always necessary to sense the transistor current, to protect against overcurrent failures. We may as well use the information during normal operation, to obtain better control
  - Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$
  - Transformer saturation problems in bridge or push-pull converters can be mitigated
- A disadvantage: susceptibility to noise

THE UNIVERSITY OF TENNESSEE KNOXVILLE

A Simple First-Order Model



THE UNIVERSITY OF TENNESSEE KNOXVILLE

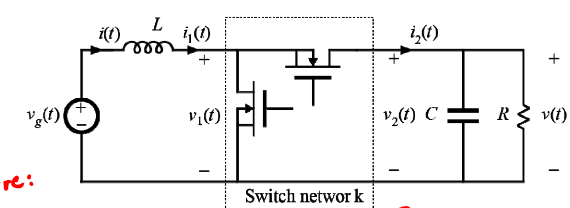
The First-Order Approximation

$$\langle i_L(t) \rangle_{T_s} = i_c(t)$$

- Neglects switching ripple
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small
- Accurate when artificial ramp (discussed later) small
- Resulting small-signal relation:

$$\hat{i}_L(s) \approx \hat{i}_c(s)$$

Averaged Modeling



from before:

AC: (1) $L\frac{d\hat{i}_L}{dt} = \hat{v}_g - D'\hat{v} + V\hat{d}$ (2) $C\frac{d\hat{v}}{dt} = -I_L\hat{d} + D'\hat{i}_L - \frac{\hat{v}}{R}$

Apply $\hat{i}_L = \hat{i}_c$

solve (1) for $\hat{d}$ → plug into (2)

$$\hat{d} = \frac{1}{V}\left(sL\hat{i}_c - \hat{v}_g + D'\hat{v}\right)$$

→ duty cycle is determined by: $\hat{i}_c$, $\hat{v}_g$, $\hat{v}$

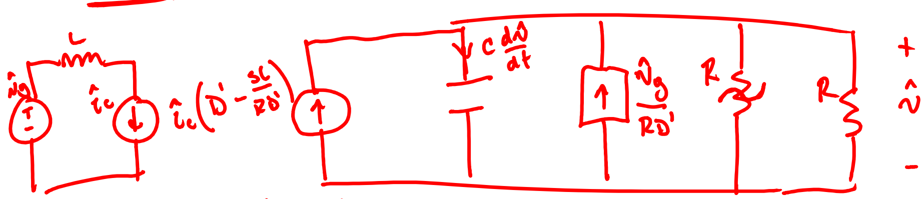
Apply $I_L = \frac{V}{RD'}$, $V = \frac{V_g}{1-D}$

$$C\frac{d\hat{v}}{dt} = -\frac{I_L}{V}\left(sL\hat{i}_c - \hat{v}_g + D'\hat{v}\right) + D'\hat{i}_c - \frac{\hat{v}}{R}$$

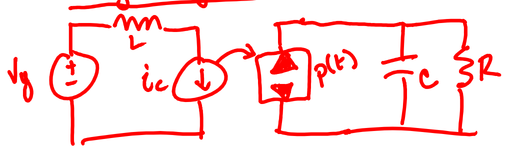
$$C\frac{d\hat{v}}{dt} = \frac{-1}{RD'}\left(sL\hat{i}_c - \hat{v}_g + D'\hat{v}\right) + D'\hat{i}_c - \frac{\hat{v}}{R}$$

$$C\frac{d\hat{v}}{dt} = \hat{i}_c\left(D' - \frac{sL}{RD'}\right) + \frac{\hat{v}_g}{RD'} - \frac{\hat{v}}{R} - \frac{\hat{v}}{R}$$

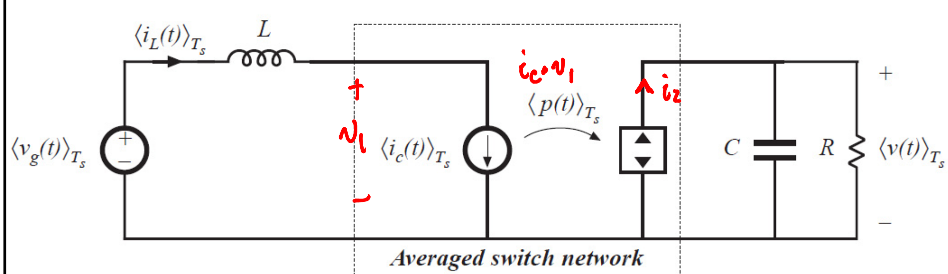
AC equiv circuit model:



Large-signal nonlinear model

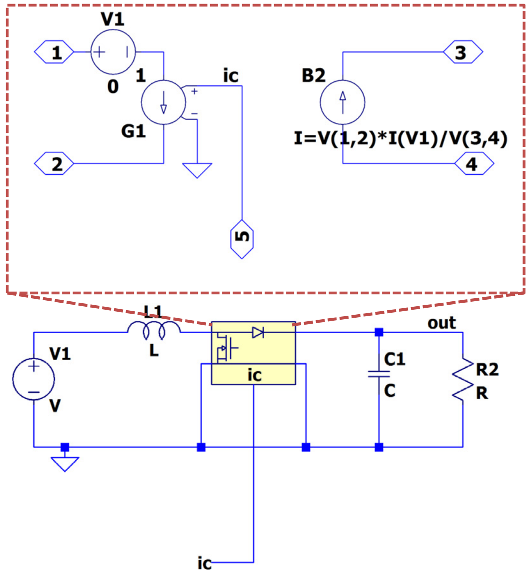


Large-Signal Nonlinear Model



e.g. $i_2 = \frac{v_1 \cdot i_c}{v}$

Implementation in LTSpice

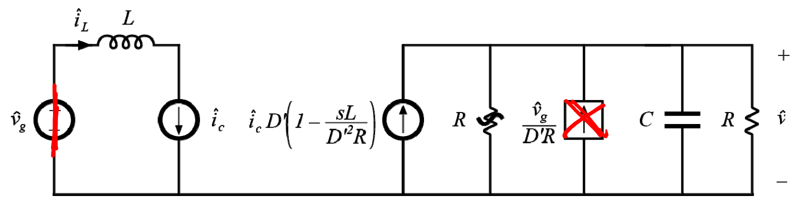


THE UNIVERSITY OF TENNESSEE KNOXVILLE

Perturb and Linearize

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Boost CCM CPM Small-Signal Model



$$G_{vc} = \frac{\hat{v}}{\hat{i}_c}\bigg|_{\hat{v}_g=0} = D'\left(1-\frac{sL}{D'^2R}\right)\left(\frac{1}{sC}\,\|\,R\,\|\,R\right)$$

$$= D'\left(1-\frac{sL}{D'^2R}\right)\frac{R/2}{1+s\frac{CR}{2}}$$

$$G_{vc} = \frac{D'R}{2}\,\frac{\left(1-\frac{sL}{D'^2R}\right)}{1+s\frac{CR}{2}}$$

← same RHP zero from D-control Boost

← Single Pole!

still limit BW to ~ $\frac{f_s}{10}$ ($\frac{f_s}{5}$ aggressive)

CPM Transfer Functions

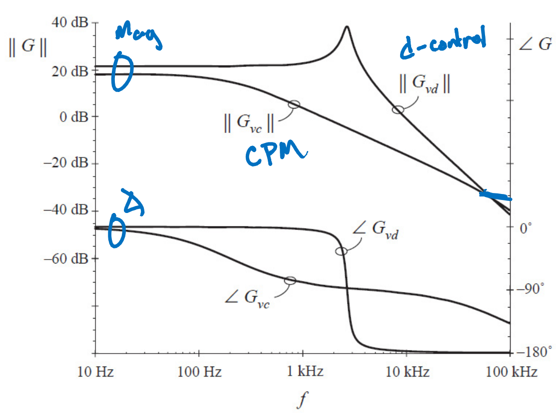
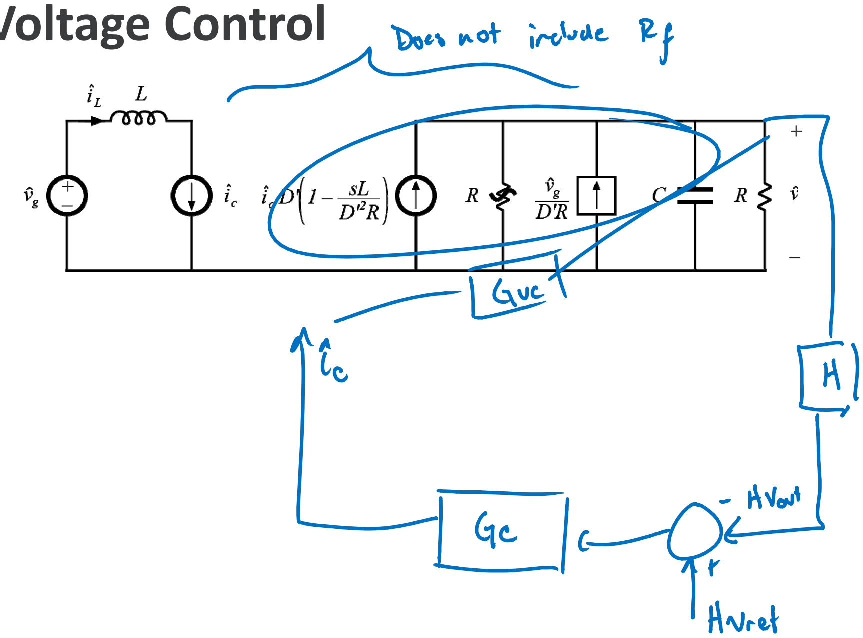


Fig. 12.28 Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.

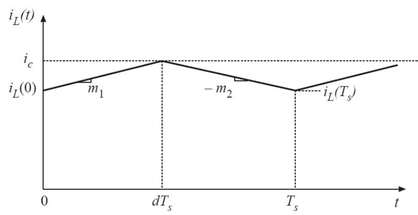
Voltage Control



CPM Oscillations for D>0.5

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology
- Controller can be stabilized by addition of an artificial ramp

Inductor Current Waveform in CCM



Inductor current slopes m_1 *and* $-m_2$

buck converter

$$m_1 = \frac{v_g - v}{L} \qquad -m_2 = -\frac{v}{L}$$

boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v_g - v}{L}$$

buck–boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v}{L}$$

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Volt-Second Balancing

First interval: i_1

$$i_L(dT_s) = i_c = i_L(0) + m_1 dT_s$$

Solve for d:

$$d = \frac{i_c - i_L(0)}{m_1 T_s}$$

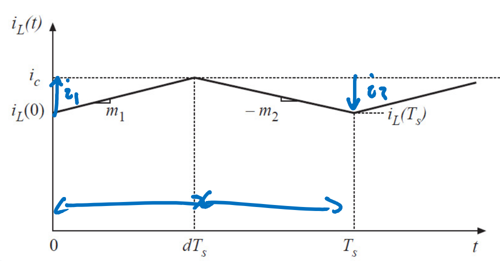
Second interval: i_2

$$i_L(T_s) = i_L(dT_s) - m_2 d' T_s$$
$$= i_L(0) + m_1 dT_s - m_2 d' T_s$$

In steady state:

$$0 = M_1 D T_s - M_2 D' T_s$$

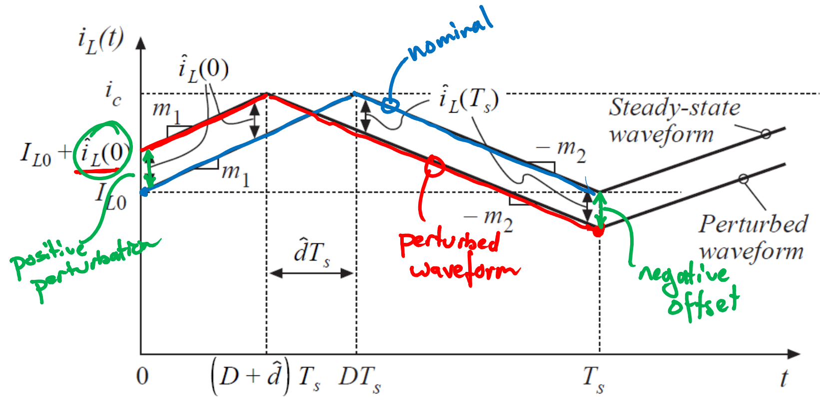
$$\frac{M_2}{M_1} = \frac{D}{D'}$$



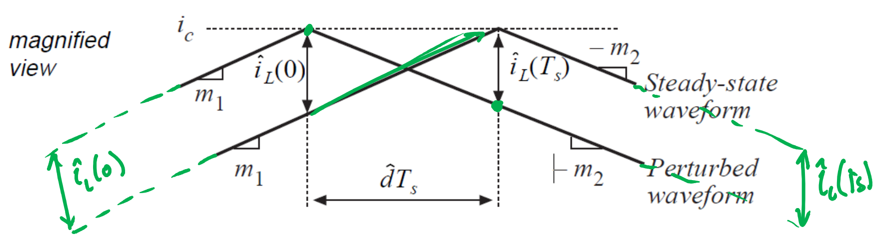
In steady state
$i_1 = i_2$

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Introducing a Perturbation



Change in Inductor Current Over T_s



$$\hat{i}_L(0) = -\, m_1 \hat{d} T_s$$

$$\hat{i}_L(T_s) = m_2 \hat{d} T_s$$

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2}{m_1}\right)$$

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)$$

$$\hat{i}_L(2T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^2$$

$$\hat{i}_L(nT_s) = \hat{i}_L(0)\left(\frac{-D}{D'}\right)^n$$

Stable only if $\frac{D}{D'} < 1 \rightarrow D < 0.5$

Final Value of Inductor Current

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)$$

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^2$$

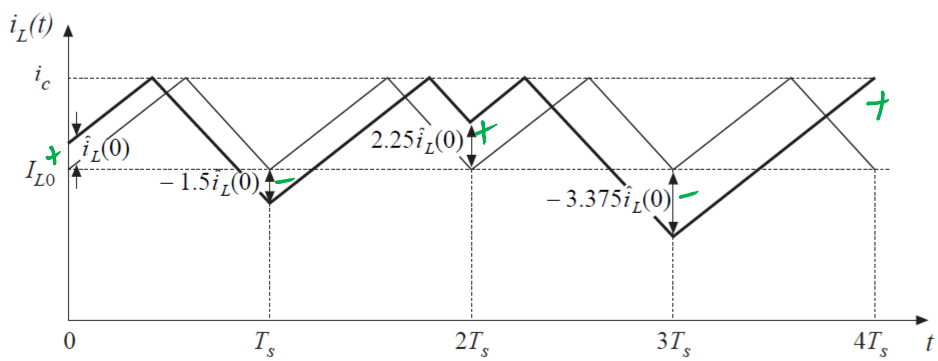
$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^n$$

$$\left|\hat{i}_L(nT_s)\right| \rightarrow \begin{cases} 0 & \text{when } \left|-\frac{D}{D'}\right| < 1 \\ \infty & \text{when } \left|-\frac{D}{D'}\right| > 1 \end{cases}$$

For stability: $D < 0.5$

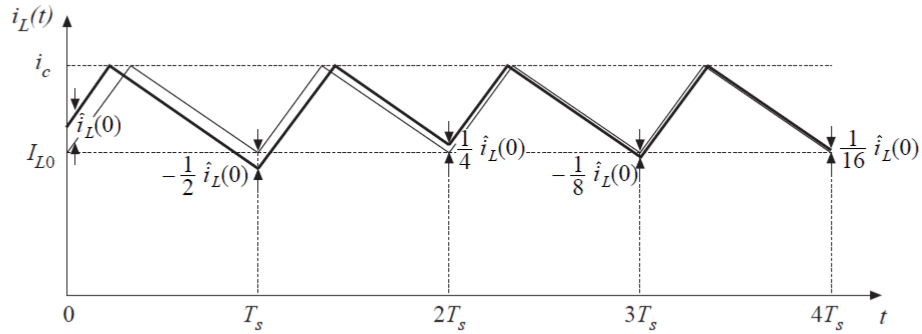
Example: Unstable operation for D=0.6

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5$$

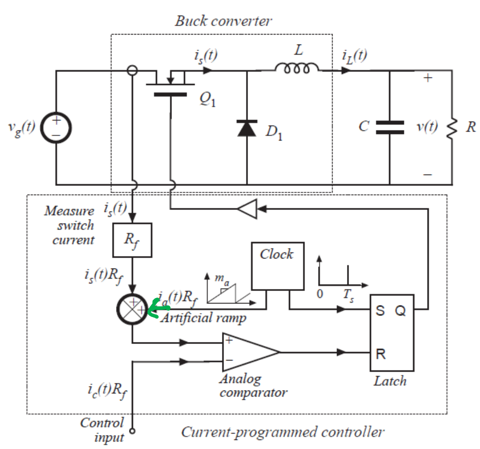


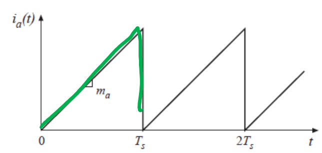
Example: Stable operation for D=1/3

$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5$$



Stabilization Through Artificial Ramp





Now, transistor switches off when

$$i_a(dT_s) + i_L(dT_s) = i_c$$

or,

$$i_L(dT_s) = i_c - i_a(dT_s)$$

Final Value of Inductor Current

First subinterval:

$$\hat{i}_L(0) = -\hat{d}T_s\left(m_1 + m_a\right)$$

Second subinterval:

$$\hat{i}_L(T_s) = -\hat{d}T_s\left(m_a - m_2\right)$$

Net change over one switching period:

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)$$

After n switching periods:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = \hat{i}_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = \hat{i}_L(0)\,\alpha^n$$

Characteristic value:

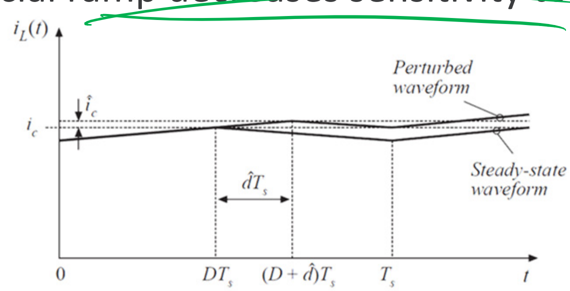
$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a}$$

$$\left|\hat{i}_L(nT_s)\right| \rightarrow \begin{cases} 0 & \text{when } \left|\alpha\right| < 1 \\ \infty & \text{when } \left|\alpha\right| > 1 \end{cases}$$

Artificial Ramp: Additional Notes

- For stability, require $|\alpha| < 1$
- Common choices:
  - $m_a = 0.5\, m_2$
  - $m_a = m_2$
- Artificial ramp decreases sensitivity to noise

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}}$$

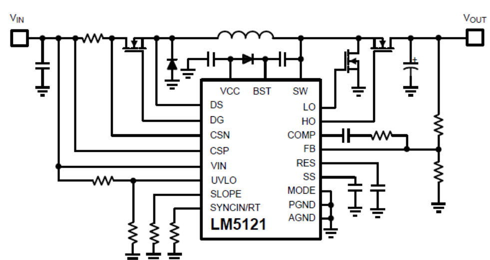


More Accurate Models

- The simple models of the previous section yield insight into the low- frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:
  - Line-to-output transfer function of the buck converter
  - Dynamics at frequencies approaching f_s
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller
- See Section 12.3 for additional info

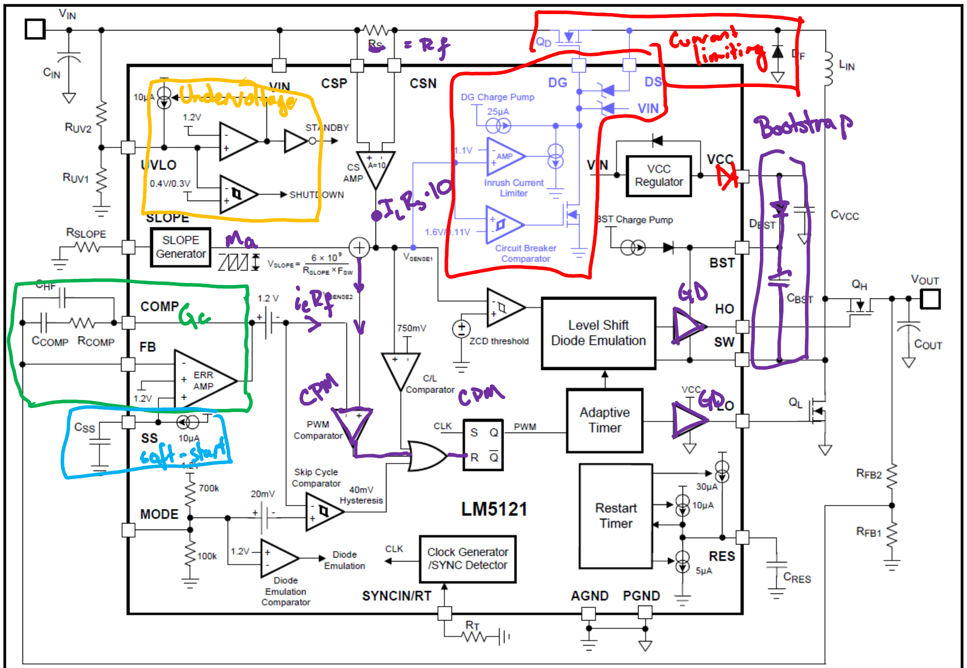
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Application to Experiment 4

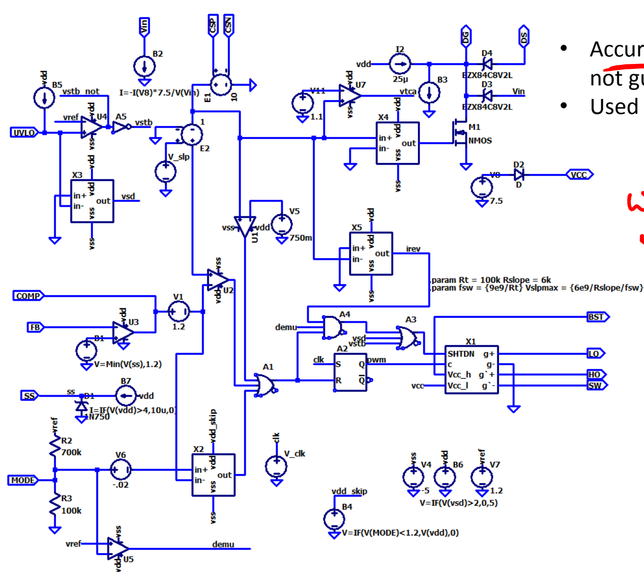


- Complex switching controller
- **Read** the datasheet first

THE UNIVERSITY OF TENNESSEE KNOXVILLE



Internal Functional Model in LTSpice



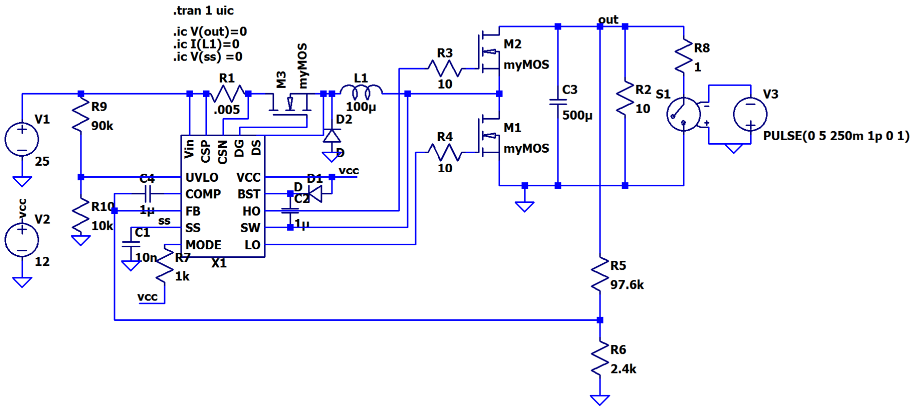
- Accuracy/functionality not guaranteed
- Used for insight only

Works only in 'forced PWM'
- Not diode emulation
- Not burst mode

In-Circuit Simulation

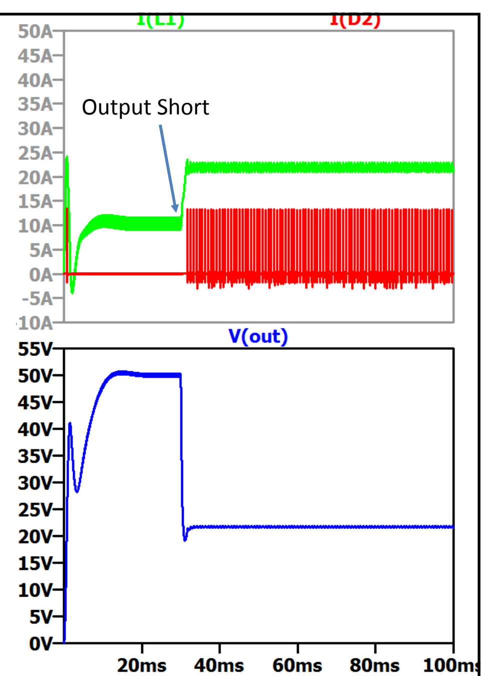
.model mysw sw(Von=3 Voff=2 Ron=.1 Roff = 1Meg)

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rs=10m Rb=17m Kp=30 Cgdmax=.5p Cgdmin=.05n Cgs=.2n Cjo=.03p Is=88p)



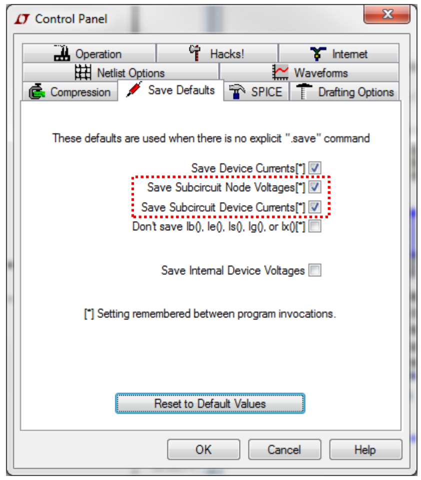
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Sim Results



THE UNIVERSITY OF TENNESSEE KNOXVILLE

A Tip: Debug Internal of Subcircuit



THE UNIVERSITY OF TENNESSEE KNOXVILLE