PCB Layout

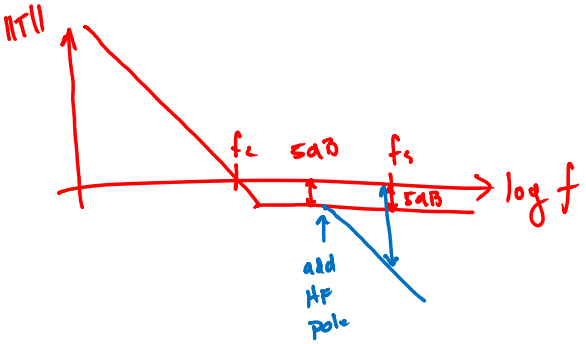
ECE 482 Lecture 5
March 7, 2016

THE UNIVERSITY OF TENNESSEE KNOXVILLE

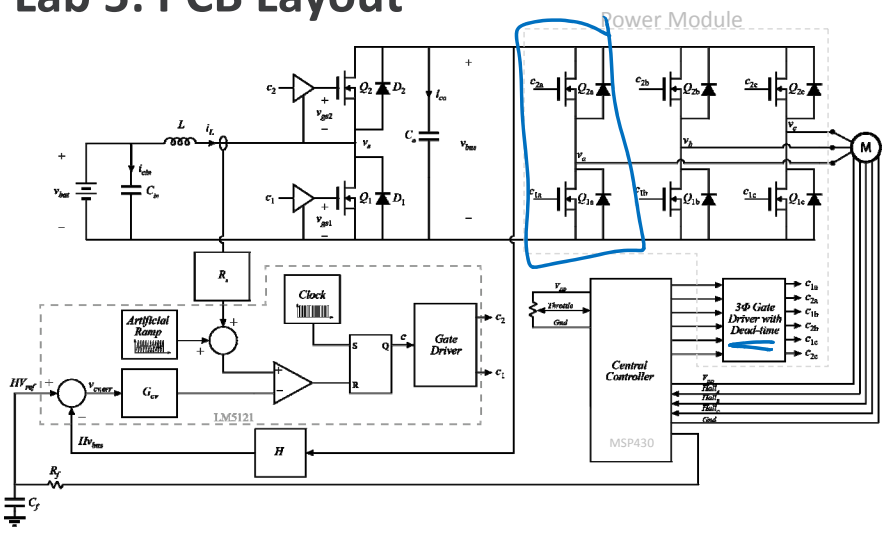
Announcements

- Prelab 5 due Tuesday
  - Decide on System Improvements
  - Redesign using GaN Devices
- Experiment 4 report moved to Thurs. 3/24
- Midterm after spring break
  - Open note, book, instructor
- Today: Experiment 5
  - No report; deliverables are layout files

Prelab 5: HF Attenuation



Lab 5: PCB Layout

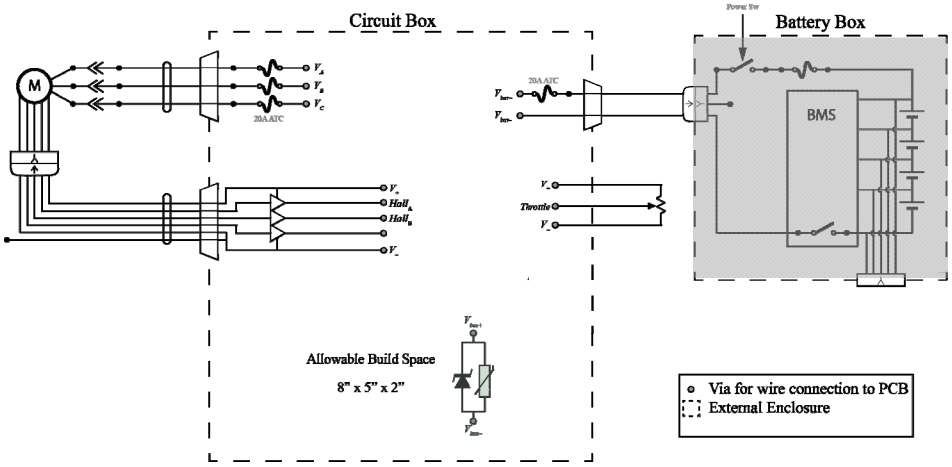


- More information on motor drive in Experiment 5

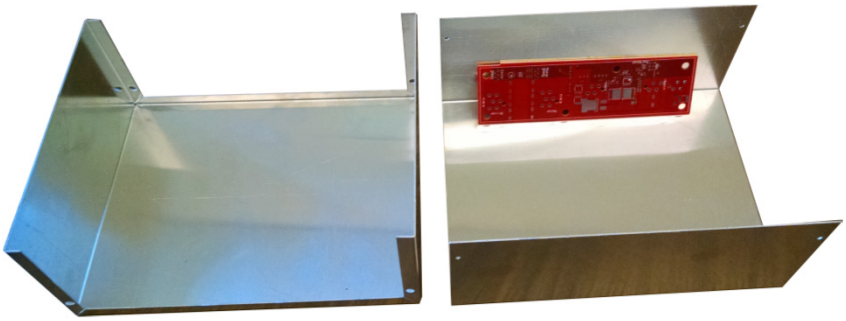
Design Modification

- You may order additional parts, at reasonable cost/benefit
  - Will need to provide a listing of parts from digikey with final Exp 5 files
- Reuse components from lab kit where possible
- Use SMD ceramic, low ESR caps for power stage and gate drive decoupling

Circuit Connections



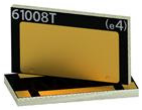
Circuit Enclosure



Prelab for Experiment 5: Redesign with GaN

GaN Systems GS61008T

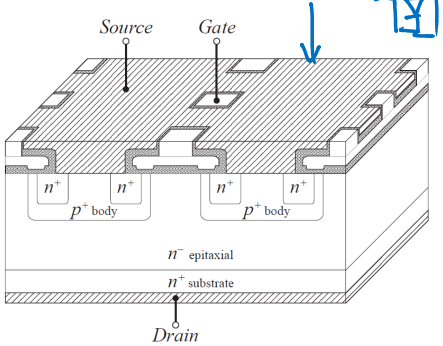
- 7.4 mOhm
- 100V/80A
- Q_g = 12 nC
- C_{oss} = 250 pF (80V)
- Top-cooled



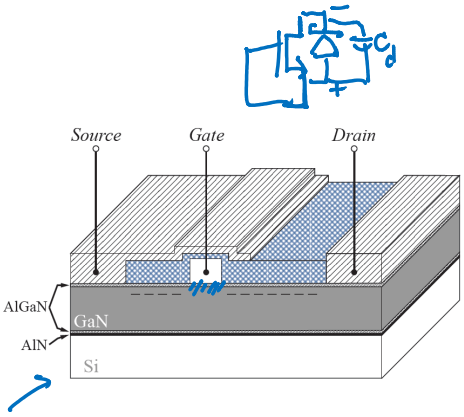
EPC EPC2001C

- 7 mOhm
- 100V/36A
- Q_g = 9 nC
- C_{oss} = 375 pF (80V)
- Bottom-cooled

GaN Devices



Vertical Silicon Power MOSFET



Lateral GaN HEMT

- No body diode (reverse conduction due to $V_{gd} > V_{gd,th} \approx 2V$)
  - Use antiparallel (schottky) diode or precise dead time
- Significantly faster switching

Designing with GaN

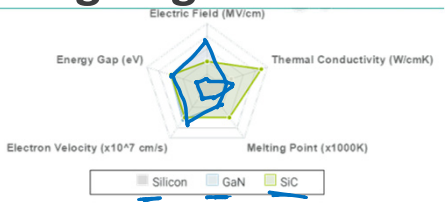
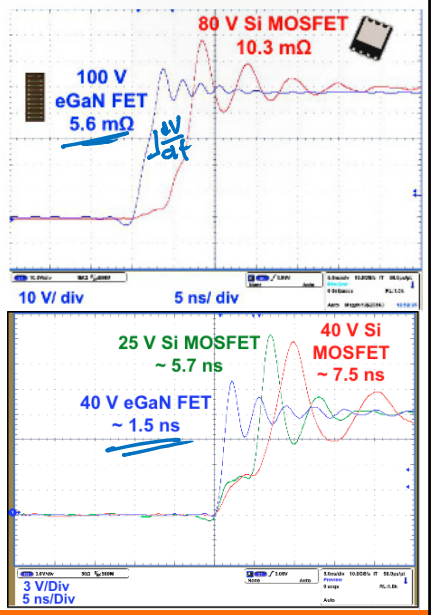


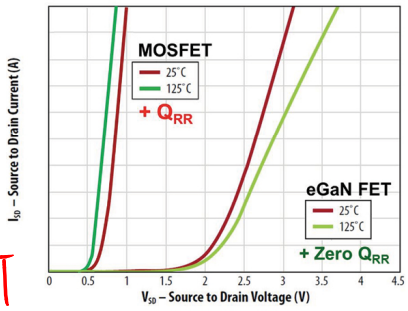
Fig. 1: Material properties of silicon, silicon carbide, and gallium nitride.

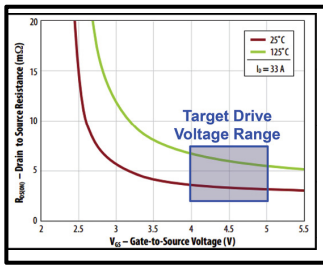
- Because of high electric breakdown field and high electron velocity, GaN devices with comparable R_{on} can be significantly smaller and switch must faster.
- Need **very** good layout to prevent ringing from causing overvoltage and device failure.

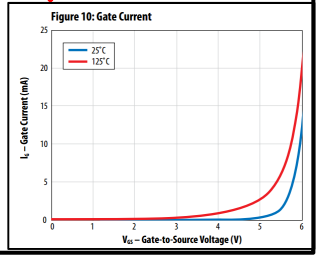


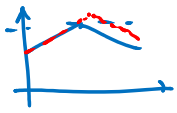
GaN Design Issues

1. Reverse conduction mechanism
2. Sensitivity to parasitics
3. Gate robustness









WBG Device Characterization

- Seminar Monday, March 7th, 12:00-4:00pm
- Registration (w/ lunch)
  - https://docs.google.com/forms/d/15xaqCM_jwjD1CW0e9Iny0jaBLruwjLZXFPu7Za8FWcM/viewform
- Also available remotely via WebEx

Basic PCB Layout Concepts

- Trace Parasitics
- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances
- Ground Plane / Return Currents
- Partitioning

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Trace Parasitics

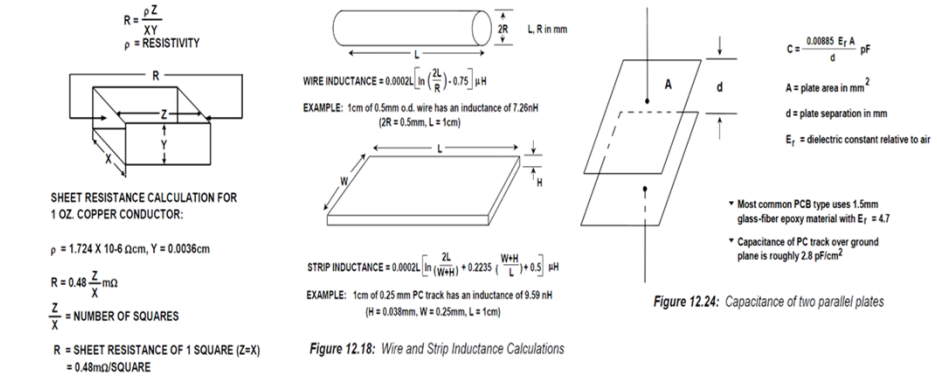


Figure 12.2: Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors

Figure 12.18: Wire and Strip Inductance Calculations

Figure 12.24: Capacitance of two parallel plates

Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Trace Sizing Rough Guidelines

2.2 *PCB Etch*

Table 1 is helpful to determine the current carrying capacity of PCB etches. The table assumes:

- 1oz/sq foot copper (0.035mm thickness).
- 10°C rise on outer layers, 20°C inner layers
- Groups of high current tracks are de-rated
- Tracks are not near or over heat sink areas

Table 1. Current Capacity PCB Etch

WIDTH	CURRENT CAPACITY
0.010"	0.8 A
0.015"	1.2 A
0.020"	1.5 A
0.050"	3.2 A
0.100"	6.0 A

2.3 *Vias or Feedthrus*

Vias limit the current and add inductance between the power supply and load. Layouts are usually done with 10-mil inner ring feedthrus. At this size, current capability is about 1 A per feedthru.

Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Kelvin Connection

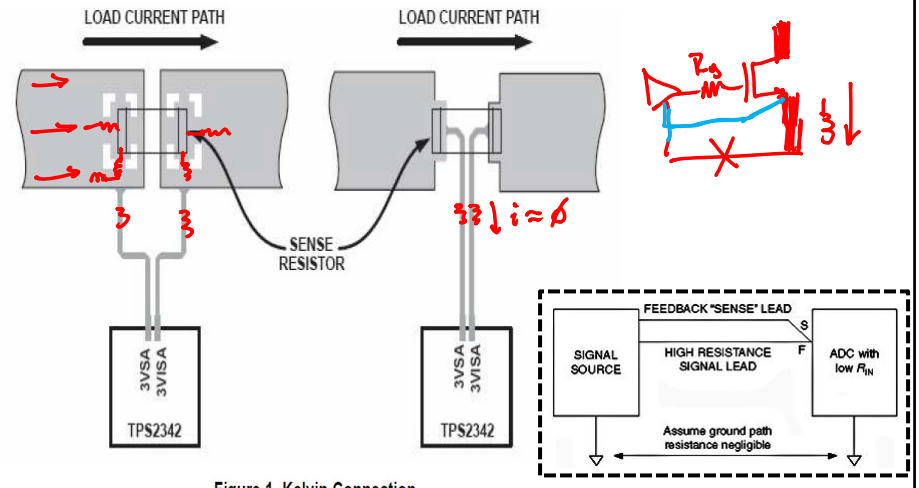
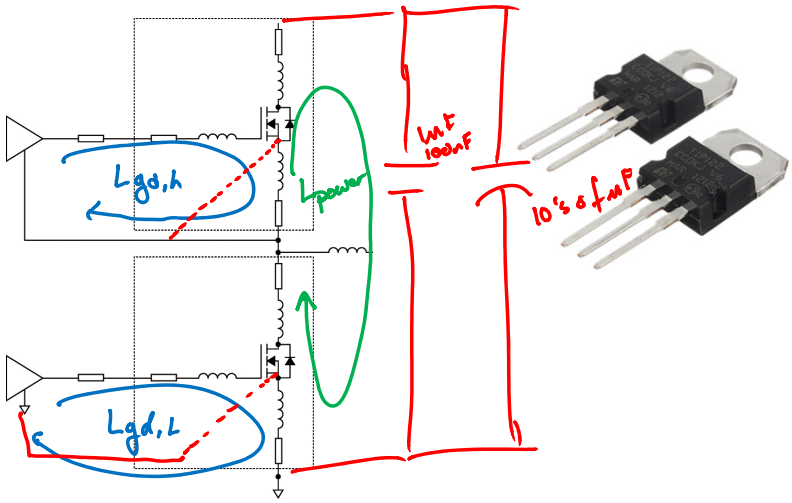


Figure 1. Kelvin Connection

Texas Instruments, "LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers"

THE UNIVERSITY OF TENNESSEE KNOXVILLE

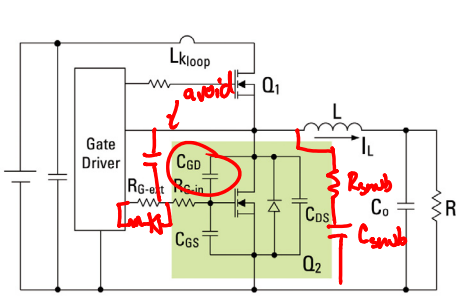
Common Source Inductance

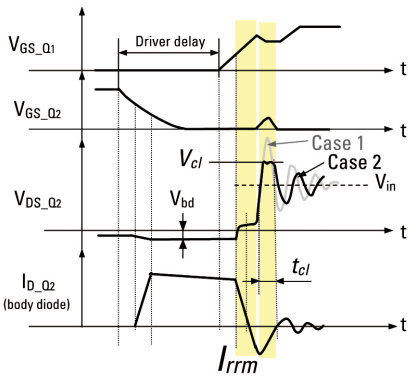


Persson E., "What really limits MOSFET performance: silicon, package, driver or circuit board?"

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Gate-Drain Capacitance





Persson E., "What really limits MOSFET performance: silicon, package, driver or circuit board?"

THE UNIVERSITY OF TENNESSEE KNOXVILLE

High Impedance Nodes and Capacitive Coupling

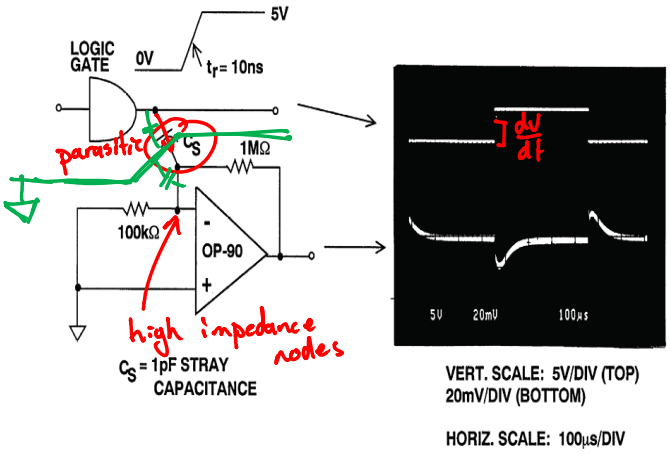


Figure 12.29 *High Circuit Impedances Increase Susceptibility to Noise Pickup*

Capacitive Shielding

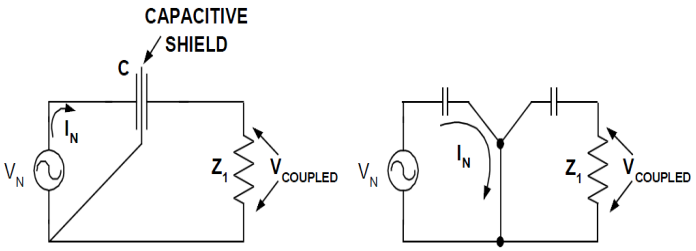
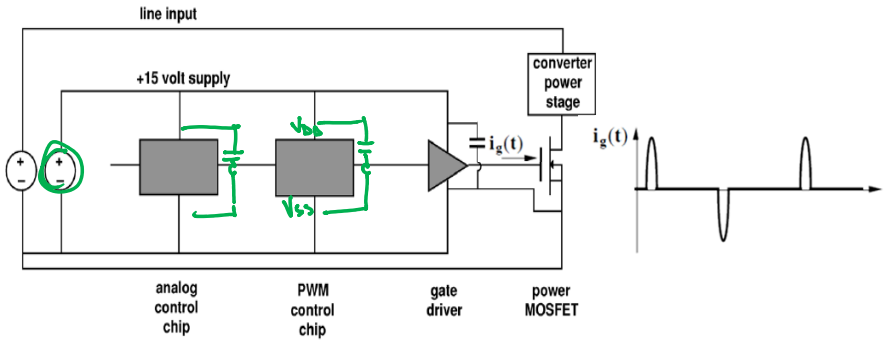


Figure 12.26: *An Operational Model of a Faraday Shield*

Supply Decoupling



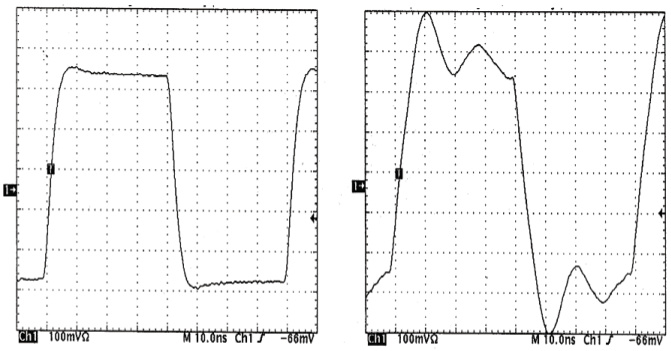
High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

Pulsed Circuit Decoupling

PROPER DECOUPLING

NO DECOUPLING



VERTICAL SCALE: 100mV/div
HORIZONTAL SCALE: 10ns/div

Figure 12.68: *Effects of Inadequate Decoupling on the Phase Response of the AD9631 Op Amp*

Analog Devices, "Decoupling Techniques," MT-101

Decoupling Capacitance

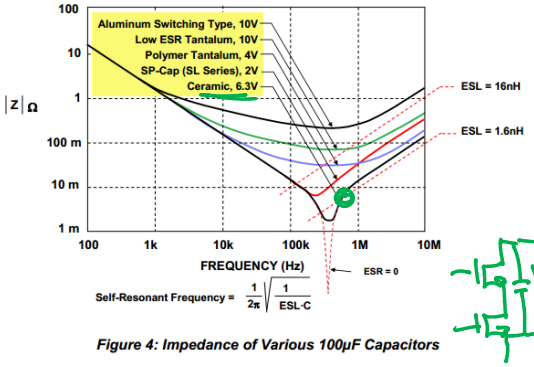


Figure 4: Impedance of Various 100µF Capacitors

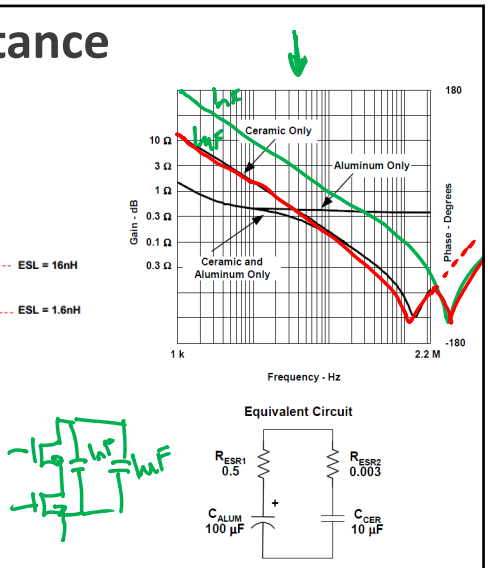


Fig. 8. Paralleled capacitors minimize impedance over frequency.

Analog Devices, "Decoupling Techniques," MT-101

THE UNIVERSITY OF TENNESSEE KNOXVILLE

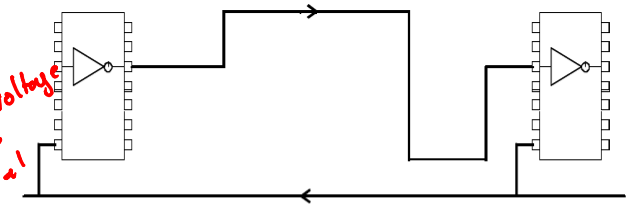
Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

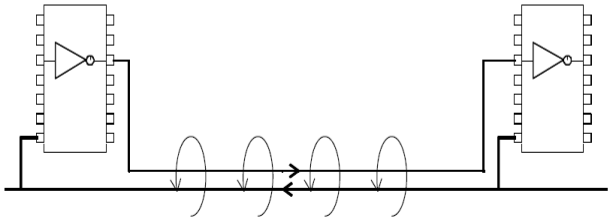
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Loop Inductances

* Always consider voltage signals as differential



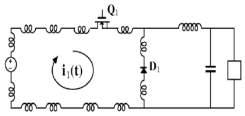
Bad practice: wide separation of signal and return



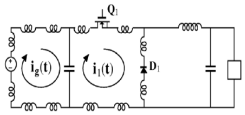
Good practice: close coupling of signal and return

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

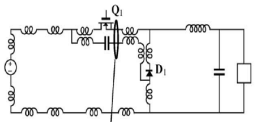


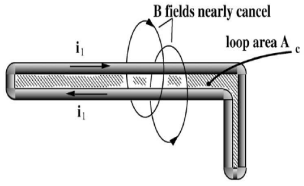
Addition of bypass capacitor confines the pulsating current to a smaller loop:



high frequency currents are shunted through capacitor instead of input source

Even better: minimize area of the high frequency loop, thereby minimizing its inductance





Gate Drive Signal Routing

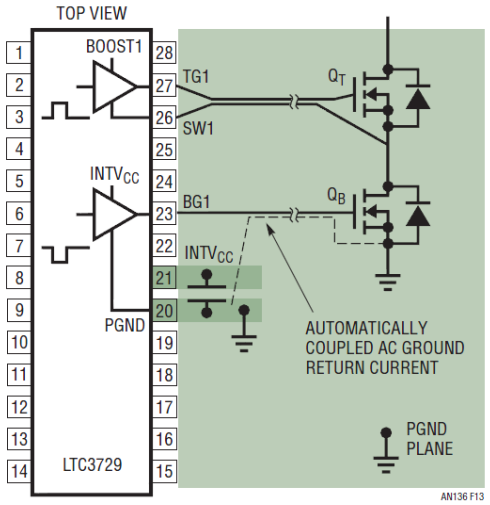


Figure 13. Gate Driver Trace Routing of the MOSFETs

Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize

Buck Example Bridge Layout

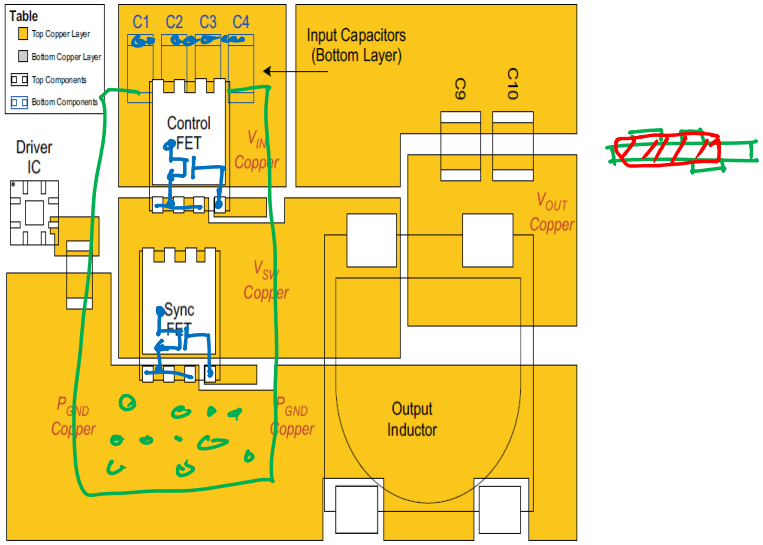
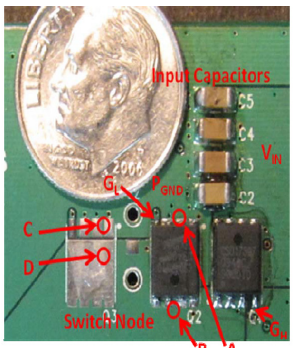


Figure 2. Typical Placement and PCB Layout of the Power Stage Components

Example Bridge Layout #2



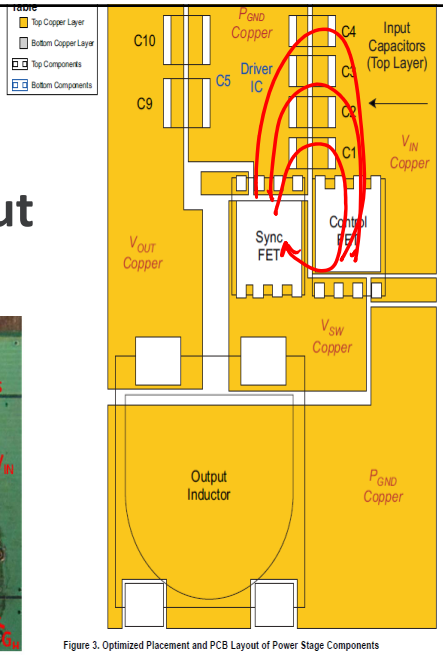


Figure 3. Optimized Placement and PCB Layout of Power Stage Components

Example Layout Experimental Results

Example Layout #1

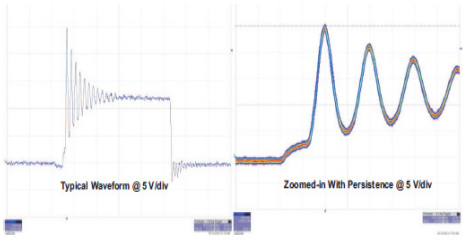


Figure 4. Switch Node (VSW) Voltage Ringing on Typical Layout

Example Layout #2

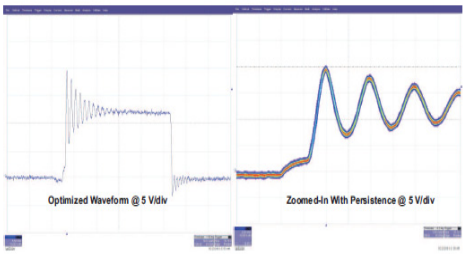


Figure 5. Switch Node (VSW) Voltage Ringing on Optimized Layout

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Star-Grounding Vs. Daisy Chain

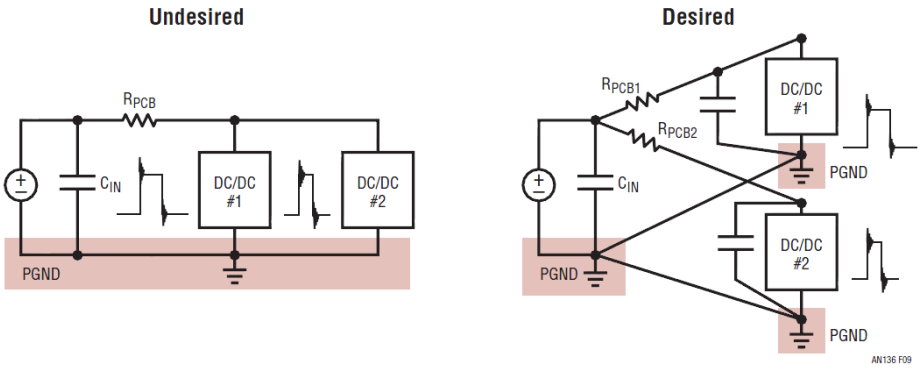
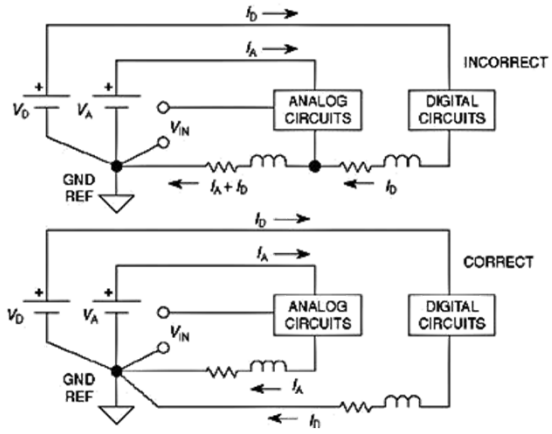


Figure 9. Separate the Input Current Paths Among Supplies

THE UNIVERSITY OF TENNESSEE KNOXVILLE

Another View



Kester, W. "Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects"

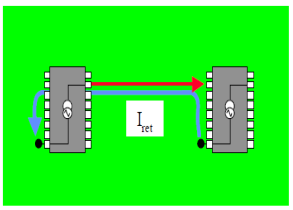
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Ground Plane

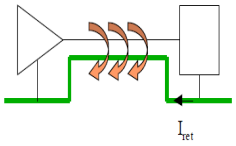
- Benefits:
  - Common reference voltage
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable

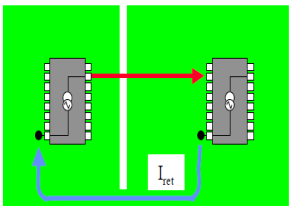
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Ground Currents

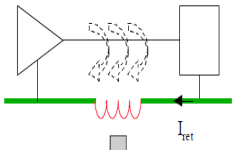


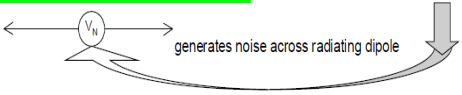
No split: high mutual inductance, low ground inductance



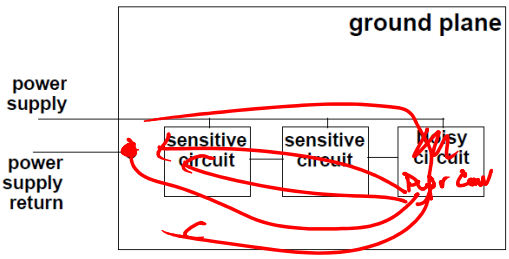


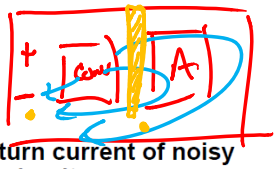
Extra return path adds ground inductance



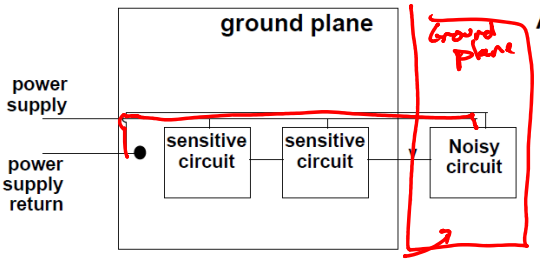


Ground Plane Isolation





Return current of noisy circuit runs underneath sensitive circuits, and can still corrupt their ground references

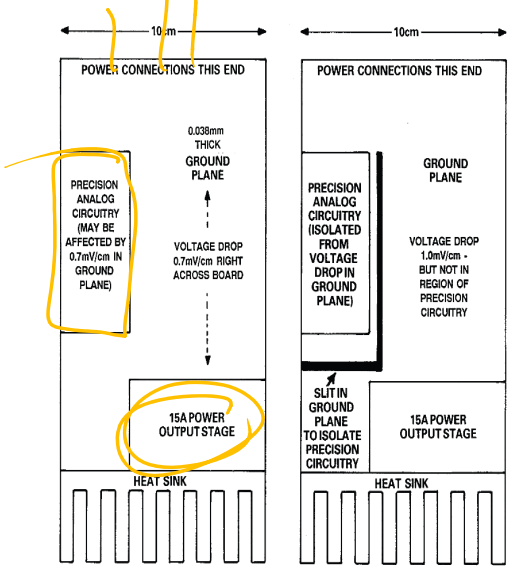


A solution is to remove the noisy circuit from the ground plane. One could then run a separate ground wire for the noisy circuit. The only drawback is that noise can be coupled into the input signal v.

Cuts in Ground Plane

- Goals:
  - minimize inductance/loops
  - Minimize ground interference
- Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
- Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
- Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

Effective Ground Plane Cuts



Experiment 5: Starting Files