

# Power Electronics Circuits

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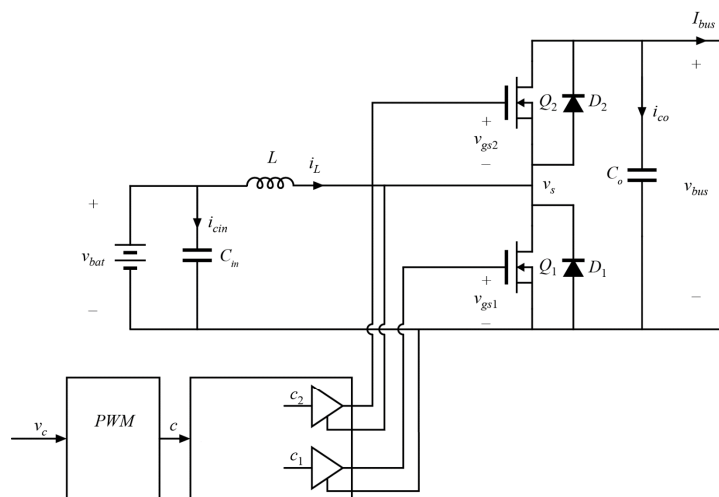
ECE 482 Lecture 3

January 26, 2016



THE UNIVERSITY OF  
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## Experiment 3



## Prelab Assignment

### Experiment 3

#### ECE 482

Fig. 1 shows the power stage of the drivetrain boost converter to be assembled in experiment 3. For all parts of this prelab, consider operation of the converter at an operating point around which:

- $V_{bat} = 25 \text{ V}$
- $V_{bat} \leq 50 \text{ V}$
- $5 \text{ kHz} \leq f_s \leq 1 \text{ MHz}$
- $\Delta V_{out} \leq 1 \text{ V}$

*under-constrained*

*$f_s = ?$   
 $\Delta V = ?$   
 $P_{max} = ?$*

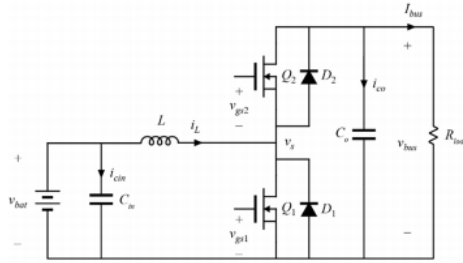


Figure 1: Open loop boost converter (implementation shown with MOSFET devices)

## Design Assessment

In experiment 3, a portion of your grade will be the performance of the design that you choose to build. A 20% segment of the lab grade will be determined by the following formula, which rewards designs with small size, high efficiency, and high power capability:

$$\text{Grade [\%]} = 25 - \kappa_{core} - 100 \cdot (0.98 - \eta_{P_{out}=100}) - \frac{P_{max} - 250}{50},$$

where

$$\kappa_{core} = \begin{cases} 0, & \text{ETD29 / EFD25} \\ 3, & \text{ETD39} \\ 6, & \text{ETD44} \\ 9, & \text{ETD49} \end{cases}$$

According to the inductor core you have chosen for your design.  $P_{max}$  is the maximum power tested, which must be at least 100W, and may be as high as 250W.

## Boost Design

Power Semiconductor

Part No.	Quantity	Description
<a href="#">irfb4615pbf</a>	1	60 V, 195 A, StrongIRFET
<a href="#">AOT2500L</a>	X	150 V, 150 A, High Voltage Trench MOSFET
<a href="#">FDP083N15A</a>	X	150 V, 117 A PowerTrench MOSFET
<a href="#">IPP200N15N3</a>	X	150 V, 50 A OptiMOS Power MOSFET
<a href="#">irfb4615pbf</a>	X	150 V, 35 A HEXFET Power MOSFET
<a href="#">FGPF50N33BT</a>	X	330 V, PDP Trench IGBT
<a href="#">ISL9V3040D</a>	X	400 V, N-Channel IGBT

Choose transistor

Core Geometry	Material
<a href="#">ETD29</a>	<a href="#">Ferroxcube 3C90</a> <a href="#">Ferroxcube 3F3</a>
<a href="#">ETD39</a>	<a href="#">Ferroxcube 3C90</a> <a href="#">Ferroxcube 3F3</a>
<a href="#">ETD44</a>	<a href="#">Ferroxcube 3C90</a> <a href="#">Ferroxcube 3F3</a>
<a href="#">ETD49</a>	<a href="#">Ferroxcube 3C90</a> <a href="#">Ferroxcube 3F3</a>

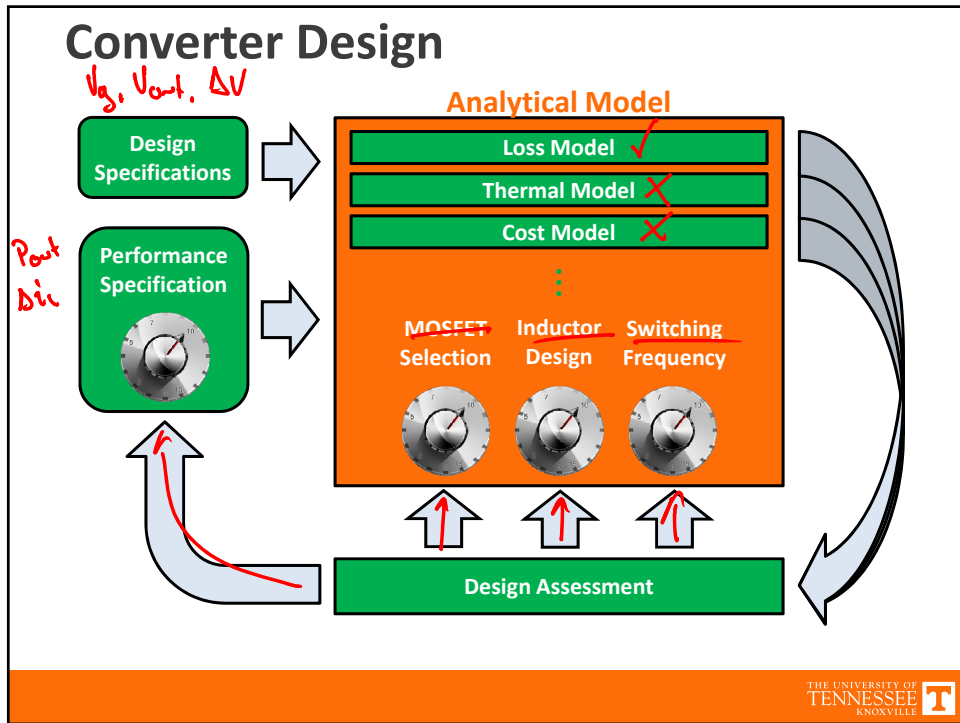
Choose Ferrite core

Wire Gauge	Diameter [cm]
AWG 10	0.267
AWG 12	0.213
AWG 14	0.171
AWG 16	0.137
AWG 20	0.0874

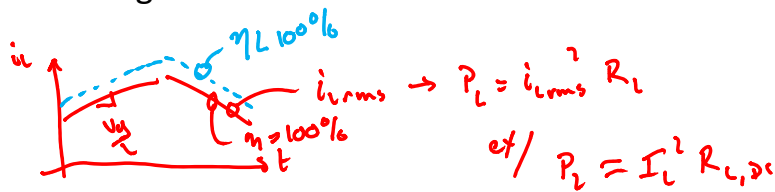
Choose AWG  
(others available if necessary)

[Full AWG table](#)

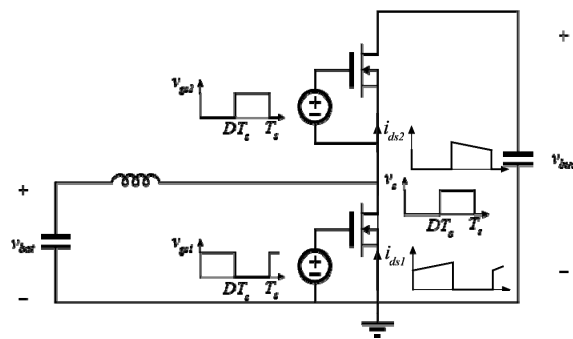


## Analytical Loss Modeling

- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
- Argue which losses need to be included, and which may be neglected
  - “Rough” approximation to gain insight into significance

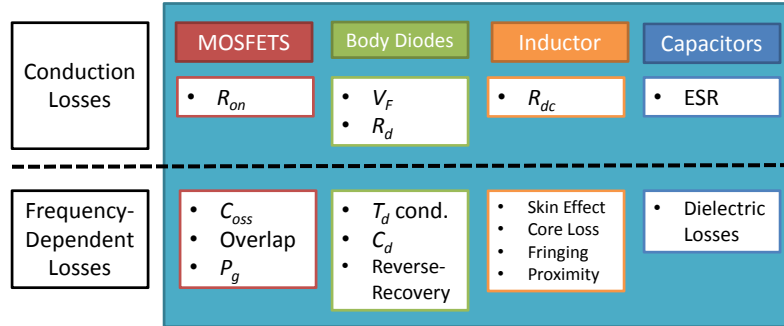


## Boost Converter Loss Analysis



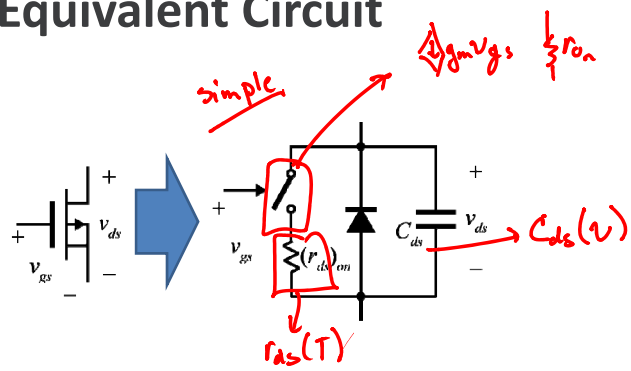
- Begin by solving important waveforms throughout converter assuming lossless operation

## Power Stage Losses



## Conduction Losses

## MOSFET Equivalent Circuit

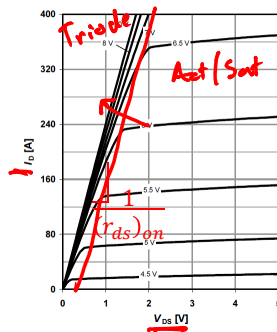


- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

## MOSFET On Resistance

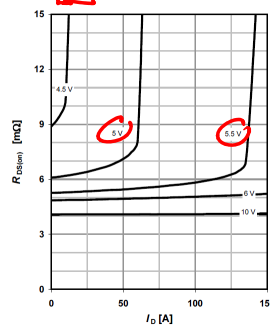
5 Typ. output characteristics

$I_D = f(V_{DS})$ ;  $T_J = 25^\circ\text{C}$   
parameter:  $V_{GS}$



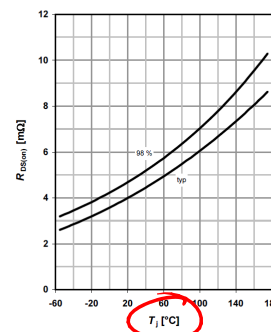
6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D)$ ;  $T_J = 25^\circ\text{C}$   
parameter:  $V_{GS}$



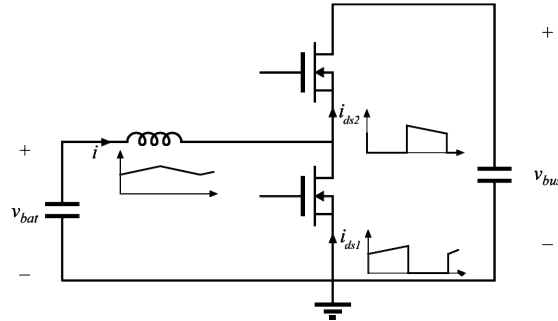
9 Drain-source on-state resistance

$R_{DS(on)} = f(T_J)$ ;  $I_D = 100\text{ A}$ ;  $V_{GS} = 10\text{ V}$



- On resistance extracted from datasheet waveforms
- Significantly dependent on  $V_{GS}$  amplitude, temperature

## Boost Converter RMS Currents



- MOSFET conduction losses due to  $(r_{ds})_{on}$  depend given as

$$P_{cond,FET} = I_{di,rms}^2 (r_{ds})_{on}$$

## MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i}{I}\right)^2} \quad (A.6)$$

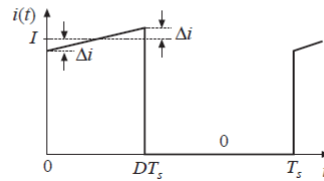
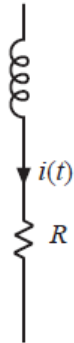


Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

## DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

winding length  
 $l_b = n \cdot MLT$

- At room temp,  $\rho = 1.724 \cdot 10^{-6} \Omega\text{-cm}$
- At 100°C,  $\rho = 2.3 \cdot 10^{-6} \Omega\text{-cm}$
- Losses due to DC current:

$$P_{cu,DC} = I_{L,rms}^2 R_{DC}$$

## Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$r_{ms} = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2} \quad (\text{A.2})$$

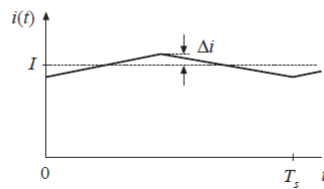
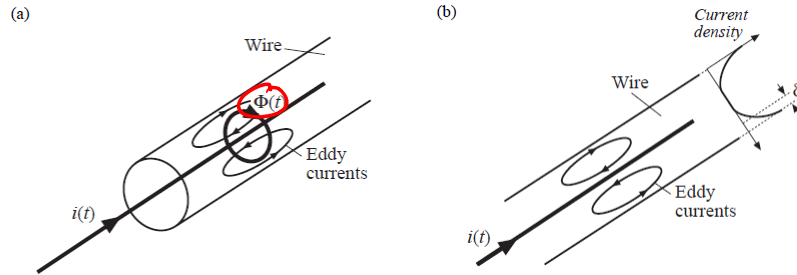


Fig. A.2

- Conduction losses dependent on RMS current through inductor



## Skin Effect in Copper Wire



- Current profile at high frequency is exponential function of distance from center with characteristic length  $\delta$

## Skin Depth

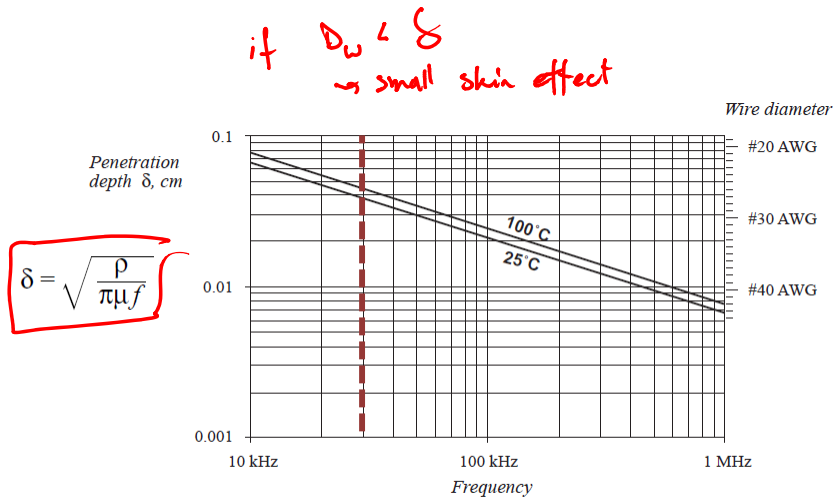
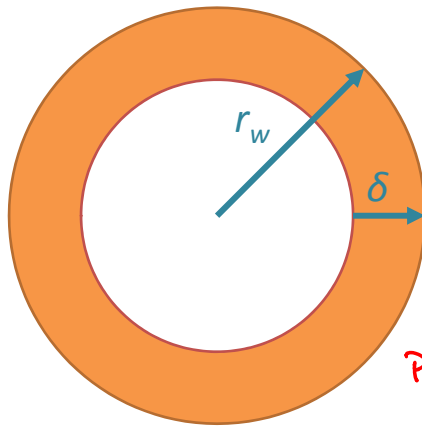


Fig. 13.23 Penetration depth  $\delta$ , as a function of frequency  $f$ , for copper wire.

## AC Resistance



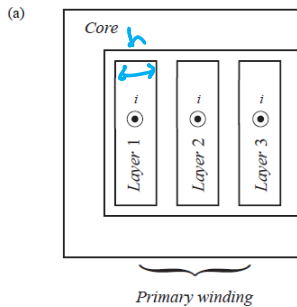
$$A_{w,eff} = \pi r_w^2 - \pi (r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$

$$P_{L,cond} \approx I_L^2 R_{DC} + i_{rip,rms}^2 R_{ac,fs}$$



## Proximity Effect



- In foil conductor closely spaced with  $h \gg \delta$ , flux between layers generates additional current according to Lenz's law.

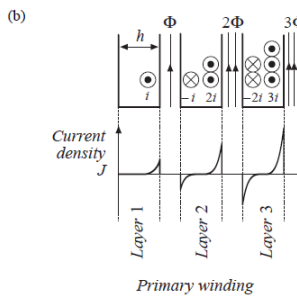
$$P_1 = I_{L,rms}^2 R_{ac}$$

*occurs (significantly) when  $D_w \gg \delta$   
• Many layers*

- Power loss in layer 2:

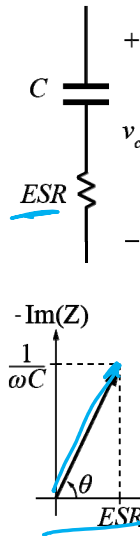
$$P_2 = I_{L,rms}^2 R_{ac} + (2I_{L,rms})^2 R_{ac}$$

$$P_2 = 5P_1$$



- Needs modification for non-foil conductors

## Capacitor Loss Model



- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:

$$\delta = \frac{\pi}{2} - \theta$$

$$D = \tan(\delta)$$

## Capacitor ESR Extraction



WV (Vdc)	Cap (µF)	Case size φD×L(mm)	Impedance (Ωmax/100kHz)		Rated ripple current (mA rms/105°C, 100kHz)	Part No.
			20°C	-10°C		
6.8	5×11		1.4	5.6	125	EKZE101E□□6R8ME11D
15	6.3×11		0.57	2.3	205	EKZE101E□□150MF11D
27	8×11.5		0.36	1.4	355	EKZE101E□□270MHB5D
39	8×15		0.25	1.0	450	EKZE101E□□390MH15D
47	10×12.5		0.17	0.66	480	EKZE101E□□470MJCS5
56	8×20		0.19	0.76	565	EKZE101E□□560MH20D
68	10×16		0.11	0.47	600	EKZE101E□□680MJ16S
82	10×20		0.084	0.34	800	EKZE101E□□820MJ20S
100	12.5×16		0.11	0.34	750	EKZE101E□□101MK16S
120	10×25		0.069	0.28	900	EKZE101E□□121MJ25S
150	12.5×20		0.062	0.18	1,100	EKZE101E□□151MK20S
220	12.5×25		0.047	0.14	1,250	EKZE101E□□221MK25S
220	16×20		0.048	0.15	1,350	EKZE101E□□221ML20S
270	12.5×30		0.042	0.13	1,500	EKZE101E□□271MK30S



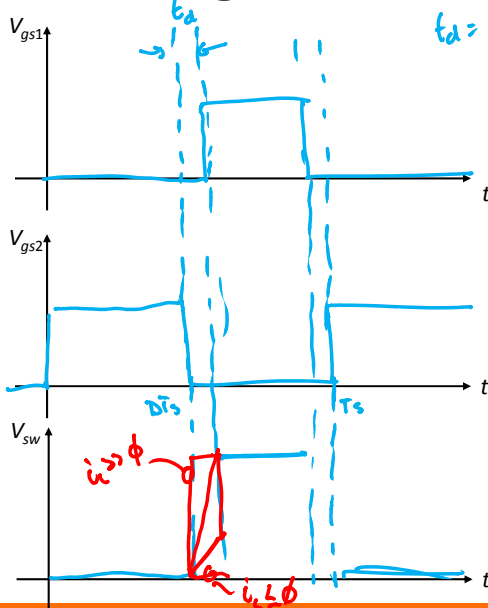
**Dissipation Factor: 1% Max. (25 °C, 1kHz)**

Dissipation Factor (tanδ)	Rated voltage (Vdc)	6.3V	10V	16V	25V	35V	50V	63V	80V	100V
		tanδ (Max)		0.22	0.19	0.16	0.14	0.12	0.10	0.09

When nominal capacitance exceeds 1,000µF, add 0.02 to the value above for each 1,000µF increase. (at 20°C, 120Hz)

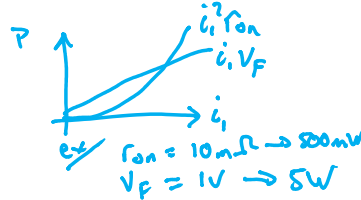
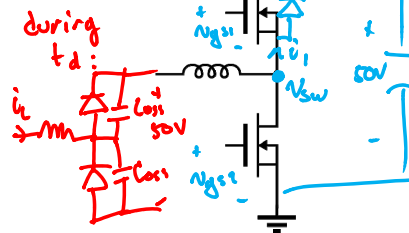
# Switching Loss

## Switching Loss Modeling



$t_d =$  "dead time"

synchronous half-bridge



## Types of Switching Loss

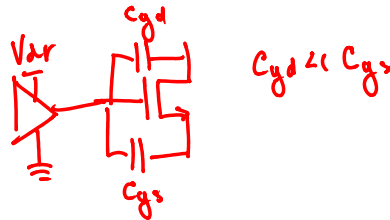
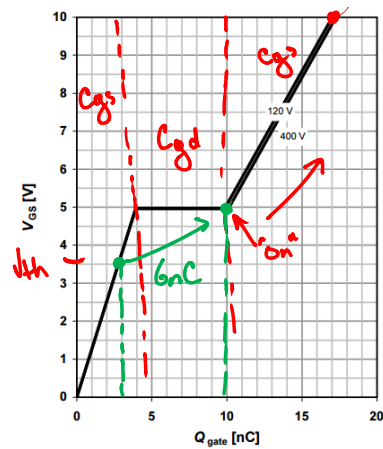
1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. ~~Inductive Losses~~ <sup>Parameter</sup>

## Gate Charge Loss

9 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 5.2 \text{ A pulsed}$

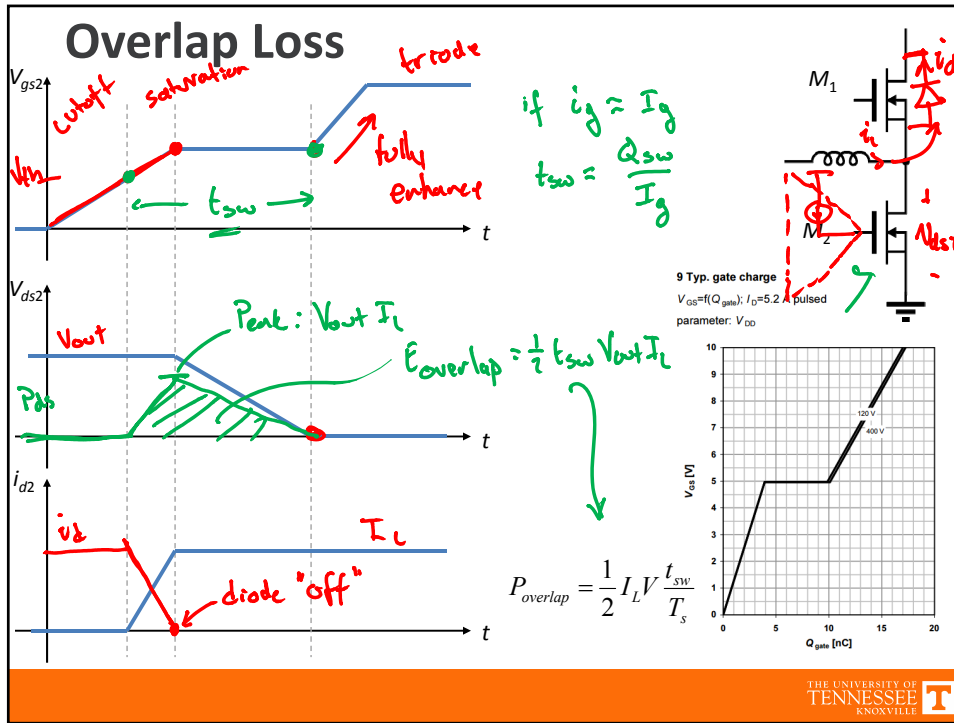
parameter:  $V_{DD}$



$C_{gd} \approx C_{gs}$

$E = Q_g(V_{var}) \cdot V_{var}$

$P_g = Q_g V_{dr} f_s$  <sup>Per device</sup>



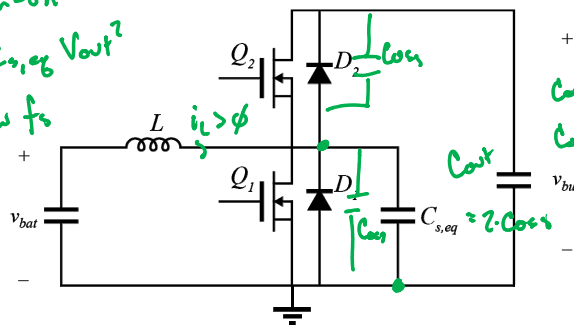
## Lump Switched Node Capacitance

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices

@  $Q_1$  turn-on

$E_{sw} = \frac{1}{2} C_{s,eq} V_{out}^2$

$P_{sw} = E_{sw} f_s$

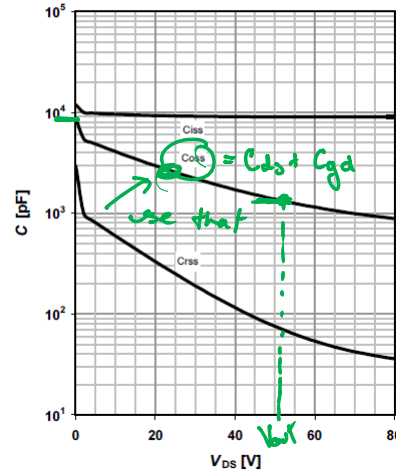


# Device Output Capacitances

$$E_{oss} = \int_0^{V_{max}} v C(v) dv$$

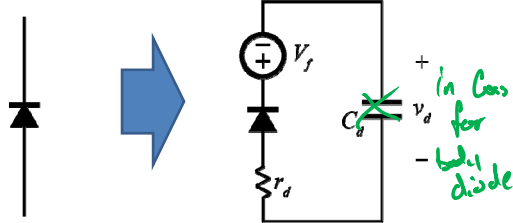
11 Typ. capacitances

$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$



# Diode Loss Model

$$P_{diode, con} = (V_f I + I^2 r_a) t_d \cdot f_s$$



- Example loss model includes resistance and forward voltage drop extracted from datasheet

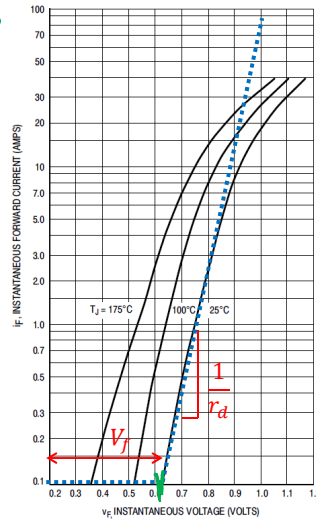
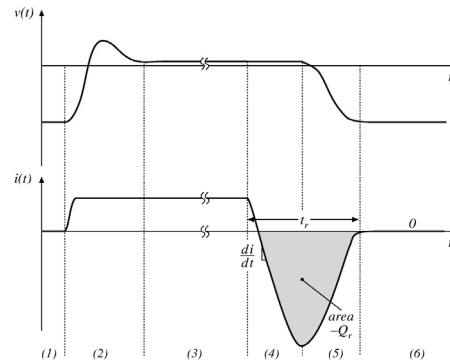


Figure 1. Typical Forward Voltage

## Diode Reverse Recovery

- Diodes will turn on during dead time intervals
- Significant reverse recovery possible on both body diode and external diode



in low-side MOSFET ←  $E_{on,rr} = ((I_L - \Delta i_L)t_{rr} + Q_{rr})V_{bus}$

## Inductor AC Losses



## Inductor Core Loss

- Governed by Steinmetz Equation:

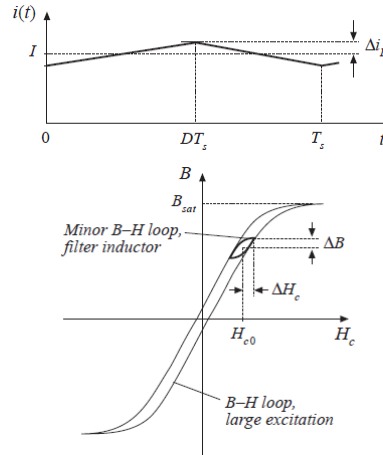
$P_{fe} \uparrow$  w/  $\uparrow \Delta i_L$  &  $\uparrow f_s$

$$P_v = K_{fe} f_s^\alpha (\Delta B)^\beta \quad [\text{mW/cm}^3]$$

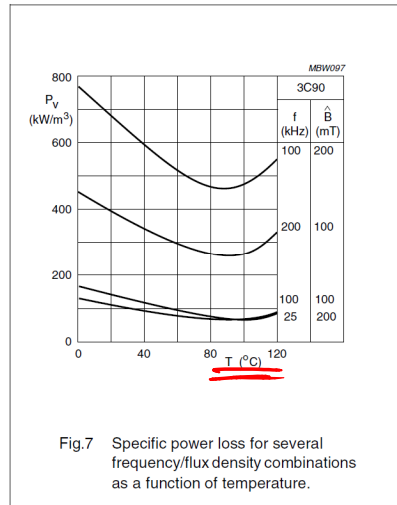
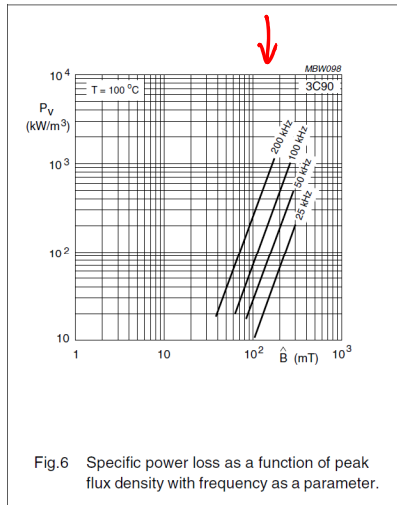
- Parameters  $K_{fe}$ ,  $\alpha$ , and  $\beta$  extracted from manufacturer data

$$P_{fe} = P_v A_c m$$

- $\Delta B \propto \Delta i_L \rightarrow$  small losses with small ripple



## Steinmetz Parameter Extraction



## Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated <sup>(2)</sup> by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \quad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{peak}^y \quad [mW/cm^3]$$

ferrite	f (kHz)	Cm	x	y	ct <sub>2</sub>	ct <sub>1</sub>	ct <sub>0</sub>
3C30	20-100	7.13.10 <sup>-3</sup>	1.42	3.02	3.65.10 <sup>-4</sup>	6.65.10 <sup>-2</sup>	4
	100-200	7.13.10 <sup>-3</sup>	1.42	3.02	4.10 <sup>-4</sup>	6.8.10 <sup>-2</sup>	3.8
3C90	20-200	3.2.10 <sup>-3</sup>	1.46	2.75	1.65.10 <sup>-4</sup>	3.1.10 <sup>-2</sup>	2.45
3C94	20-200	2.37.10 <sup>-3</sup>	1.46	2.75	1.65.10 <sup>-4</sup>	3.1.10 <sup>-2</sup>	2.45
	200-400	2.10 <sup>-9</sup>	2.6	2.75	1.65.10 <sup>-4</sup>	3.1.10 <sup>-2</sup>	2.45
3F3	100-300	0.25.10 <sup>-3</sup>	1.63	2.45	0.79.10 <sup>-4</sup>	1.05.10 <sup>-2</sup>	1.26
	300-500	2.10 <sup>-5</sup>	1.8	2.5	0.77.10 <sup>-4</sup>	1.05.10 <sup>-2</sup>	1.28
	500-1000	3.6.10 <sup>-9</sup>	2.4	2.25	0.67.10 <sup>-4</sup>	0.81.10 <sup>-2</sup>	1.14
3F4	500-1000	12.10 <sup>-4</sup>	1.75	2.9	0.95.10 <sup>-4</sup>	1.1.10 <sup>-2</sup>	1.15
	1000-3000	1.1.10 <sup>-11</sup>	2.8	2.4	0.34.10 <sup>-4</sup>	0.01.10 <sup>-2</sup>	0.67

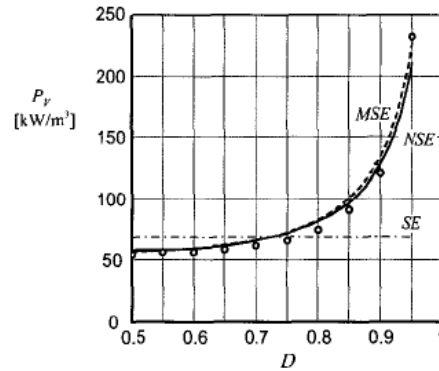
Table 1: Fit parameters to calculate the power loss density



## NSE/iGSE

- More complex empirical loss models exist, and remain valid for non-sinusoidal waveforms
- NSE/iGSE:

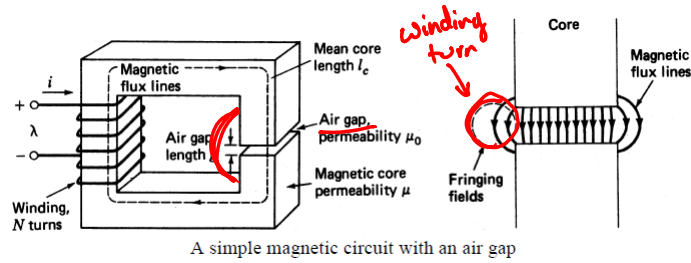
$$P_{NSE} = \left( \frac{\Delta B}{2} \right)^{\beta-\alpha} \frac{k_N}{T} \int_0^{T_1} \left| \frac{dB}{dt} \right|^\alpha dt$$



Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; "Measurement and loss model of ferrites with non-sinusoidal waveforms," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol.6, no., pp. 4814- 4818 Vol.6, 20-25 June 2004 doi: 10.1109/PESC.2004.1354851

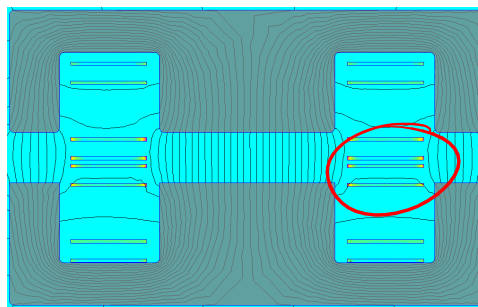


## Fringing



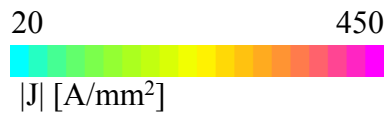
- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors

## Finite Element Simulations

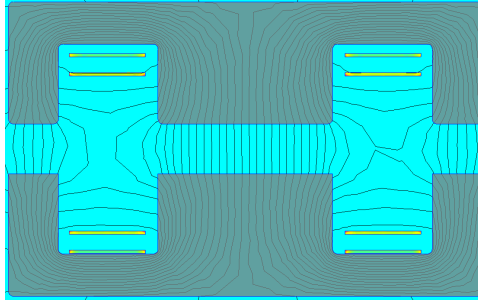


$$P_{cond} = 330 \text{ W}$$

- Design to replace commercial 50nH inductor
- For a two-turn inductor, ER0906 core, 1 mm air gap causes significant fringing
- Large eddy current losses in inner layers
- 4 layers in parallel

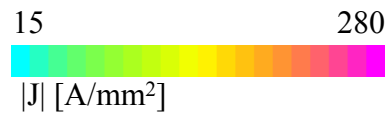


## Removing Copper From Fringing Field



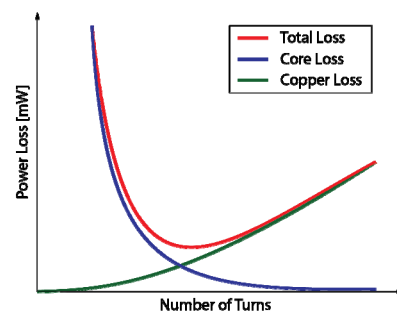
$$P_{cond} = 180 \text{ W}$$

- Removing inner layers entirely reduces loss by about 50% at 1 MHz
- DC resistance doubled, but AC losses decreased significantly



## Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved for



## Spreadsheet Design

The spreadsheet shows the following key parameters and results:

- Input Parameters:**
  - Vg[V]: 25
  - Vout[V]: 50
  - fs [kHz]: 2
  - Pmax[W]: 250
  - L[mH]: 2.00E+0
  - dt [s]: 2
  - Rg\_on[Ω]: 10
  - Rg\_off[Ω]: 2
- Currents and Voltages:**
  - Iout[A]: 5.00
  - I[A]: 10.00
  - imax[A]: 11.25
  - imin[A]: 8.75
  - Irms[A]: 10.03
  - Iq1rms[A]: 7.09
  - Iq2rms[A]: 7.09
  - Ioms[A]: 6.03
  - Vin[V]: 25
  - Vout[V]: 50
  - Vsw\_on[V]: 175
  - Vsw\_off[V]: 35
  - VrDC [mV]: 4.71
  - PLAC [mV]: 10.05
  - PLcopper: 0.48
  - PLcore: 0.08
  - PL [W]: 0.54
  - PL [W]: 2.48
  - PL [W]: 0.44
- Losses and Efficiency:**
  - Total Losses: 3.44
  - Eff: 98.64
- Core and Material Parameters:**
  - Core: ETD49-3C90
  - Core Ac [mm<sup>2</sup>]: 211
  - Core Wa [mm]: 273
  - Core Wb [mm]: 24000
  - Core MLT [mm]: 85
  - Core Material Parameters:
    - μ: 2300
    - Bsat [mT]: 470
    - Cm: 0.0032
    - n: 145
    - ρ: 2.75
    - α: 0.000165
    - αT: 0.031
    - αD: 2.45
- Inductor Design Parameters:**
  - Inductor n: 30
  - Inductor Core: ETD49-3C90
  - Inductor Ac [mm<sup>2</sup>]: 211
  - Inductor Wa [mm]: 273
  - Inductor Wb [mm]: 24000
  - Inductor MLT [mm]: 85
  - Inductor Cmf: 31.25
  - Inductor Design G: 16.64
- Warnings:**
  - Wire significant thicker than one skin depth, AC losses may be significant.

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.



## Matlab (Programmatic) Design

```

1 function [n, lg, Pq1, Pq2, Pl, etc, Cmin] = TestBoostDesign(Fmax, fs, L, dt, core_geom, core_mat, MOSFET)
2 %TestBoostDesign calculate boost converter efficiency and temperature rise
3 %for various designs
4 % fs = switching frequency (in Hz)
5 % L = inductance (in Henries)
6 % n = number of turns on inductor
7 % dt = switching dead time (in seconds)
8 % core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
9 % core_mat = core material, chosen from '3F3', '3C90', or '3F4'
10 % MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
11 % 'CSD' or 'IPPO'
12
13 Vg = 25;
14 Vout = 50;
15 Iout = Fmax/Vout;
16 Ts = 1/fs;
17 D = 1-Vg/Vout;
18 dVout = 2;
19 Vdr = 12;
20
21 Rgon = 10;
22 Rgoff = 2;
23
24 rho = 1.724e-6; %ohms*cm
25 u0 = 4*pi*1e-7;
26
27 %% Inductor Datasheet Parameters
28 switch core_geom
29 case 'EFD25'
30     MLT = 46.4; %mm
31     Ac = 58; %mm^2
32     Ve = 3300; %mm^3
33     Wa = 40.2; %mm^2

```

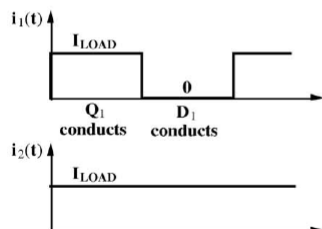
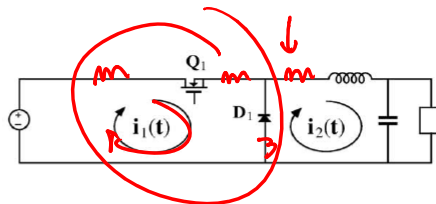
- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation



# Layout

## Power Converter Layout: Buck Example

Use loop analysis

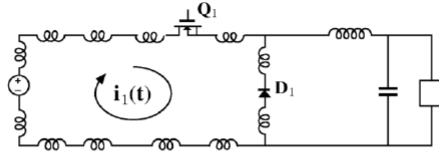


switched input current  $i_1(t)$  contains large high frequency harmonics  
—hence inductance of input loop is critical  
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

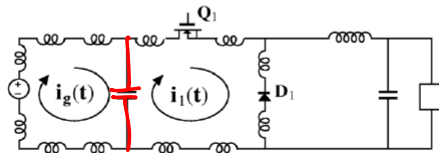
the second loop contains a filter inductor, and hence its current  $i_2(t)$  is nearly dc  
—hence additional inductance is not a significant problem in the second loop

## Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:



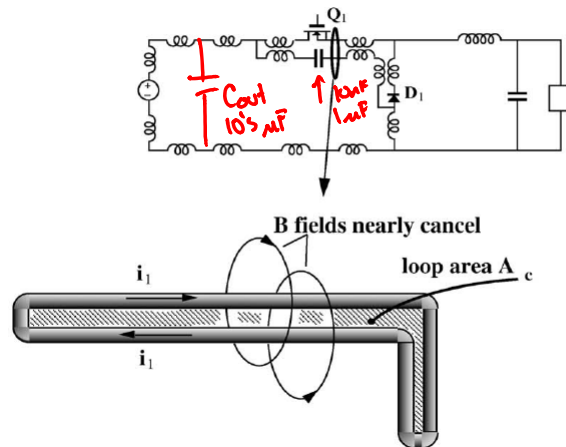
Addition of bypass capacitor confines the pulsating current to a smaller loop:



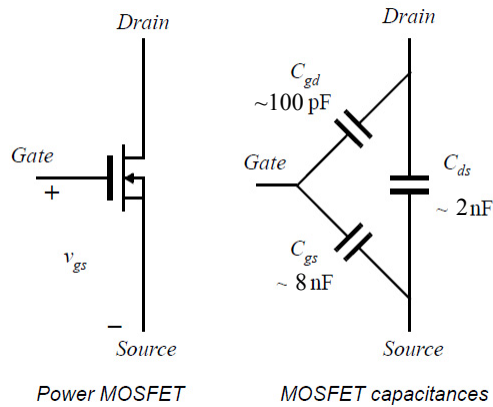
high frequency currents are shunted through capacitor instead of input source

## Loop Minimization

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

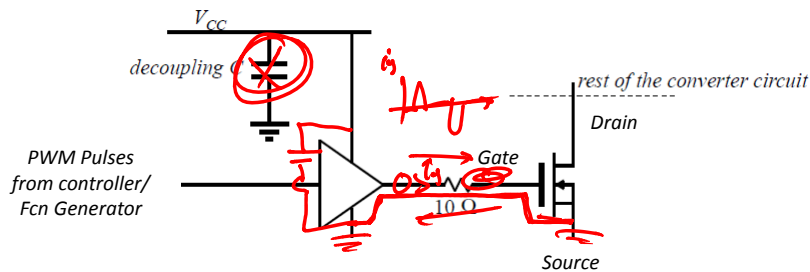


## Driving a Power MOSFET Switch



- MOSFET is off when  $v_{gs} < V_{th} \approx 3 \text{ V}$
- MOSFET fully on when  $v_{gs}$  is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when  $v_{gs} > 20 \text{ V}$ .
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

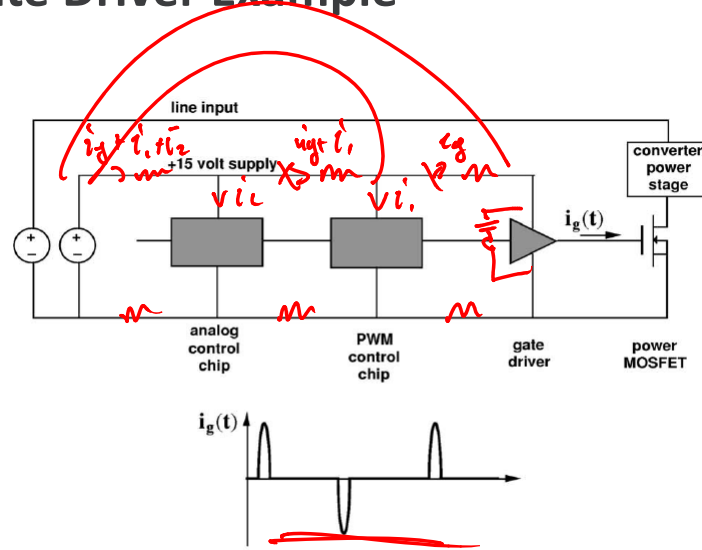
## Driving a Power MOSFET Switch



- MOSFET gate driver is used as a logic buffer with high output current ( $\sim 1.8 \text{ A}$ ) capability
- The amplitude of the gate voltage equals the supply voltage  $V_{CC}$
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow  $dv/dt$  at switch node

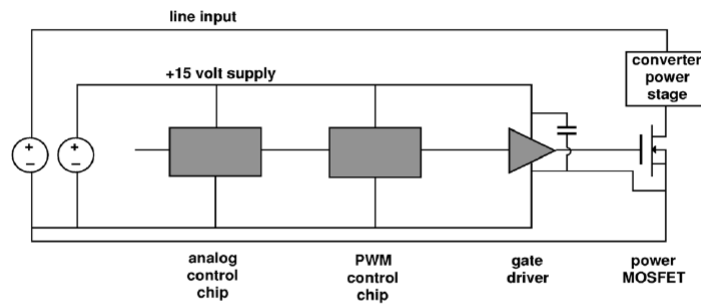


## Gate Driver Example



## Bypass Capacitor Placement

**Solution: bypass capacitor and close coupling of gate and return leads**



High frequency components of gate drive current are confined to a small loop

A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

# Parasitics to be Aware of

