Power Electronics Circuits

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ECE 482 Lecture 3
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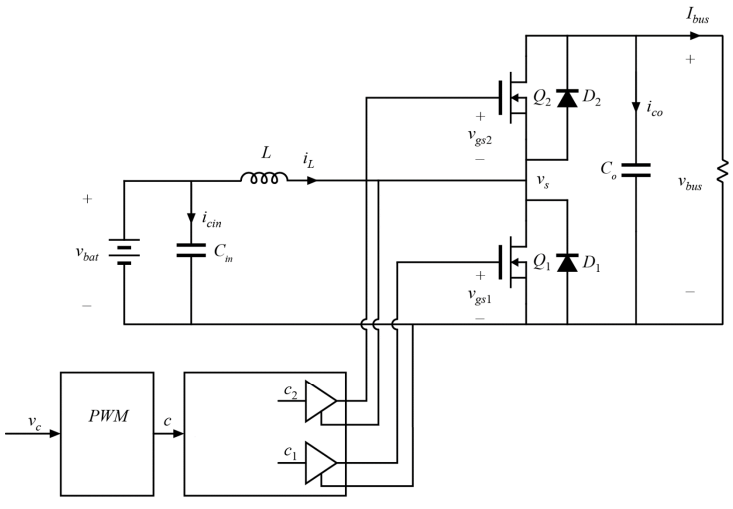
Experiment 3



Prelab Assignment

Experiment 3
ECE 482

Fig. 1 shows the power stage of the drivetrain boost converter to be assembled in experiment 3. For all parts of this prelab, consider operation of the converter at an operating point around which:

- $V_{bat} = 25$ V
- $V_{bus} \leq 50$ V
- $5\text{ kHz} \leq f_s \leq 1\text{ MHz}$
- $\Delta v_{out} \leq 1$V

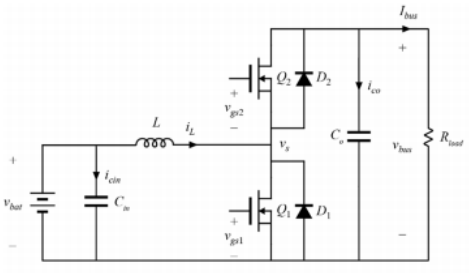


Figure 1: Open loop boost converter (implementation shown with MOSFET devices)

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Design Assessment

In experiment 3, a portion of your grade will be the performance of the design that you choose to build. A 20% segment of the lab grade will be determined by the following formula, which rewards designs with small size, high efficiency, and high power capability:

$$\text{Grade } [\%] = 25 - \kappa_{core} - 100\cdot(0.98 - \eta_{Pout=100}) - \frac{P_{\max} - 250}{50},$$

where

$$\kappa_{core} = \begin{cases} 0, & ETD29 / EFD25 \\ 3, & ETD39 \\ 6, & ETD44 \\ 9, & ETD49 \end{cases}$$

According to the inductor core you have chosen for your design. P_{max} is the maximum power tested, which must be at least 100W, and may be as high as 250W.

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Boost Design

Power Semiconductors

Part No.	Quantity	Description
irfb4615pbf	1	60 V, 195 A, StrongIRFET
AOT2500L	X	150 V, 150 A, High Voltage Trench MOSFET
FDP083N15A	X	150 V, 117 A PowerTrench MOSFET
IPP200N15N3	X	150 V, 50 A OptiMOS Power MOSFET
irfb4615pbf	X	150 V, 35 A HEXFET Power MOSFET
FGPF50N33BT	X	330 V, PDP Trench IGBT
ISL9V3040D	X	400 V, N-Channel IGBT

Core Geometry	Material
ETD29	Ferroxcube 3C90 Ferroxcube 3F3
ETD39	Ferroxcube 3C90 Ferroxcube 3F3
ETD44	Ferroxcube 3C90 Ferroxcube 3F3
ETD49	Ferroxcube 3C90 Ferroxcube 3F3

Wire Gauge	Diameter [cm]
AWG 10	0.267
AWG 12	0.213
AWG 14	0.171
AWG 16	0.137
AWG 20	0.0874

Full AWG table

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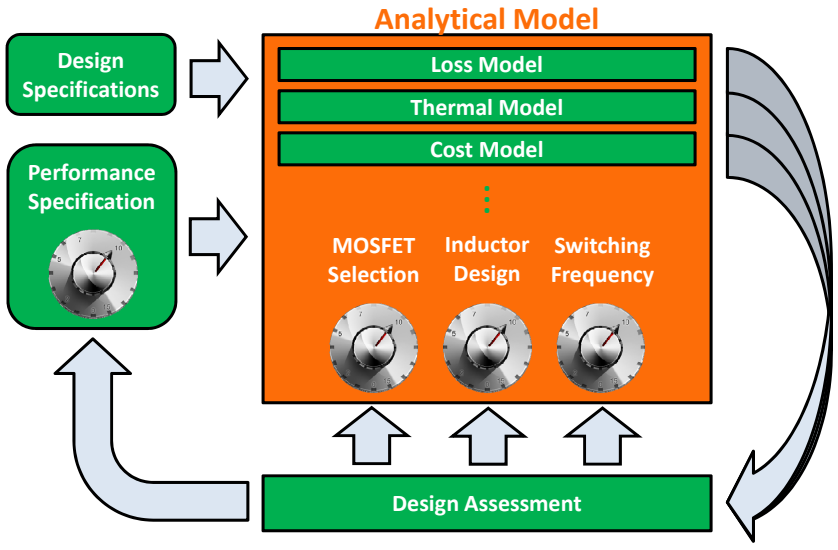
Converter Design



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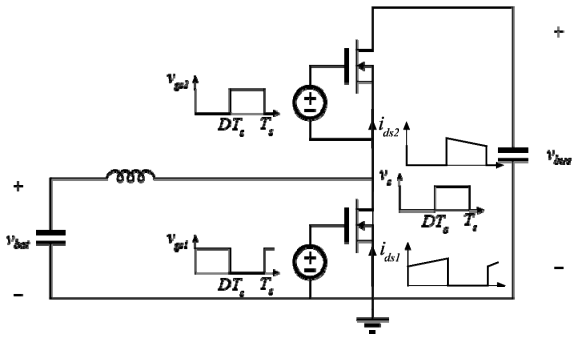
Analytical Loss Modeling

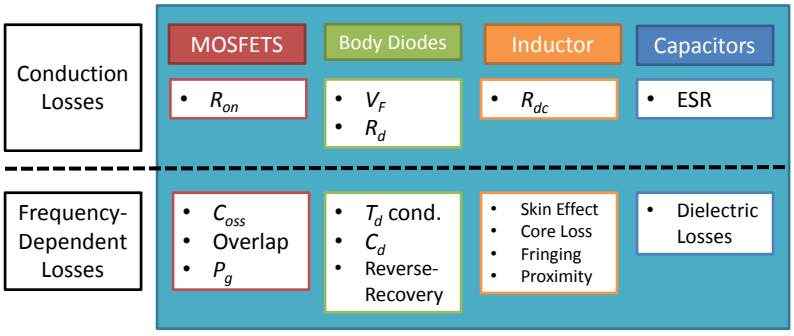
- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
- Argue which losses need to be included, and which may be neglected
  - "Rough" approximation to gain insight into significance

Boost Converter Loss Analysis



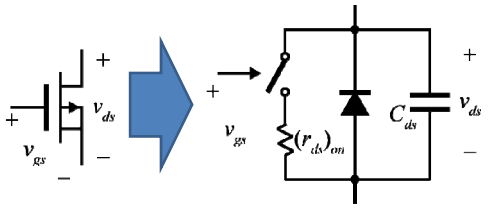
- Begin by solving important waveforms throughout converter assuming lossless operation

Power Stage Losses



Conduction Losses

MOSFET Equivalent Circuit



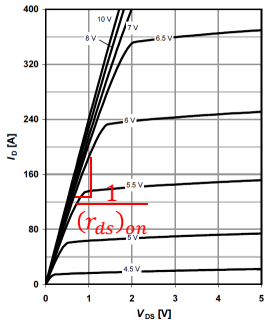
- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

MOSFET On Resistance

5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

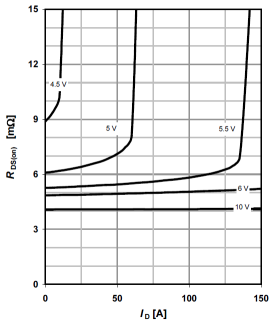
parameter: V_{GS}



6 Typ. drain-source on resistance

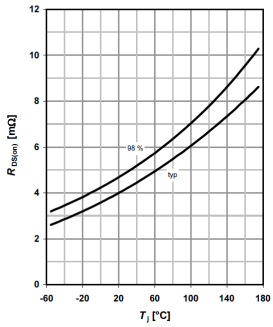
$R_{DS(on)}$=f(I_D); T_j=25 °C

parameter: V_{GS}



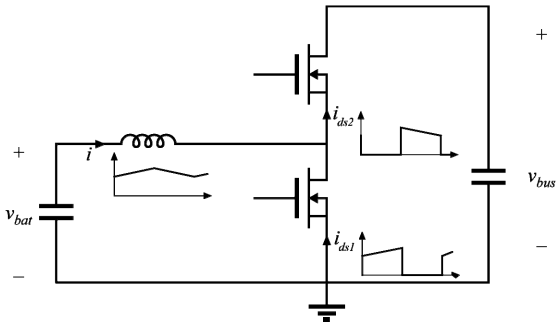
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V



- On resistance extracted from datasheet waveforms
- Significantly dependent on V_{gs} amplitude, temperature

Boost Converter RMS Currents



- MOSFET conduction losses due to $(r_{ds})_{on}$ depend given as

$$P_{cond,FET} = {I_{di,rms}}^2 (r_{ds})_{on}$$

MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

$$rms = I\sqrt{D}\sqrt{1+\frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \qquad \text{(A.6)}$$

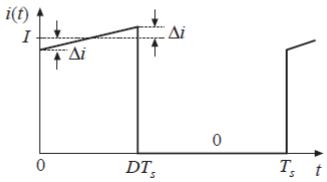
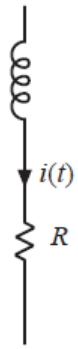


Fig. A.6

- RMS values of commonly observed waveforms appendix from Power Book

DC Inductor Resistance



- DC Resistance given by

$$R_{DC} = \rho \frac{l_b}{A_w}$$

- At room temp, ρ = 1.724·10^{-6} Ω-cm
- At 100°C, ρ = 2.3·10^{-6} Ω-cm
- Losses due to DC current:

$$P_{cu,DC} = {I_{L,rms}}^2 R_{DC}$$

Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

$$rms = I\sqrt{1 + \frac{1}{3}\left(\frac{\Delta i}{I}\right)^2} \qquad \text{(A.2)}$$

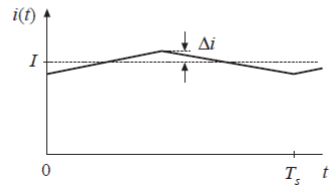
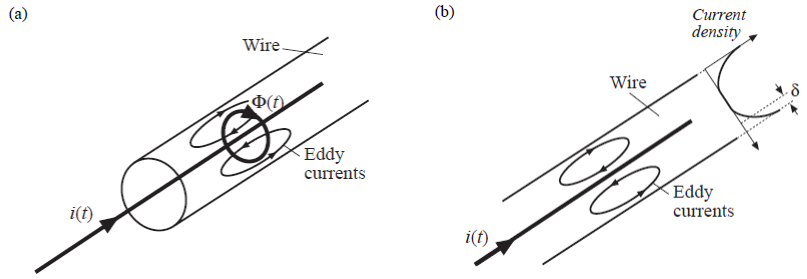


Fig. A.2

- Conduction losses dependent on RMS current through inductor

Skin Effect in Copper Wire



- Current profile at high frequency is exponential function of distance from center with characteristic length δ

Skin Depth

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

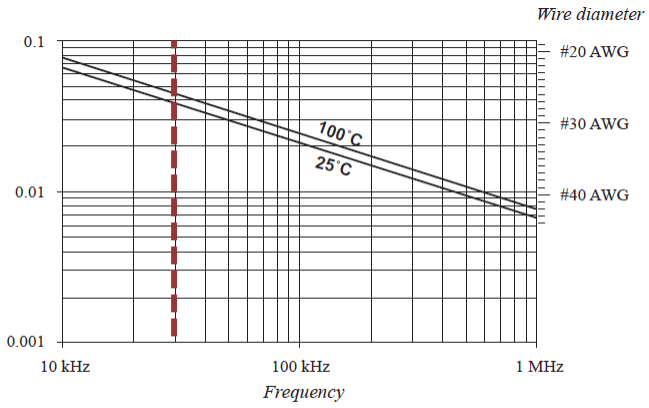
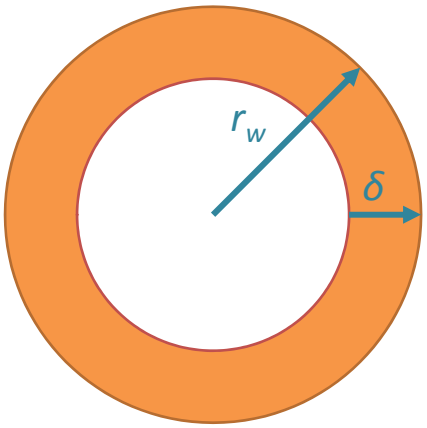


Fig. 13.23 Penetration depth δ, as a function of frequency *f*, for copper wire.

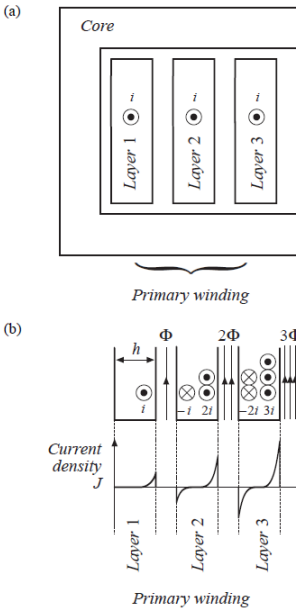
AC Resistance



$$A_{w,eff} = \pi {r_w}^2 - \pi(r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$

Proximity Effect



- In *foil* conductor closely spaced with $h >> \delta$, flux between layers generates additional current according to Lentz's law.

$$P_1 = {I_{L,rms}}^2 R_{ac}$$

- Power loss in layer 2:

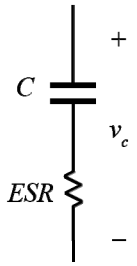
$$P_2 = {I_{L,rms}}^2 R_{ac} + \left(2I_{L,rms}\right)^2 R_{ac}$$

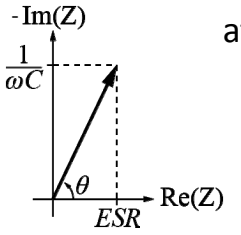
$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

See *Fundamentals of Power Electronics*, Section 13.4

Capacitor Loss Model





- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:

$$\delta = \frac{\pi}{2} - \theta$$

$$D = \tan(\delta)$$

Capacitor ESR Extraction

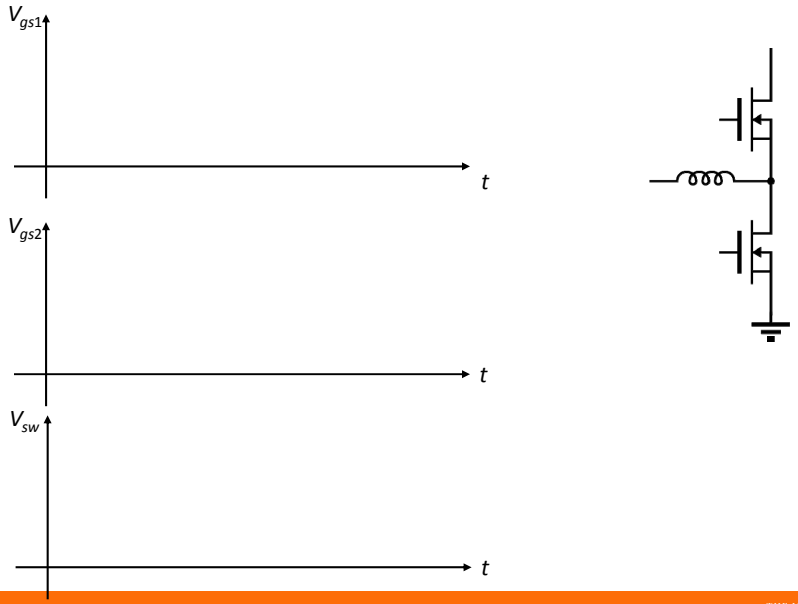
WV (Vdc)	Cap (μF)	Case size φD×L(mm)	Impedance (Ωmax/100kHz) 20℃	Impedance (Ωmax/100kHz) -10℃	Rated ripple current (mArms/105℃, 100kHz)	Part No.
100	6.8	5×11	1.4	5.6	125	EKZE101E□□6R8ME11D
	15	6.3×11	0.57	2.3	205	EKZE101E□□150MF11D
	27	8×11.5	0.36	1.4	355	EKZE101E□□270MHB5D
	39	8×15	0.25	1.0	450	EKZE101E□□390MH15D
	47	10×12.5	0.17	0.66	480	EKZE101E□□470MJC5S
	56	8×20	0.19	0.76	565	EKZE101E□□560MH20D
	68	10×16	0.11	0.47	600	EKZE101E□□680MJ16S
	82	10×20	0.084	0.34	800	EKZE101E□□820MJ20S
	100	12.5×16	0.11	0.34	750	EKZE101E□□101MK16S
	120	10×25	0.069	0.28	900	EKZE101E□□121MJ25S
	150	12.5×20	0.062	0.18	1,100	EKZE101E□□151MK20S
	220	12.5×25	0.047	0.14	1,250	EKZE101E□□221MK25S
	220	16×20	0.048	0.15	1,350	EKZE101E□□221ML20S
	270	12.5×30	0.042	0.13	1,500	EKZE101E□□271MK30S

Dissipation Factor: 1% Max. (25 °C, 1kHz)

Dissipation Factor (tanδ)	Rated voltage (Vdc)	6.3V	10V	16V	25V	35V	50V	63V	80V	100V
	tanδ (Max.)	0.22	0.19	0.16	0.14	0.12	0.10	0.09	0.09	0.08
	When nominal capacitance exceeds 1,000μF, add 0.02 to the value above for each 1,000μF increase. (at 20℃, 120Hz)									

Switching Loss

Switching Loss Modeling



Types of Switching Loss

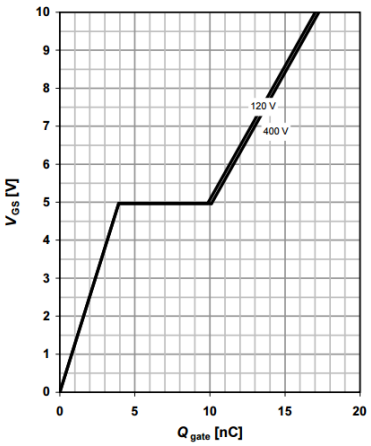
1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Inductive Losses

Gate Charge Loss

9 Typ. gate charge

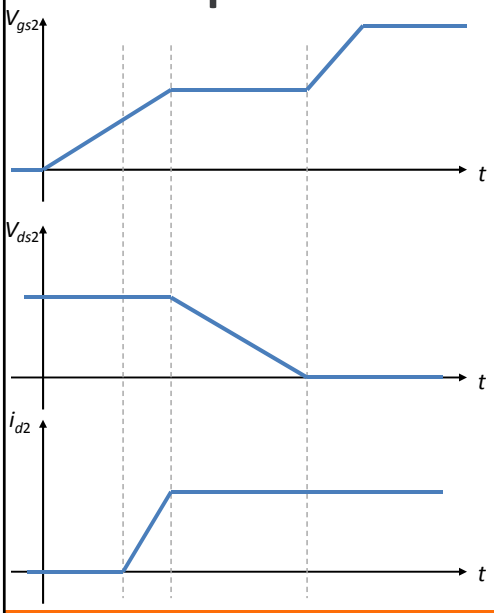
V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

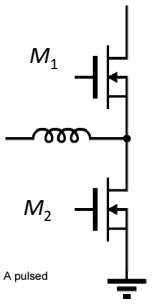
parameter: V_{DD}

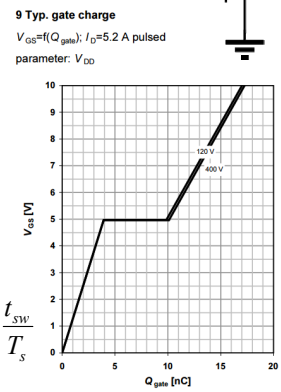


$$P_g = Q_g V_{cc} f_s$$

Overlap Loss



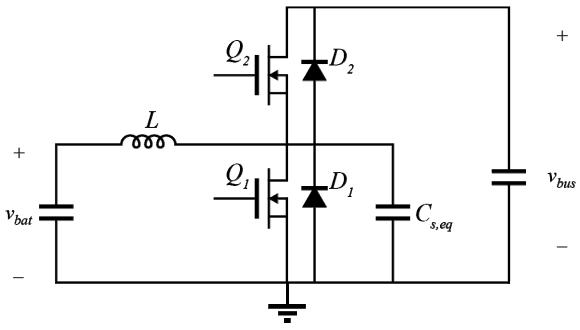




$$P_{overlap} = \frac{1}{2} I_L V \frac{t_{sw}}{T_s}$$

Lump Switched Node Capacitance

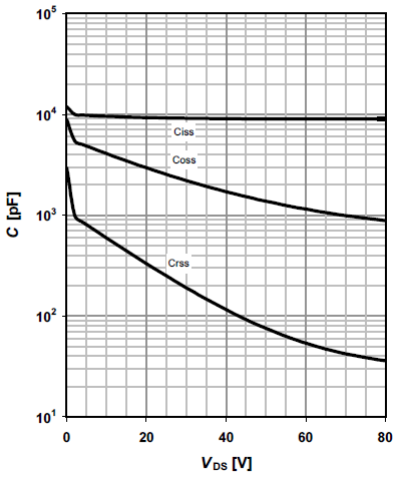
- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices



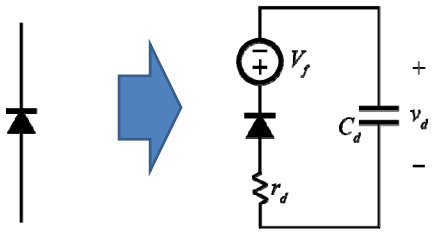
Device Output Capacitances

11 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



Diode Loss Model



- Example loss model includes resistance and forward voltage drop extracted from datasheet

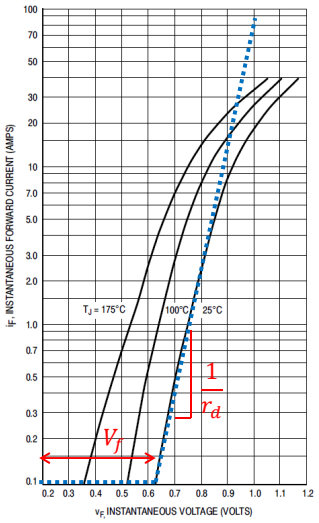
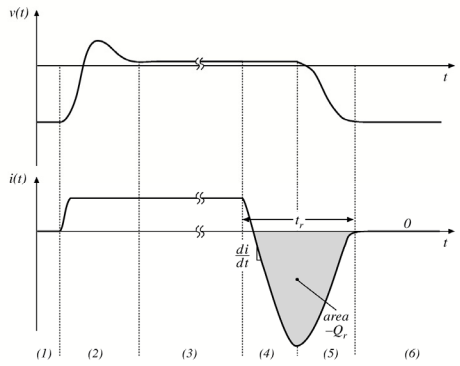


Figure 1. Typical Forward Voltage

Diode Reverse Recovery

- Diodes will turn on during dead time intervals
- Significant reverse recovery possible on both body diode and external diode



$$E_{on,rr} = \left(\left(I_L - \Delta i_L\right)t_{rr} + Q_{rr}\right)V_{bus}$$

Inductor AC Losses

Inductor Core Loss

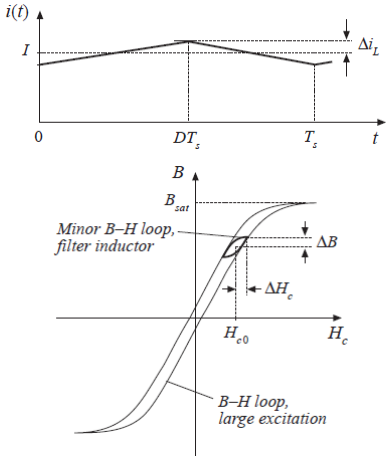
- Governed by Steinmetz Equation:

$$P_v = K_{fe} f_s^{\alpha} (\Delta B)^{\beta} \quad [\text{mW/cm}^3]$$

- Parameters K_{fe}, α, and β extracted from manufacturer data

$$P_{fe} = P_v A_c l_m \text{ [mW]}$$

- $\Delta B \propto \Delta i_L \rightarrow$ small losses with small ripple



Steinmetz Parameter Extraction

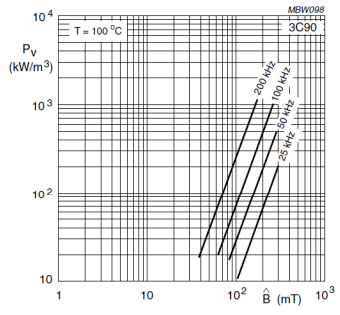


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

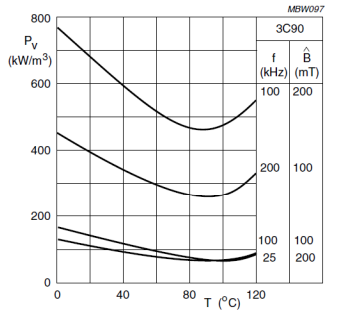


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula :

$$P_{core} = C_m \cdot f^x \cdot B_{peak}^y (ct_0 - ct_1 T + ct_2 T^2) \quad [3]$$

$$= C_m \cdot C_T \cdot f^x \cdot B_{peak}^y \quad [mW/cm^3]$$

ferrite	f (kHz)	Cm	x	y	ct_2	ct_1	ct_0
3C30	20-100	$7.13.10^{-3}$	1.42	3.02	$3.65.10^{-4}$	$6.65.10^{-2}$	4
	100-200	$7.13.10^{-3}$	1.42	3.02	4.10^{-4}	$6.8.10^{-2}$	3.8
3C90	20-200	$3.2.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3C94	20-200	$2.37.10^{-3}$	1.46	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
	200-400	2.10^{-9}	2.6	2.75	$1.65.10^{-4}$	$3.1.10^{-2}$	2.45
3F3	100-300	$0.25.10^{-3}$	1.63	2.45	$0.79.10^{-4}$	$1.05.10^{-2}$	1.26
	300-500	2.10^{-5}	1.8	2.5	$0.77.10^{-4}$	$1.05.10^{-2}$	1.28
	500-1000	$3.6.10^{-9}$	2.4	2.25	$0.67.10^{-4}$	$0.81.10^{-2}$	1.14
3F4	500-1000	12.10^{-4}	1.75	2.9	$0.95.10^{-4}$	$1.1.10^{-2}$	1.15
	1000-3000	$1.1.10^{-11}$	2.8	2.4	$0.34.10^{-4}$	$0.01.10^{-2}$	0.67

Table 1: Fit parameters to calculate the power loss density

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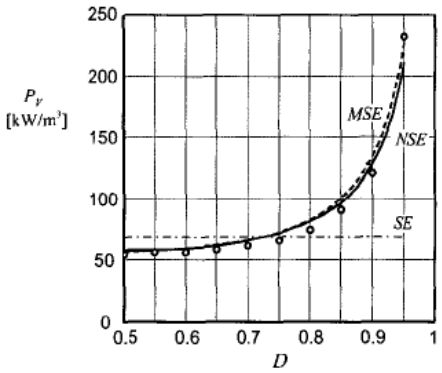
NSE/iGSE

- More complex empirical loss models exist, and remain valid for non-sinusoidal waveforms
- NSE/iGSE:

$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt$$



Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; , "Measurement and loss model of ferrites with non-sinusoidal waveforms," *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual* , vol.6, no., pp. 4814- 4818 Vol.6, 20-25 June 2004 doi: 10.1109/PESC.2004.1354851

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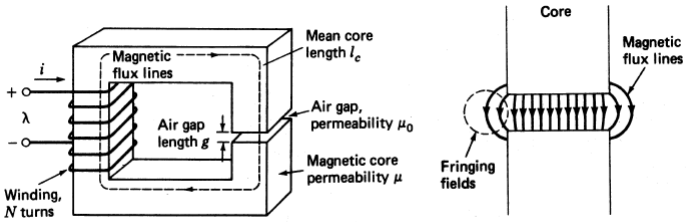
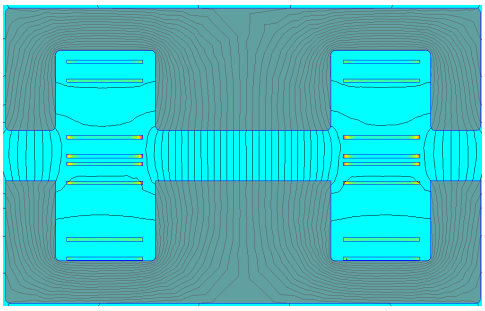
Fringing



A simple magnetic circuit with an air gap

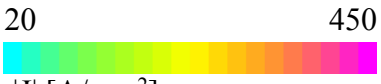
- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors

Finite Element Simulations

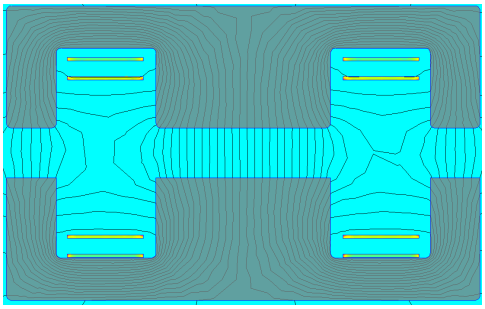


$P_{cond} = 330$ W

- Design to replace commercial 50nH inductor
- For a two-turn inductor, ER0906 core, 1 mm air gap causes significant fringing
- Large eddy current losses in inner layers
- 4 layers in parallel



Removing Copper From Fringing Field



$P_{cond} = 180$ W

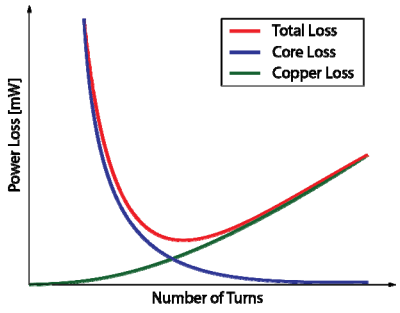
- Removing inner layers entirely reduces loss by about 50% at 1 MHz
- DC resistance doubled, but AC losses decreased significantly

15 280

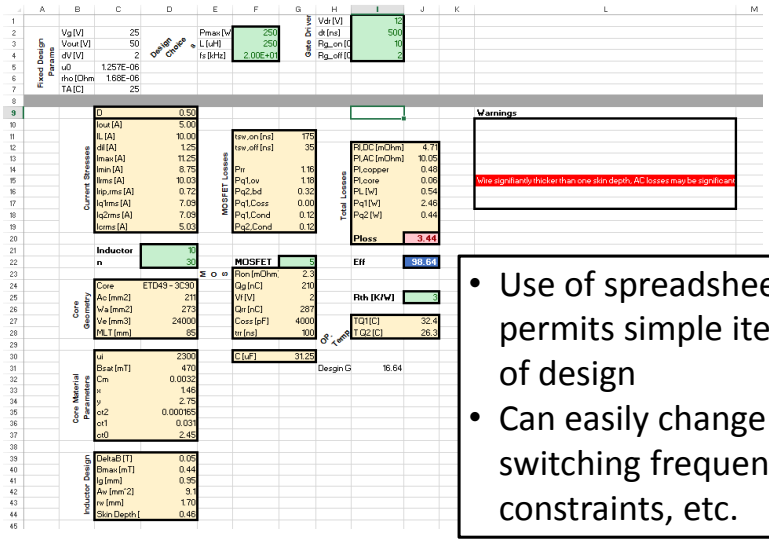
|J| [A/mm^2]

Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved for



Spreadsheet Design



- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

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Matlab (Programmatic) Design

```
function [n, lg, Pq1, Pq2, Pl, eta, Cmin ] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
%TestBoostDesign calculate boost conveter efficiency and temperature rise
%for various designs
%   fs  = switching frequency (in Hz)
%   L = inductance (in Henries)
%   n = number of turns on inductor
%   dt = switching dead time (in seconds)
%   core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
%   core_mat = core material, chosen from '3F3', '3C90', or '3F4'
%   MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
%   'CSD' or 'IPP0'

Vg = 25;
Vout = 50;
Iout = Pmax/Vout;
Ts = 1/fs;
D = 1-Vg/Vout;
dVout = 2;
Vdr = 12;

Rgon = 10;
Rgoff = 2;

rho = 1.724e-6; %ohms*cm
u0 = 4*pi*1e-7;

%% Inductor Datasheet Parameters
switch core_geom
    case 'EFD25'
        MLT = 46.4; %mm
        Ac = 58; %mm^2
        Ve = 3300; %mm^3
        Wa = 40.2; %mm^2
```

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

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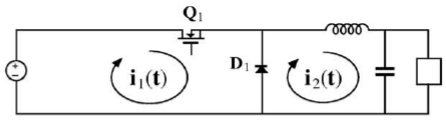
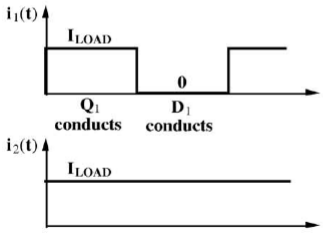
Layout

Power Converter Layout: Buck Example

Use loop analysis





switched input current $i_1(t)$ contains large high frequency harmonics

—hence inductance of input loop is critical

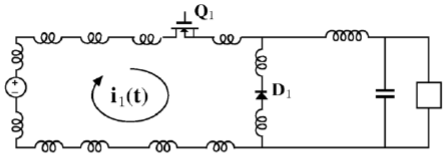
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc

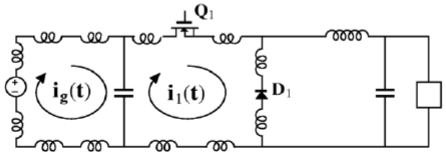
—hence additional inductance is not a significant problem in the second loop

Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:



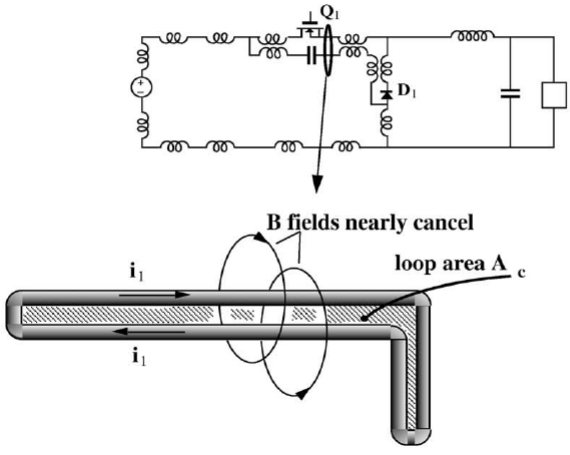
Addition of bypass capacitor confines the pulsating current to a smaller loop:



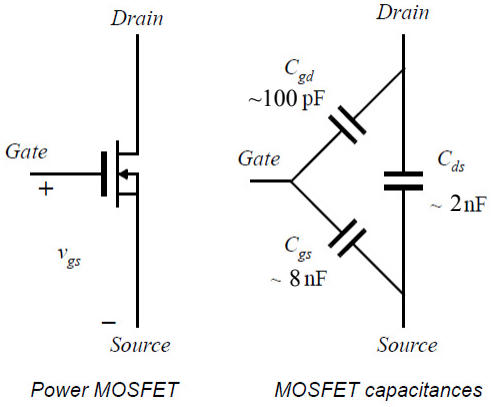
high frequency currents are shunted through capacitor instead of input source

Loop Minimization

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

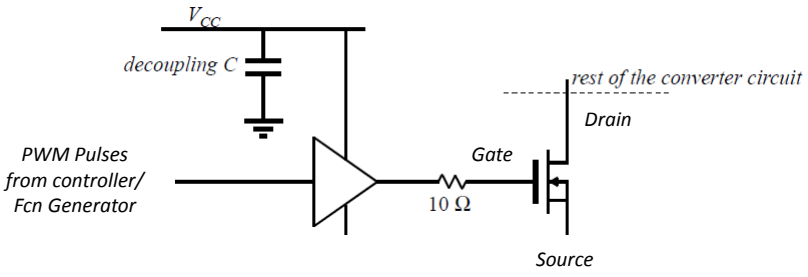


Driving a Power MOSFET Switch



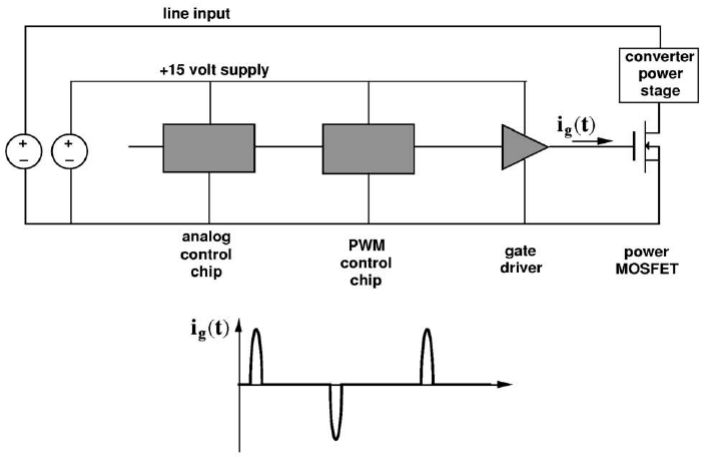
- MOSFET is off when $v_{gs} < V_{th} \approx$ 3 V
- MOSFET fully on when v_{gs} is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when $v_{gs} > 20$ V.
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

Driving a Power MOSFET Switch



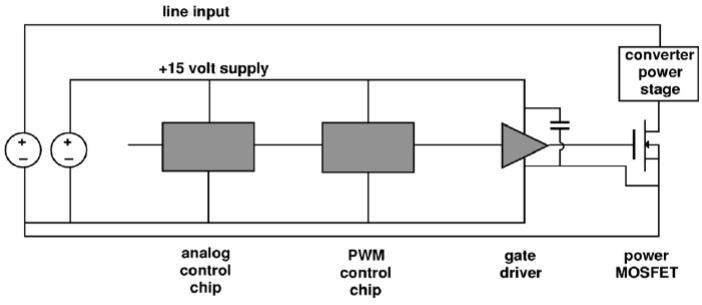
- MOSFET gate driver is used as a logic buffer with high output current (~1.8 A) capability
- The amplitude of the gate voltage equals the supply voltage *VCC*
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow dv/dt at switch node

Gate Driver Example



Bypass Capacitor Placement

Solution: bypass capacitor and close coupling of gate and return leads



- High frequency components of gate drive current are confined to a small loop
- A dc component of current is still drawn output of 15V supply, and flows past the control chips. Hence, return conductor size must be sufficiently large

Parasitics to be Aware of