# Experiment 4
Closed Loop Boost Converter Operation
ECE 482

The objectives of this experiment are:

- To design current and voltage control loops and compensators for the boost converter constructed in Experiment 3
- To become familiar with dynamic and frequency response characteristics of power converters
- To understand small- and large-signal behaviors of closed-loop power converters

Before beginning the experiment, discuss your prelab with all members of your group, and arrive at a decision on how to set and select the various operating modes of the LM5121 for your application.
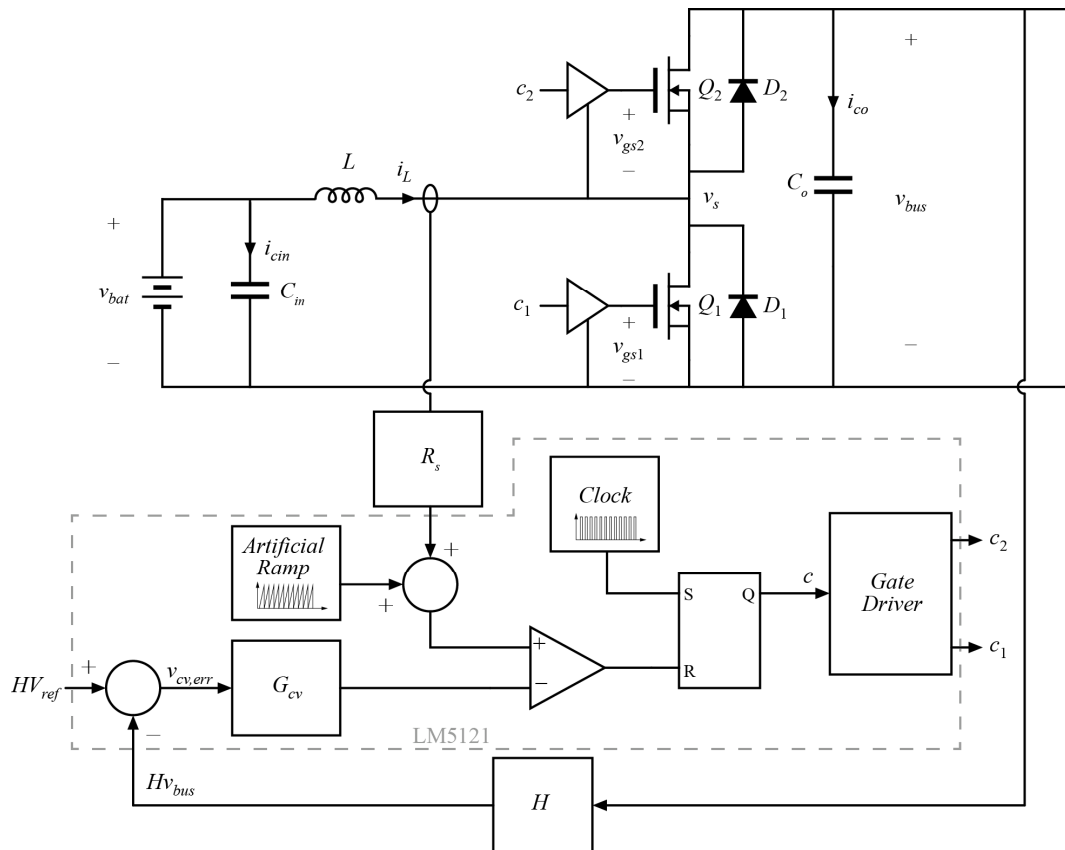
Figure 1: Closed-loop CPM boost converter

I. Averaged Switch Modeling and Simulation in LTSpice

Beginning with your compensator designs from the prelab, simulate the closed-loop boost converter in LTspice. Verify stability of your proposed feedback loop through time domain

simulations, across operating powers from 0-150 W and output voltages in the range $25 < V_{bus} < 50$ V. Use frequency domain simulations to verify converter and compensator transfer functions and loop gains. Include basic models of important loss mechanisms from Experiment 3, and refine your compensator design as necessary to obtain desirable closed-loop behavior. Show the results of this verification in your lab report. Discuss how, if at all, the inclusion of loss mechanisms has altered the transfer functions, and whether or not the simulation of all operating points required a change in compensator transfer function from your original perlab-based design.

II.   Switching Model Simulation in LTSpice

Using the internal model of the LM5121 in LTSpice, or the manufacturer-provided model in PSpice, run a subset of simulations to verify that startup, overcurrent, and other non-averaged proper behavior in your intended circuit configuration with the LM5121 chip.

Test a step change in load resistance at the following operating point and document the results.

$$V_g = 25 \text{ V} \qquad\qquad V_{out} = 50 \text{ V} \qquad\qquad R_{load} = 50 \text{ } \Omega \text{ to } 25 \text{ } \Omega$$

Compare the behavior of this simulation to that of your averaged model. If they are not well matched, diagnose and report on the source of the discrepancy. You will later test this same step in hardware.

III.   Open-Loop LM5121 Implementation in Hardware

Decide whether your group would like to use the internal gate driver of the LM5121, eliminating the UCC27211A gate driver from the previous experiment, or continue to use the UCC27211A. Using an external gate driver will introduce additional delay (slightly harming the performance of CPM control) but will protect the LM5121 from power stage transients and allow minimal change in steady-state efficiency from the previous experiment.
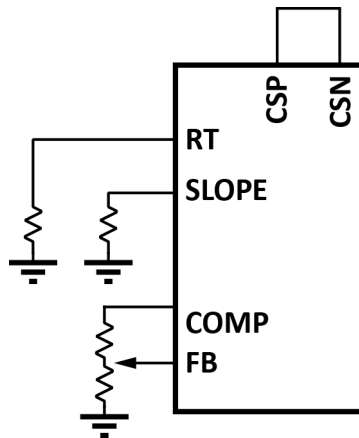
Figure 2: Open-loop duty-cycle controlled modulator connections.

Begin by testing in open-loop to make sure that proper operation is achieved. Note that, in this step we are "tricking" the LM5121 control chip into operating in open-loop, which it is not normally used for, in order to make sure basic functions are working before going to closed-loop operation.

Open loop operation can be achieved, for example, by shorting CSP and CSN so that the sensed current is zero. Then, the "artificial ramp" will behave as a sawtooth wave for the PWM modulator, with the RT and SLOPE pins setting the frequency and amplitude, respectively. Implementing a resistor divider between the COMP and FB pins, as shown in Fig. 2, will allow you to set a comparison threshold to set the duty cycle. Note that other connections will need to be made in addition to those shown explicitly in Fig. 2. Be aware of limits on the artificial ramp voltage, and other signals, shown in the datasheet block diagram. The LM5121 will not begin modulation of the proper voltages are not seen on the DS and DG pins.

Before connecting to the power stage, verify that you are able to produce gate drive signals at your selected operating frequency with controllable duty cycle in open loop. Once this has been verified, connect the power stage and test operation, still in open-loop. With an output voltage of 50 V, measure the efficiency of the converter using the LM5121 in open-loop and compare to your results from Experiment 3. Discuss any discrepancies in your report.

IV. Closed-Loop Implementation

Implement closed-loop operation in two steps. First, implement the current loop and test to ensure it is functioning as expected and able to regulate current to a reference. Once the current loop functionality is verified, move on to closing the voltage loop.

a. Current Loop

Using the current sense resistor from your lab kit, implement the CPM control of the inductor current, but retain the open-loop setting of the current reference as in the previous step. Ensure that, by adjusting the resistor divider ratio, you are able to control the input current as expected. For this test, it may be easiest to configure the output electronic load as a voltage sink; in any event, make sure that you consider the output voltage and current that will result from the input current setting.
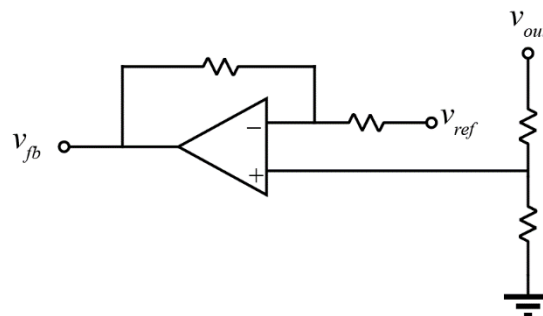
Figure 3: Voltage loop reference circuit.

b. Voltage Loop

Once you are convinced that the CPM loop is operating as expected, implement the closed-loop voltage control. Using an op-amp, incorporate an analog voltage reference which determines the setpoint of the voltage control loop. An example is shown in Fig. 3. In the final system, v_{ref} will be generated using a PWM output from the MSP and appropriate R-C filtering. It is not necessary to include this functionality in Experiment 4; v_{ref} may be derived from a voltage source and/or resistor divider.

Using the electronic load, test the step response that you simulated in Section II experimentally. Measure and record the output voltage and inductor current waveforms. Compare the simulation and experimental results in your lab report, discussing any differences.

Measure the load regulation of your closed-loop boost converter between output powers of 50 W and P_{max}. With a constant voltage reference, load regulation is defined as the percent change in the *average* output voltage over the specified load range

$$\frac{\Delta V}{V} = \frac{V_{max} - V_{min}}{V_{nom}} \times 100\%$$

V_{max}, V_{min}, and V_{nom} are the DC values of the output voltage at P_{max}, 50W, and the ideal commanded reference value, respectively. Note that this is not the high frequency ripple. If the closed-loop gain at DC and low frequencies is very large, then the closed-loop regulation should be very good, i.e., very close to 0%. Include the measured value in your report. Also measure the line regulation of your boost converter for V_{bat} varied from 20 to 30 V, all with $P_{out} = 100$ W, again using the above formula.