Simulation Modeling

Circuit Simulation

- LTSpice
  - Other tools accepted, but not supported
- Choose model type (switching, averaged, dynamic)
- Supplement analytical work rather than repeating it
- Show results which clearly demonstrate what matches and what does not with respect to experiments (i.e. ringing, slopes, etc.)
LTSpice Modeling Examples

- Example files added to course materials page
  - Custom model
  - VDMOS model
  - Manufacturer Model

Custom Transistor Model

```plaintext
.model myD D(n=.001)
.model mySw SW(Ron=10m Roff=1G Von=1 Voff = .5 )
```
VDMOS Model

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Unit</th>
<th>INFALL</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vto</td>
<td>Threshold voltage</td>
<td>V</td>
<td>0</td>
<td>1.0</td>
</tr>
<tr>
<td>Kp</td>
<td>Transconductance parameter</td>
<td>A/V²</td>
<td>1.</td>
<td>1.5</td>
</tr>
<tr>
<td>Fhi</td>
<td>Surface inversion potential</td>
<td>V</td>
<td>0.6</td>
<td>0.65</td>
</tr>
<tr>
<td>LDDBA</td>
<td>Channel-length modulation</td>
<td>1/V</td>
<td>0.</td>
<td>0.02</td>
</tr>
<tr>
<td>ntriode</td>
<td>Conductance multiplier in triode region</td>
<td>-</td>
<td>1.</td>
<td>2.</td>
</tr>
<tr>
<td>subthres</td>
<td>Current (per volt) for switching from square law to flat response in subthreshold region</td>
<td>A/V</td>
<td>0.</td>
<td>1n</td>
</tr>
<tr>
<td>BV</td>
<td>Vds breakdown voltage</td>
<td>V</td>
<td>Inf.</td>
<td>40</td>
</tr>
<tr>
<td>IMY</td>
<td>Current at Ybar</td>
<td>A</td>
<td>100μA</td>
<td>1μ</td>
</tr>
<tr>
<td>NEV</td>
<td>Vds breakdown emission coefficient</td>
<td>-</td>
<td>1.</td>
<td>10</td>
</tr>
<tr>
<td>Rd</td>
<td>Drain-channel resistance</td>
<td>Ω</td>
<td>0.</td>
<td>1.</td>
</tr>
<tr>
<td>Rn</td>
<td>Source-channel resistance</td>
<td>Ω</td>
<td>0.</td>
<td>1.</td>
</tr>
<tr>
<td>Rg</td>
<td>Gate-ohmic resistance</td>
<td>Ω</td>
<td>0.</td>
<td>2.</td>
</tr>
<tr>
<td>Rds</td>
<td>Drain-source sheet resistance</td>
<td>Ω</td>
<td>Inf.</td>
<td>100Ω</td>
</tr>
<tr>
<td>Mh</td>
<td>Body diode channel resistance</td>
<td>Ω</td>
<td>0.</td>
<td>0.5</td>
</tr>
<tr>
<td>Cto</td>
<td>Parasitic body diode capacitance</td>
<td>f</td>
<td>0.</td>
<td>1n</td>
</tr>
</tbody>
</table>

http://ltwiki.org/LTspiceHelp/LTspiceHelp/M_MOSFET.htm

• Note: any other parameters ignored
  • E.g. ron = 3m Qg = 1n mfg = Infineon

Manufacturer Device Model

• Text-only netlist model of device including additional parasitics and temperature effects
• May slow or stop simulation if timestep and accuracy are not adjusted appropriately
Full Switching Simulation

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rss=10m Rbr=17m Kp=30 Cgdmax=5p Cgdmix=5m Cgs=2n Cjox=0.3n Is=88p)
.lib switch.lib
.tran 1
.ic V(out)y0
.ic I(L)0
.out

Full Switching Simulation

.model myMOS VDMOS(Rg=1 Vto=4.5 Rd=14m Rss=10m Rbr=17m Kp=30 Cgdmax=5p Cgdmix=5m Cgs=2n Cjox=0.3n Is=88p)
.lib switch.lib
.tran 1
.ic V(out)y0
.ic I(L)0
.out
Full Switching Model

- Gives valuable insight into circuit operation
  - Understand expected waveforms
  - Identify discrepancies between predicted and experimental operation
- Slow to simulate; significant high frequency content
- Cannot perform AC analysis

Available on Exp 3 Webpage
Averaged Switch Modeling: Motivation

- A large-signal, nonlinear model of converter is difficult for hand analysis, but well suited to simulation across a wide range of operating points
- Want an averaged model to speed up simulation speed
- Also allows linearization (AC analysis) for control design

Nonlinear, Averaged Circuit

\[
L \frac{d\langle i_L \rangle}{dt} = \langle v_{\text{bus}} \rangle - (1 - d)\langle v_{\text{bus}} \rangle
\]

\[
C \frac{d\langle v_{\text{bus}} \rangle}{dt} = (1 - d)\langle i_L \rangle - \langle i_{\text{bus}} \rangle
\]
Implementation in LTSpice

\[ \langle v_1(t) \rangle_T = d(t) \langle v_2(t) \rangle_T \]
\[ \langle i_2(t) \rangle_T = d(t) \langle i_1(t) \rangle_T \]

Averaged Switch Model
What known error(s) will be present in loss predictions with this model?

Experiment 4
Experiment 4: Closed-Loop Boost

Experiment 3: Open Loop

Experiment 4: Closed Loop

Current Control

Current Controller:
Regulate $i_L(t) = \text{control input}$
Current Programmed Control (CPM)

CPM Voltage Loop

Today: set $R_P = 1, \# = 1$

The peak transistor current replaces the duty cycle as the converter control input.
**Current Programmed Control**

- Covered in Ch. 12 of *Fundamentals of Power Electronics*
- Advantages of current programmed control:
  - Simpler dynamics — inductor pole is moved to high frequency
  - Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
  - Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$
  - It is always necessary to sense the transistor current, to protect against overcurrent failures
  - Transformer saturation problems in bridge or push-pull converters can be mitigated
- A disadvantage: susceptibility to noise

**A Simple First-Order Model**

![Diagram of a simple first-order model](image)
The First-Order Approximation

\[ \langle i_L(t) \rangle_{T_s} = i_c(t) \]

- Neglects switching ripple
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small)
- Accurate when artificial ramp (discussed later) is small
- Resulting small-signal relation:

\[ i_L(s) \approx i_c(s) \]
Averaged, Nonlinear Model

\[ i_c(t) \approx i_e(t) \]

\[ v_i, i_e = P(t) \]

Large-Signal Nonlinear Model
Implementation in LTSpice

Averaged, Small-Signal Model

\[
sc \hat{u} = \frac{-I_L}{V} \left( sc \hat{e} - \frac{\hat{u}}{R} + b' \hat{v} \right) + b' \hat{e} - \frac{\hat{v}}{R}
\]

Substitute: \( I_L = \frac{V}{R_D} \) and \( V = \frac{V_o}{D} \)

\[
sc \hat{u} = \frac{-\frac{V}{R_D}}{\frac{V_o}{D}} \left( sc \hat{e} - \frac{\hat{u}}{R} + b' \hat{v} \right) + b' \hat{e} - \frac{\hat{v}}{R}
\]

\[
= sc \hat{u} = \hat{e} \left( \frac{\hat{v}}{R_D} \right) + \frac{\hat{v}}{R_D} - \frac{\hat{v}}{R} - \frac{\hat{v}}{R}
\]

\[
\hat{c} (\frac{\hat{v}}{R_D})
\]

control input
Boost CCM CPM Small-Signal Model

\[ G_{vc} = \frac{\Delta V_c}{\Delta V_o} \approx \frac{1}{g_{m}} \]

\[ \Delta V_c = \frac{D}{D R} (1 - \frac{\Delta L}{D R}) (R \parallel R) \parallel \frac{1}{s C} \]

\[ G_{vc} = \frac{b R}{2} \left( \frac{1 - \frac{\Delta L}{b R}}{1 + \frac{b C}{2}} \right) \]

same RHP zero as in \( D \)-control

single pole!

CPM Transfer Functions

Fig. 12.28: Comparison of CPM control with duty-cycle control, for the control-to-output frequency response of the buck converter example.
Voltage Control

CPM Oscillations for D>0.5

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology.
- Controller can be stabilized by addition of an artificial ramp.
Inductor Current Waveform in CCM

Inductor current slopes $m_1$ and $-m_2$

- buck converter
  \[ m_1 = \frac{v_s - v}{L} \quad -m_2 = \frac{-v}{L} \]

- boost converter
  \[ m_1 = \frac{v_s}{L} \quad -m_2 = \frac{v_s - v}{L} \]

- buck-boost converter
  \[ m_1 = \frac{v_s}{L} \quad -m_2 = \frac{v}{L} \]

Introducing a Perturbation
Change in Inductor Current Over $T_s$

- Magnified view

Steady-state waveform

Perturbed waveform

$\hat{i}_L(0) = m_1 \Delta T_s$

$\hat{i}_L(T_s) = m_2 \Delta T_s$

$\hat{i}_L(T_s) = \hat{i}_L(0) \left( -\frac{m_2}{m_1} \right)$

$\hat{i}_L(2T_s) = \hat{i}_L(T_s) \left( -\frac{m_2}{m_1} \right) = \hat{i}_L(0) \left( -\frac{m_2}{m_1} \right)^2$

$\hat{i}_L(nT_s) = \hat{i}_L(0) \left( -\frac{m_2}{m_1} \right)^n$

Convergence?

Yes $i_f$

$\frac{m_2}{m_1} < 1 \Rightarrow D < 0.5$

Final Value of Inductor Current
Example: Unstable operation for $D=0.6$

\[ \alpha = -\frac{D}{D'} = \left( -\frac{0.6}{0.4} \right) = -1.5 \]

Example: Stable operation for $D=1/3$

\[ \alpha = -\frac{D}{D'} = \left( -\frac{1/3}{2/3} \right) = -0.5 \]
Stabilization Through Artificial Ramp

Now, transistor switches off when
\[ i_s(dT_s) + i_d(dT_s) = i_e \]
or,
\[ i_L(dT_s) = i_e - i_s(dT_s) \]

Final Value of Inductor Current

First subinterval:
\[ i_L(0) = -\alpha T_s \left( m_1 + m_a \right) \]

Second subinterval:
\[ i_L(T_s) = -\alpha T_s \left( m_a - m_2 \right) \]

Net change over one switching period:
\[ \dot{i}_L(T_s) = i_L(0) \left( \frac{m_2 - m_a}{m_1 + m_a} \right) \]

After \( n \) switching periods:
\[ \dot{i}_L(nT_s) = \dot{i}_L((n-1)T_s) \left( \frac{m_2 - m_a}{m_1 + m_a} \right) = i_L(0) \left( \frac{m_2 - m_a}{m_1 + m_a} \right)^n = i_L(0) \alpha^n \]

Characteristic value:
\[ \alpha = \frac{m_2 - m_a}{m_1 + m_a} \]
\[ |i_L(nT_s)| \rightarrow \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases} \]
**Artificial Ramp: Additional Notes**

- For stability, require $|\alpha| < 1$
  \[ \alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}} \]
- Common choices:
  - $m_a = 0.5 \ m_2$
  - $m_a = m_2$
- Artificial ramp decreases sensitivity to noise

**More Accurate Models**

- The simple models of the previous section yield insight into the low-frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:
  - Line-to-output transfer function of the buck converter
  - Dynamics at frequencies approaching $f_s$
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller
- See Section 12.3 for additional info
Application to Experiment 4

- Complex switching controller
- **Read** the datasheet first

Startup: Switching
Startup: No Switching

Short-Circuit: Switching
Short-Circuit: No Switching

LM5121: Functionality
Internal Functional Model in LTSpice

- Accuracy/functionality not guaranteed
- Used for insight only

In-Circuit Simulation

```
.model mysw Vsw(0 3 Voff=2 Rs=1 Roff = 1Meq)
.model myMOS VDMOS(Kp=1 Vto=4.5 Rs=14m Rb=10m Rb=17m Kp=30 Cgdsmax=5p Cgdsmin=0.5n Cgs=0.2n Cjs=0.5p Cjs=88p)
```

Right-click to set some parameters
Sim Results

A Tip: Debug Internal of Subcircuit
Experiment 4: Gate Driver Selection

Experiment 4: Closing the Loop

- Closed-loop operation in steps
  1. Open-loop operation with LM5121 modulator
     - Requires “tricking” LM5121
  2. Closed-loop current regulation
  3. Closed-loop voltage and current regulation
Open-Loop Operation

Setting the Electronic Load