Announcements

- Experiment 1 Report Due Tuesday
- Prelab 3 due Thursday
- All assignments turned in digitally
  - By e-mailing to Daniel.costinett@utk.edu
  - Include [ECE 482] in the subject
- Parts kit purchased prior to Tuesday’s class
- Capture waveforms, even if something is malfunctioning, for report

Outline

1. Motor Back EMF Shape
2. Power Converter Layout
3. Loss Analysis and Design
   - Low Frequency Conduction Losses
   - Inductor AC Losses
   - Core Losses
   - Inductor Design Approaches

PMSM vs BLDC

BACK EMF SHAPE
Single Phase Motor (Simplified)

Assume magnet produces a constant total flux $\Phi_m$

$\Phi_{coil} = \phi_m$

Voltage equation:

$v_x = \frac{d}{dt} \Phi_{coil} = n \frac{d}{dt} \Phi_m$

$\lambda_m = flux \ linkage$

$\Phi_{coil} = f(\theta_r)$

If $\theta_r = f(\theta)$

$\Phi_{coil} = \int f(\theta_r) \, d\theta_r$

$\Phi_{coil} = f(\theta_r)$

$\Phi_{coil} = \int f(\theta_r) \, d\theta_r = n \frac{d}{dt} \Phi_m$ (simplified)

Winding Voltage Equation

$\lambda_m = flux \ linkage$

\[ v_x = n \Phi_m \frac{d}{dt} f(\theta_r) \]

\[ \lambda_m = flux \ linkage \]

\[ f(\theta_r) = \sin \theta_r \]

Assuming constant angular speed

\[ v_x = \lambda_m \cos \theta_r \frac{d\theta_r}{dt} = \lambda_m \omega_r \cos \theta_r \]

Look at $P_a = N_a i_a$

$P_a = i_a^2 R_w + i_a L \frac{di_a}{dt} + i_a \lambda_m w_k \cos \theta_r$

Conduction loss

Reactive only

Converted to mechanical

Shape of Back EMF – PMSM Winding

- Sinusoidal back EMF achieved with sinusoidal winding distribution
- Generally termed Permanent Magnet Synchronous Motor (PMSM)

BLDC Motor Winding

- Brushless DC (BLDC) Motors are not wound sinusoidally
- This results in Trapezoidal back emf, rather than sinusoidal
- Can be driven simply with Square-waves to achieve relatively low torque ripple

http://web.eecs.utk.edu/courses/spring2017/ece482/materials/brushless-motor.swf
Outer- vs. Inner-Rotor

- Traditional motors are inner-rotor
- On e-bike, need hub to remain stationary and outer wheel to spin

Motor Teeth/Poles Example

- (a) 36-slot/6-pole
- (b) 9-slot/6-pole (all teeth wound)
- (c) 12-slot/10-pole (all teeth wound)
- (d) 12-pole/10-pole (alternate teeth wound)

Stator Winding

- Complete winding of Phase A
- Complete winding of all phases
- 56 pole
- 63 teeth

Rotor and Poles

- Outer rotor (to which spokes/wheel are attached)
- Magnets alternate N-S
Shape of Back EMF

- 33 Teeth, 22 Poles
- Teeth/Pole/Phase = 0.5

Simulation of BLDC and PMSM

(a) Trapezoidal commutation with BLDC
(b) Trapezoidal commutation with PMSM
(c) Sinusoidal Commutation with PMSM

Shape of Back EMF

- 36 Teeth, 22 Poles
- Teeth/Pole/Phase = 0.5455

Experiment 3
Prelab Assignment
Experiment 3
ECE 482

Fig. 1 shows the power stage of the drivetrain boost converter to be assembled in experiment 3. For all parts of this prelab, consider operation of the converter at an operating point around which:

- $V_{bus} = 25 \text{ V}$
- $V_{bus} \leq 50 \text{ V}$
- $5 \text{ kHz} \leq f \leq 1 \text{ MHz}$
- $\Delta V_{out} \leq 1 \text{ V}$

![Diagram of the boost converter](image)

Figure 1. Open loop boost converter (implementation shown with MOSFET devices)

Design Assessment

In experiment 3, a portion of your grade will be the performance of the design that you choose to build. A 20% segment of the lab grade will be determined by the following formula, which rewards designs with small size, high efficiency, and high power capability:

$$\text{Grade} = 25 - \kappa_{core} - 100 \cdot (0.98 - \eta_{\text{Power 100}}) - \frac{P_{\text{max}} - 250}{50}$$

where

$$\kappa_{core} = \begin{cases} 0, & \text{ETD29/ETD25} \\ 3, & \text{ETD39} \\ 6, & \text{ETD44} \\ 9, & \text{ETD49} \end{cases}$$

According to the inductor core you have chosen for your design, $P_{\text{max}}$ is the maximum power tested, which must be at least 100W, and may be as high as 250W.

Boost Design

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<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Description</th>
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<td>60 V, 155 A, Infineon FET</td>
</tr>
<tr>
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<td>150 V, 155 A, Infineon FET</td>
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<td>150 V, 25 A, Infineon FET</td>
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<td>60 V, 155 A, Infineon FET</td>
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<tr>
<td>FSP2003N38BT</td>
<td>X</td>
<td>380 V, 155 A, Infineon FET</td>
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<tr>
<td>R1542545H</td>
<td>X</td>
<td>400 V, N-Channel IGBT</td>
</tr>
</tbody>
</table>

Core geometry

- ETD2
- ETD4
- ETD49
- ETD49

Wire Gauge Diameter [mm]

- AWG 10: 0.257
- AWG 12: 0.213
- AWG 14: 0.171
- AWG 16: 0.137
- AWG 20: 0.087

POWER CONVERTER LAYOUT
Parasitic Wire Inductances

Even better: minimize area of the high frequency loop. Thereby minimizing its inductance.

L(loop) = 0.4 nH
L(loop) = 1.6 nH

Power Converter Layout: Buck Example
Half Bridge Gate Drive Waveforms

- Gate driver chip must implement $v_{gs}$ waveforms
- Sources will have pulsating currents and need decoupling

Driving a Power MOSFET Switch

- MOSFET is off when $v_{gs} < V_{th} \approx 3 \text{ V}$
- MOSFET fully on when $v_{gs}$ is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when $v_{gs} > 20 \text{ V}$
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

Gate Drive Implementation

- Gate driver is cascades back half-bridges of decreasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections
Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

Capacitor Sizing Notes

\[ \frac{q_{\text{gate}}}{\Delta V_{DD}} = C \]

- Area of current pulse is total charge supplied to gate of capacitor
- All charge must be supplied from gate drive decoupling capacitor

Gate Drive Losses

\[ E_{\text{loss}} = q_{\text{gate}}V_{DD} \]
\[ P_{\text{sw,g}} = E_{\text{loss}}f_s \]

- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

High Side Signal Ground

- Gate driver chip must implement \( v_{gs} \) waveforms
- Issue: source of \( Q_2 \) is not grounded
• Isolated supplies sometimes used; Isolated DC-DC, batteries
• Bootstrap concept: capacitor can be charged when $V_s$ is low, then switched

**UCC27211a Internal Diagram**

- Direct Drive
- Floating Supply Gate Drive
- Transformer Coupled Drive
- Charge Pump Drive
- Bootstrap Drive

**A Note on Grounding**

- Easiest high-side application the MOSFET can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: $V_{CC} < V_{DD}$, and $V_{DC} < V_{CC}$.
- Cost impact of isolated supply is significant. Optocoupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.
- Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.
- The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.
- Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.
Parasitics to be Aware of

Power Loop Inductances

Persson E., “What really limits MOSFET performance: silicon, package, driver or circuit board?”

Complete Routing of Signal

• Always consider return path
• Ground plane can help, but still need to consider the path and optimize

Star-Grounding Vs. Daisy Chain

Figure 9. Separate the Input Current Paths Among Supplies
Another View

Kester, W. “Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects”

Kelvin Connection

Efficiency Measurement

Boost Converter

POWER CONVERTER DESIGN AND LOSS ANALYSIS
Converter Design

Analytical Loss Modeling

- High efficiency approximation is acceptable for hand calculations, as long as it is justified
  - Solve ideal waveforms of lossless converter, then calculate losses
  - Argue which losses need to be included, and which may be neglected
    - “Rough” approximation to gain insight into significance

Additional Resources

- Additional lectures in ECE581
  - [http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php](http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php)
  - Accessible only from campus network
- Switching Overlap Loss L4-L5
- Device Capacitances L6-L7
- Magnetics Losses L19(2\textsuperscript{nd} half) and L20

Boost Converter Loss Analysis

- Begin by solving important waveforms throughout converter assuming lossless operation
Power Stage Losses

- **Low-Frequency Losses**
  - MOSFETS: $R_{on}$, $V_f$, $R_d$
  - Body Diodes: $C_{oss}$, Overlap, $P_g$
  - Inductor: $T_d$ cond.
  - Capacitors: $C_{oss}$, Overlap, $P_g$
  - $R_{dc}$
  - ESR
- **Frequency-Dependent Losses**
  - Skin Effect
  - Core Loss
  - Fringing
  - Proximity
  - Dielectric Losses

LOW FREQUENCY CONDUCTION LOSSES

MOSFET Equivalent Circuit
- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

MOSFET On Resistance
- On resistance extracted from datasheet waveforms
- Significantly dependent on $V_{gs}$ amplitude, temperature
**Boost Converter RMS Currents**

- MOSFET conduction losses due to \((r_{ds})_{on}\) depend given as
  
  \[ P_{cond,FET} = I_{di,rms}^2 (r_{ds})_{on} \]

**MOSFET Conduction Losses**

- RMS values of commonly observed waveforms appendix from Power Book

**Capacitor Loss Model**

- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
  
  - Equivalent Series Resistance (ESR) is *highly* frequency dependent
  
  -Datasheets may give effective impedance at a frequency, or loss factor:
    
    \[ \delta = \frac{\pi}{2} - \theta \]
    \[ D = \tan(\delta) \]

**DC Inductor Resistance**

- DC Resistance given by
  
  \[ R_{DC} = \rho \frac{l_b}{A_w} \]
  
  - At room temp, \( \rho = 1.724 \cdot 10^{-6} \Omega\cdot\text{cm} \)
  
  - At 100°C, \( \rho = 2.3 \cdot 10^{-6} \Omega\cdot\text{cm} \)
  
- Losses due to DC current:
  
  \[ P_{cu,DC} = I_{L,rms}^2 R_{DC} \]
Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

\[ rmz = I \sqrt{1 + \frac{1}{2} \left( \frac{\Delta I}{I} \right)^2} \]  

(A.2)

- Conduction losses dependent on RMS current through inductor

Switching Loss

Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses
**Gate Charge Loss**

\[ P_g = Q_g V_{CC} f_s \]

**Overlap Loss**

\[ P_{overlap} = \frac{1}{2} I_d V_{f} \frac{T_{on}}{T_s} \]

**Lump Switched Node Capacitance**

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices.

**Diode Loss Model**

- Example loss model includes resistance and forward voltage drop extracted from datasheet.
**Diode Reverse Recovery**

- Diodes will turn on during dead time intervals
- Significant reverse recovery possible on both body diode and external diode

**INDUCTOR AC LOSSES**

\[ E_{on,rr} = (I_L - \Delta i_L) t_{rr} + Q_{rr} V_{bus} \]

**Skin Effect in Copper Wire**

- Current profile at high frequency is exponential function of distance from center with characteristic length \( \delta \)

**AC Resistance**

\[ A_{w,eff} = \pi r_w^2 - \pi (r_w - \delta)^2 \]

\[ R_{ac} = \rho \frac{l_b}{A_{w,eff}} \]
Skin Depth

\[ \delta = \sqrt{\frac{\rho}{\pi f \mu}} \]

\[ \begin{align*}
\text{Penetration depth} \delta, \text{cm} & \quad \text{Wire diameter} \\
\text{25°C} & \quad \#20 \text{ AWG} \\
\text{100°C} & \quad \#30 \text{ AWG} \\
& \quad \#40 \text{ AWG}
\end{align*} \]

\[ \begin{align*}
10 \text{ kHz} & \quad 100 \text{ kHz} & \quad 1 \text{ MHz} \\
0.1 & \quad 0.01 & \quad 0.001
\end{align*} \]

Fig. 13.23 Penetration depth \( \delta \) as a function of frequency \( f \) for copper wire.

Proximity Effect

- In foil conductor closely spaced with \( h >> \delta \), flux between layers generates additional current according to Lentz's law.

\[ P_1 = I_{L,rms}^2 R_{ac} \]

- Power loss in layer 2:

\[ P_2 = I_{L,rms}^2 R_{ac} + (2I_{L,rms})^2 R_{ac} \]

\[ P_2 = 5P_1 \]

- Needs modification for non-foil conductors

Simulation Example

- AWG#30 copper wire
  - Diameter \( d = 0.294 \text{ mm} \)
  - \( d = \delta \) at around 50 kHz
- 1:1 transformer
  - Primary and secondary are the same, 30 turns in 3 layers
- Sinusoidal currents,

\[ I_{1,rms} = I_{2,rms} = 1 \text{ A} \]

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, http://www.femm.info/wiki/HomePage

Flux density magnitude

Current density magnitude
Frequency: 1 kHz

Total copper losses 1.8 larger than at 1 kHz

Frequency: 1 MHz

Total copper losses 20 times larger than at 1 kHz

Frequency: 100 kHz

Frequency: 10 MHz

Very significant proximity effect
Total copper losses = 65 times larger than at 1 kHz
**Fringing**

- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors

**Physical Origin of Core Loss**

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting

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**Inductor Core Loss**

- Governed by Steinmetz Equation:
  \[ P_v = K_f e f_s^\alpha (\Delta B)^\beta \text{ [mW/cm}^3\text{]} \]
- Parameters \( K_f, \alpha, \) and \( \beta \) extracted from manufacturer data
  \[ P_{fe} = P_v A c l_m \text{ [mW]} \]
- \( \Delta B \propto \Delta i_L \rightarrow \) small losses with small ripple

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**Steinmetz Parameter Extraction**

- Fig. 6: Specific power loss as a function of peak flux density with frequency as a parameter
- Fig. 7: Specific power loss for several frequency/flux density combinations as a function of temperature
Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula:

\[ P_{\text{core}} = C_m \cdot f^x \cdot B_{\text{peak}}^y \cdot (c_0 - c_1 f + c_2 T^2) \]  

\[ = C_m \cdot C_T \cdot f^x \cdot B_{\text{peak}}^y \quad [\text{mW/cm}^3] \]

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<th>f (kHz)</th>
<th>Cm</th>
<th>x</th>
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<td>0.34 \times 10^{-4}</td>
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<td>0.67</td>
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Table 1: Fit parameters to calculate the power loss density

Non-Sinusoidal Waveforms

- Modified Steinmetz Equation (MSE)
  - “Guess” that losses depend on \( dB/dt \)
  - Calculate \( dB/dt \) and find frequency of equivalent sinusoid

\[ P_{\text{NSE}} = \left( \frac{\Delta B}{2} \right)^{\beta - \alpha} \frac{k_N}{T} \int_0^T \left( dB \right)^{\alpha} dt \]

\[ k_N = \frac{k}{(2\pi)^{\beta - 1} \int_0^{2\pi} \cos^{\beta - \alpha} \theta d\theta} \]

Simple Formula for Square-wave voltages:

\[ P_{\text{NSE}} = k_N \left( 2f \right)^{\beta} \left( 2\pi \right)^{\beta} \left( D^{1 - \alpha} + (1 - D)^{1 - \alpha} \right) \]

where 
- \( f \) is the operating frequency;
- \( \Delta B / 2 \) is the peak induction;
- \( D \) is the duty ratio of the square wave voltage.

Note: The second and third harmonics are dominant at moderate values of duty ratio \( D \). For extreme values of \( D \) (95%), a higher value of \( \alpha \) could give better matching to the actual losses.


Albach, Durbau and Brockmeyer, 1996
Reinert, Brockmeyer, and Doncker, 1999

INDUCTOR DESIGN

Fig. 8. Comparison between measurement and calculation as a function of duty cycle.
Inductor Design

**Freedoms:**
1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

**Constraints:**
1. Obtain Designed $L$
2. Prevent Saturation
3. Minimize Losses

**Minimization of Losses**
- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance
- A minimum sum of the two exists and can be solved
- Design always subject to constraint $B_{\text{max}} < B_{\text{sat}}$

**Equivalent Circuit**

**Spreadsheet Design**
- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.
Matlab (Programmatic) Design

Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

Closed-Form Design Methods

- Fundamentals of Power Electronics Ch 13-15
  - Step-by-Step design methods
  - Simplified, and may require additional calculations

**$K_g$ and $K_{gfe}$ Methods**

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) Steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

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<th>$K_{gfe}$</th>
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<td>DC Copper, SE Core Loss</td>
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<tr>
<td>(specified)</td>
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<td>(optimized)</td>
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<tr>
<td>Saturation</td>
<td>Specified</td>
<td>Checked After</td>
</tr>
<tr>
<td>$B_{max}$</td>
<td>Specified</td>
<td>Optimized</td>
</tr>
</tbody>
</table>

**$K_g$ Method**

- Method useful for filter inductors where $\Delta B$ is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired $B_{max}$ is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website
**Method**

- **K_{gfe} Method**
  - Method useful for cases when core loss and copper loss are expected to be significant
  - Saturation is not included in the method, rather it must be checked afterward
  - Enforces a design where the sum of core and copper is minimized

**K_{gfe} Procedure**

The following quantities are specified, using the units noted:

- Wire effective resistivity \( \rho \) (\( \Omega \)-cm)
- Total rms winding current, ref to pri \( I_{sw} \) (A)
- Des red turns ratios \( n_1/n_2, n_3/n_4, \) etc.
- Applied pri volt-sec \( \lambda_1 \) (V-sec)
- Allowed total power dissipation \( P_{sw} \) (W)
- Winding fill factor \( K_f \)
- Core loss exponent \( \beta \)
- Core loss coefficient \( K_{fe} \) (W/cm³T³)

Other quantities and their dimensions:

- Core cross-sectional area \( A_c \) (cm²)
- Core window area \( W_c \) (cm²)
- Mean length per turn \( MLT \) (cm)
- Magnetic path length \( \ell_c \) (cm)
- Wire areas \( A_{w} \) ...
- Peak ac flux density \( \Delta B \) (T)

**K_{gfe} Procedure Formula**

\[
K_{gfe} = 4K_f \left( \frac{P_{sw}}{\lambda_1 (MLT) \frac{1}{\beta+2}} \right) 10^8
\]

\[
\Delta B = 10^8 \frac{\rho \lambda_1^2 I_{sw}^2}{2K_f \lambda W_c A_c (\ell_m \beta K_{fe})^{\frac{1}{\beta+2}}}
\]

\[
n_1 = \frac{\lambda_1}{2 \Delta B A_c} 10^4 \quad n_3 = n_1 n_2
\]

\[
\alpha_k = \frac{n_3 I_3}{n_1 I_{sw}} \quad A_{wk} \leq \frac{\alpha_k K_w A_c}{n_2}
\]
$K_{gfe}$ Method: Summary

- Method enforces an operating $\Delta B$ in which core and copper losses are minimized
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal
- Does not consider high frequency losses
- Step-by-step design procedure included on website