Announcements

- Thursday class TA
- Prelab 5
  - Decide on System Improvements
  - Redesign using GaN Devices
- Midterm after Experiment 5
  - Open note, book, instructor
- Today: Experiment 5
  - No report; deliverables are layout files and BOM

Lab 5: PCB Layout

- More information on motor drive in Experiment 5
Design Modification

- You may order additional parts, at reasonable cost/benefit
  - Will need to provide a listing of parts from digikey with final Exp 5 files
- Reuse components from lab kit where possible
- Use SMD ceramic, low ESR caps for power stage and gate drive decoupling

Circuit Enclosure
Circuit Enclosure - Mounting

Circuit Connections

Allowable Build Volume
7” x 4” x 2”
Prelab for Experiment 5: Redesign with GaN

GaN Systems GS61008T
- 7.4 mOhm
- 100V/80A
- \( Q_g = 12 \) nC
- \( C_{oss} = 250 \) pF (80V)

EPC EPC2001C
- 7 mOhm
- 100V/36A
- \( Q_g = 9 \) nC
- \( C_{oss} = 375 \) pF (80V)

GaN Devices

Vertical Silicon Power MOSFET
- No body diode (reverse conduction due to \( V_{gd} > V_{gd,th} \approx 2V \))
- Use antiparallel (schottky) diode or precise dead time
- Significantly faster switching

Lateral GaN HEMT
Designing with GaN

Because of high electric breakdown field and high electron velocity, GaN devices with comparable $R_{on}$ can be significantly smaller and switch must faster.

Need **very** good layout to prevent ringing from causing overvoltage and device failure.

More information:

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GaN Design Issues

1. Reverse conduction mechanism
2. Sensitivity to parasitics
3. Gate robustness
4. Small size -> Thermal, soldering difficult
Motor Control

• Motor control is open-loop
• User throttle monotonically increases power
  – Controlled as BLDC motor
• Two options to change throttle
  – Alter boost output voltage
  – Alter duty cycle of motor drive

Motor Driver: Trapezoidal Control

![Diagram of BLDC Motor Power Topology and Hall Sensor Logic vs Bridge State Logic](attachment:image.png)
Trapezoidal Control: HF PWM

Sinusoidal (Vector) Control
A Note: Reflected Voltages

Control Scheme - Filtering
Motor Control Bandwidth

No Filter

$$f_c = 15 \text{ mHz}$$

Throttle Release
Motor Control Bandwidth

\[ f_c = 8 \text{ mHz} + \text{antiparallel diode} \]

Motor Drive

- Power Stage
  - IRAM power module (recommended)
    - Integrated devices, drivers
  - Build your own power stage

- Controller
  - Allegro A4915
  - Toshiba TB6551FAG
  - Other options

- Example Schematics in Starter Files for Experiment 5
PCB Layout for Experiment 5

- Include test points for voltages/currents to aid debugging
- Where possible, give yourself “backup options”
- Make sure parts you select are available and have sufficient stock
  - even if some get ordered in the interim

Basic PCB Layout Concepts

- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances / Complete Routing
- Decoupling
- Ground Plane / Return Currents
- Partitioning
Trace Parasitics

\[ R = \frac{Z}{\rho \cdot Y} \]

\( \rho = \text{RESISTIVITY} \)

\[ Z \]

\( R \)

\[ Y \]

\[ \text{SHEET RESISTANCE CALCULATION FOR 1 OZ. COPPER CONDUCTOR:} \]

\[ \rho = 1.724 \times 10^{-6} \text{ohm} \cdot \text{cm}, \quad Y = 0.0038 \text{cm} \]

\[ R = 0.42 \times \frac{Z}{X} \text{m} \Omega \]

\( Z \)

\( X \)

\[ \text{NUMBER OF SQUARES} \]

\[ R = \text{SHEET RESISTANCE OF 1 SQUARE (Z/X)} \]

\[ = 0.42 \times \text{m} \Omega / \text{SQUARE} \]

**Figure 12.2:** Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors

Kester, W. “Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects”

Kelvin Connection

**Figure 1. Kelvin Connection**

Texas Instruments, “LMP8640/-Q1/HV Precision High Voltage Current Sense Amplifiers”
Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt

Decoupling Capacitance

Figure 4: Impedance of Various 100μF Capacitors
High Impedance Nodes and Capacitive Coupling

Figure 12.29: High Circuit Impedances Increase Susceptibility to Noise Pickup

Capacitive Shielding

Figure 12.26: An Operational Model of a Faraday Shield

Analog Devices, “Decoupling Techniques,” MT-101
Loop Inductances

Bad practice: wide separation of signal and return

Good practice: close coupling of signal and return

Ground Plane

- Benefits:
  - Common reference
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)
- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable
Cuts in Ground Plane

• Goals:
  - minimize inductance/loops
  - Minimize ground interference
• Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
• Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
• Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

Ground Plane Cuts

Ground return current path
Ground Plane Cuts

Signal routing with ground plane cuts

- Split in the plane
- Signal
- Return path
- Loop area

Bad Practice

Good Practice

Analog area

Digital area
Ground Plane Example

Ground Plane Example
Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source

Bridge Layout
Half Bridge Layout: Another Example

Lateral  Vertical  “Optimal”

Layout Impact Measurements

- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss