PCB Layout

ECE 482 Lecture 5
February 28, 2017

Announcements

• Prelab 5
  – Decide on System Improvements
  – Redesign using GaN Devices
• Midterm after Experiment 5
  – Open note, book, instructor
• Today: Experiment 5
  – No report; deliverables are layout files and BOM
Lab 5: PCB Layout

- More information on motor drive in Experiment 5

Design Modification

- You may order additional parts, at reasonable cost/benefit
  - Will need to provide a listing of parts from digikey with final Exp 5 files
- Reuse components from lab kit where possible
- Use SMD ceramic, low ESR caps for power stage and gate drive decoupling
Prelab for Experiment 5: **Redesign** with GaN

**GaN Systems GS61008T**
- 7.4 mOhm
- 100V/80A
- $Q_g = 12$ nC
- $C_{oss} = 250$ pF (80V)

**EPC EPC2001C**
- 7 mOhm
- 100V/36A
- $Q_g = 9$ nC
- $C_{oss} = 375$ pF (80V)
GaN Devices

Vertical Silicon Power MOSFET  
Lateral GaN HEMT

- No body diode (reverse conduction due to $V_{gd} > V_{gd,th} \approx 2V$)
  - Use antiparallel (schottky) diode or precise dead time
  - Significantly faster switching

Designing with GaN

- Because of high electric breakdown field and high electron velocity, GaN devices with comparable $R_{on}$ can be significantly smaller and switch must faster.
- Need very good layout to prevent ringing from causing overvoltage and device failure.
- More information:

How to GaN: Simplifying Design with DrGaN
GaN Design Issues

1. Reverse conduction mechanism
2. Sensitivity to parasitics
3. Gate robustness
4. Small size -> Thermal, soldering difficult

Motor Control

- Motor control is open-loop
- User throttle monotonically increases power
  - Controlled as BLDC motor
- Two options to change throttle
  - Alter boost output voltage
  - Alter duty cycle of motor drive
Motor Driver: Trapezoidal Control

Trapezoidal Control: HF PWM
Sinusoidal (Vector) Control

A Note: Reflected Voltages
Control Scheme - Filtering

Motor Control Bandwidth

No Filter
Motor Control Bandwidth

\[ f_c = 15 \text{ mHz} \]

Motor Control Bandwidth

\[ f_c = 8 \text{ mHz} + \text{antiparallel diode} \]
Motor Drive

• Power Stage
  – IRAM power module (recommended)
    ▪ Integrated devices, drivers
  – Build your own power stage
• Controller
  – Allegro A4915
  – Toshiba TB6551FAG
  – Other options
• Example Schematics in Starter Files for Experiment 5

PCB Layout for Experiment 5

• Include test points for voltages/currents to aid debugging
• Where possible, give yourself “backup options”
• Make sure parts you select are available and have sufficient stock
  – even if some get ordered in the interim
Basic PCB Layout Concepts

- Kelvin Connection
- Parasitic Capacitances and Decoupling
- Loop Inductances / Complete Routing
- Decoupling
- Ground Plane / Return Currents
- Partitioning

Trace Parasitics

Figure 12.2: Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors

Figure 12.18: Wire and Strip Inductance Calculations

Figure 12.24: Capacitance of two parallel plates

Kester, W. “Tips about printed circuit board design: Part 1 - Dealing with harmful PCB effects”
Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt
Decoupling Capacitance

Figure 4: Impedance of Various 100μF Capacitors

Half Bridge Loop Inductance

Parasitic inductances of input loop explicitly shown:

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source
High Impedance Nodes and Capacitive Coupling

**Figure 12.29** High Circuit Impedances Increase Susceptibility to Noise Pickup

Analog Devices, “Decoupling Techniques,” MT-101

Capacitive Shielding

**Figure 12.26:** An Operational Model of a Faraday Shield

Analog Devices, “Decoupling Techniques,” MT-101
Loop Inductances

![Diagram of loop inductances with bad and good practices](image)

**Benefits:**
- Common reference
- Shielding
- Heat dissipation
- Reduced inductance (increased capacitance)

**Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable**

Ground Plane

- Benefits:
  - Common reference
  - Shielding
  - Heat dissipation
  - Reduced inductance (increased capacitance)

- Resist urge to cut ground plane as much as possible; consider paths of return currents when cuts are unavoidable
Cuts in Ground Plane

• Goals:
  − minimize inductance/loops
  − Minimize ground interference
• Routing cuts should be kept short and out of the path of any significant (high frequency) return paths
• Cuts can be used effectively for ground isolation, and to reduce noise coupled between digital/analog/power circuitry
• Reducing parasitic capacitance in sensitive signal locations (i.e. op-amp circuitry)

Ground Plane Cuts

Ground return current path
Ground Plane Cuts

Ground return current path

Signal routing with ground plane cuts

Split in the plane

Bad Practice

Good Practice

Analog area

Digital area

High Speed Design in Altium Designer
Ground Plane Example

Maxim, TUTORIAL 5450, “Successful PCB Grounding with Mixed-Signal Chips - Follow the Path of Least Impedance”

Ground Plane Example

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Ground Plane Example

Maxim, TUTORIAL 5450, “Successful PCB Grounding with Mixed-Signal Chips - Follow the Path of Least Impedance”
Bridge Layout

Half Bridge Layout: Another Example

Lateral  Vertical  “Optimal”

D. Reusch & J Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter”
Layout Impact Measurements

- Smallest Loop Area results in
  - Smaller overvoltage
  - Lower switching loss

D. Reusch & J Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter”

Experiment 5: Starting Files