Outline

1. Experiment 3 Introduction
2. Power Converter Layout
3. Loss Analysis and Design
   - Low Frequency Conduction Losses
   - Inductor AC Losses
   - Core Losses
   - Inductor Design Approaches

Experiment 3
Prelab Assignment
Experiment 3
ECE 482

Fig. 1 shows the power stage of the drivetrain boost converter to be assembled in experiment 3. For all parts of this prelab, consider operation of the converter at an operating point around which:

- $V_{bat} = 25$ V
- $V_{bus} \leq 50$ V
- $5$ kHz $\leq f_i \leq 1$ MHz
- $\Delta v_{out} \leq 1$ V

![Diagram of open loop boost converter](image)

**Figure 1.** Open loop boost converter (implementation shown with MOSFET devices)

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**Design Assessment**

In experiment 3, a portion of your grade will be the performance of the design that you choose to build. A 20% segment of the lab grade will be determined by the following formula, which rewards designs with small size, high efficiency, and high power capability:

$$\text{Grade} \%) = 25 - \kappa_{core} - 100 \times (0.98 - \eta_{P=100}) - \frac{P_{\text{max}} - 250}{50},$$

where

$$\kappa_{core} = \begin{cases} 0, & ETD29/ EFD25 \\ 3, & ETD39 \\ 6, & ETD44 \\ 9, & ETD49 \end{cases}$$

According to the inductor core you have chosen for your design. $P_{\text{max}}$ is the maximum power tested, which must be at least 100W, and may be as high as 250W.
Boost Design

Contents of Magnetics Library
ECE 482 Spring 2018

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Core Loss Parameters for Ferroxcube Materials

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<th>Wire Gauge</th>
<th>Diameter [cm]</th>
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<tr>
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<td>AWG 16</td>
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<td>AWG 20</td>
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</table>

Full AWG table

POWER CONVERTER LAYOUT
Power Converter Layout: Buck Example

Use loop analysis

switched input current \( i_1(t) \) contains large high frequency harmonics
—hence inductance of input loop is critical
inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

the second loop contains a filter inductor, and hence its current \( i_2(t) \) is nearly dc
—hence additional inductance is not a significant problem in the second loop

Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

high frequency currents are shunted through capacitor instead of input source
Loop Minimization

Even better: minimize area of the high frequency loop, thereby minimizing its inductance.

\[ L_{\text{loop}} = 0.4 \text{nH} \]

\[ L_{\text{loop}} = 1.6 \text{nH} \]

Effect of Loop Inductance

100% Overshoot

\[ L_{\text{loop}} = 1.6 \text{nH} \]

30% Overshoot

\[ L_{\text{loop}} = 0.4 \text{nH} \]
Half Bridge Gate Drive Waveforms

- Gate driver chip must implement $v_{gs}$ waveforms
- Sources will have pulsating currents and need decoupling

Driving a Power MOSFET Switch

- MOSFET is off when $v_{gs} < V_{th} \approx 3$ V
- MOSFET fully on when $v_{gs}$ is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when $v_{gs} > 20$ V.
- Fast turn on or turn off (10's of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

Power MOSFET 
MOSFET capacitances

$C_{gs} \gg C_{ds} \gg C_{gd}$
Driving a Power MOSFET Switch

- MOSFET gate driver is used as a logic buffer with high output current (~1.8 A) capability
- The amplitude of the gate voltage equals the supply voltage $V_{CC}$
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow $dv/dt$ at switch node

Gate Drive Implementation

- Gate driver is cascaded half-bridges of increasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections
Decoupling

• Always add bypass capacitor at power supply for any IC/reference
• Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
• Limit loop for any di/dt
Capacitor Sizing – Filter Caps

\[ c \frac{1}{1} \rightarrow \frac{1}{\frac{\frac{1}{3} \cdot \frac{1}{E_{SL}}}{\frac{1}{E_{SR}}}} \]

Area of current pulse is total charge supplied to gate of capacitor

All charge must be supplied from gate drive decoupling capacitor

• Gate driver chip must implement $v_{gs}$ waveforms
• Issue: source of $Q_2$ is not grounded

Generating Floating Supply

• Isolated supplies sometimes used; Isolated DC-DC, batteries
• Bootstrap concept: capacitor can be charged when $V_s$ is low, then switched
# UCC27211a Internal Diagram

![Diagram of UCC27211a Internal Diagram]

## Direct Drive

Easiest high-side application the MOSFET and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows:

\[
V_{CC} < V_{GS_{MAX}} \quad \text{and} \quad V_{DC} < V_{CC} - V_{GS_{MAX}}
\]

## Floating Supply Gate Drive

Cost impact of isolated supply is significant. Optocoupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.

## Transformer Coupled Drive

Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.

## Charge Pump Drive

The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.

## Bootstrap Drive

Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.

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*Fairchild Semi App Note AN-6076*
A Note on Grounding

Parasitics to be Aware of

- All probes all the time grounded

Remedy: Hx turns ON
1. Decrease Rl
2. Decrease in → a) increase Rh
   b) add snubber

\[ V_{gs} = 15V - V_{d} \]
Power Loop Inductances

Persson E., “What really limits MOSFET performance: silicon, package, driver or circuit board?”

Complete Routing of Signal

• Always consider return path
• Ground plane can help, but still need to consider the path and optimize
Star-Grounding Vs. Daisy Chain

Figure 9. Separate the input current paths among supplies

Kelvin Connection

\[ i(t) = \frac{R_{\text{sense}}}{R_p} + R_p \frac{di(t)}{dt} \]
Efficiency Measurement

High Impedance Nodes

\[ R_1 \approx R_2 \text{ are very large (100's of kOhms)} \]

- Makes node high-\( z \) susceptible to noise
- \( R_1 \approx R_2 \) deal with loss
- Add cap to decouple (if possible)
POWER CONVERTER DESIGN AND LOSS ANALYSIS

Converter Design

Analytical Model
- Loss Model
- Thermal Model
- Cost Model
- MOSFET Selection
- Inductor Design
- Switching Frequency

Design Specifications
Performance Specification
Design Assessment
Analytical Loss Modeling

• High efficiency approximation is acceptable for hand calculations, as long as it is justified
  • Solve ideal waveforms of lossless converter, then calculate losses
• Argue which losses need to be included, and which may be neglected
  • “Rough” approximation to gain insight into significance

Additional Recorded Lectures

- ECE581
  - [http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php](http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php)
    ▪ Switching Overlap Loss L4-L5
    ▪ Device Capacitances L6-L7
    ▪ Magnetics Losses L19-L20
- ECE 481
  - [http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php](http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php)
    ▪ Switching Loss L13
    ▪ Magnetics Design L37-39
Boost Converter Loss Analysis

- Begin by solving important waveforms throughout converter assuming lossless operation

Power Stage Losses

- **Low-Frequency Losses**
  - MOSFETS: $R_{on}$, $V_F$, $R_d$
  - Body Diodes: $V_F$, $R_d$
  - Inductor: $R_{dc}$
  - Capacitors: ESR

- **Frequency-Dependent Losses**
  - MOSFETS: $C_{oss}$, Overlap, $P_g$
  - Inductor: $T_d$ cond., $C_d$, Reverse-Recovery
  - Capacitors: Skin Effect, Core Loss, Fringing, Proximity
  - Dielectric Losses
LOW FREQUENCY CONDUCTION LOSSES

MOSFET Equivalent Circuit

• Considering only power stage losses (gate drive neglected)
• MOSFET operated as power switch
• Intrinsic body diode behaviors considered using normal diode analysis
Datasheet Interpretation

- On resistance extracted from datasheet waveforms
- Significantly dependent on $V_{gs}$ amplitude, temperature

Boost Converter RMS Currents

- MOSFET conduction losses due to $(r_{ds})_{on}$ depend given as

$$P_{\text{cond,FET}} = I_{di,rms}^2 (r_{ds})_{on}$$
MOSFET Conduction Losses

RMS values of commonly observed waveforms appendix from Power Book

Capacitor Loss Model

- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is highly frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:
  \[
  \delta = \frac{\pi}{2} - \theta \\
  D = \tan(\delta)
  \]
DC Inductor Resistance

- DC Resistance given by
  \[ R_{DC} = \rho \frac{l_b}{A_w} \]
- At room temp, \( \rho = 1.724 \cdot 10^{-6} \ \Omega\text{-cm} \)
- At 100°C, \( \rho = 2.3 \cdot 10^{-6} \ \Omega\text{-cm} \)
- Losses due to DC current:
  \[ P_{cu,DC} = I_{L,rms}^2 R_{DC} \]

Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

\[ \text{rms} = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I}{I} \right)^2} \]  \hspace{1cm} (A.2)

- Conduction losses dependent on RMS current through inductor
Switching Loss

Switching Loss Modeling

\[ V_{gs1}, V_{gs2}, V_{sw} \]

\[ t \]

\[ i_c, i_d \]

\[ C_d, i_r \]
Dead Time Selection

Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses
Gate Drive Losses

- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off

\[ E_{\text{loss}} = q_{\text{gate}} V_{\text{DD}} \]
\[ P_{\text{sw, } g} = E_{\text{loss}} f_s \]

 Gate Charge Loss

9 Typ. gate charge

\[ V_{\text{gs}} = f(Q_{\text{gs}}) \]

\[ I_D = 5.2 \text{ A pulsed} \]

Parameter: \( V_{\text{cc}} = 120 \text{ V, } Q_g = 17 \text{ nC} \)

\[ P_g = Q_g V_{\text{cc}} f_s \]

during switching

\[ i_g \approx \frac{V_{\text{gs}} - V_m}{R_{1l}} \]
Overlap Loss

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices
Diode Loss Model

- Example loss model includes resistance and forward voltage drop extracted from datasheet

Diode Reverse Recovery

- FET body diodes may turn on during dead time intervals
- Significant reverse recovery losses possible

\[ E_{on,rr} = ((I_L - \Delta i_L) \Delta t + Q_{rr}) V_{bus} \]
Reverse Recovery – Rough Approximations

- $E_{rr} \approx E_{rr\_datasheet} \frac{I_F}{I_{F\_datasheet}} \frac{V_{DC}}{V_{DC\_datasheet}}$

- Rough approximation with $I_F \ll I_{max}$
INDUCTOR AC LOSSES

Skin Effect in Copper Wire

- Current profile at high frequency is exponential function of distance from center with characteristic length $\delta$
AC Resistance

\[ A_{W,eff} = \pi r_w^2 - \pi (r_w - \delta)^2 \]

\[ R_{ac} = \rho \frac{l_b}{A_{W,eff}} \]

Skin Depth

\[ \delta = \sqrt{\frac{\rho}{\pi \mu f}} \]

Fig. 13.23 Penetration depth \( \delta \), as a function of frequency \( f \), for copper wire.
Proximity Effect

- In foil conductor closely spaced with $h >> \delta$, flux between layers generates additional current according to Lentz’s law.

$$P_1 = I_{L,\text{rms}}^2 R_{ac}$$

- Power loss in layer 2:

$$P_2 = I_{L,\text{rms}}^2 R_{ac} + (2I_{L,\text{rms}})^2 R_{ac}$$

$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

See Fundamentals of Power Electronics, Section 13.4

Simulation Example

- AWG#30 copper wire
  - Diameter $d = 0.294$ mm
  - $d = \delta$ at around 50 kHz
- 1:1 transformer
  - Primary and secondary are the same, 30 turns in 3 layers
- Sinusoidal currents,
  $$I_{1,\text{rms}} = I_{2,\text{rms}} = 1 \text{ A}$$

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, http://www.femm.info/wiki/HomePage
Frequency: 1 kHz

Flux density

Current Density
Frequency: 100 kHz

Flux density

Current Density

Total copper losses 1.8 larger than at 1 kHz

Frequency: 1 MHz

Flux density

Current Density

Total copper losses 20 times larger than at 1 kHz
Frequency: 10 MHz

Very significant proximity effect
Total copper losses = 65 times larger than at 1 KHz

Fringing

- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors
Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting

Inductor Core Loss

- Governed by Steinmetz Equation:
  $$P_v = K_{fe} f_s^\alpha (\Delta B)^\beta \text{ [mW/cm}^3\text{]}$$
- Parameters $K_{fe}$, $\alpha$, and $\beta$ extracted from manufacturer data
  $$P_{fe} = P_v A_c l_m \text{ [mW]}$$
- $\Delta B \propto \Delta i_L \rightarrow$ small losses with small ripple
Steinmetz Parameter Extraction

Fig. 6 Specific power loss as a function of peak flux density with frequency as a parameter.

Fig. 7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula:

\[ P_{\text{core}} = C_m \cdot f^x \cdot B_{\text{peak}}^y \left( c_{t0} - c_{t1} T + c_{t2} T^2 \right) \]

\[ = C_m \cdot C_T \cdot f^x \cdot B_{\text{peak}}^y \quad [\text{mW/cm}^3] \]

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<th>ferrite</th>
<th>f (kHz)</th>
<th>Cm</th>
<th>x</th>
<th>y</th>
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<td>3.02</td>
<td>4.10^{-4}</td>
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<td>2.9</td>
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<td>1000-3000</td>
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<td>2.8</td>
<td>2.4</td>
<td>0.34 \times 10^{-4}</td>
<td>0.01 \times 10^{-2}</td>
<td>0.67</td>
</tr>
</tbody>
</table>

Table 1: Fit parameters to calculate the power loss density
\[ P_{\text{NSE}} = \left( \frac{\Delta B}{2} \right)^{\beta - \alpha} \frac{k_N}{T} \int_0^T \left| \frac{dB}{dt} \right|^\alpha \, dt \]

\[ k_N = \frac{k}{(2\pi)^{\alpha-1}} \int_0^{2\pi} |\cos \theta|^\alpha \, d\theta \]

Simple Formula for Square-wave voltages:

\[ P_{\text{NSE}} = k_N (2f)^{\alpha} (\Delta B)^{\beta} (D^{1-\alpha} + (1-D)^{1-\alpha}) \]  

(10)

where  
\( f \) is the operating frequency;  
\( \Delta B / 2 \) is the peak induction;  
\( D \) is the duty ratio of the square wave voltage.

**Note:** The second and third harmonics are dominant at moderate values of duty ratio \( D \). For extreme values of \( D \) (95%), a higher value of \( \alpha \) could give better matching to the actual losses.

K. Venkatachalam; C. R. Sullivan; T. Abdallah; H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters.”

**INDUCTOR DESIGN**
Inductor Design

Freedoms:
1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

Constraints:
1. Obtain Designed $L$
2. Prevent Saturation
3. Minimize Losses

Minimization of Losses

• For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance

• A minimum sum of the two exists and can be solved

• Design always subject to constraint $B_{\text{max}} < B_{\text{sat}}$
Spreadsheet Design

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

Matlab (Programmatic) Design

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation
Closed-Form Design Methods

- Fundamentals of Power Electronics Ch 13-15
  - Step-by-Step design methods
  - Simplified, and may require additional calculations

*Kg* and *Kgfe* Methods

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) Steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

<table>
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<tr>
<th></th>
<th><em>Kg</em></th>
<th><em>Kgfe</em></th>
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<tr>
<td>Losses</td>
<td>DC Copper (specified)</td>
<td>DC Copper, SE Core Loss (optimized)</td>
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<td>Saturation</td>
<td>Specified</td>
<td>Checked After</td>
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<tr>
<td><em>B</em>&lt;sub&gt;max&lt;/sub&gt;</td>
<td>Specified</td>
<td>Optimized</td>
</tr>
</tbody>
</table>
**$K_g$ Method**

- Method useful for filter inductors where $\Delta B$ is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired $B_{max}$ is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website

The following quantities are specified, using the units:

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wire resistivity</td>
<td>$\rho$ (Ω·cm)</td>
</tr>
<tr>
<td>Peak winding current</td>
<td>$I_{max}$ (A)</td>
</tr>
<tr>
<td>Inductance</td>
<td>$L$ (H)</td>
</tr>
<tr>
<td>Winding resistance</td>
<td>$R$ (Ω)</td>
</tr>
<tr>
<td>Winding fill factor</td>
<td>$K_w$</td>
</tr>
<tr>
<td>Core maximum flux density</td>
<td>$B_{max}$ (T)</td>
</tr>
</tbody>
</table>

The core dimensions are expressed in cm:

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core cross-sectional area</td>
<td>$A_c$ (cm²)</td>
</tr>
<tr>
<td>Core window area</td>
<td>$W_A$ (cm²)</td>
</tr>
<tr>
<td>Mean length per turn</td>
<td>$MLT$ (cm)</td>
</tr>
</tbody>
</table>

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} \times 10^8 \text{ (cm}^5)$$

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} \times 10^4 \text{ (m)}$$

$$n = \frac{L I_{max}}{B_{max} A_c} \times 10^4$$

$$A_w \leq \frac{K_u W_A}{n} \text{ (cm}^2)$$

$$R = \frac{\rho n (MLT)}{A_w} \text{ (Ω)}$$
**$K_{gfe}$ Method**

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized

**$K_{gfe}$ Procedure**

The following quantities are specified, using the units noted:

- Wire effective resistivity $\rho$ (Ω·cm)
- Total rms winding current, ref to pri $I_{tot}$ (A)
- Desired turns ratios $n_2/n_1$, $n_3/n_1$, etc.
- Applied pri volt-sec $\lambda_1$ (V·sec)
- Allowed total power dissipation $P_{tot}$ (W)
- Winding fill factor $K_u$
- Core loss exponent $\beta$
- Core loss coefficient $K_{fe}$ (W/cm³·T³)

Other quantities and their dimensions:

- Core cross-sectional area $A_c$ (cm²)
- Core window area $W_A$ (cm²)
- Mean length per turn $MLT$ (cm)
- Magnetic path length $\ell_e$ (cm)
- Wire areas $A_{w,1}$, ... (cm²)
- Peak ac flux density $\Delta B$ (T)
\[ K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{2/\beta}}{4K_u (P_{tot})^{(\beta + 2)/\beta}} \times 10^8 \]

\[ \Delta B = \left| 10^8 \frac{\rho \lambda_1^2 I_{tot}^2 (MLT)}{2K_u W_A A_c L_m} \frac{1}{\beta K_{fe}} \right| \]

\[ n_1 = \frac{\lambda_1}{2\Delta B A_c} \times 10^4 \quad n_k = n_1 \frac{n_k}{n_1} \]

\[ \alpha_k = \frac{n_k I_k}{n_1 I_{tot}} \quad A_{wk} \leq \frac{\alpha_k K_u W_A}{n_2} \]

Verify

**\( K_{gfe} \) Method: Summary**

- Method enforces an operating \( \Delta B \) in which core and copper losses are minimized.
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal.
- Does not consider high frequency losses.
- Step-by-step design procedure included on website.