Announcements

• Tuesday:
  – Complete experiment #2
  – Experiment #1 report due

• Thursday:
  – Prelab #3 due (start of class)
  – Experiment #2 signoff (if not completed Tuesday)

• All assignments turned in digitally
  – By e-mailing to Daniel.costinett@utk.edu
  – Include [ECE 482] in the subject

• Parts kit purchased prior to Tuesday’s class

• Capture waveforms, even if something is malfunctioning, for report

Outline

1. Experiment 3 Introduction
2. Power Converter Layout
3. Loss Analysis and Design
   – Low Frequency Conduction Losses
   – Inductor AC Losses
   – Core Losses
   – Inductor Design Approaches
**Prelab Assignment**

**Experiment 3**  
**ECE 482**

Fig. 1 shows the power stage of the drivetrain boost converter to be assembled in experiment 3. For all parts of this prelab, consider operation of the converter at an operating point around which:

- $V_{bat} = 25$ V
- $V_{bus} \leq 50$ V
- $5$ kHz $\leq f_s \leq 1$ MHz
- $\Delta v_{out} \leq 1$ V

**Figure 1:** Open loop boost converter (implementation shown with MOSFET devices)
Design Assessment

In experiment 3, a portion of your grade will be the performance of the design that you choose to build. A 20% segment of the lab grade will be determined by the following formula, which rewards designs with small size, high efficiency, and high power capability:

\[
\text{Grade} \, [\%] = 25 - \kappa_{\text{core}} - 100 \cdot (0.98 - \eta_{\text{Fmax}=100}) - \left| \frac{P_{\text{max}} - 250}{50} \right|
\]

where

\[
\kappa_{\text{core}} = \begin{cases} 
0, & \text{ETD29/ EFD25} \\
3, & \text{ETD39} \\
6, & \text{ETD44} \\
9, & \text{ETD49} 
\end{cases}
\]

According to the inductor core you have chosen for your design. \(P_{\text{max}}\) is the maximum power tested, which must be at least 100W, and may be as high as 250W.

Boost Design

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1N5401X01</td>
<td>X</td>
<td>60 V, 10 A, Fast RECTIFIER</td>
</tr>
<tr>
<td>AOT2501L</td>
<td>X</td>
<td>150 V, 150 A, High Voltage Trench MOSFET</td>
</tr>
<tr>
<td>FDP9611MA</td>
<td>X</td>
<td>150 V, 117 A PowerTrench MOSFET</td>
</tr>
<tr>
<td>IPP300U33N3</td>
<td>X</td>
<td>150 V, 50 A OptMOS Power MOSFET</td>
</tr>
<tr>
<td>n6f45401pbf</td>
<td>X</td>
<td>150 V, 35 A HEXFET Power MOSFET</td>
</tr>
<tr>
<td>FGPF30N12HT</td>
<td>X</td>
<td>330 V, PDP Trench IGBT</td>
</tr>
<tr>
<td>ISL5935030D</td>
<td>X</td>
<td>400 V, N-Channel IGBT</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Core Geometry</th>
<th>Material</th>
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<tbody>
<tr>
<td>ETD29</td>
<td>Ferrotec 3C90</td>
</tr>
<tr>
<td></td>
<td>Ferrotec 3F3</td>
</tr>
<tr>
<td>ETD39</td>
<td>Ferrotec 3C90</td>
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<td>Ferrotec 3F3</td>
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<tr>
<td>ETD44</td>
<td>Ferrotec 3C90</td>
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<td>Ferrotec 3F3</td>
</tr>
<tr>
<td>ETD49</td>
<td>Ferrotec 3C90</td>
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<tr>
<td></td>
<td>Ferrotec 3F3</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Wire Gauge</th>
<th>Diameter [cm]</th>
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<tbody>
<tr>
<td>AWG 10</td>
<td>0.267</td>
</tr>
<tr>
<td>AWG 12</td>
<td>0.213</td>
</tr>
<tr>
<td>AWG 14</td>
<td>0.171</td>
</tr>
<tr>
<td>AWG 16</td>
<td>0.137</td>
</tr>
<tr>
<td>AWG 20</td>
<td>0.0874</td>
</tr>
</tbody>
</table>

Full AWG table
Power Converter Layout: Buck Example

Use loop analysis

- Switched input current $i_1(t)$ contains large high frequency harmonics
  - Hence inductance of input loop is critical
- Inductance causes ringing, voltage spikes, switching loss, generation of B- and E-fields, radiated EMI

- The second loop contains a filter inductor, and hence its current $i_2(t)$ is nearly dc
  - Hence additional inductance is not a significant problem in the second loop
Parasitic Wire Inductances

Parasitic inductances of input loop explicitly shown:

Addition of bypass capacitor confines the pulsating current to a smaller loop:

High frequency currents are shunted through capacitor instead of input source

Loop Minimization

Even better: minimize area of the high frequency loop, thereby minimizing its inductance

B fields nearly cancel

Loop area $A_c$
Effect of Loop Inductance

\[ L_{\text{loop}} = 1.6\,\text{nH} \]

\[ L_{\text{loop}} = 0.4\,\text{nH} \]

- Gate driver chip must implement \( v_{gs} \) waveforms
- Sources will have pulsating currents and need decoupling
Driving a Power MOSFET Switch

- MOSFET is off when \( v_{gs} < V_{th} \approx 3 \text{ V} \)
- MOSFET fully on when \( v_{gs} \) is sufficiently large (10-15 V)
- Warning: MOSFET gate oxide breaks down and the device fails when \( v_{gs} > 20 \text{ V} \).
- Fast turn on or turn off (10’s of ns) requires a large spike (1-2 A) of gate current to charge or discharge the gate capacitance
- MOSFET gate driver is a logic buffer that has high output current capability

![MOSFET Diagram](image)

Driving a Power MOSFET Switch

- MOSFET gate driver is used as a logic buffer with high output current (~1.8 A) capability
- The amplitude of the gate voltage equals the supply voltage \( VCC \)
- Decoupling capacitors are necessary at all supply pins of LM5104 (and all ICs)
- Gate resistance used to slow \( dv/dt \) at switch node
Gate Drive Implementation

- Gate driver is cascaded half-bridges of increasing size to obtain quick rise times
- Reminder: keep loops which handle pulsating current small by decoupling and making close connections

Decoupling

- Always add bypass capacitor at power supply for any IC/reference
- Use small-valued (~100nf), low ESR and ESL capacitors (ceramic)
- Limit loop for any di/dt
Decoupling

IC

V_{DD}

GND

Capacitor Sizing – Filter Caps

Capacitor Sizing – Pulsed Caps

- Area of current pulse is total charge supplied to gate of capacitor
- All charge must be supplied from gate drive decoupling capacitor

High Side Signal Ground

- Gate driver chip must implement $v_{gs}$ waveforms
- Issue: source of $Q_2$ is not grounded
• Isolated supplies sometimes used; Isolated DC-DC, batteries
• Bootstrap concept: capacitor can be charged when $V_s$ is low, then switched

UCC27211a Internal Diagram
<table>
<thead>
<tr>
<th>Direct Drive</th>
<th>Easiest high-side application the MOSFET and can be driven directly by the PWM controller or by a ground referenced driver, but it must meet two conditions, as follows: ( V_{CC} &lt; V_{gs,MAX} ) and ( V_{DC} &lt; V_{CC} - V_{gs,MIN} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating Supply Gate Drive</td>
<td>Cost impact of isolated supply is significant. Optocoupler tends to be relatively expensive, limited in bandwidth, and noise sensitive.</td>
</tr>
<tr>
<td>Transformer Coupled Drive</td>
<td>Gives full gate control for an indefinite period of time, but is somewhat limited in switching performance. This can be improved with added complexity.</td>
</tr>
<tr>
<td>Charge Pump Drive</td>
<td>The turn-on times tend to be long for switching applications. Inefficiencies in the voltage multiplication circuit may require more than low stages of pumping.</td>
</tr>
<tr>
<td>Bootstrap Drive</td>
<td>Simple and inexpensive with limitations; such as, the duty cycle and on-time are both constrained by the need to refresh the bootstrap capacitor. Requires level shift, with the associated difficulties.</td>
</tr>
</tbody>
</table>

**A Note on Grounding**

Fairchild Semi App Note AN-6076
Parasitics to be Aware of

Power Loop Inductances

Persson E., “What really limits MOSFET performance: silicon, package, driver or circuit board?”
Complete Routing of Signal

- Always consider return path
- Ground plane can help, but still need to consider the path and optimize

Star-Grounding Vs. Daisy Chain

Figure 9. Separate the Input Current Paths Among Supplies
Kelvin Connection

Efficiency Measurement

Boost Converter
High Impedance Nodes

POWER CONVERTER DESIGN AND LOSS ANALYSIS
Analytical Loss Modeling

• High efficiency approximation is acceptable for hand calculations, as long as it is justified
  • Solve ideal waveforms of lossless converter, then calculate losses
  • Argue which losses need to be included, and which may be neglected
    • “Rough” approximation to gain insight into significance
Additional Recorded Lectures

- ECE581
  - [http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php](http://web.eecs.utk.edu/~dcostine/ECE581/Fall2016/schedule.php)
    - Switching Overlap Loss L4-L5
    - Device Capacitances L6-L7
    - Magnetics Losses L19-L20

- ECE 481
  - [http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php](http://web.eecs.utk.edu/~dcostine/ECE481/Fall2017/schedule.php)
    - Switching Loss L13
    - Magnetics Design L37-39

Boost Converter Loss Analysis

• Begin by solving important waveforms throughout converter assuming lossless operation
## Power Stage Losses

<table>
<thead>
<tr>
<th>Low-Frequency Losses</th>
<th>MOSFETS</th>
<th>Body Diodes</th>
<th>Inductor</th>
<th>Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{on} )</td>
<td>( V_F )</td>
<td>( R_{dc} )</td>
<td>( ESR )</td>
<td></td>
</tr>
<tr>
<td>( V_F )</td>
<td>( R_d )</td>
<td></td>
<td></td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Frequency-Dependent Losses</th>
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<th></th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td>( C_{oss} )</td>
<td>( T_d ) cond.</td>
<td>( C_d )</td>
<td>Skin Effect</td>
<td>Dielectric Losses</td>
</tr>
<tr>
<td>( \text{Overlap} )</td>
<td>( \text{Reverse-Recovery} )</td>
<td></td>
<td>Core Loss</td>
<td>Losses</td>
</tr>
<tr>
<td>( P_g )</td>
<td></td>
<td></td>
<td>Fringing</td>
<td></td>
</tr>
</tbody>
</table>

**LOW FREQUENCY CONDUCTION LOSSES**
MOSFET Equivalent Circuit

- Considering only power stage losses (gate drive neglected)
- MOSFET operated as power switch
- Intrinsic body diode behaviors considered using normal diode analysis

Datasheet Interpretation

- On resistance extracted from datasheet waveforms
- Significantly dependent on $V_{gs}$ amplitude, temperature
Boost Converter RMS Currents

- MOSFET conduction losses due to \( (r_{ds})_{on} \) depend given as

\[
P_{\text{cond,FET}} = I_{di,rms}^2 (r_{ds})_{on}
\]

MOSFET Conduction Losses

Pulsating waveform with linear ripple, Fig. A.6:

\[
rms = I \sqrt{D} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta i}{I} \right)^2}
\]

(A.6)

- RMS values of commonly observed waveforms appendix from Power Book
Capacitor Loss Model

- Operation well below resonance
- All loss mechanisms in a capacitor are generally lumped into an empirical loss model
- Equivalent Series Resistance (ESR) is *highly* frequency dependent
- Datasheets may give effective impedance at a frequency, or loss factor:
  \[ \delta = \frac{\pi}{2} - \theta \]
  \[ D = \tan(\delta) \]

DC Inductor Resistance

- DC Resistance given by
  \[ R_{DC} = \rho \frac{l_b}{A_w} \]
- At room temp, \( \rho = 1.724 \cdot 10^{-6} \, \Omega \text{-cm} \)
- At 100°C, \( \rho = 2.3 \cdot 10^{-6} \, \Omega \text{-cm} \)
- Losses due to DC current:
  \[ P_{cu,DC} = I_{L,rms}^2 R_{DC} \]
Inductor Conduction Losses

DC plus linear ripple, Fig. A.2:

\[ \text{rms} = I \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I}{I} \right)^2} \]  \hfill (A.2)

- Conduction losses dependent on RMS current through inductor

Switching Loss
Switching Loss Modeling

Dead Time Selection
Types of Switching Loss

1. Gate Charge Loss
2. Overlap Loss
3. Capacitive Loss
4. Body Diode Conduction
5. Reverse Recovery
6. Parasitic Inductive Losses
7. Anomalous Losses

Gate Drive Losses

\[ E_{loss} = q_{gate}V_{DD} \]
\[ P_{sw,g} = E_{loss}f_s \]

- Gate charge is supplied through driver resistance during switch turn-on
- Gate charge is dissipated in gate driver on switch turn-off
Gate Charge Loss

9 Typ. gate charge
$V_{ds} = f(Q_{g}, t)$; $I_d = 5.2$ A pulsed
parameter: $V_{cc}$

$P_g = Q_g V_{cc} f_s$

Overlap Loss

$P_{overlap} = \frac{1}{2} I_L V_L \frac{t_{on}}{T_s}$
Lump Switched Node Capacitance

- Consider a single equivalent capacitor at switched node which combines energy storage due to all four semiconductor devices.

Diode Loss Model

- Example loss model includes resistance and forward voltage drop extracted from datasheet.
Diode Reverse Recovery

- FET body diodes may turn on during dead time intervals
- Significant reverse recovery losses possible

\[ E_{on,rr} = \left( (I_L - \Delta I_L) t_{rr} + Q_{rr} \right) V_{bus} \]

Reverse Recovery - Datasheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
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<tbody>
<tr>
<td>Dynamic Characteristics</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Reverse recovery time</td>
<td>( t_{rr} )</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=25^\circ C )</td>
<td></td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=125^\circ C )</td>
<td></td>
<td>185</td>
<td></td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=150^\circ C )</td>
<td></td>
<td>195</td>
<td></td>
</tr>
<tr>
<td>Reverse recovery charge</td>
<td>( Q_{rr} )</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=25^\circ C )</td>
<td></td>
<td>1400</td>
<td></td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=125^\circ C )</td>
<td></td>
<td>2650</td>
<td></td>
</tr>
<tr>
<td>( V_R = 400V, I_f = 45A, \text{dip/dt}=1000A/\mu s, T_j=150^\circ C )</td>
<td></td>
<td>2900</td>
<td></td>
</tr>
</tbody>
</table>

5 Typ. reverse recovery time
\( t_{rr} = f(\text{dip/dt}) \)

parameter: \( V_R = 400V, T_j = 125^\circ C \)
Reverse Recovery – Rough Approximations

- \( E_{rr} \approx E_{rr\_datasheet} \frac{I_F}{I_{F\_datasheet}} \frac{V_{DC}}{V_{DC\_datasheet}} \)
- **Rough** approximation with \( I_F \ll I_{max} \)

**INDUCTOR AC LOSSES**
Skin Effect in Copper Wire

- Current profile at high frequency is exponential function of distance from center with characteristic length $\delta$

AC Resistance

$$A_{w,eff} = \pi r_w^2 - \pi (r_w - \delta)^2$$

$$R_{ac} = \rho \frac{l_b}{A_{w,eff}}$$
Skin Depth

Fig. 13.23 Penetration depth $\delta$, as a function of frequency $f$, for copper wire.

Proximity Effect

- In foil conductor closely spaced with $h >> \delta$, flux between layers generates additional current according to Lentz’s law.

$$P_1 = I_{L, rms}^2 R_{ac}$$

- Power loss in layer 2:

$$P_2 = I_{L, rms}^2 R_{ac} + (2I_{L, rms})^2 R_{ac}$$

$$P_2 = 5P_1$$

- Needs modification for non-foil conductors

See Fundamentals of Power Electronics, Section 13.4
Simulation Example

- AWG#30 copper wire
  - Diameter \( d = 0.294 \text{ mm} \)
  - \( d = \delta \) at around 50 kHz
- 1:1 transformer
  - Primary and secondary are the same, 30 turns in 3 layers
- Sinusoidal currents,
  \[ l_{1\text{rms}} = l_{2\text{rms}} = 1 \text{ A} \]

Numerical field and current density solutions using FEMM (Finite Element Method Magnetics), a free 2D solver, http://www.femm.info/wiki/HomePage
Frequency: 1 kHz

Frequency: 100 kHz

Total copper losses 1.8 larger than at 1 kHz
Frequency: 1 MHz

Total copper losses 20 times larger than at 1 kHz

Frequency: 10 MHz

Very significant proximity effect
Total copper losses = 65 times larger than at 1 KHz
Fringing

- Near air gap, flux may bow out significantly, causing additional eddy current losses in nearby conductors.

Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material.
- Both Hysteresis and Eddy Current losses occur from domain wall shifting.
Inductor Core Loss

- Governed by Steinmetz Equation:

\[ P_v = K_{fe} f_s^\alpha (\Delta B)^\beta \text{ [mW/cm}^3\text{]} \]

- Parameters \( K_{fe}, \alpha, \) and \( \beta \) extracted from manufacturer data

\[ P_{fe} = P_v A_c l_m \text{ [mW]} \]

- \( \Delta B \propto \Delta i_L \rightarrow \) small losses with small ripple

Steinmetz Parameter Extraction

Fig. 6: Specific power loss as a function of peak flux density with frequency as a parameter.

Fig. 7: Specific power loss for several frequency/flux density combinations as a function of temperature.
Ferroxcube Curve Fit Parameters

Power losses in our ferrites have been measured as a function of frequency (f in Hz), peak flux density (B in T) and temperature (T in °C). Core loss density can be approximated (2) by the following formula:

\[ P_{\text{core}} = C_m \cdot f^x \cdot B_{\text{peak}}^y \cdot (ct_0 - ct_1 T + ct_2 T^2) \]  \[ [3] \]

\[ = C_m \cdot C_T \cdot f^x \cdot B_{\text{peak}}^y \quad \text{[mW/cm}^3\text{]} \]

<table>
<thead>
<tr>
<th>ferrite</th>
<th>f (kHz)</th>
<th>Cm</th>
<th>x</th>
<th>y</th>
<th>ct2</th>
<th>ct1</th>
<th>ct0</th>
</tr>
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<tr>
<td>3C30</td>
<td>20-100</td>
<td>7.13.10^-3</td>
<td>1.42</td>
<td>3.02</td>
<td>3.65.10^-4</td>
<td>6.65.10^-2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>100-200</td>
<td>7.13.10^-3</td>
<td>1.42</td>
<td>3.02</td>
<td>4.10^-4</td>
<td>6.8.10^-2</td>
<td>3.8</td>
</tr>
<tr>
<td>3C90</td>
<td>20-200</td>
<td>3.2.10^-3</td>
<td>1.46</td>
<td>2.75</td>
<td>1.65.10^-4</td>
<td>3.1.10^-2</td>
<td>2.45</td>
</tr>
<tr>
<td>3C94</td>
<td>20-200</td>
<td>2.37.10^-3</td>
<td>1.46</td>
<td>2.75</td>
<td>1.65.10^-4</td>
<td>3.1.10^-2</td>
<td>2.45</td>
</tr>
<tr>
<td></td>
<td>200-400</td>
<td>2.10^-3</td>
<td>2.6</td>
<td>2.75</td>
<td>1.65.10^-4</td>
<td>3.1.10^-2</td>
<td>2.45</td>
</tr>
<tr>
<td>3F3</td>
<td>100-300</td>
<td>0.25.10^-3</td>
<td>1.63</td>
<td>2.45</td>
<td>0.79.10^-4</td>
<td>1.05.10^-2</td>
<td>1.26</td>
</tr>
<tr>
<td>300-500</td>
<td>2.10^-3</td>
<td>1.8</td>
<td>2.5</td>
<td>0.77.10^-4</td>
<td>1.05.10^-2</td>
<td>1.28</td>
<td></td>
</tr>
<tr>
<td>500-1000</td>
<td>3.6.10^-4</td>
<td>2.4</td>
<td>2.25</td>
<td>0.67.10^-4</td>
<td>0.81.10^-2</td>
<td>1.14</td>
<td></td>
</tr>
<tr>
<td>3F4</td>
<td>500-1000</td>
<td>1.2.10^-4</td>
<td>1.75</td>
<td>2.9</td>
<td>0.95.10^-4</td>
<td>1.1.10^-2</td>
<td>1.15</td>
</tr>
<tr>
<td>1000-3000</td>
<td>1.1.10^-1</td>
<td>2.8</td>
<td>2.4</td>
<td>0.34.10^-4</td>
<td>0.01.10^-2</td>
<td>0.67</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: Fit parameters to calculate the power loss density

NSE/iGSE

\[ P_{\text{NSE}} = \left( \frac{\Delta B}{2} \right)^{\beta - \alpha} \int_0^T \left| \frac{dB}{dt} \right|^\alpha dt \]

\[ k_N = \frac{k}{\left(2\pi\right)^{\alpha-1}} \int_0^{\pi} \cos^{-\alpha} d\theta \]

Simple Formula for Square-wave voltages:

\[ P_{\text{NSE}} = k_N \cdot (2f)^\phi \left( \Delta B \right)^\beta \left( D^{1-\alpha} + (1-D)^{1-\alpha} \right) \]  \[ (10) \]

where \( f \) is the operating frequency; \( \Delta B / 2 \) is the peak induction; \( D \) is the duty ratio of the square wave voltage.

Note: The second and third harmonics are dominant at moderate values of duty ratio \( D \). For extreme values of \( D \) (95%), a higher value of \( \alpha \) could give better matching to the actual losses.

K. Venkatachalam; C. R. Sullivan; T. Abdallah; H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters”
Inductor Design

Freedoms:
1. Core Size and Material
2. Number of turns and wire gauge
3. Length of Air Gap

Constraints:
1. Obtain Designed $L$
2. Prevent Saturation
3. Minimize Losses
Minimization of Losses

- For given core, number of turns can be used to index possible designs, with air gap solved after (and limited) to get correct inductance

- A minimum sum of the two exists and can be solved

- Design always subject to constraint $B_{\text{max}} < B_{\text{sat}}$

Spreadsheet Design

- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.
Matlab (Programmatic) Design

```
function [n, Ig, Pq1, Pq2, P1, eta, Cmin ] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
% for various designs
% fs = switching frequency (in Hz)
% L = inductance (in Henries)
% n = number of turns on inductor
% dt = switching dead time (in seconds)
% core_geom = core geometry, chosen from 'EFD2S', 'ETD29', 'ETD44', or 'ETD49'
% core_mat = core material, chosen from '3F3', '3C90', or '3F4'
% MOSFET = MOSFET selection, chosen from 'ACT', 'TD', 'IPF2', 'IRF',
% 'CSD', or 'IPF0'
Vg = 25;
Vout = 50;
Iout = Pmax/Vout;
Ts = 1/fs;
D = 1-Vg/Vout;
dVout = 2;
Vdr = 12;
Rgon = 10;
Rgoff = 2;
 rho = 1.724e-6; \text{*cm}\n\text{** Inductor Datasheet Parameters**}

% switch core_geom
\text{case 'EFD2S'}
\text{MLT = 46.4; \text{*mm}}
\text{Ac = 58; \text{*mm}^2}
\text{Ve = 3300; \text{*mm}^3}
\text{Wa = 40.2; \text{*mm}^2}
```

• Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

Closed-Form Design Methods

• Fundamentals of Power Electronics Ch 13-15
  – Step-by-Step design methods
  – Simplified, and may require additional calculations
**$K_g$ and $K_{gfe}$ Methods**

- Two closed-form methods to solve for the optimal inductor design *under certain constraints/assumptions*
- Neither method considers losses other than DC copper and (possibly) steinmetz core loss
- Both methods particularly well suited to spreadsheet/iterative design procedures

<table>
<thead>
<tr>
<th></th>
<th>$K_g$</th>
<th>$K_{gfe}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Losses</td>
<td>DC Copper (specified)</td>
<td>DC Copper, SE Core Loss (optimized)</td>
</tr>
<tr>
<td>Saturation</td>
<td>Specified</td>
<td>Checked After</td>
</tr>
<tr>
<td>$B_{max}$</td>
<td>Specified</td>
<td>Optimized</td>
</tr>
</tbody>
</table>

**$K_g$ Method**

- Method useful for filter inductors where $\Delta B$ is small
- Core loss is not included, but may be significant particularly if large ripple is present
- Copper loss is specified through a set target resistance
- The desired $B_{max}$ is given as a constraint
- Method does not check feasibility of design; must ensure that air gap is not extremely large or wire size excessively small
- Simple first-cut design technique; useful for determining approximate core size required
- Step-by-step design procedure included on website
The following quantities are specified, using the units:

- Wire resistivity $\rho$ (Ω·cm)
- Peak winding current $I_{\text{max}}$ (A)
- Inductance $L$ (H)
- Winding resistance $R$ (Ω)
- Winding fill factor $K_u$
- Core maximum flux density $B_{\text{max}}$ (T)

The core dimensions are expressed in cm:

- Core cross-sectional area $A_c$ (cm²)
- Core window area $W_A$ (cm²)
- Mean length per turn $MLT$ (cm)

\[ K_g = \frac{\rho L^2 I_{\text{max}}^2}{B_{\text{max}}^2 R K_u} \times 10^8 \quad (\text{cm}^5) \]

\[ \ell_g = \frac{\mu_0 L I_{\text{max}}^2}{B_{\text{max}}^2 A_c} \times 10^4 \quad (\text{m}) \]

\[ n = \frac{L I_{\text{max}}}{B_{\text{max}} A_c} \times 10^4 \]

\[ A_w \leq \frac{K_u W_A}{n} \quad (\text{cm}^2) \]

\[ R = \frac{\rho n (MLT)}{A_w} \quad (\Omega) \]

**$K_{gfe}$ Method**

- Method useful for cases when core loss and copper loss are expected to be significant
- Saturation is not included in the method, rather it must be checked afterward
- Enforces a design where the sum of core and copper is minimized
The following quantities are specified, using the units noted:

- Wire effective resistivity \( \rho \) (\( \Omega \cdot \text{cm} \))
- Total rms winding current, ref to pri \( I_{\text{tot}} \) (A)
- Desired turns ratios \( n_{2}/n_1, n_{3}/n_1, \text{etc.} \)
- Applied pri volt-sec \( \lambda_1 \) (V·sec)
- Allowed total power dissipation \( P_{\text{tot}} \) (W)
- Winding fill factor \( K_u \)
- Core loss exponent \( \beta \)
- Core loss coefficient \( K_{fe} \) (W/cm³Tⁿ)

Other quantities and their dimensions:
- Core cross-sectional area \( A_c \) (cm²)
- Core window area \( W_A \) (cm²)
- Mean length per turn \( M\ell_T \) (cm)
- Magnetic path length \( \ell_m \) (cm)
- Wire areas \( A_{w_1}, \ldots \) (cm²)
- Peak ac flux density \( \Delta B \) (T)

\[
K_{gfe} \geq \frac{\rho \lambda_1^2 I_{\text{tot}}^2 K_{fe}^{2(\beta)}}{4K_u P_{\text{tot}}^{(\beta + 2)\beta}} 10^8
\]

\[
\Delta B = \left[ 10^8 \frac{\rho \lambda_1^2 I_{\text{tot}}^2}{2K_u} \frac{M\ell_T}{W_A A_c^3 \ell_m} \frac{1}{\beta K_{fe}} \right]^{\frac{1}{\beta + 2}}
\]

\[
n_1 = \frac{\lambda_1}{2\Delta B A_c} 10^4 \quad n_k = n_1 \frac{n_k}{n_1}
\]

\[
\alpha_k = \frac{n_k I_k}{n_1 I_{\text{tot}}} \quad A_{wk} \leq \frac{\alpha_k K_u W_A}{n_2}
\]

Verify
$K_{gfe}$ Method: Summary

- Method enforces an operating $\Delta B$ in which core and copper losses are minimized.
- Only takes into account losses from standard Steinmetz equation; not correct unless waveforms are sinusoidal.
- Does not consider high frequency losses.
- Step-by-step design procedure included on website.