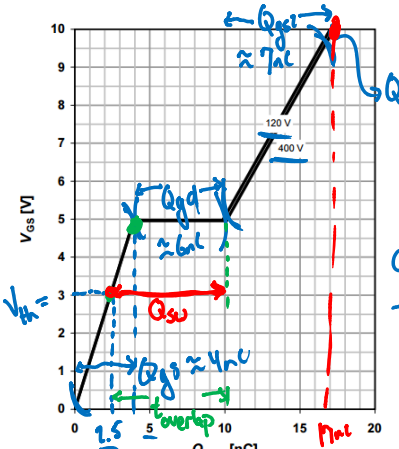
Overlap Time

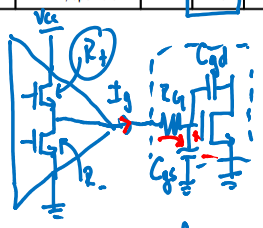
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, I_D=0.34 mA	2.5	3	3.5	
Gate resistance	R_G	f=1 MHz, open drain	-	1.8	-	Ω

9 Typ. gate charge

$V_{GS}=f(Q_{gate})$; I_D=5.2 A pulsed

parameter: V_{DD}

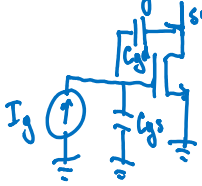


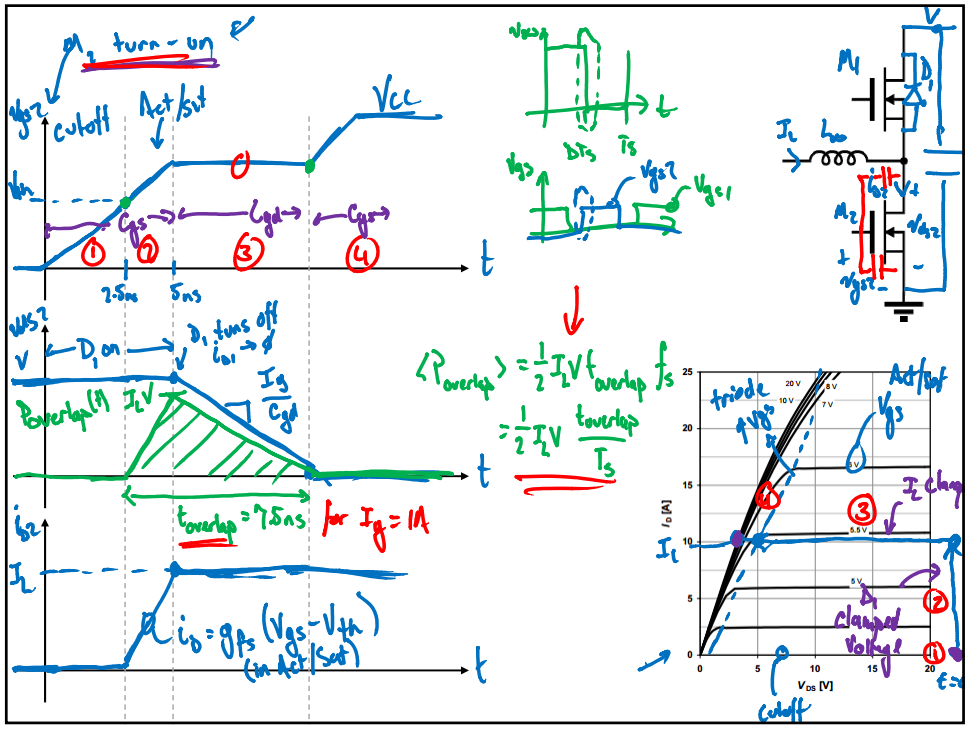


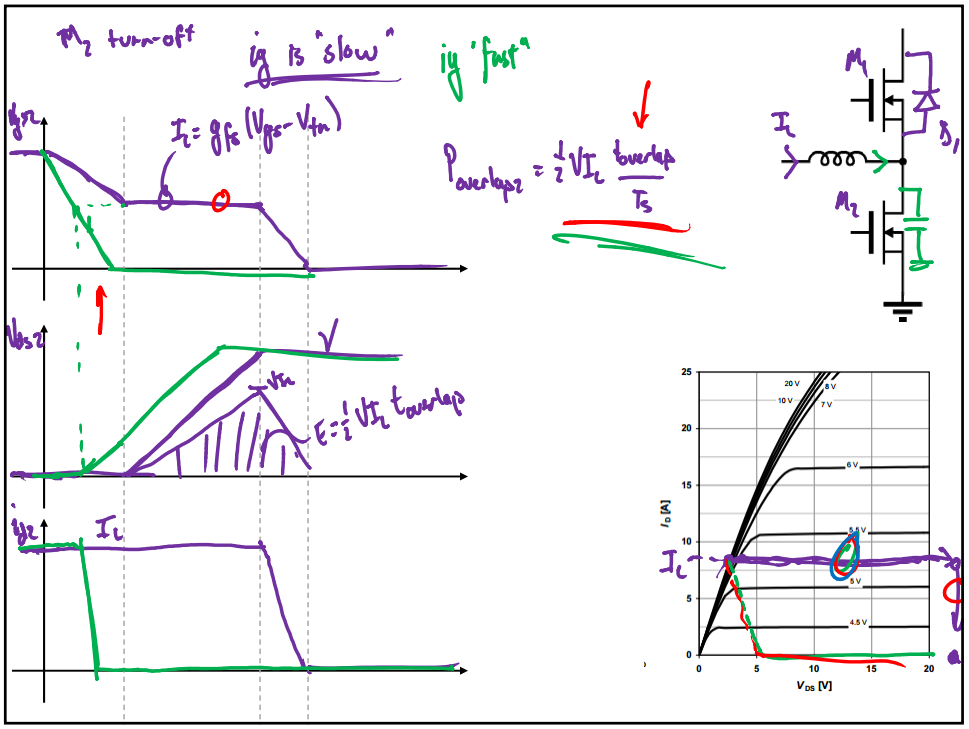
$C_{gd} << C_{gs}$

simplifying Assumption

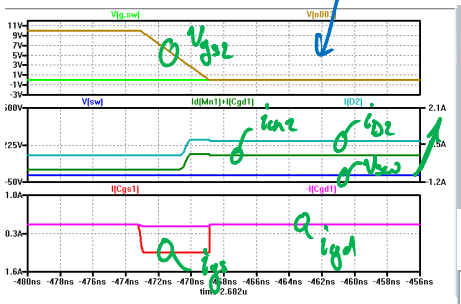
$I_g \approx$ const during switching

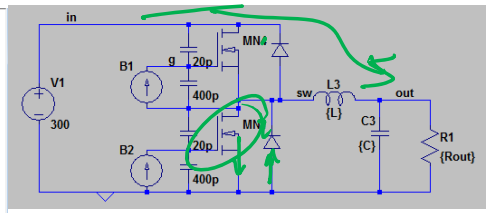


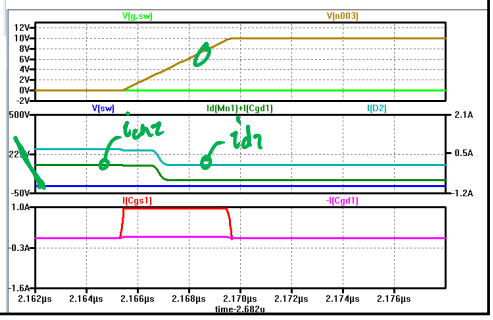




Synchronous MOSFET Overlap







- No Powerlap in synchronous device

Example Calculation

Assume gate driver supplies $\pm I_g$ (or ϕ)

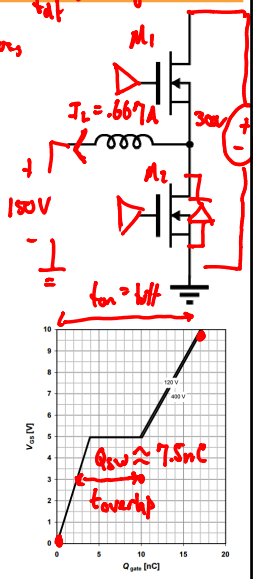
$t_{on} = t_{off} = \frac{Q_g}{I_g}$

$t_{overlap} = \frac{Q_{sw}}{I_g} = \begin{cases} 7.5\text{ ns} & @\ I_g = 1\text{A} \\ 750\text{ ps} & @\ I_g = 10\text{A} \end{cases}$

Worst case:

$P_{overlap} = \frac{1}{2} V_g I_L \frac{t_{overlap}}{T_s}$ (M_1 turn-on) $+ \frac{1}{2} V_g I_L \frac{t_{overlap}}{T_s}$ (M_1 turn-off (worst-case))

$= V_g I_L \frac{Q_{sw}}{I_g T_s} = \begin{cases} 345\text{ mW} & @\ I_g = 1\text{A} \\ 34.5\text{ mW} & @\ I_g = 10\text{A} \end{cases}$



Example Buck Efficiency (L14)

Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=5.2 A, T_j=25 °C	-	0.35	0.385 Ω
		V_{GS}=10 V, I_D=5.2 A, T_j=150 °C	-	0.94	-

$V_g = 300V - 150V$

$\eta \geq 95\%$

$P_{out} = 100W$

$P_{sw} = V_g^2 C_{gd,Q} f_s$

$P_{cond} = i_{1rms}^2 R_{ds,on1} + i_{2rms}^2 R_{ds,on2}$

$= \left(\sqrt{D} I_L\right)^2 R_{ds,on} + \left(\sqrt{1-D} I_L\right)^2 R_{ds,on}$

$= I_L^2 R_{ds,on}$

$I_L = \frac{100W}{150V}$

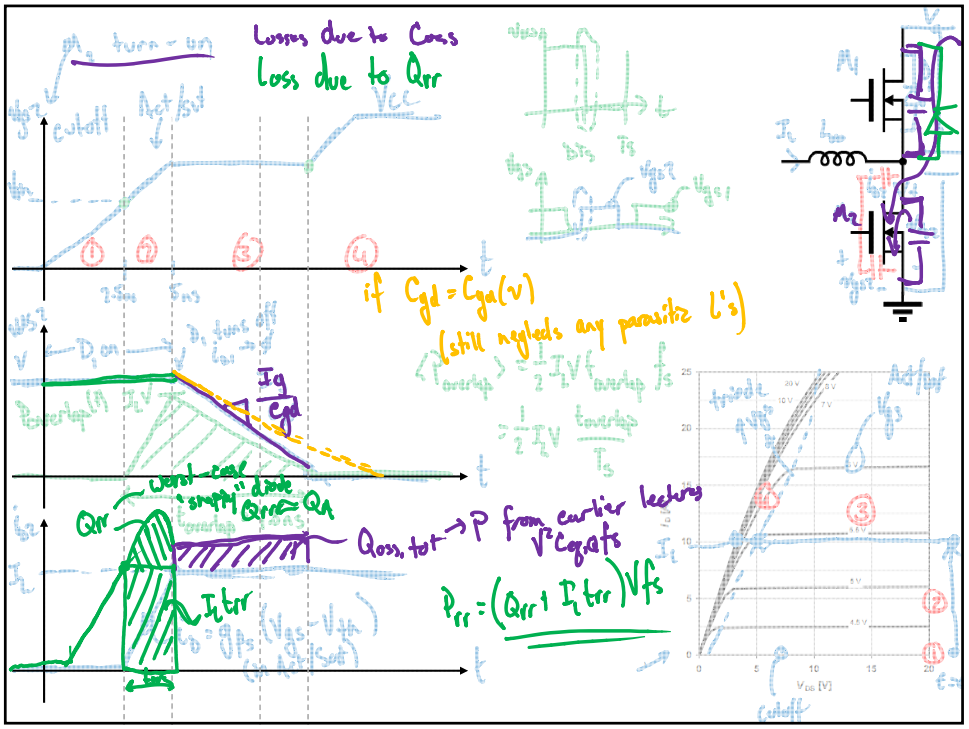
$C_{gd} = 247pF$

$\eta = \frac{P_{out}}{P_{out} + P_{cond} + P_{sw}} = \frac{100W}{100W + \left(\frac{100W}{150V}\right)^2 (.385\Omega) + (300)^2 (247pF) f_s}$

$f_s \leq \frac{\frac{100W}{.95} - 100W - \left(\frac{100W}{150V}\right)^2 (385\Omega)}{(300)^2 (247pF)} = 230\text{ kHz}$

$P_{cond} = I_L^2 R_{on} = 0.171W$

$P_{sw} = V_g^2 C_{gd,Q} f_s = 5.1W$



Switching Loss Summary

For a hard-switched device (MOSFET turns on w/ V_{ds} > 0)

Switching losses:

Coss ⇒ $P = \left(\frac{1}{2} C_{eq,E} V_{DC}^2 + C'_{eq,Q} V_{DC}^2 - \frac{1}{2} C'_{eq,E} V_{DC}^2\right) f_s$

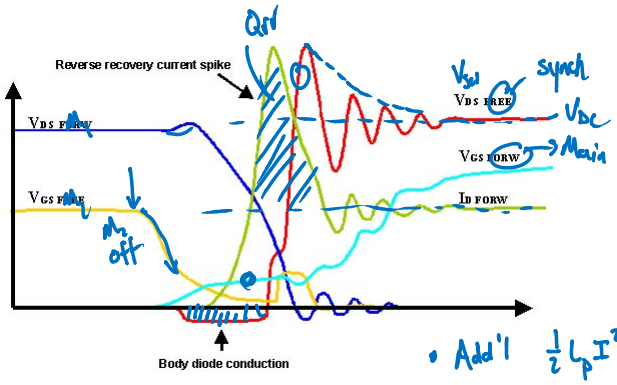
($\frac{1}{2} C_{eq,E} V_{DC}^2$: this device; $C'_{eq,Q} V_{DC}^2 - \frac{1}{2} C'_{eq,E} V_{DC}^2$: opposite device)

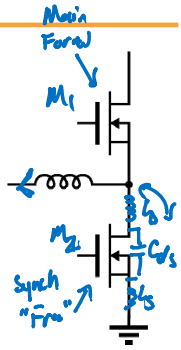
Q_g ⇒ $P_g = V_{GS} Q_g f_s$ → Losses occur in gate drive circuit (occurs 1x for each MOSFET)

V-I overlap ⇒ $P_{overlap} = V_{DC} I_L \frac{t_{overlap}}{T_s}$ → $t_{overlap} = \frac{Q_{sw}}{I_g}$

reverse recovery (if present) ⇒ $P_{rr} = V_{DC}(Q_{rr} + I_L t_{rr}) f_s$

Switching Waveforms





- Add'l $\frac{1}{2} L_p I^2 f_s$-type loss
- Voltage / current overshoot
- slowed down