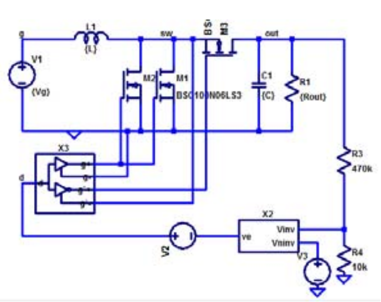
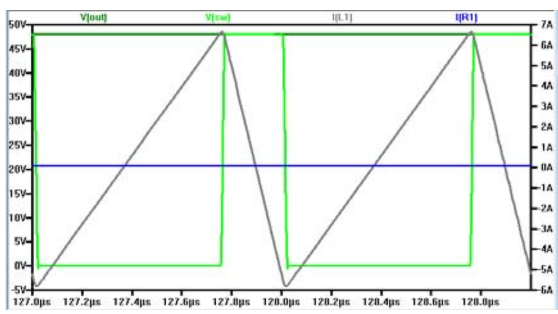
High Frequency Power Electronics

Prof. Daniel Costinett

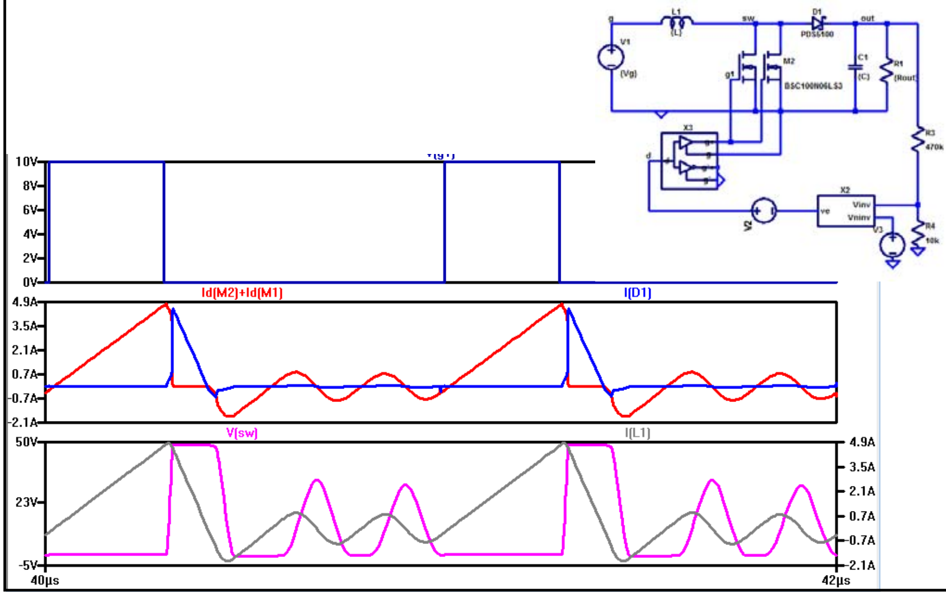
ECE 581 Lecture 4
August 27, 2014

Light Load Operation

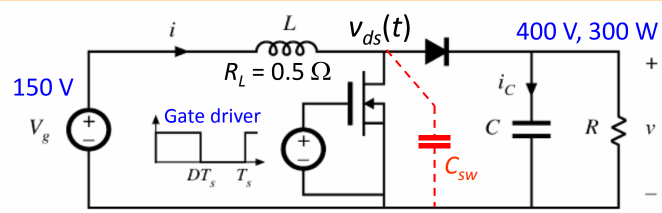




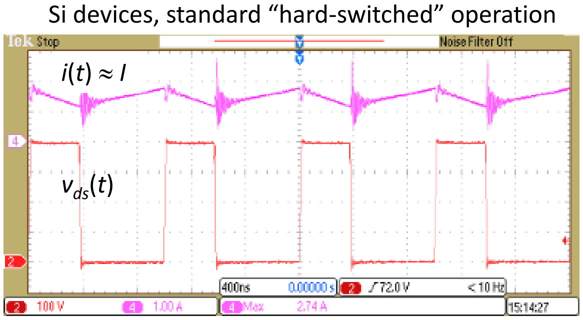
Light Load – Diode Operation



Hard-switched Si devices



Si devices, standard "hard-switched" operation



f_s = 1 MHz

MOSFET

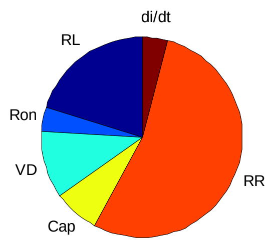
- di_F/dt = 200 A/µs
- $C_{ds,eq}$ = 45 pF
- R_{on} = 0.15 Ω

Si diode

- t_{rr} = 40 ns
- Q_{rr} = 60 nC
- $2C_{d,Qeq}-C_{d,eq}$ = 22 pF
- V_D = 1.5 V

Loss breakdown: Si Boost

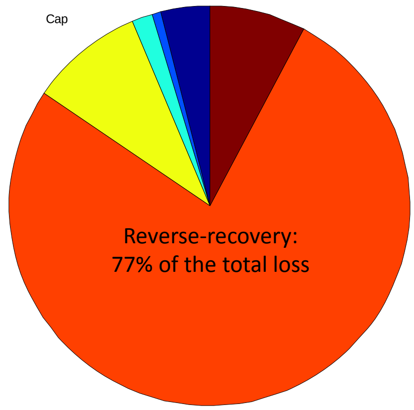
f_s = 100 kHz
P_{loss} = 10.6 W, η = 96.6%



Reverse-recovery:
54% of the total loss

Conduction losses: RL, Ron, VD
Switching losses:
"RR" reverse recovery,
"Cap" C_{sw} discharge

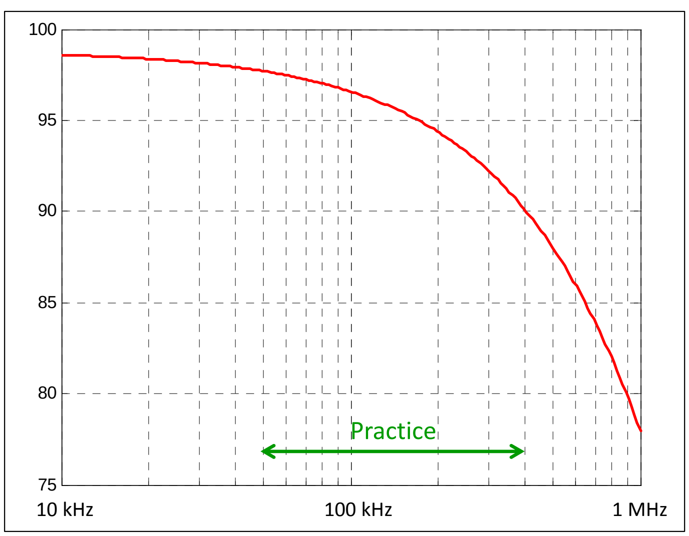
f_s = 1 MHz
P_{loss} = 84.7 W, η = 78.0 %
Experiment*: η = 81.2 %



*Pulsed measurement, continuous operation not feasible due to thermal runaway

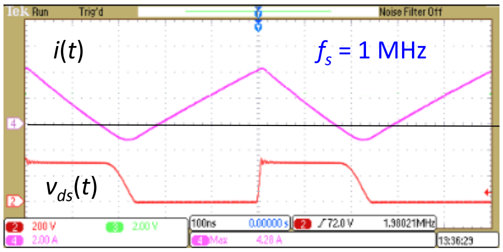
Efficiency: hard-switched Si Boost

η [%]

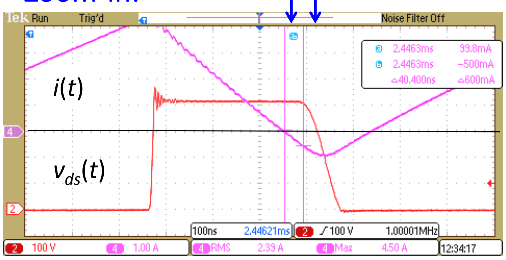


Switching frequency f_s

ZVS with Si diode



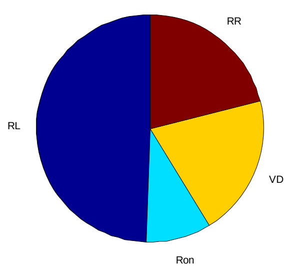
Zoom-in: t_a t_b



- ZVS turn-ON
  - Eliminated losses due to C_{sw} discharge during turn-ON transient
  - Eliminated losses due to MOSFET di_F/dt during turn-ON transient
- Diode reverse recovery still impacts the waveforms and losses
- Increased current ripple
  - Increased conduction losses (by >30%)
  - Increased dv_{ds}/dt upon turn-OFF, MOSFET turn-OFF speed is more important

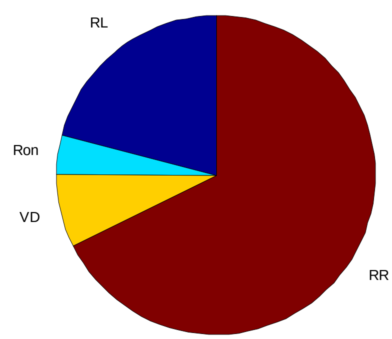
Loss Breakdown: Soft-Switched Si Boost

f_s = 100 kHz
P_{loss} = 5.7 W, η = 98.1%



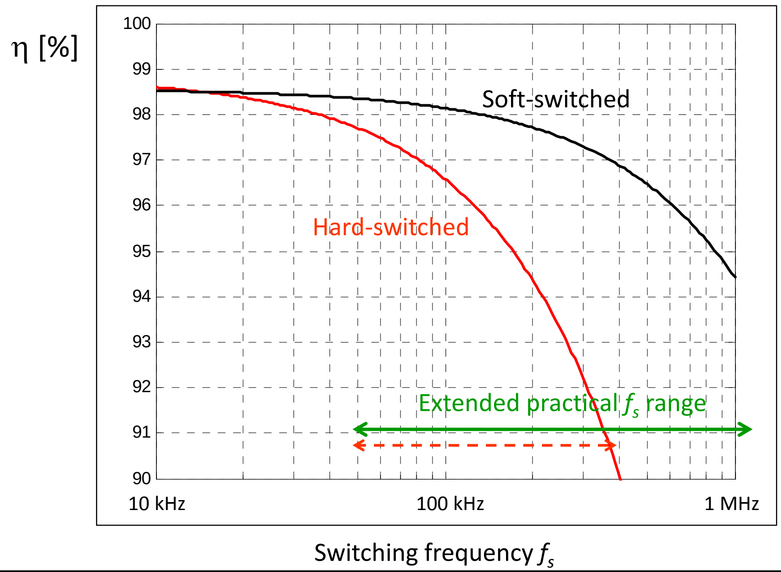
Reverse-recovery:
21% of the total loss

f_s = 1 MHz
P_{loss} = 17.7 W, η = 94.4 %
Experiment: η = 95.1 %

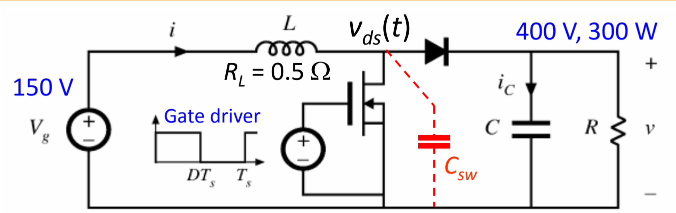


Reverse-recovery:
68% of the total loss

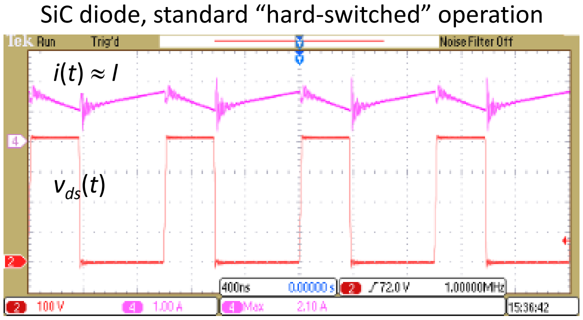
Efficiency: soft-switched Si Boost



Hard-Switched SiC Schottky Diode



SiC diode, standard "hard-switched" operation



f_s = 1 MHz

MOSFET

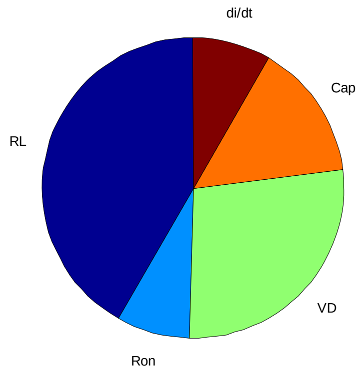
- di_F/dt = 200 A/μs
- $C_{ds,eq}$ = 45 pF
- R_{on} = 0.15 Ω

SiC diode

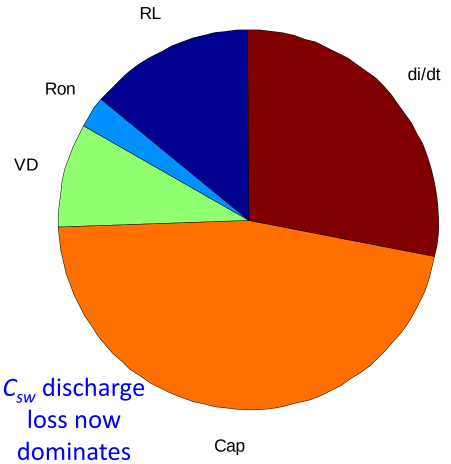
- t_{rr} = 0, Q_{rr} = 0
- $2C_{d,Qeq}$-$C_{d,eq}$ = 64 pF
- V_D = 1.8 V

Loss Breakdown: hard-switched SiC diode

f_s = 100 kHz
P_{loss} = 5 W, η = 98.4%

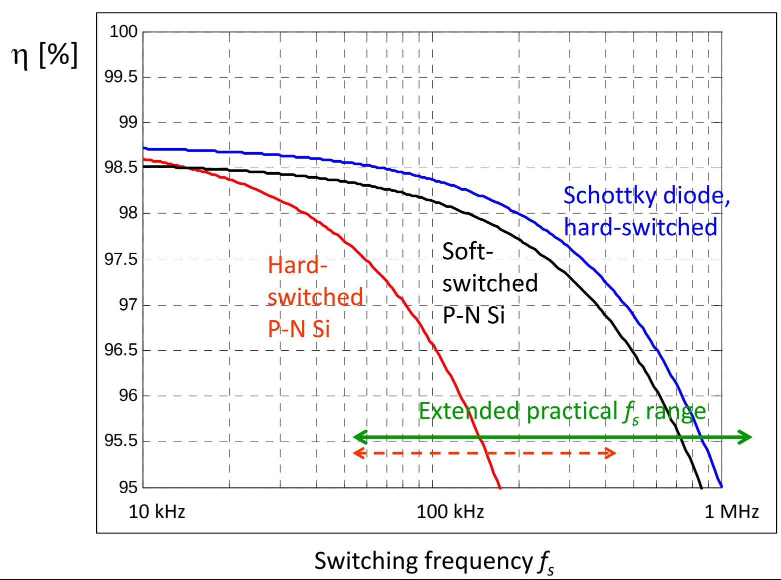


f_s = 1 MHz
P_{loss} = 15.7 W, η = 95.0 %
Experiment: η = 94.7 %

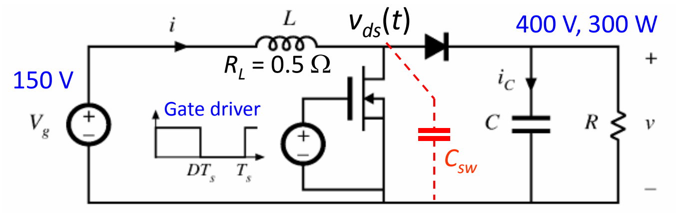


C_{sw} discharge loss now dominates

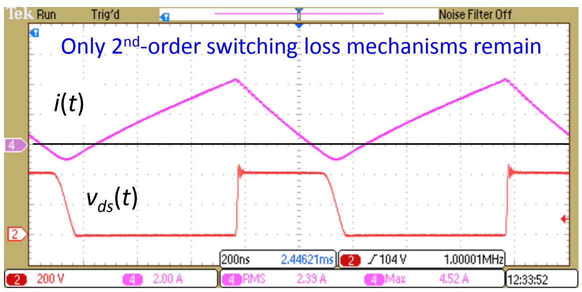
Efficiency comparison



Soft-switched SiC Schottky diode



SiC diode, soft-switched operation



f_s = 1 MHz

MOSFET

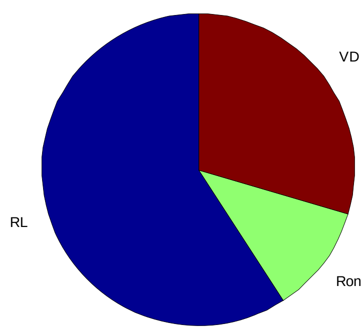
- di_F/dt = 200 A/μs
- $C_{ds,eq}$ = 45 pF
- R_{on} = 0.15 Ω

SiC diode

- t_{rr} = 0, Q_{rr} = 0
- $2C_{d,Qeq}$-$C_{d,eq}$ = 64 pF
- V_D = 1.8 V

Soft-switched Boost with SiC diode

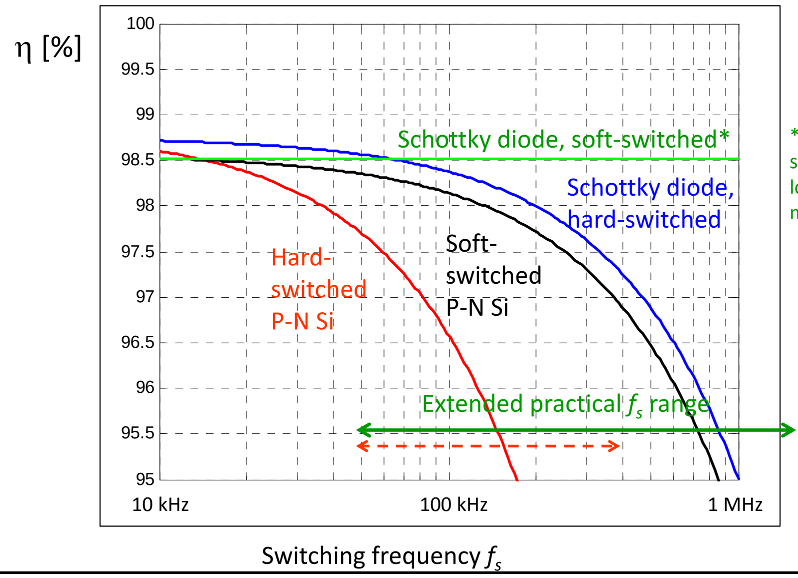
Conduction losses only, 2nd-order switching losses not included in the model



100 kHz or 1 MHz
98.5% efficiency
P_{loss} = 4.5 W

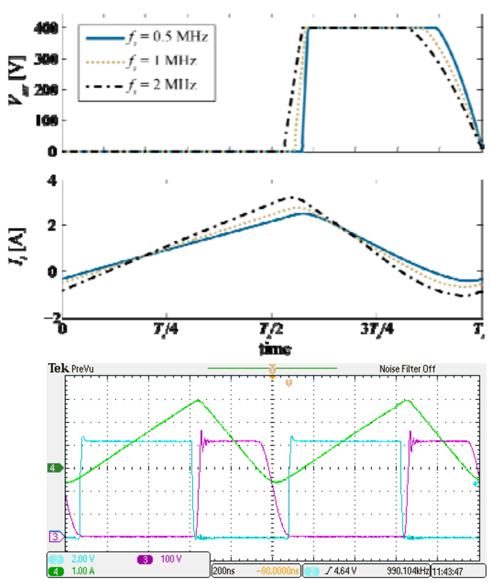
Experiments:
98.7% at 1 MHz
98.0% at 2 MHz

Efficiency comparison



*2nd-order switching losses not modeled

Limitations: t_d/T_s



Limitations: 2nd Order Loss Mechanisms

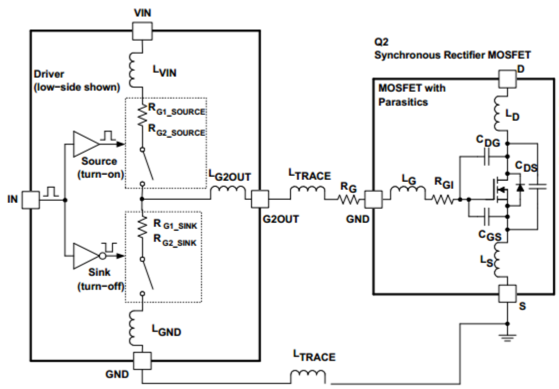
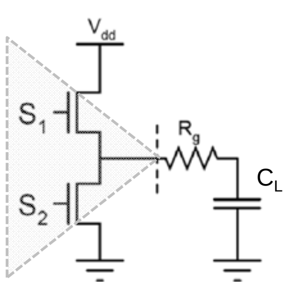


Figure 6. Low-Side Drive and MOSFET Parasitic Model

Texas Instruments, "Optimizing MOSFET Characteristics by Adjusting Gate Drive Amplitude"

Limitations: Gate Drive



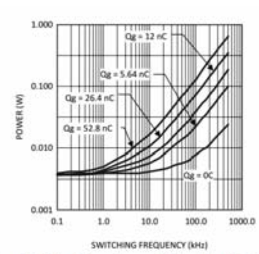


Figure 2. Gate Driver Power Dissipation (LO + HO) V_{CC} = 12V, Neglecting Diode Losses

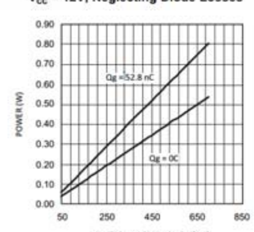
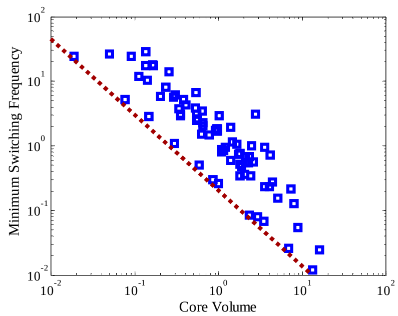
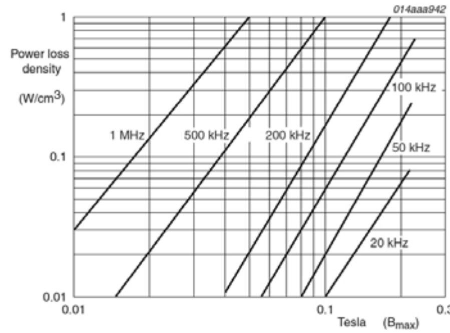


Figure 4. Diode Power Dissipation V_{IN} = 80V

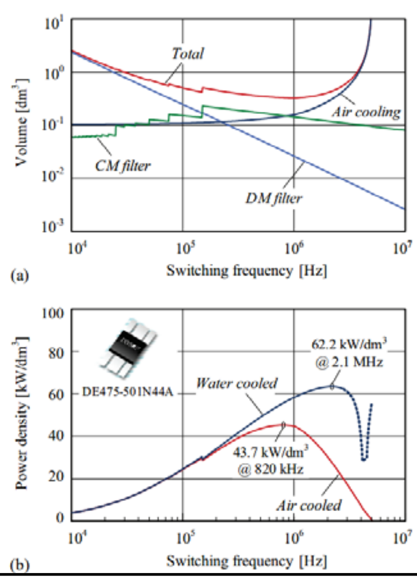
Texas Instruments, "Selection of External Bootstrap Diode for LM510X Devices"

Limitations: Magnetics Design





Limitations: Thermal



Kolar, J.W.; Drofenik, U.; Biela, J.; Heldwein, M.L.; Ertl, H.; Friedli, T.; Round, S.D., "PWM Converter Power Density Barriers," *Power Conversion Conference - Nagoya, 2007. PCC '07* , vol., no., pp.P-9,P-29, 2-5 April 2007