Announcements

- No Lecture Wednesday (& Friday)
- Design Competition Begins Today

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TiNY BOX CHALLENGE

Competition Specifications

The **winning converter** will be the unit which achieves the **highest power density**, i.e. fits in the smallest rectangular volume, while meeting the following specifications.

Parameter	Requirement	Comment
Voltage Input	60 Vdc, 10 Ω series resistor	
Maximum Output Power	60 W	
Output Voltage	12 ± 1 Vdc	
Input Ripple Current	< 5%	Measured as $I_{pk\text{-}pk}/I_{avg}$ from the DC supply, in steady state, at full output power
Output Ripple Voltage	< 2%	Measured as $V_{pk\text{-}pk}/V_{avg}$ from the DC supply, in steady state, at full output power
TPE Efficiency	> 90%	Measured using TPE method[1]
No-load Power Loss	< 3W	Measured with load disconnected, but output voltage within specified range
Volume	< 6 in^3	Volume of minimum rectangle enclosing power stage

[1]Tennessee Power Electronics (TPE) efficiency is a weighted power efficiency defined as:

$$\eta_{TPEF} = 0.1\eta_{Po=15W} + 0.15\eta_{Po=30W} + 0.25\eta_{Po=45W} + 0.5\eta_{Po=60W}$$

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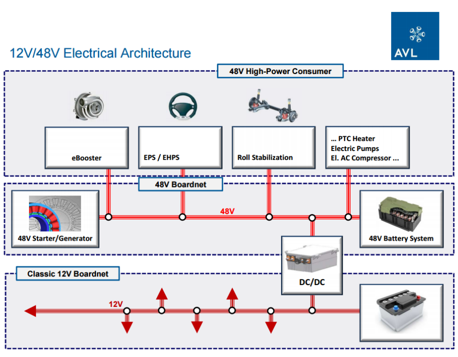
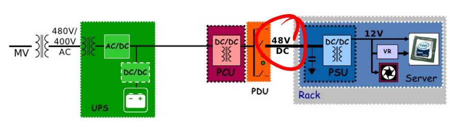
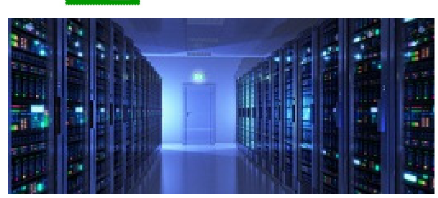
Example Applications

EV 48V Architectures



Data Centers / Telecom





NXP Semi, "Semiconductors – enablers of future mobility concepts", 2011
Audi, "Electric biturbo and hybridization", 2014
AVL, "48V Mild Hybrid Systems"

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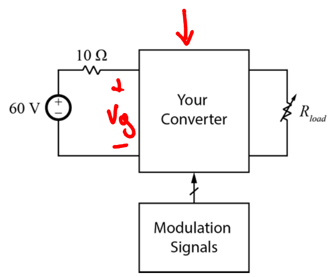
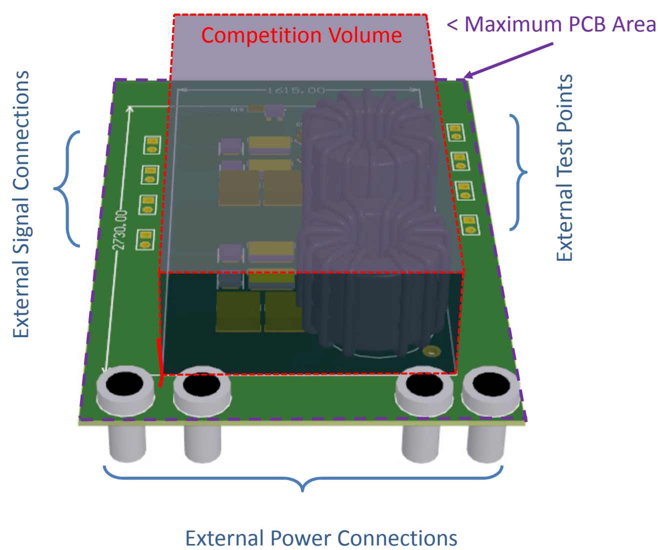
Testing Setup



How Volume is Measured



Schedule

20. Oct. 3 Magnetics Loss Analysis *Tiny Box Challenge Begins*	Oct. 5 *WoW 2016*	Oct. 7 *Fall Break*
21. Oct. 10	Oct. 12	22. Oct. 14 *Homework 6 Due*
23. Oct. 17 *TBC Paper Design Comparison Report Due*	24. Oct. 19	25. Oct. 21 *Homework 7 Due*
26. Oct. 24 *TBC Final Paper Design Report Due*	27. Oct. 26	28. Oct. 28
29. Oct. 31	30. Nov. 2 *TBC PCB Layout Due*	Nov. 4 *Homework 8 Due*
31. Nov. 7 *WiPDA 2016*	32. Nov. 9 *WiPDA 2016*	33. Nov. 11 *Homework 9 Due*
34. Nov. 14	35. Nov. 16	36. Nov. 18 *Homework 10 Due*
37. Nov. 21	38. Nov. 23 *TBC Testing Report Due*	Nov. 25 *Thanksgiving Break*

Additional Details

- Full competition specifications and example testing report on course webpage
- No regulation requirements
- First Deliverable: Monday October 17th
  - Design comparison of 4 topologies

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Magnetics Losses

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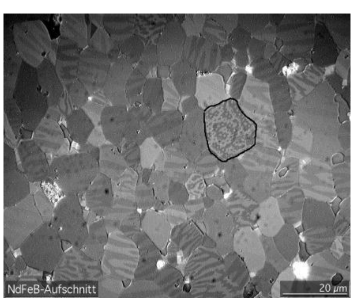
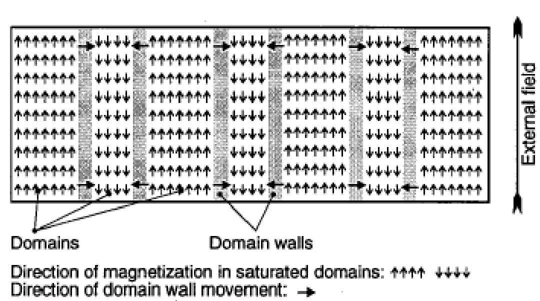
Physical Origin of Core Loss

- Magnetic material is divided into “domains” of saturated material
- Both Hysteresis and Eddy Current losses occur from domain wall shifting





Reinert, J.; Brockmeyer, A.; De Doncker, R.W.; , "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation,"

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Inductor Core Loss

- Governed by Steinmetz Equation:

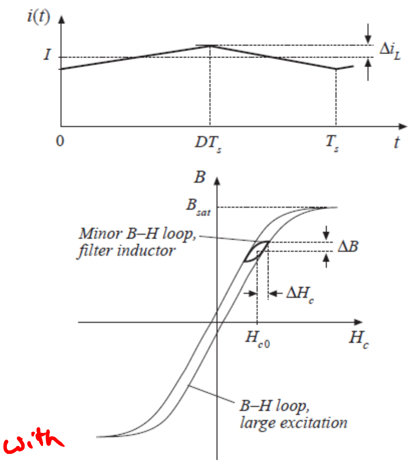
$$P_v = K_{fe} f_s^{\alpha} (\Delta B)^{\beta} \quad [\text{mW/cm}^3]$$

- Parameters K_{fe}, α, and β extracted from manufacturer data

$$P_{fe} = P_v A_c l_m \ [\text{mW}]$$

- Only valid for sinusoidal waveforms

Kfe, α, β vary with frequency



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Steinmetz Parameter Extraction

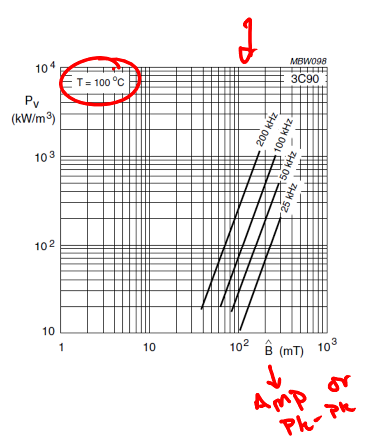

Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

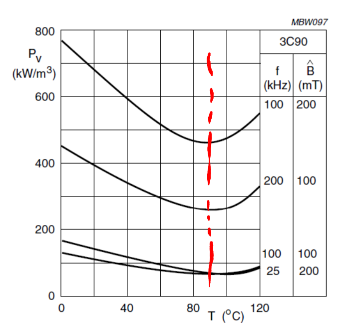

Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

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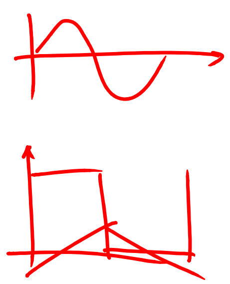
Non-Sinusoidal Waveforms

- Modified Steinmetz Equation (MSE)
  - "Guess" that losses depend on ${}^{dB}/_{dt}$
  - Calculate $\langle {}^{dB}/_{dt} \rangle$ and find frequency of equivalent sinusoid



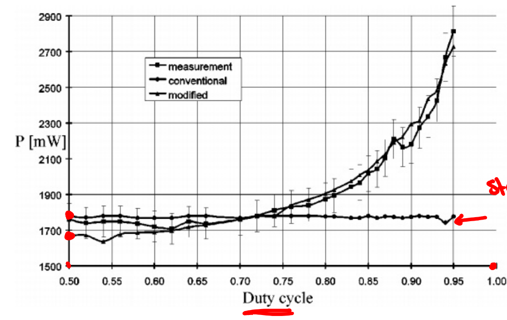


Fig. 8. Comparison between measurement and calculation as a function of duty cycle.

Albach ,Durbau and Brockmeyer, 1996
Reinert, Brockmeyer, and Doncker, 1999

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NSE/iGSE

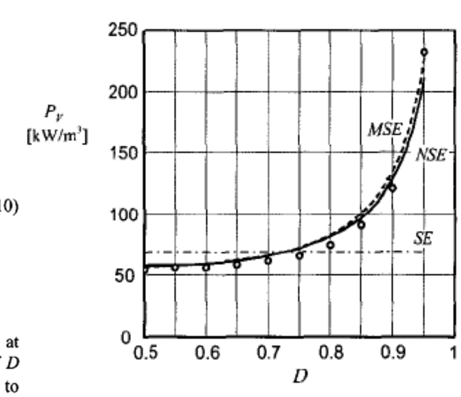
$$P_{NSE} = \left(\frac{\Delta B}{2}\right)^{\beta-\alpha} \frac{k_N}{T} \int_0^T \left|\frac{dB}{dt}\right|^{\alpha} dt \qquad k_N = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} d\vartheta}$$

Simple Formula for Square-wave voltages:

$$P_{NSE} = k_N\,(2f)^{\alpha}\,(\Delta B)^{\beta}\left(D^{1-\alpha} + (1-D)^{1-\alpha}\right) \qquad (10)$$

where f is the operating frequency;
$\Delta B/2$ is the peak induction;
D is the duty ratio of the square wave voltage.

Note: The second and third harmonics are dominant at moderate values of duty ratio D. For extreme values of D (95%), a higher value of α could give better matching to the actual losses.



Van den Bossche, A.; Valchev, V.C.; Georgiev, G.B.; , "Measurement and loss model of ferrites with non-sinusoidal waveforms,"
K. Venkatachalam; C. R. Sullivan; T. Abdallah; H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters"

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Additional Approaches

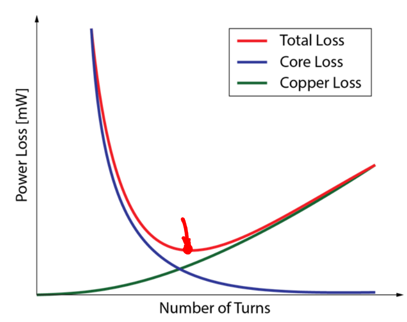
- History of Core Loss Approximation Techniques:

https://engineering.dartmouth.edu/inductor/Sullivan_APEC_2012_core_loss%20overview_with_references.pdf

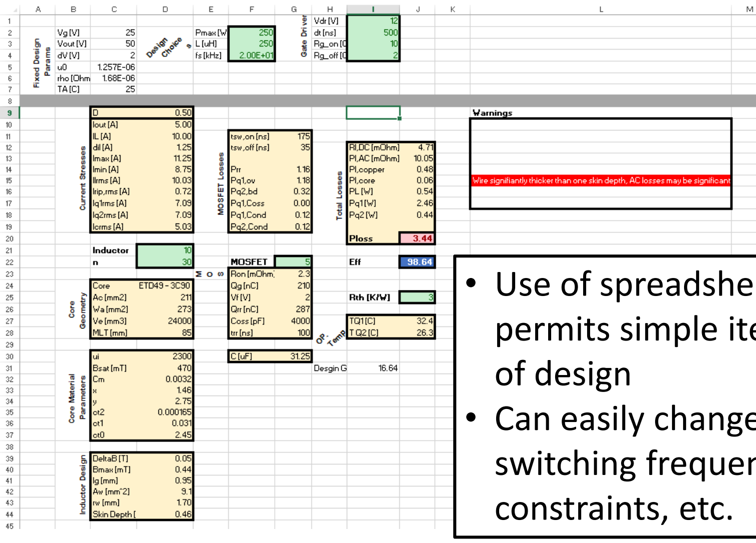
- Seminar on magnetic loss modeling:

https://www.pes.ee.ethz.ch/uploads/tx_ethpublications/APEC2012_MagneticTutorial.pdf

Minimization of Losses



Spreadsheet Design



- Use of spreadsheet permits simple iteration of design
- Can easily change core, switching frequency, loss constraints, etc.

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Matlab (Programmatic) Design

```
function [n, lg, Pq1, Pq2, Pl, eta, Cmin ] = TestBoostDesign(Pmax, fs, L, dt, core_geom, core_mat, MOSFET)
%TestBoostDesign calculate boost conveter efficiency and temperature rise
%for various designs
%   fs  = switching frequency (in Hz)
%   L = inductance (in Henries)
%   n = number of turns on inductor
%   dt = switching dead time (in seconds)
%   core_geom = core geometry, chosen from 'EFD25', 'ETD29', 'ETD39', 'ETD44', or 'ETD49'
%   core_mat = core material, chosen from '3F3', '3C90', or '3F4'
%   MOSFET = MOSFET selection, chosen from 'AOT', 'FDP', 'IPP2', 'IRF',
%   'CSD' or 'IPP0'

Vg = 25;
Vout = 50;
Iout = Pmax/Vout;
Ts = 1/fs;
D = 1-Vg/Vout;
dVout = 2;
Vdr = 12;

Rgon = 10;
Rgoff = 2;

rho = 1.724e-6; %ohms*cm
u0 = 4*pi*1e-7;

%% Inductor Datasheet Parameters
switch core_geom
    case 'EFD25'
        MLT = 46.4; %mm
        Ac = 58; %mm^2
        Ve = 3300; %mm^3
        Wa = 40.2; %mm^2
```

- Matlab, or similar, permits more powerful iteration and plotting/insight into design variation

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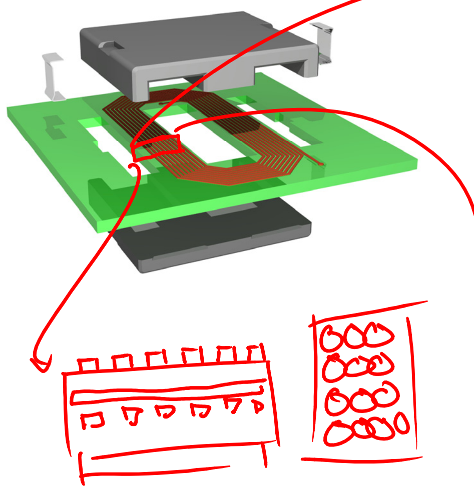
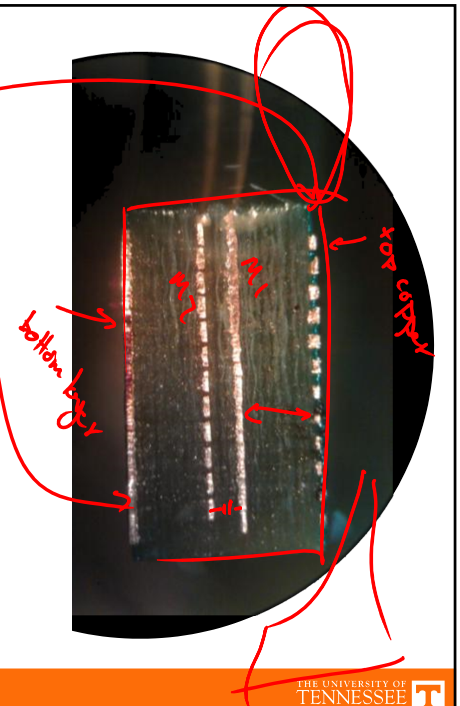
Planar Inductors





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