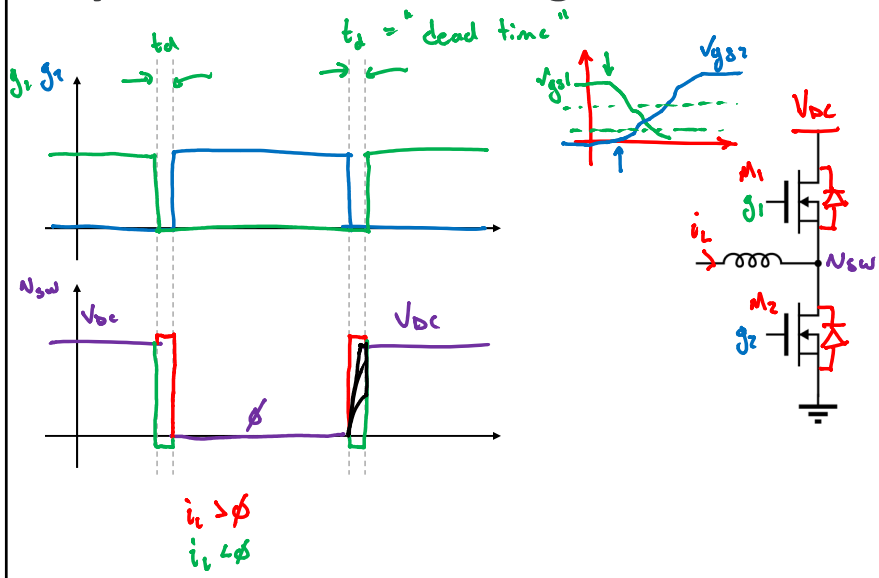
Synchronous Switching

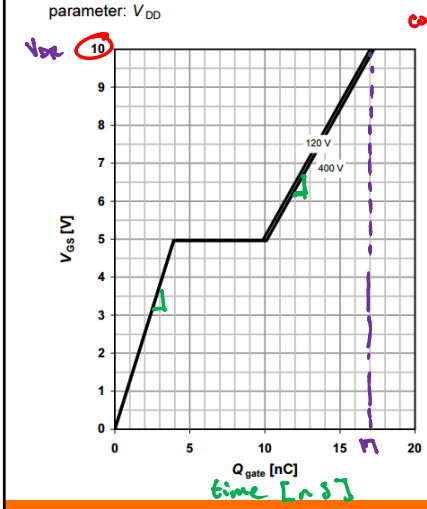


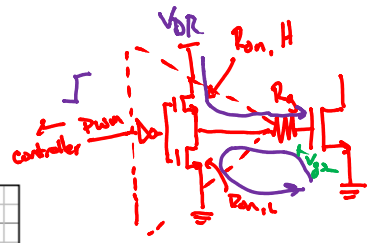
Gate Charge

9 Typ. gate charge

$V_{GS}=f(Q_{gate})$; I_D=5.2 A pulsed

parameter: V_{DD}



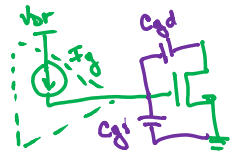


$R_{g,H} = R_g + R_{on,H}$

$E_{g,on} = V_{DR}(Q_g)$

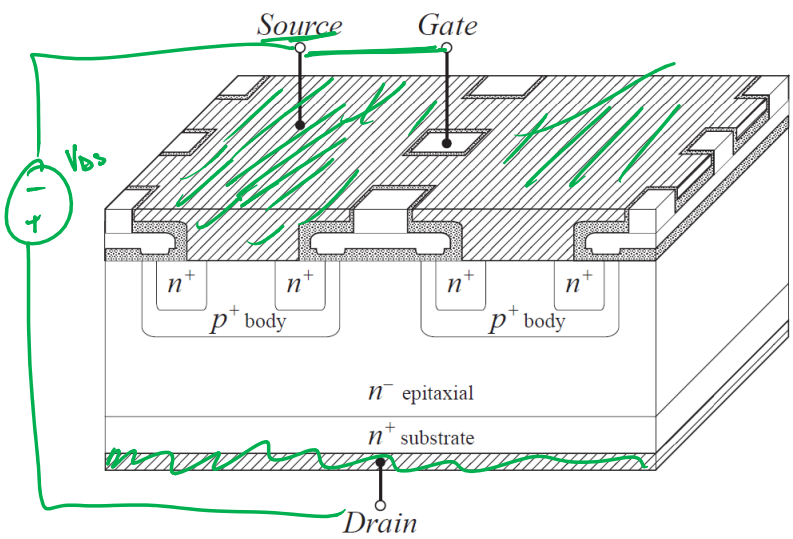
$P_g = V_{DR} Q_g f_s$

$C_{gd} \ll C_{gs}$ & nonlinear

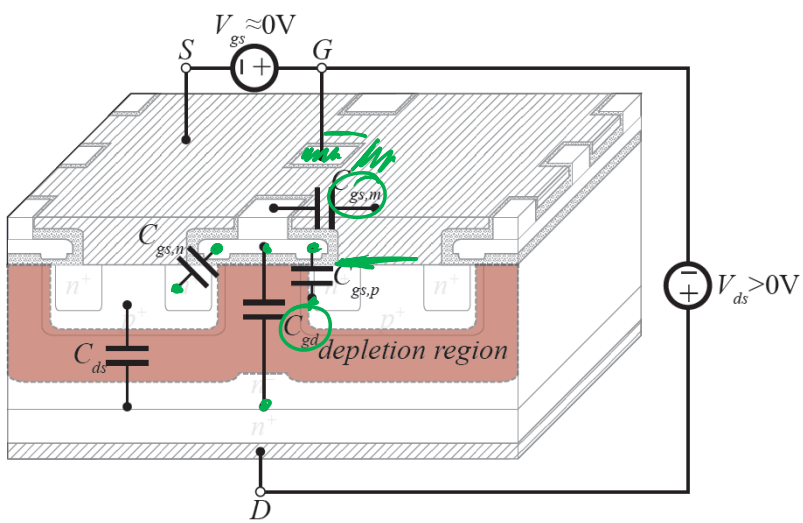


$I_g = \frac{Q}{sec}$; e.g. $I_g = 1$

MOSFET Cross Section



MOSFET Depletion capacitance



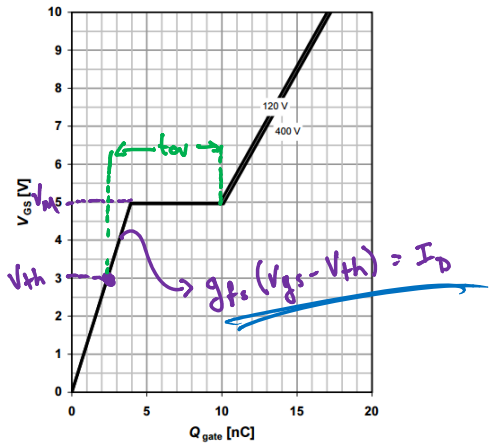
Overlap Time

9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

parameter: V_{DD}

Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.34 mA	2.5	3	3.5	
Gate resistance	R_G	f=1 MHz, open drain	-	1.8	-	Ω



$$I_{gate} = \frac{V_{DR} - V_{gs}}{R_g + R_{on,H}}$$

during turn-on

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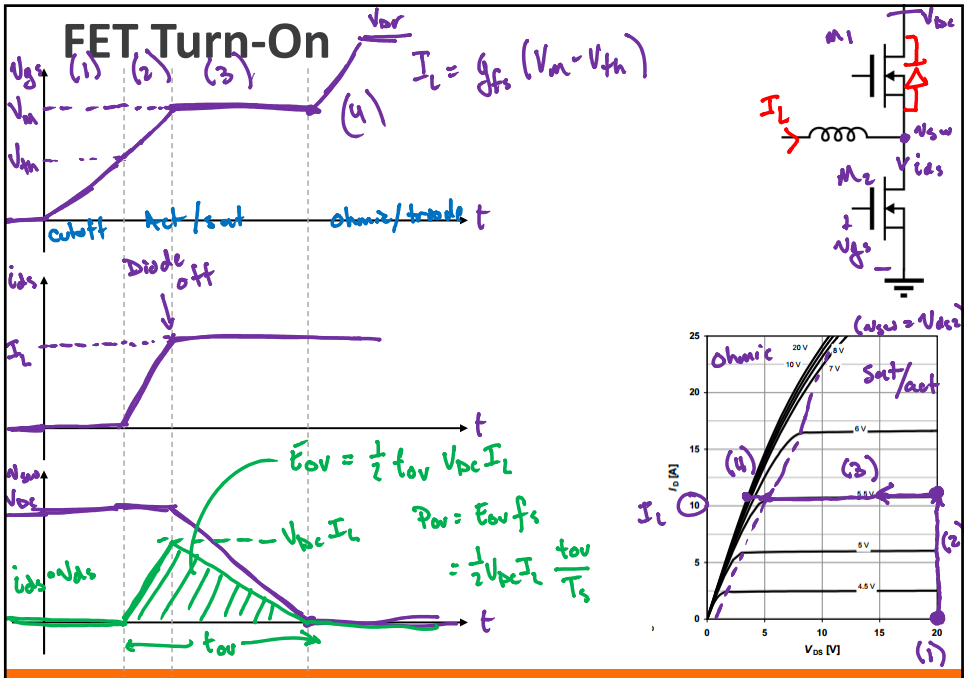
FET Turn-On



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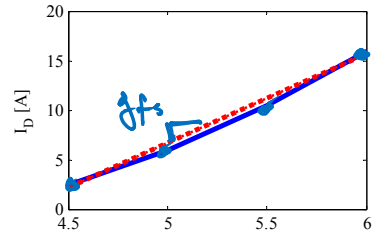
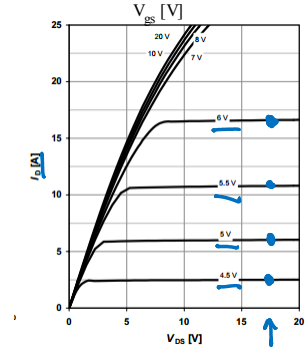
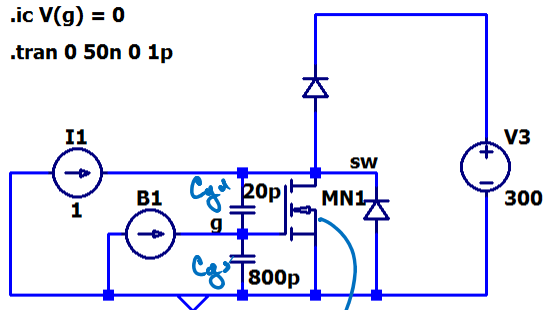
Device Transconductance





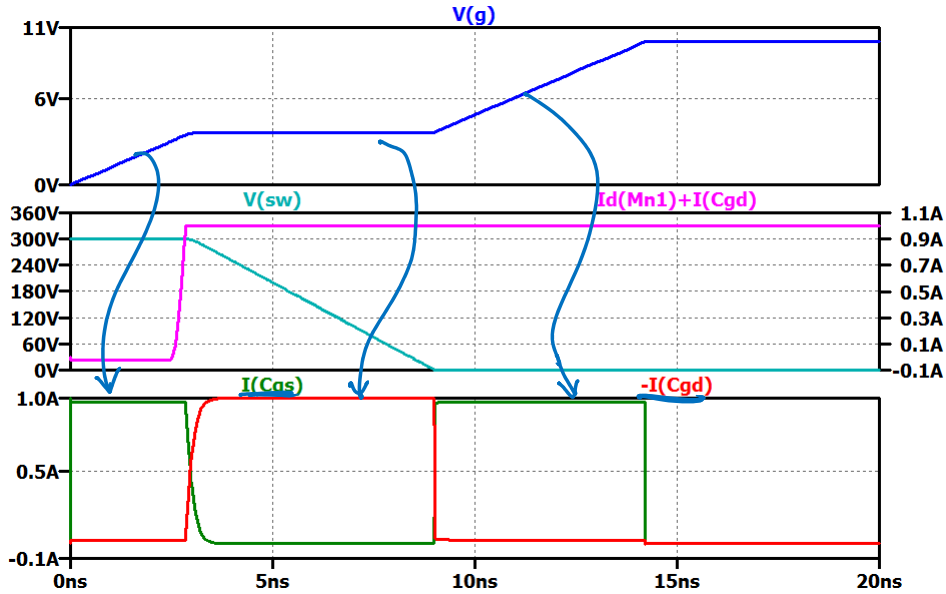
Example Simulation

```
.ic V(g) = 0
.tran 0 50n 0 1p
```




```
I=IF(V(g)<10,1,0)
.model myD D(n=.01)
.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m  Vds=600 Ron=385m Qg=0n)
```

Simulation Waveforms – Turn On



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