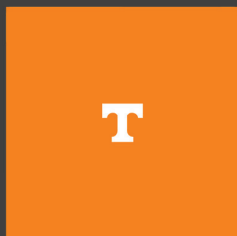


Announcements

- Tiny Box Competition
 - Begins today
 - Form teams of 2-3
 - First assignment is individual
- Midterm
 - Tentatively Nov 5-9



**TiNY BOX
CHALLENGE**

Competition Specifications

The **winning converter** will be the unit which achieves the **highest power density**, i.e. fits in the smallest rectangular volume, while meeting the following specifications.

Parameter	Requirement	Comment
Voltage Input	48 Vdc	
Maximum Output Power	12 W	
Output Voltage	1.2 ± 0.1 Vdc	
Output Ripple Voltage	< 2%	Measured as V_{pk-pk}/V_{avg} from the DC supply, in steady state, at full output power
TPE Efficiency	> 85%	Measured using TPE method ¹
No-load Power Loss	< 3W	Measured with load disconnected, but output voltage within specified range
Volume	< 6 in ³	Volume of minimum rectangle enclosing power stage

¹Tennessee Power Electronics (TPE) efficiency is a weighted power efficiency defined as:

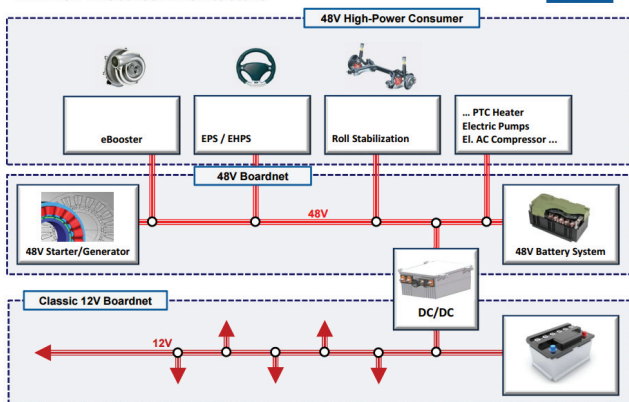
$$\eta_{TPEF} = 0.1\eta_{P_{out}=0.25 \cdot P_{max}} + 0.15\eta_{P_{out}=0.5 \cdot P_{max}} + 0.25\eta_{P_{out}=0.75 \cdot P_{max}} + 0.5\eta_{P_{out}=P_{max}}$$

Example Applications

EV 48V Architectures

Mild hybrid EV

12V/48V Electrical Architecture

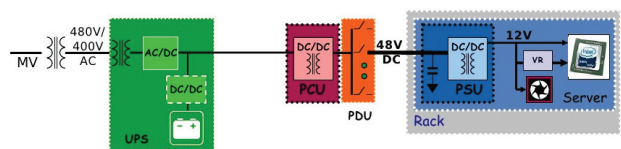


AVL UK Expo 2014 / Ulf Stenzel

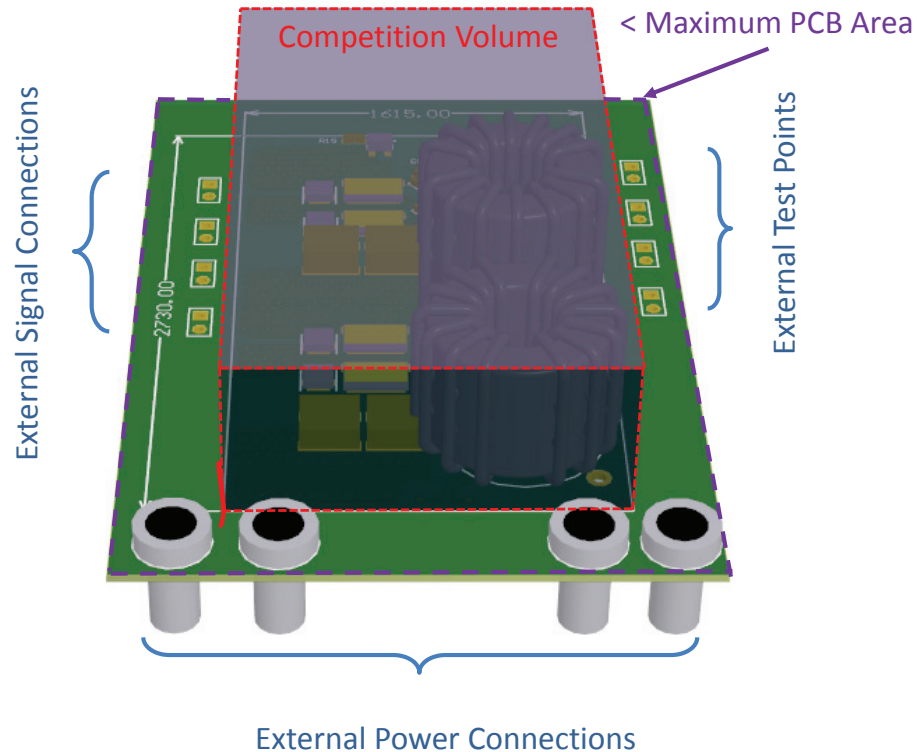
12

Data Centers / Telecom

48V VRM - Voltage Regulation Module
48V POC - Point of Contact



How Volume is Measured



Additional Details

- Full competition specifications and example testing report on course webpage
- No regulation requirements
- First Deliverable: Friday October 26th
 - Design comparison of 3 topologies
 - Due per individual
 - All other deliverables as a team

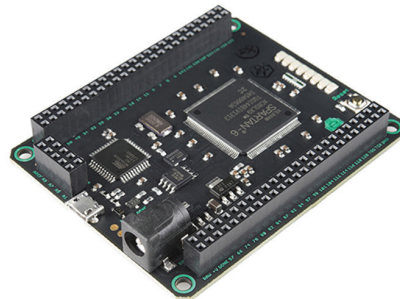
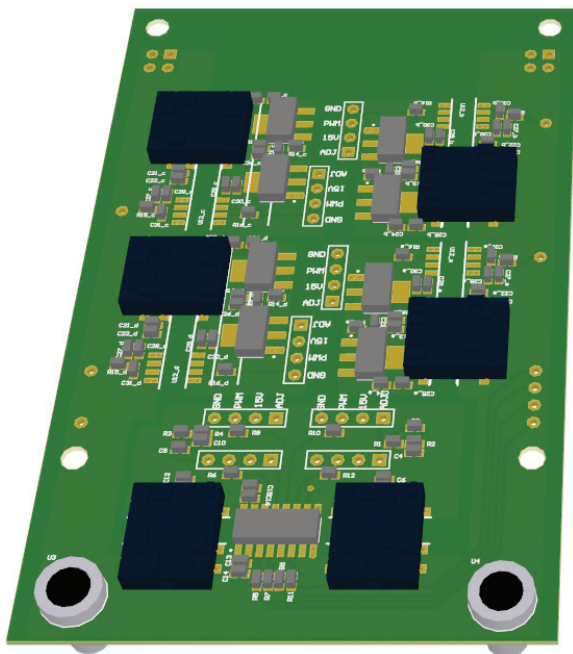
Design and Comparison Report (10/26)

1. Select three topologies from the table and compare based on
 - I. Efficiency at full power
 - II. Power loss at zero load
 - III. Output voltage ripple
 - IV. Volume of main passive components

	Class I	Class II	Class III	Class IV
<i>Definition</i>	Two-switch PWM topologies	Isolated variants of PWM topologies	AC-link topologies	Any topology not conforming to Class I-III
<i>Examples</i>	Buck, Boost, Buck-Boost, Cuk, SEPIC, etc.	Flyback, Forward, push-pull, half-bridge, full-bridge	DAB, DAHB, SRC, LLC, Full Bridge, etc.	Switched capacitor, sigma-delta, multilevel, etc.
<i>Required number</i>	--	--	> 1	> 1

2. Select (and justify) one topology, and provide a complete design including (but not limited to)
 - I. Power Devices
 - II. Gate Driver Circuitry
 - III. Passive Devices and implementation
 - IV. Switching Frequency

Modulation Signal Board



- FPGA + PWM isolation
 - 4 low-side (common ground)
 - 4 high-side (isolated grounds)
- Reference code to generate open-loop PWM signals
- Layout in Altium starter package on course website

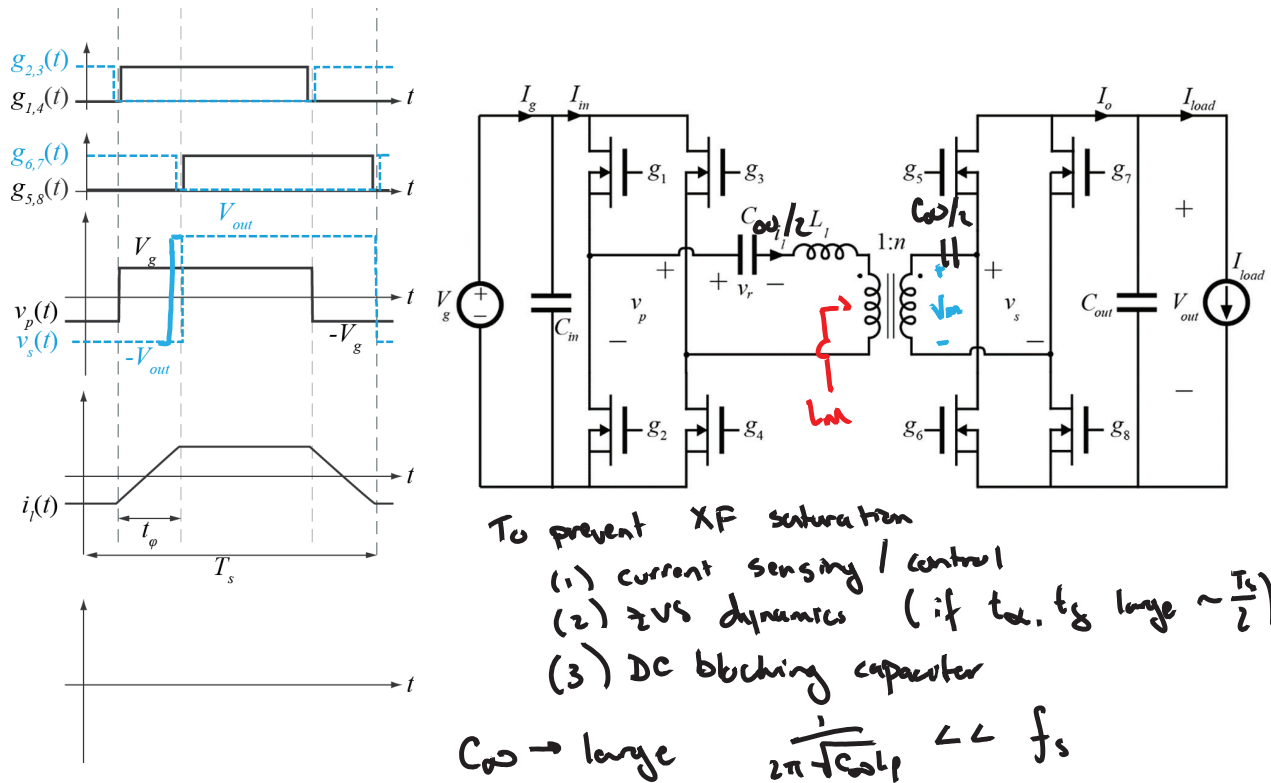
Schedule

- Select teams of 2-3 M 10/15
- Paper Design and Comparison F 10/26
- PCB Layout and BOM F 11/2
- Testing Report F 11/30

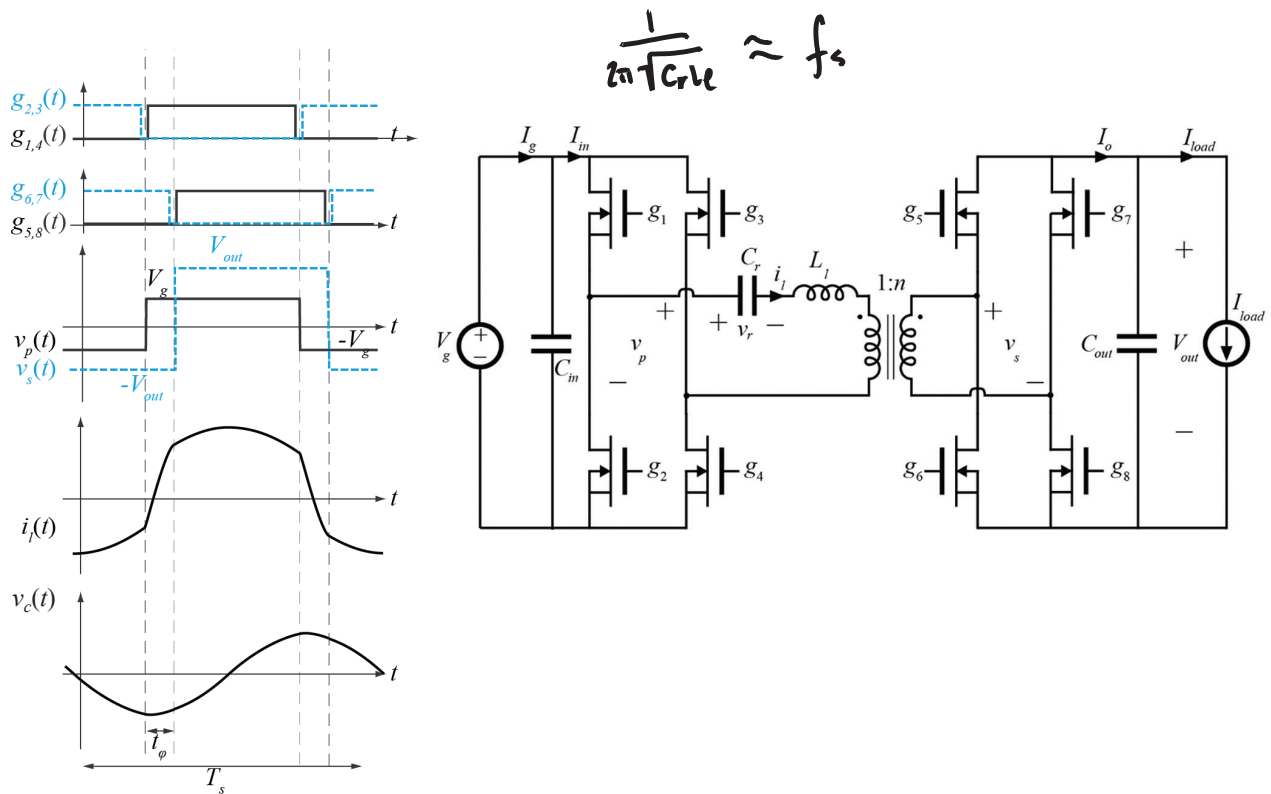
Course Schedule

L24 - Oct. 22	L25 - Oct. 24	L26 - Oct. 26 <i>TBC Design Comparison Due</i>
L27 - Oct. 29	L28 - Oct. 31	L29 - Nov. 2 <i>TBC PCB Layout Due</i>
L30 - Nov. 5	L31 - Nov. 7	L32 - Nov. 9
<i>← Midterm Exam →</i>		
L33 - Nov. 12	L34 - Nov. 14	L35 - Nov. 16
L36 - Nov. 19	L37 - Nov. 21	Nov. 23
L38 - Nov. 26	L39 - Nov. 28	L40 - Nov. 30 <i>TBC Testing Report Due</i>

DAB: Transformer Saturation



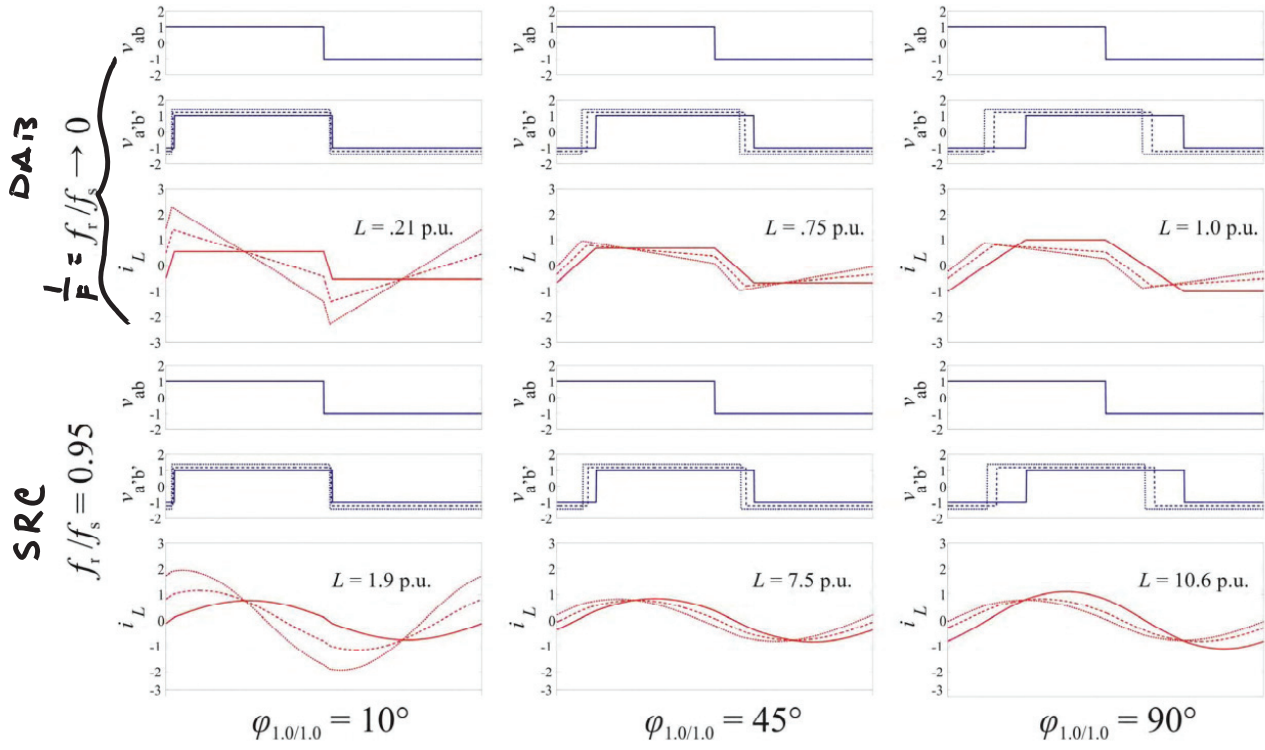
Series Resonant Converter



DAB vs SRC

solid: $V_{out} = nV_g$ $V_{out} > nV_g$ $V_{out} \gg nV_g$

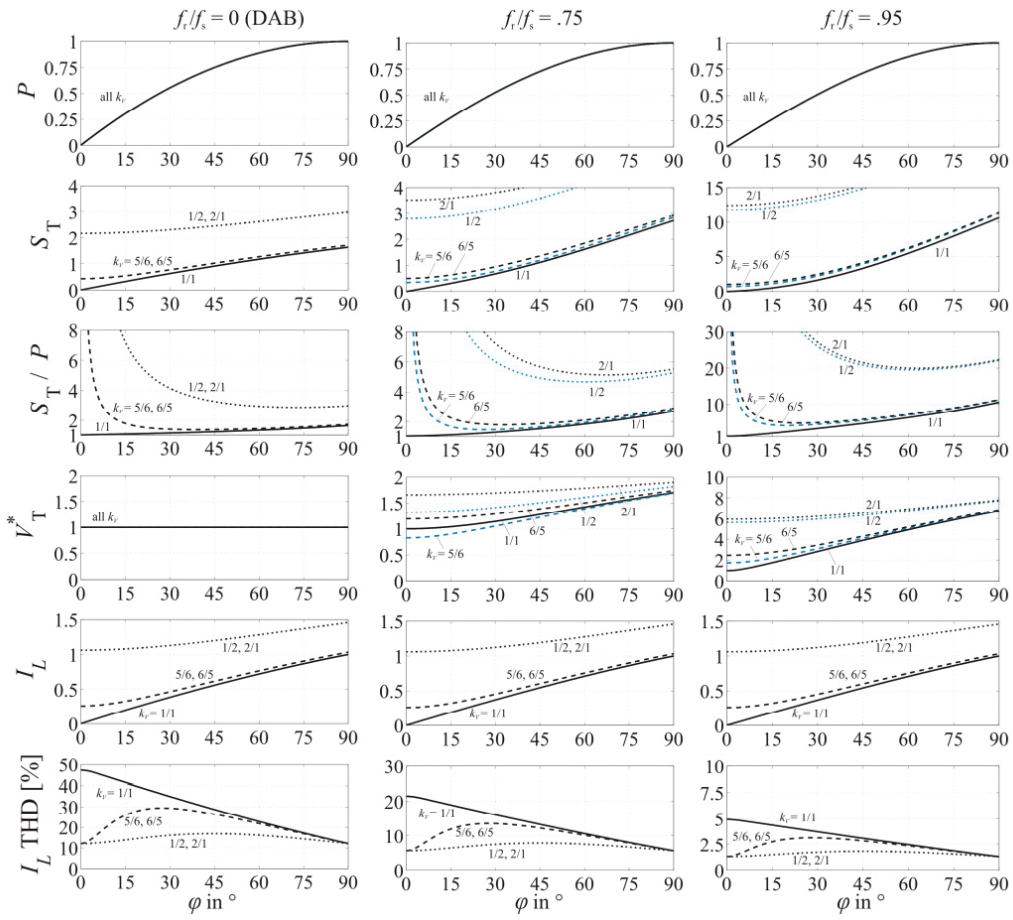
— $V_{in} = 1.0, V'_{out} = 1.0$ - - - $V_{in} = 1.0, V'_{out} = 1.2$ ····· $V_{in} = 1.0, V'_{out} = 1.4$



R. Lenke, F. Mura and R. W. De Doncker, "Comparison of non-resonant and super-resonant dual-active ZVS-operated high-power DC-DC converters,"



Dist
 $S_T = V_T I_L$
rms
 Normalized
 XF power
 Normalized
 XF voltage
 RMS Inductor
 current



R. Lenke, F. Mura and R. W. De Doncker, "Comparison of non-resonant and super-resonant dual-active ZVS-operated high-power DC-DC converters,"



DAB vs SRC: Conclusions

- (physically)
- DAB
- + Smaller resonant tank
 - + Smaller RMS currents
 - + Wider Soft-switching range

- SRC
- + Can be designed with larger XF inductance
 - + Lower AC winding losses
 - + Reduced device turn-off losses