

Course Info

- Course focuses on design and modeling of “high frequency” power electronics
 - Course website: <http://web.eecs.utk.edu/~dcostine/ECE581>
 - Goal of course is understanding of motivations and issues with high frequency power electronics; analysis and design techniques; applications
- Prerequisites: undergraduate Circuits sequence, Microelectronics, ECE 481 – Power Electronics, or equivalent

Contact Info

Instructor: Daniel Costinett

- Office: MK504
- OH: T: 11-12, W:9-10, By appointment
- E-mail: Daniel.Costinett@utk.edu
- Email questions will be answered within 24 hours (excluding weekends)
- Please use [**ECE 581**] in the subject line

Course Structure

- Course meets MWF 10:10-11:00 am
- Plan to spend ~9 hours per week on course outside of lectures
- Grading:
 - Homework/Lab: 40%
 - One homework per week
 - Assignments due on Fridays unless otherwise noted on course website
 - One design competition outside of class time
 - Midterm: 25%
 - Tentatively scheduled for October 29th
 - Final: 35%

Assignments

- Assignments due *at the start of lecture* on the day indicated on the course schedule
- No late work will be accepted except in cases of documented medical emergencies
- Collaboration is encouraged on all assignments except quizzes and exams; Turn in your own work
- All work to be turned in through canvas

Textbook and Materials

- The textbook

R.Erickson, D.Maksimovic, *Fundamentals of Power Electronics*,
Springer 2001

will reference chapters 19-20 and reference materials from prior chapters. The textbook is available on-line from campus network. Purchase is not required for this course.

- MATLAB/Simulink, LTSpice will be used; All installed in the Tesla Lab
- Lecture slides and notes, additional course materials, homework, due dates , etc. posted on the course website
- Additional information on course website

Introduction

- Why high frequency?
 - Power Density
 - Control Bandwidth
- Techniques
 - Devices
 - Control
 - Topologies
 - Passives



8 w Dimmable LED Driver

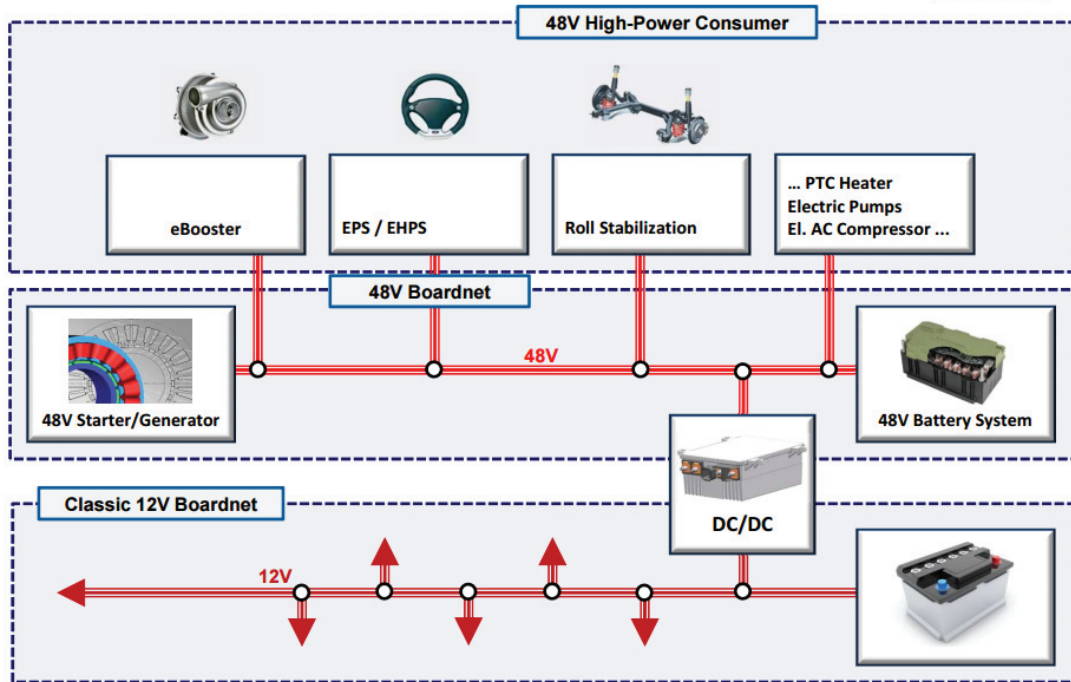


Voltage Regulation Module

Motivating Example



12V/48V Electrical Architecture



AVL UK Expo 2014 / Ulf Stenzel

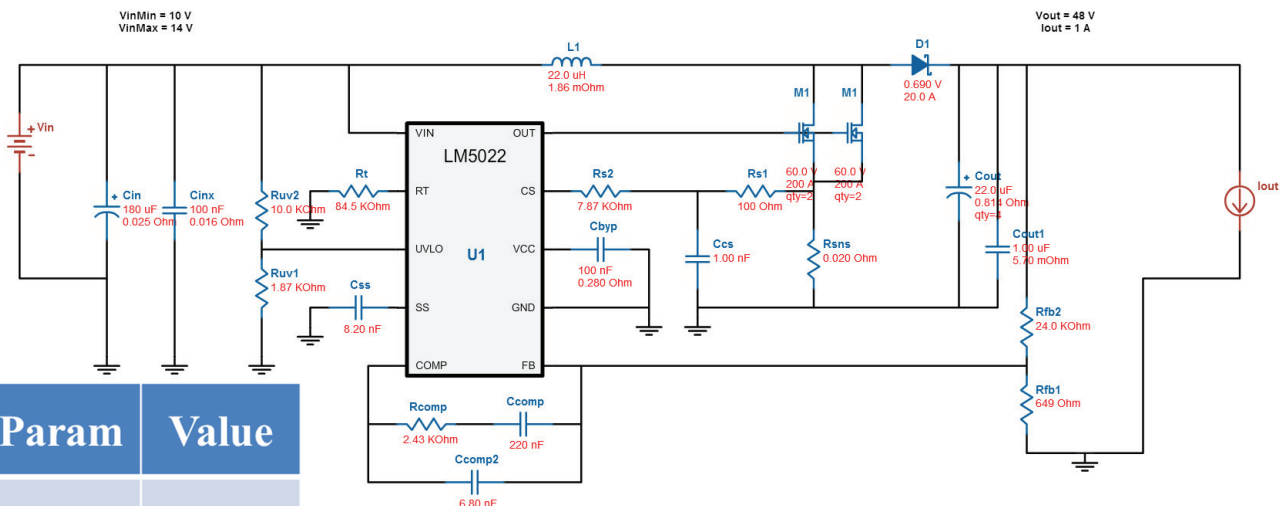
12

NXP Semi, "Semiconductors – enablers of future mobility concepts", 2011
 Audi, "Electric biturbo and hybridization", 2014
 AVL, "48V Mild Hybrid Systems"



Baseline Design

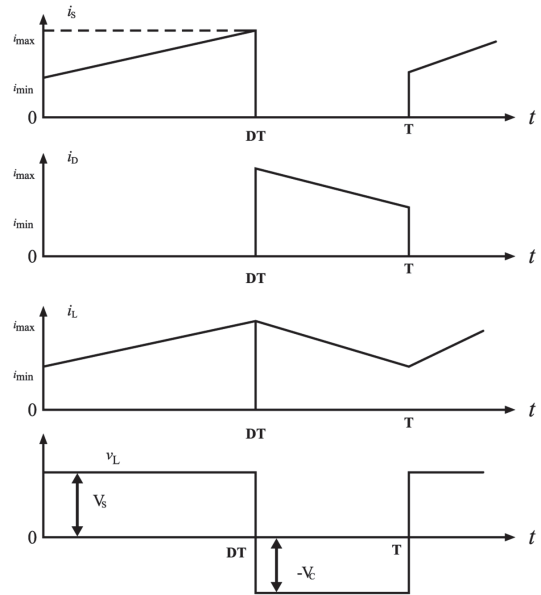
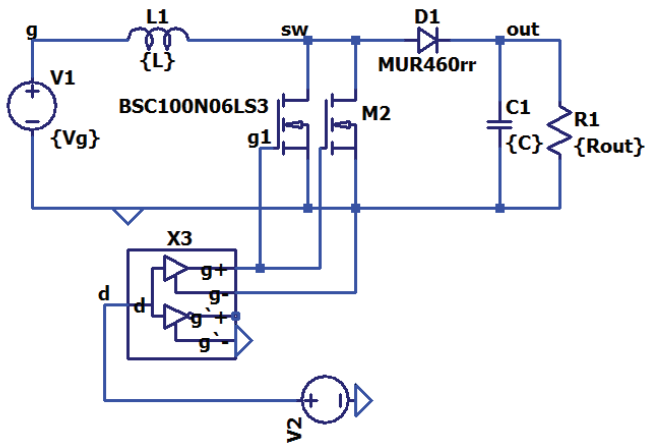
- Use TI WebBench (webench.ti.com) to get a baseline design



Param	Value
V_g	12 V
V_{out}	48 V
R_{out}	48 Ω
ΔV_{out}	0.1 V

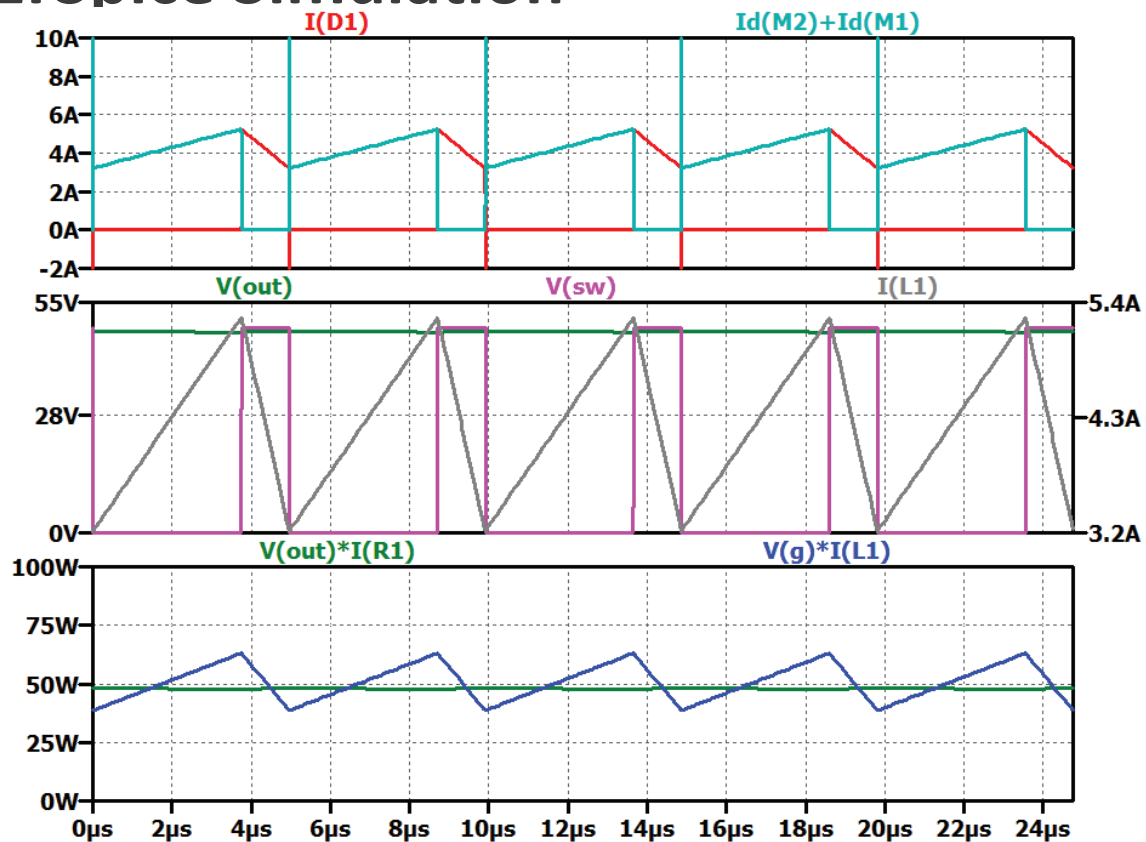


LTSpice Simulation

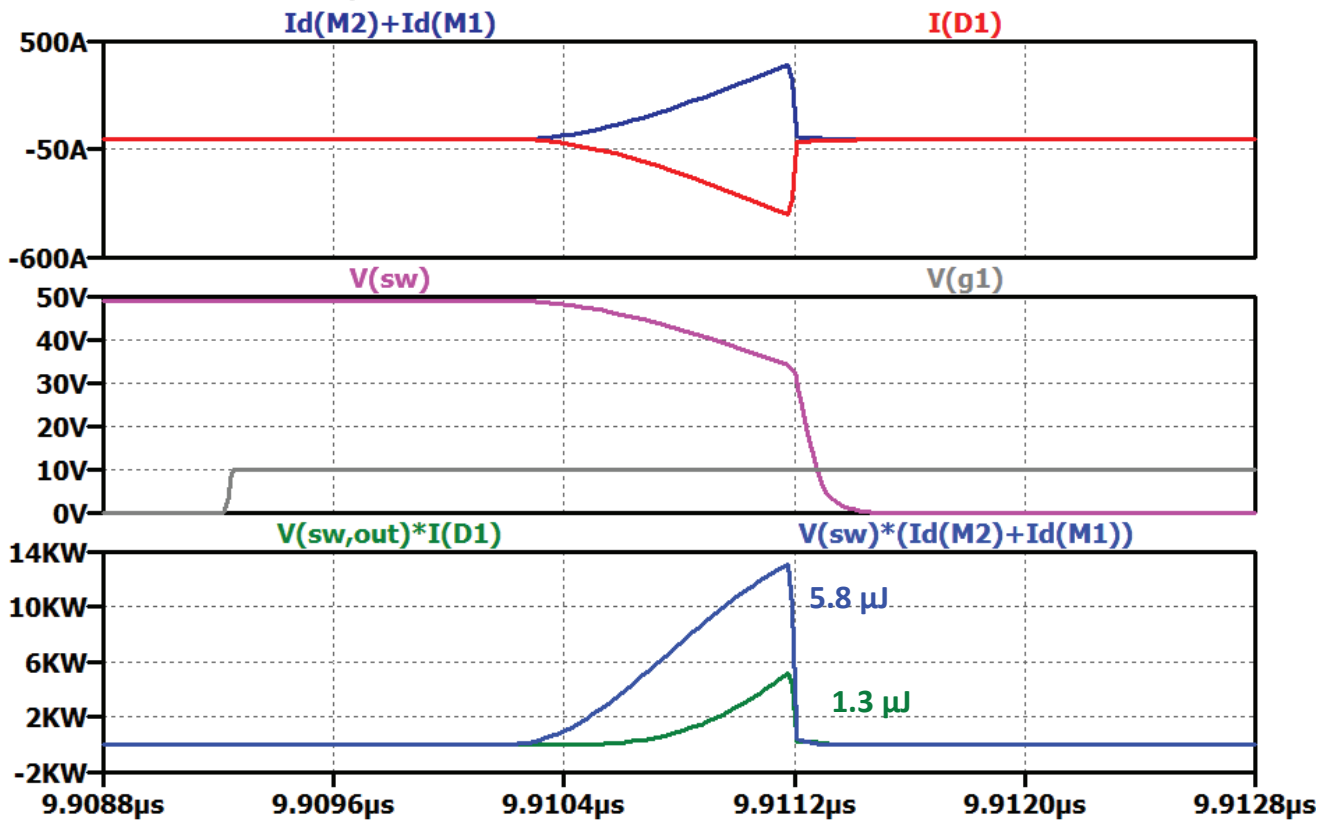


L	C_{out}	f_s	Diode	η (Sim)
22uH	22uF	202k	Si (FR)	93.9%

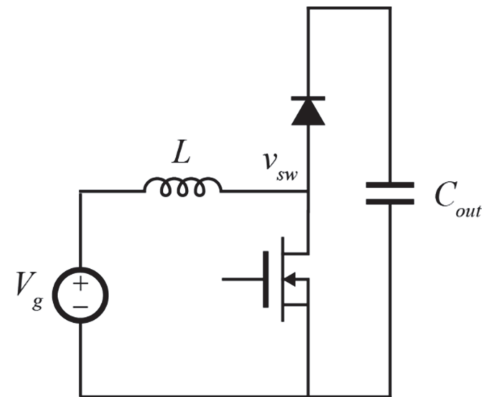
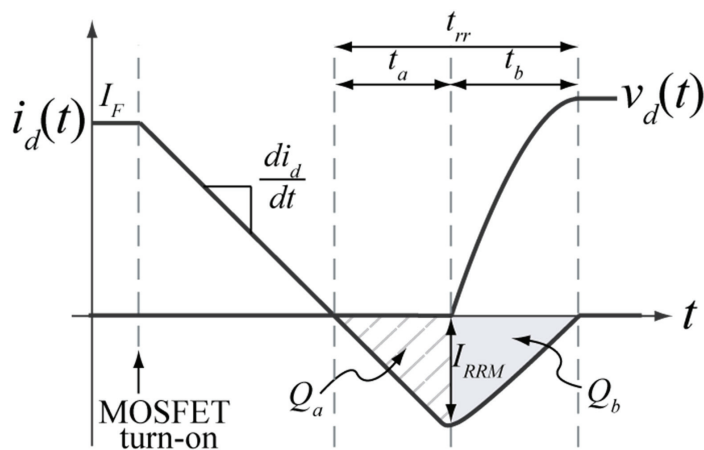
LTSpice Simulation



Switching Transition



Diode Reverse Recovery



Datasheet RR Characteristics

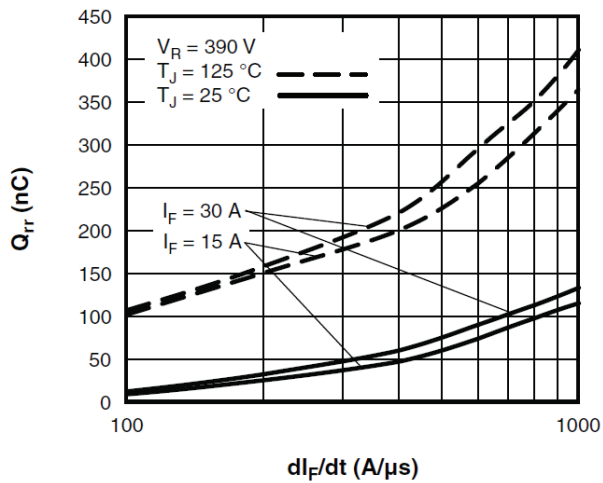


Fig. 10 - Typical Stored Charge vs. di_F/dt

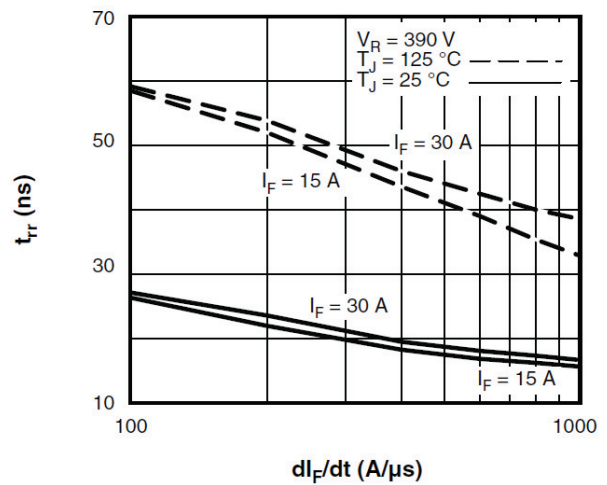
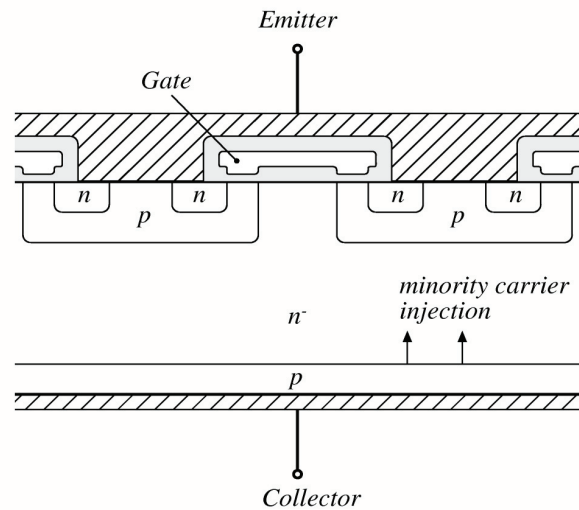
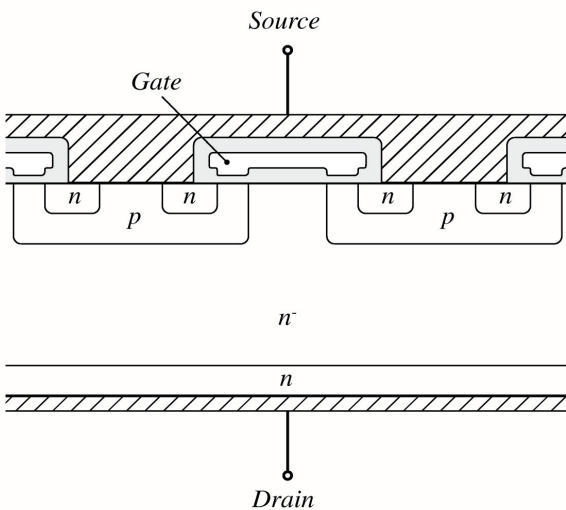
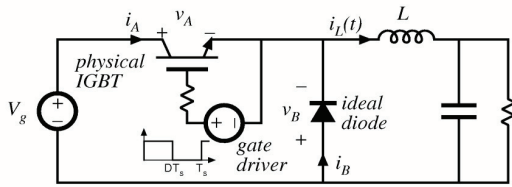


Fig. 9 - Typical Reverse Recovery Time vs. di_F/dt

Charge Storage



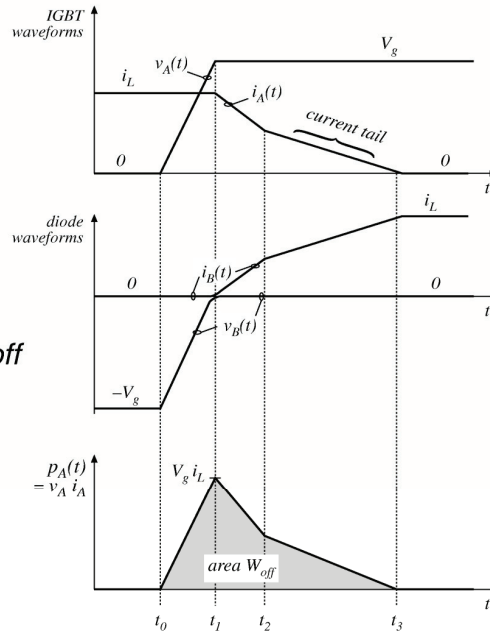
IGBT Current Tailing



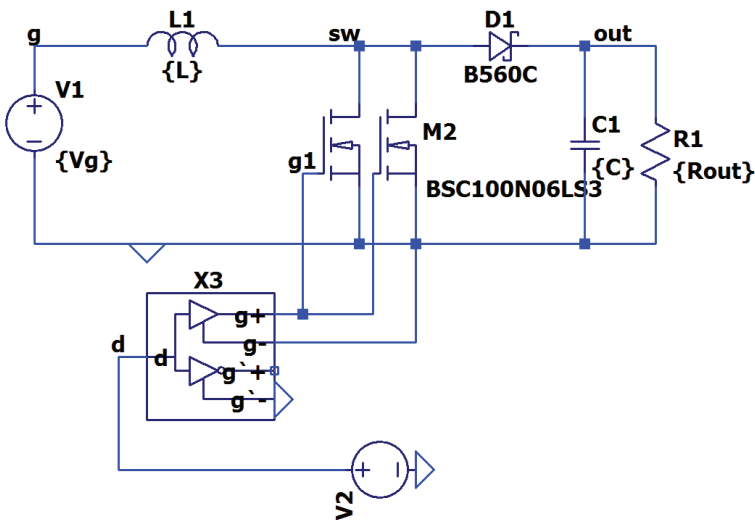
Example: buck converter with IGBT

transistor turn-off transition

$$P_{sw} = \frac{1}{T_s} \int_{\text{switching transitions}} p_A(t) dt = (W_{on} + W_{off}) f_s$$

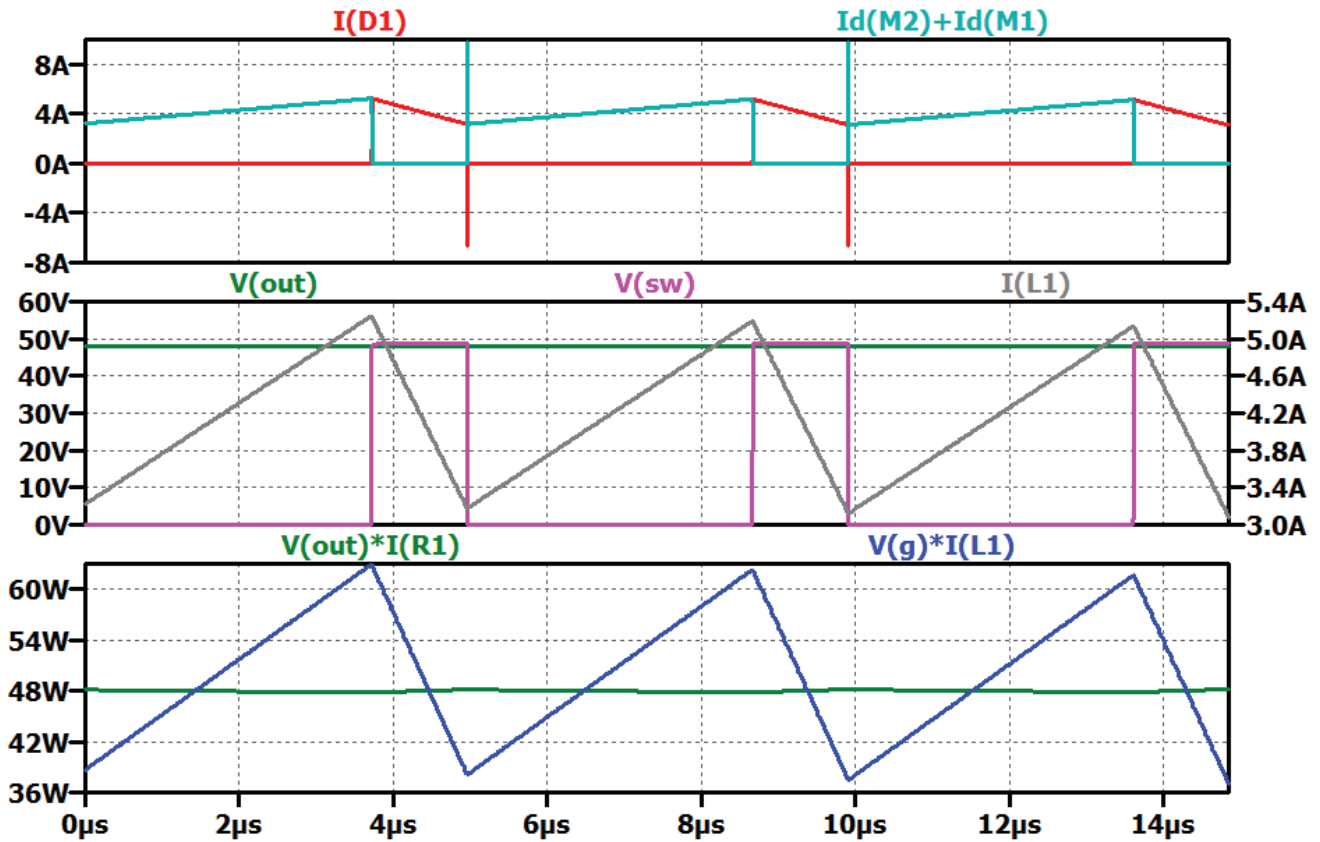


Schottky Diode

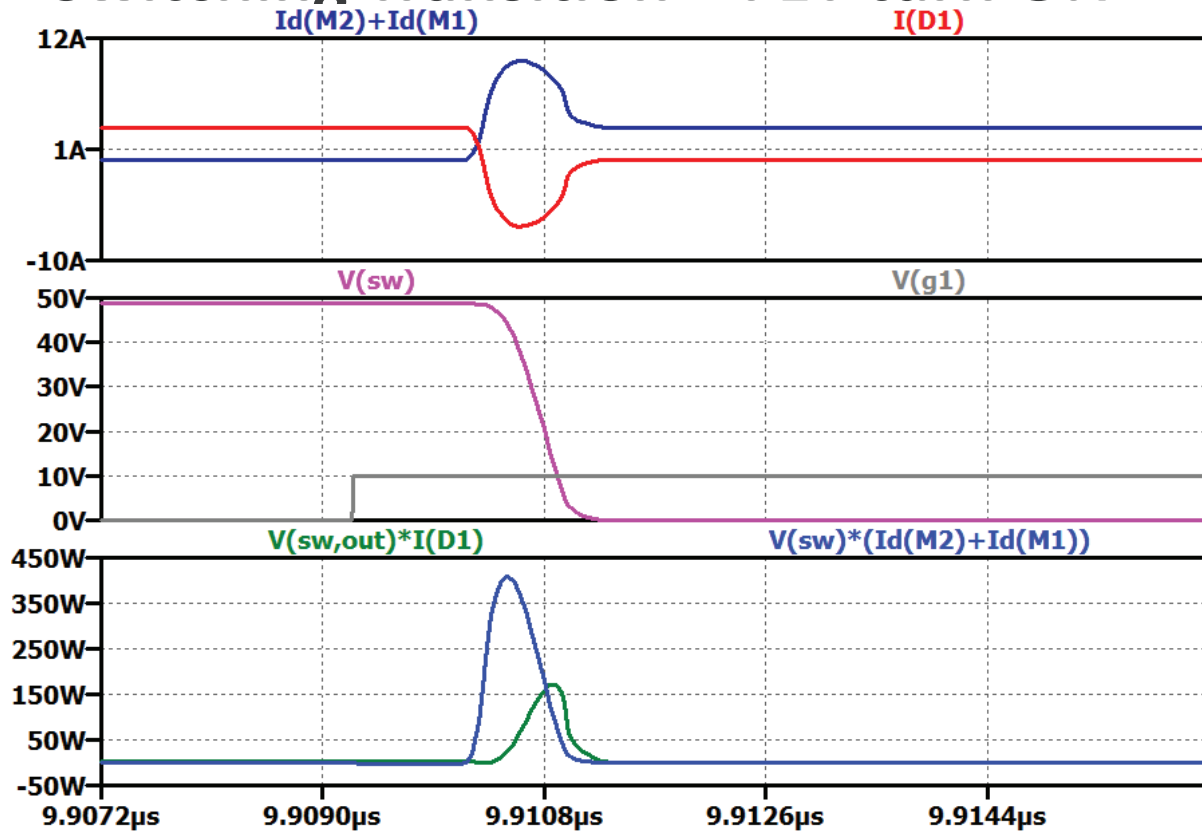


L	C _{out}	f _s	Diode	η (Sim)
22uH	22uF	202k	Si (FR)	93.9%
22uH	22uF	202k	Si Schottky	95.8%

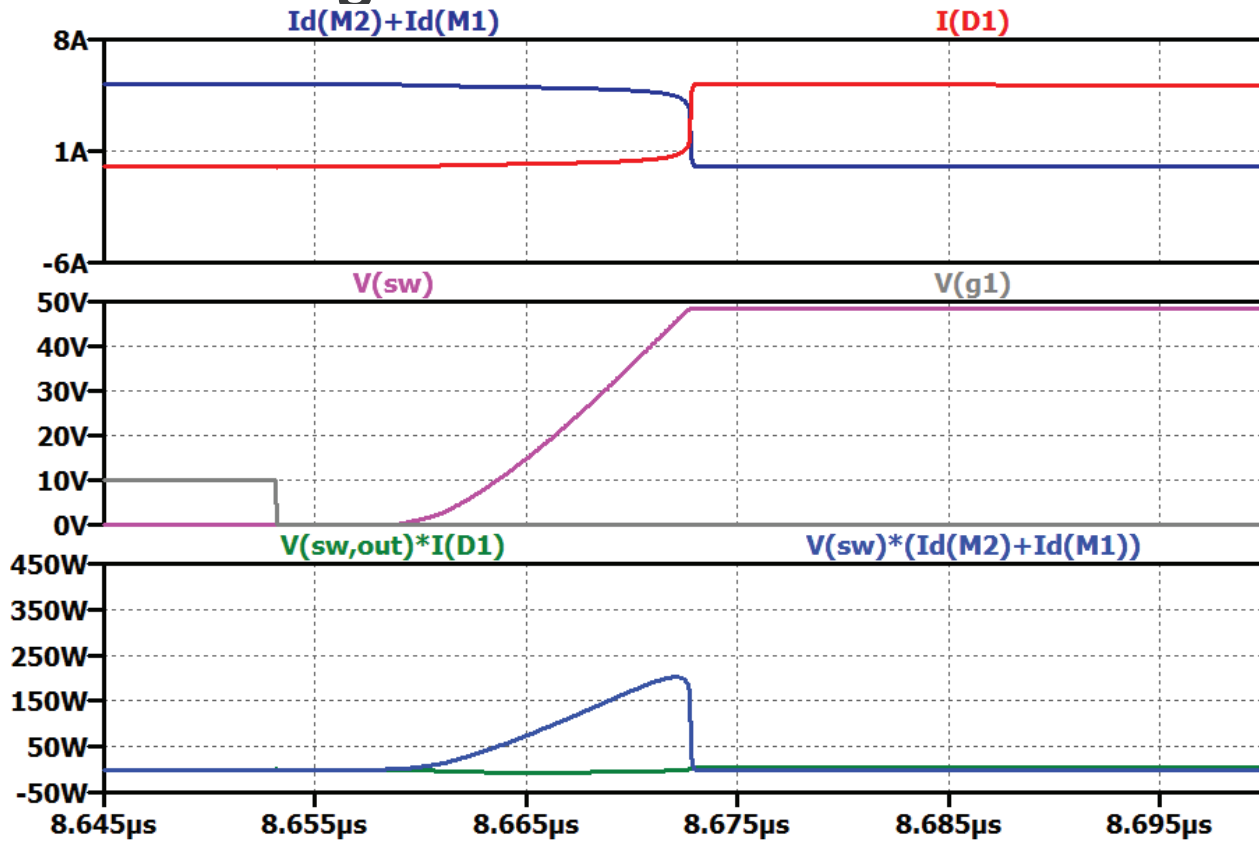
Simulation Waveforms



Switching Transition – FET turn ON



Switching Transition – FET turn OFF

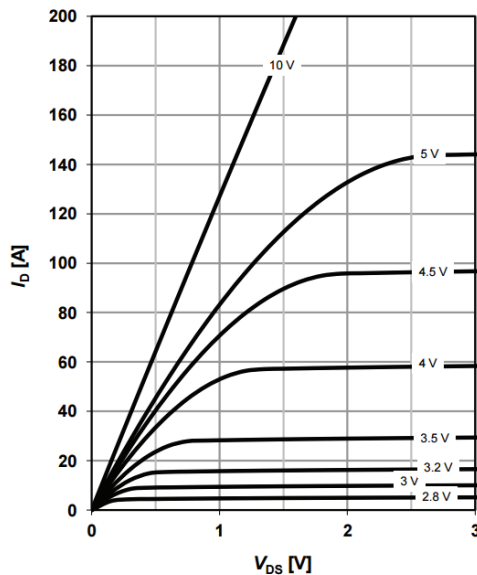


MOSFET Switching Behaviors

5 Typ. output characteristics

$$I_D = f(V_{DS}); T_J = 25^\circ C$$

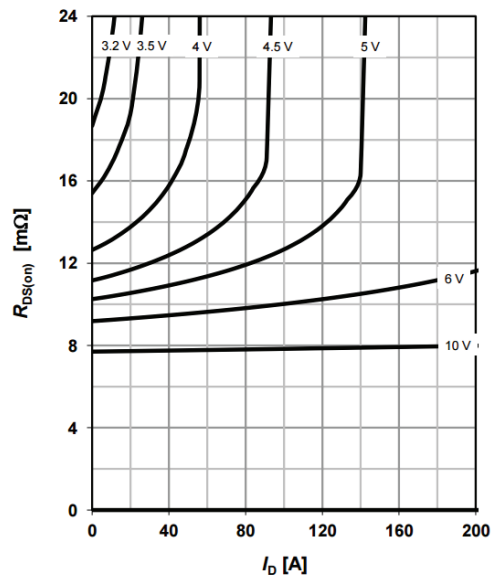
parameter: V_{GS}



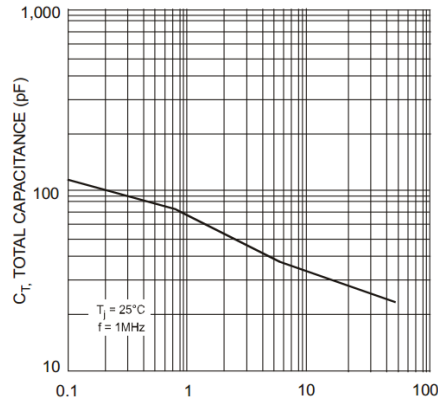
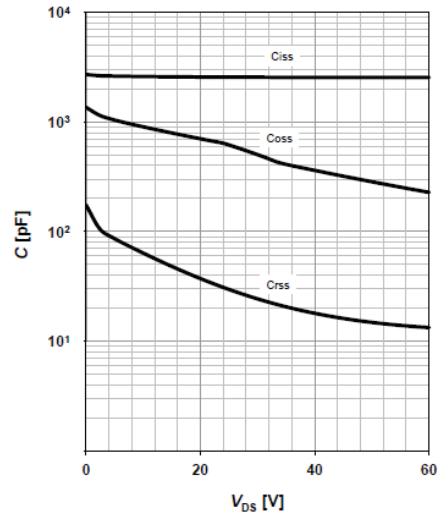
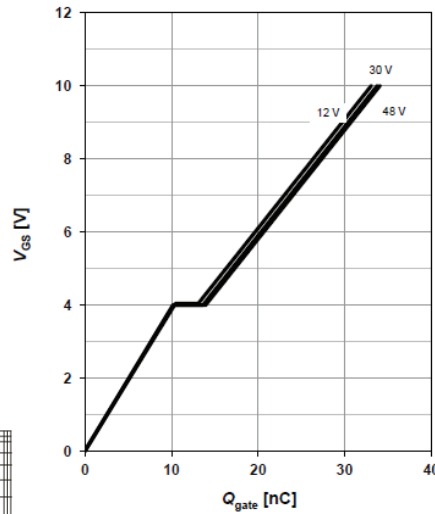
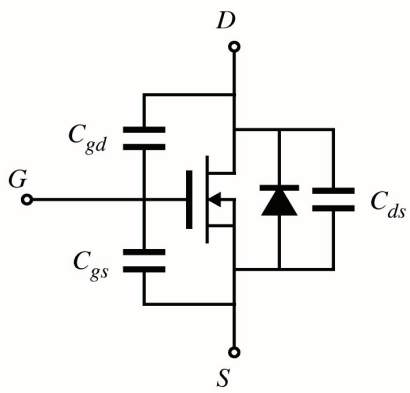
6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_J = 25^\circ C$$

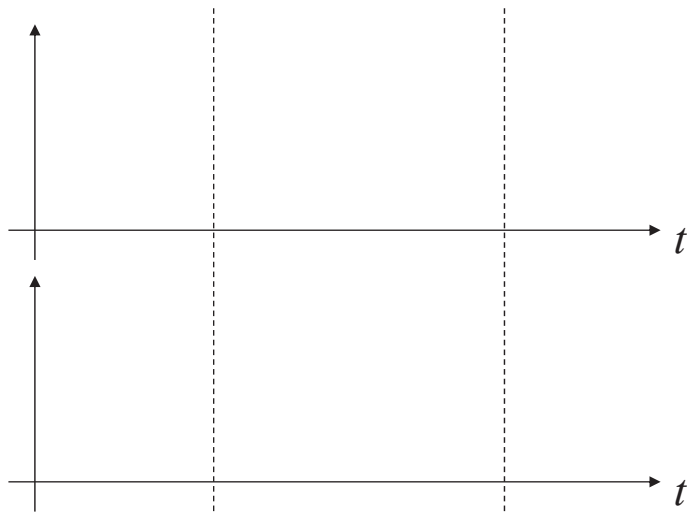
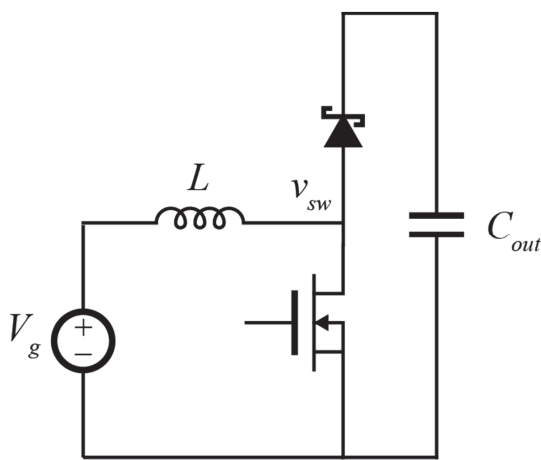
parameter: V_{GS}



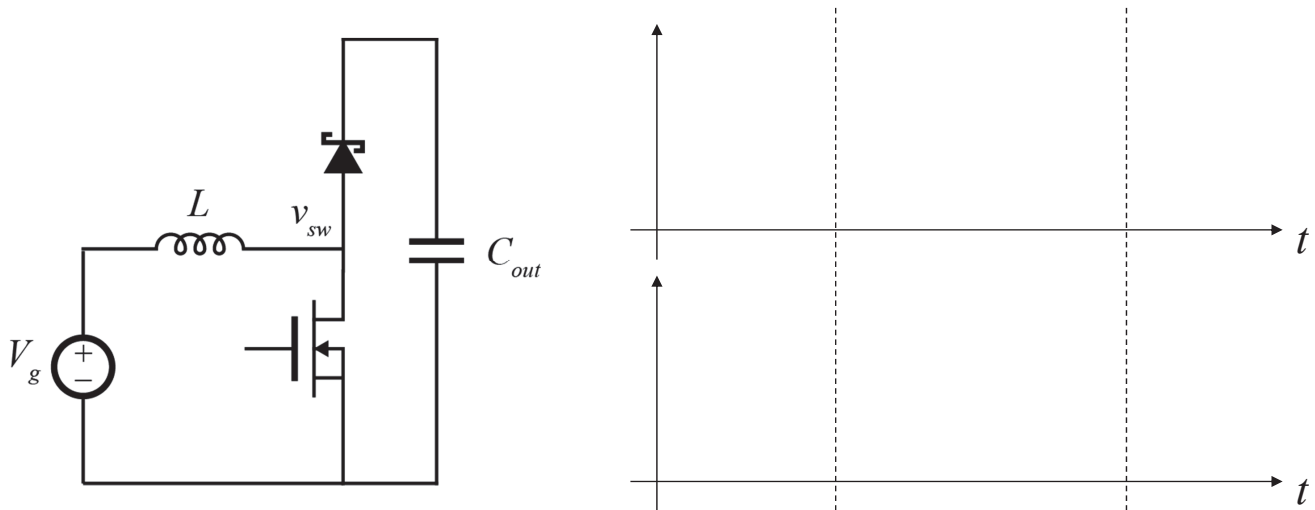
MOSFET Stored Charge



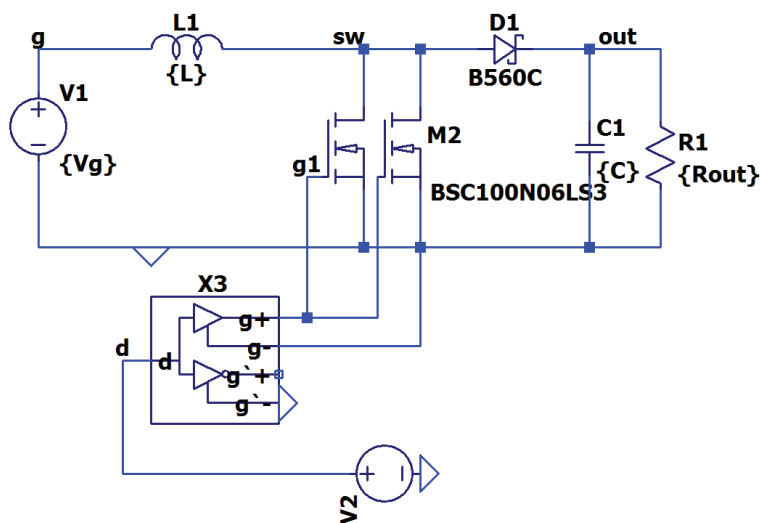
Device Capacitances



Device Capacitances

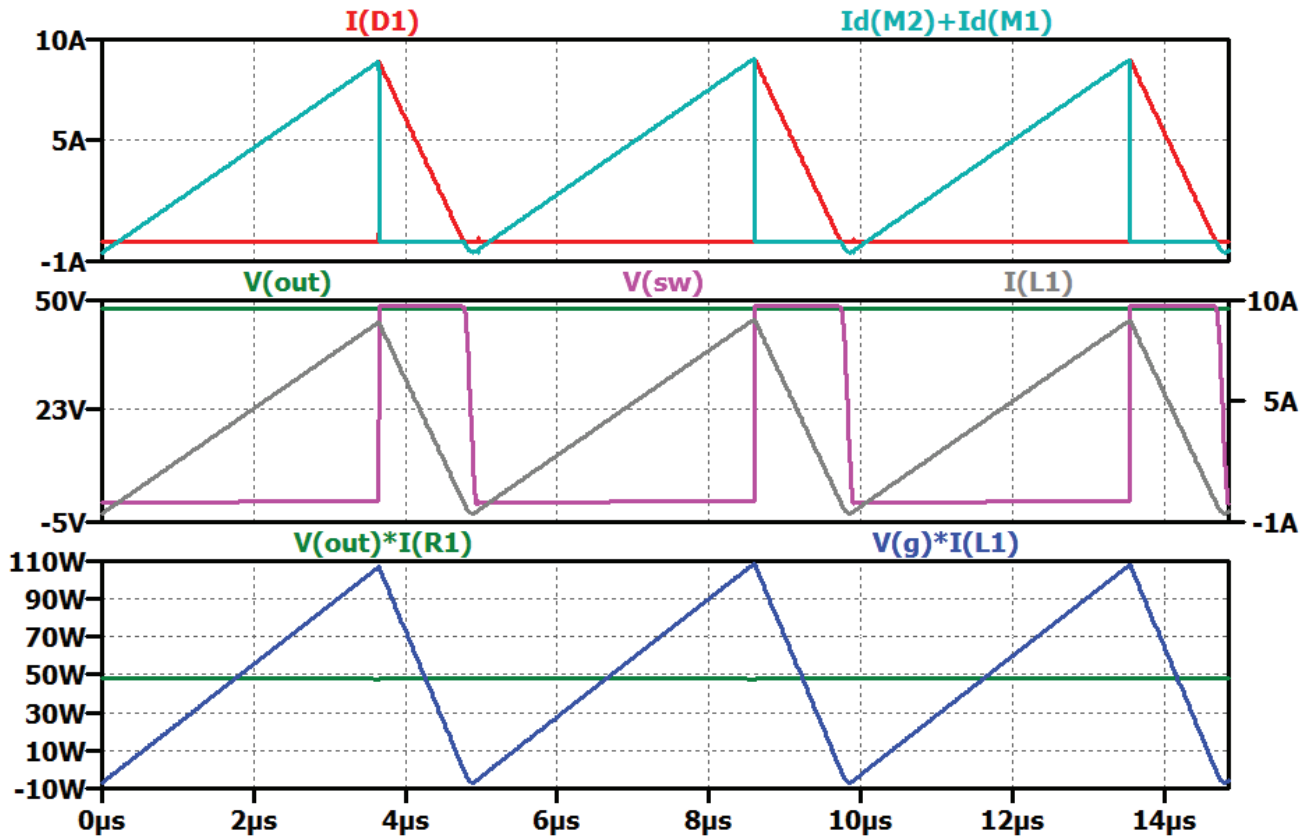


DCM: Soft Switching

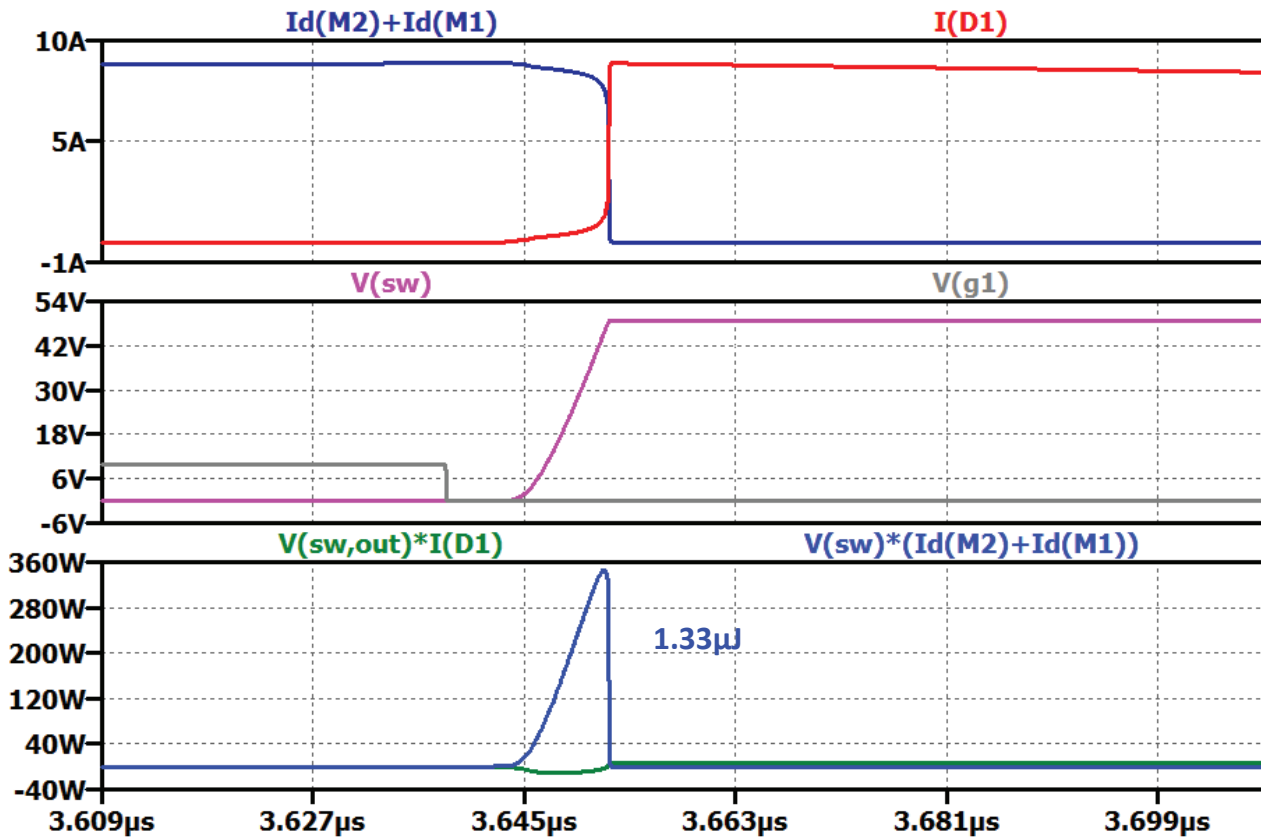


L	C_{out}	f_s	Diode	η (Sim)
22uH	22uF	202k	Si (FR)	93.9%
22uH	22uF	202k	Si Schottky	95.8%
4.6uH	22uF	202k	Si Schottky	98.2%

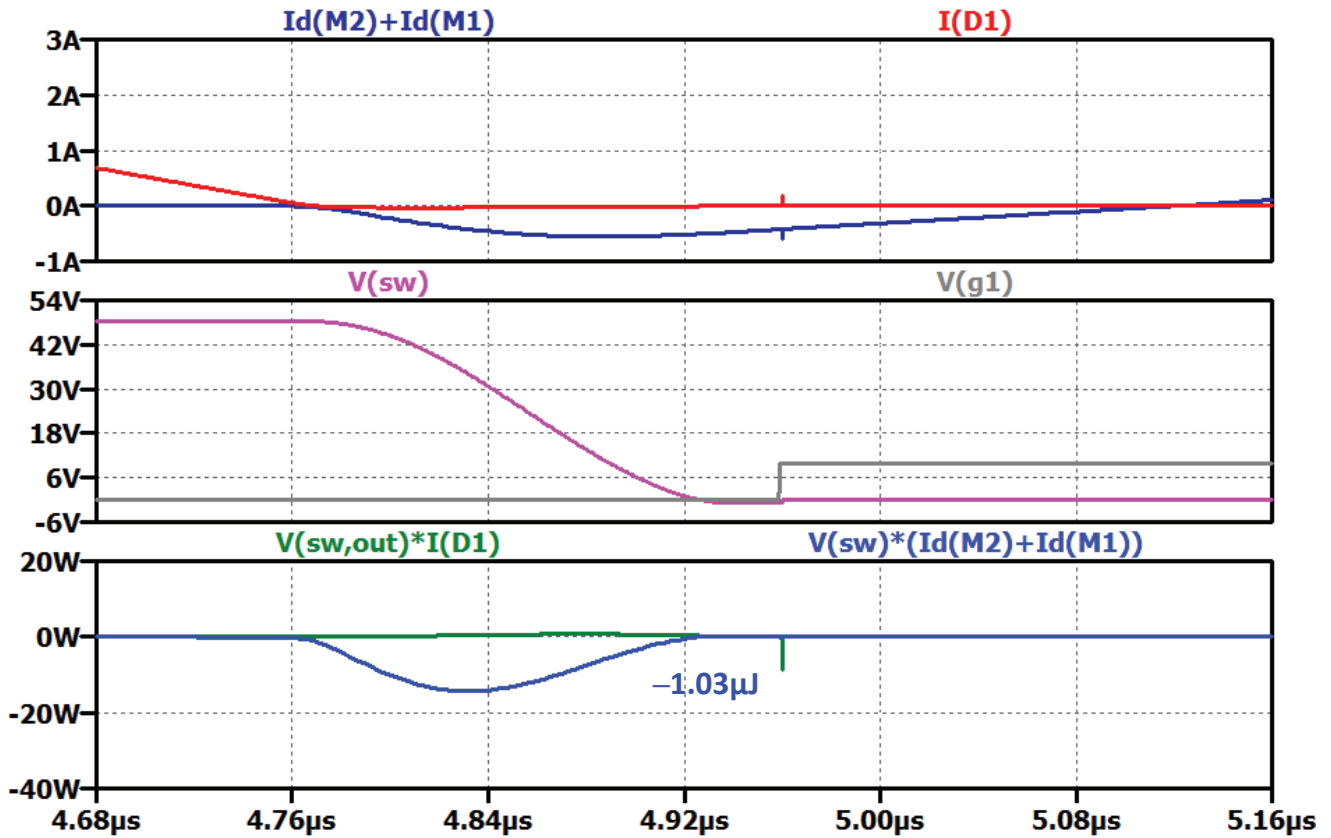
DCM Simulation



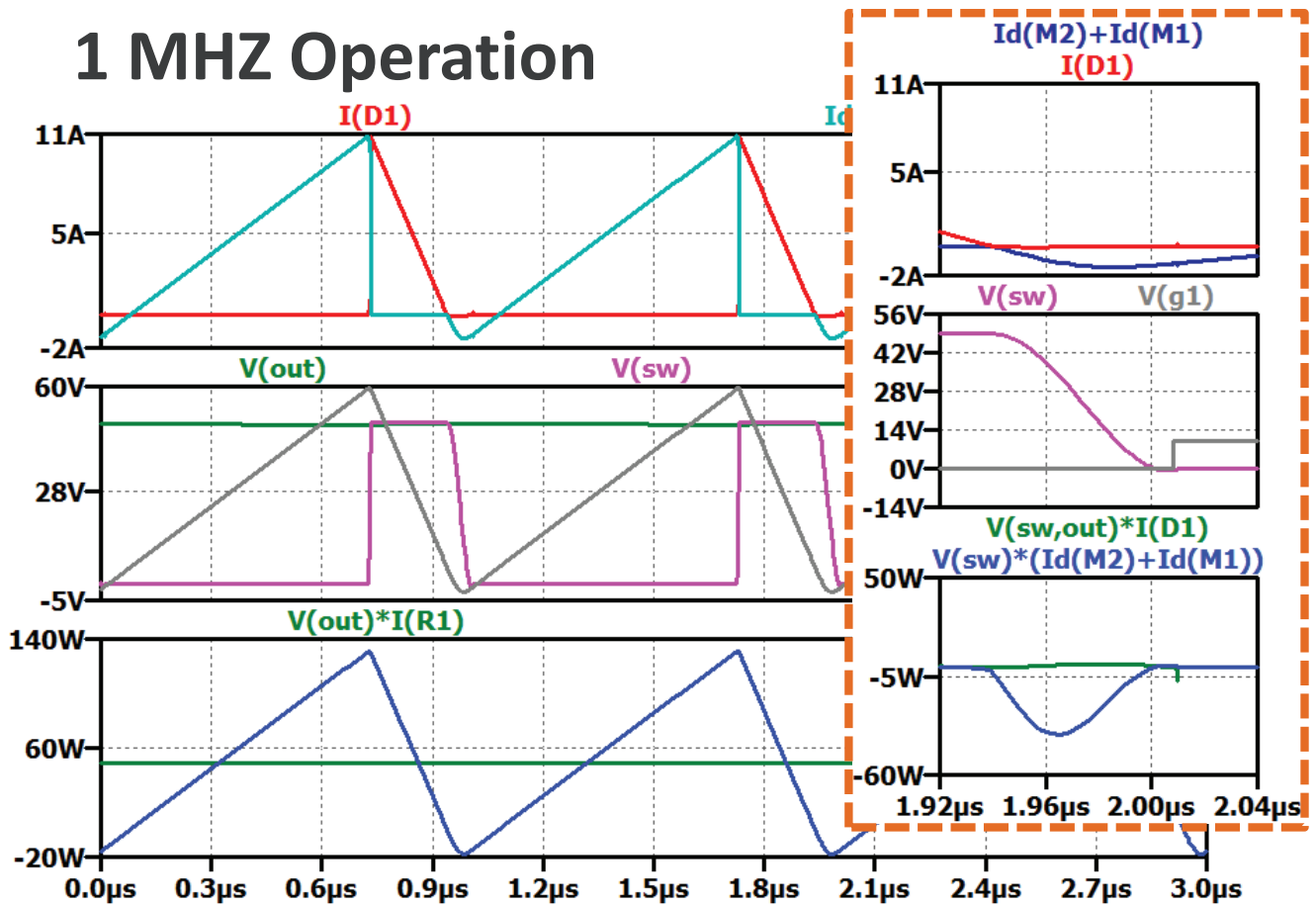
MOSFET Turn-Off



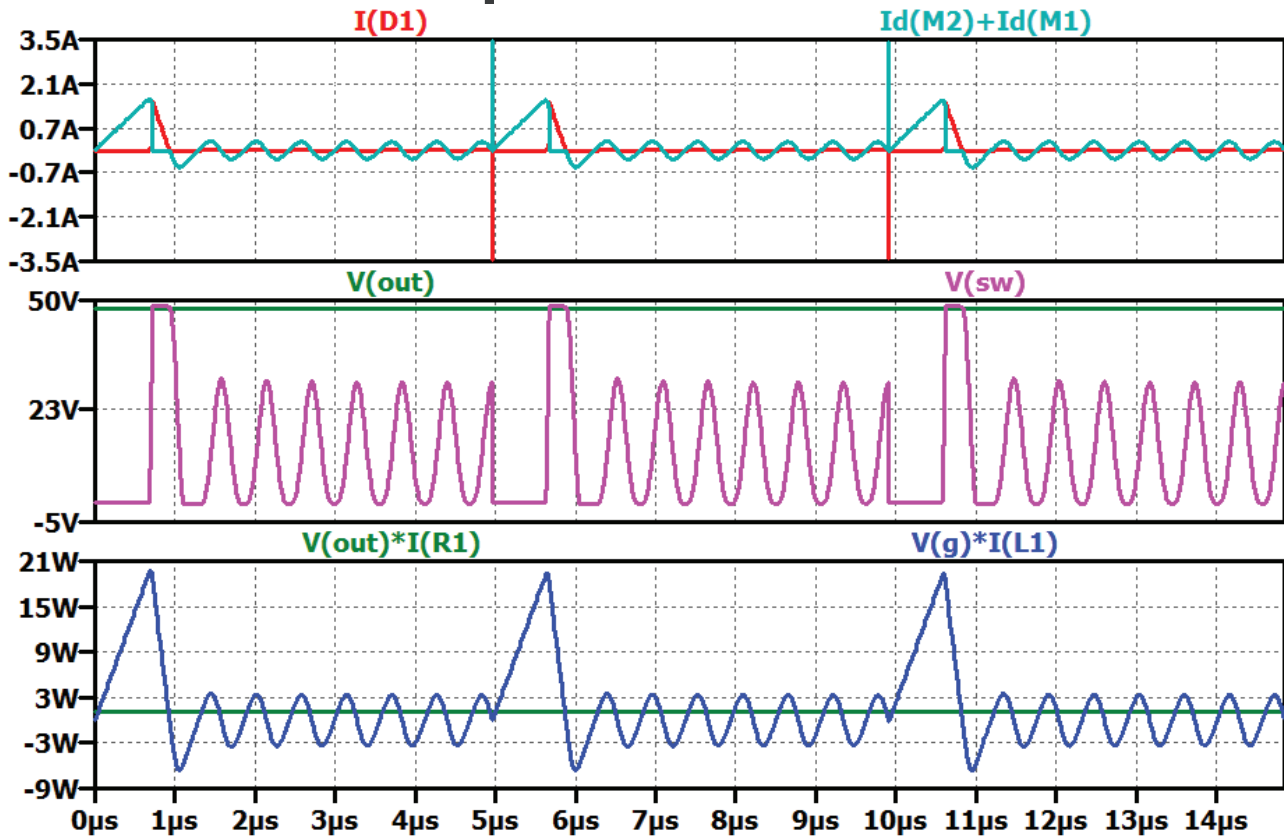
MOSFET Turn-On



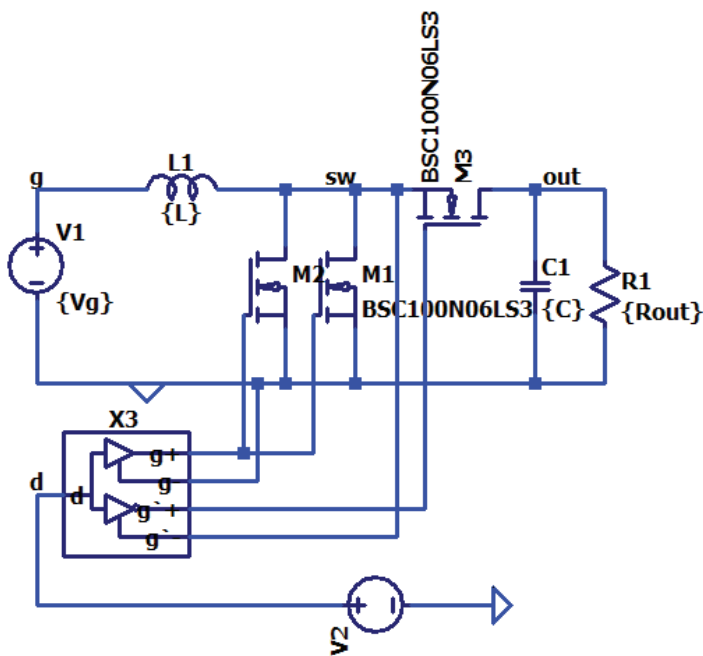
1 MHz Operation



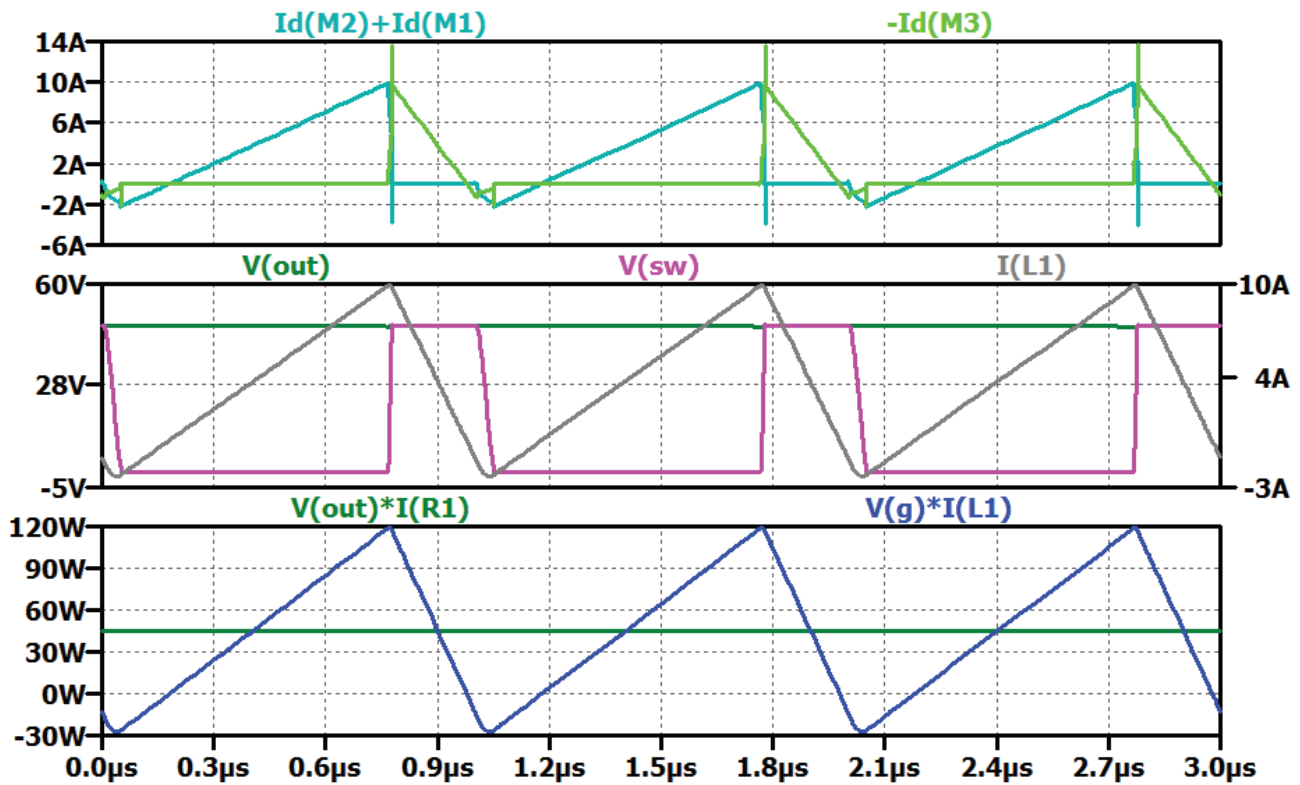
Low Power Operation



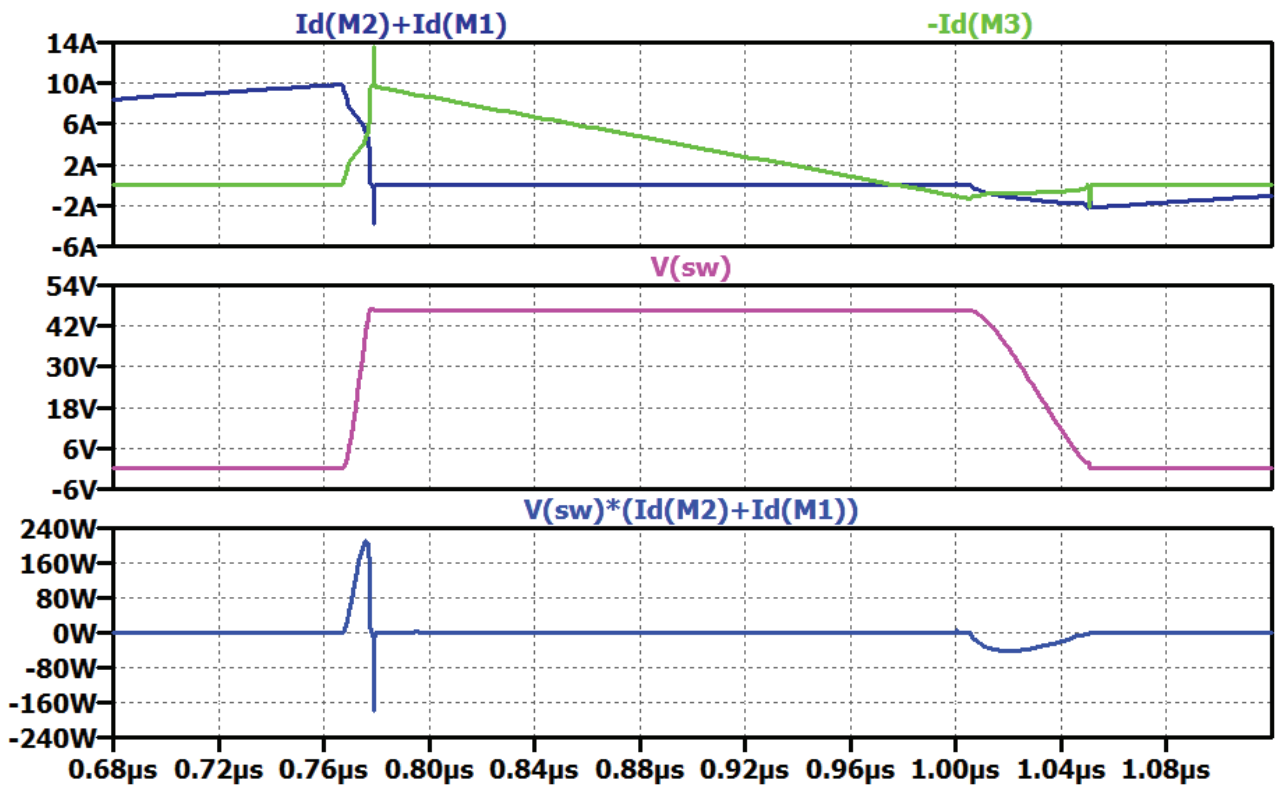
Synchronous Operation



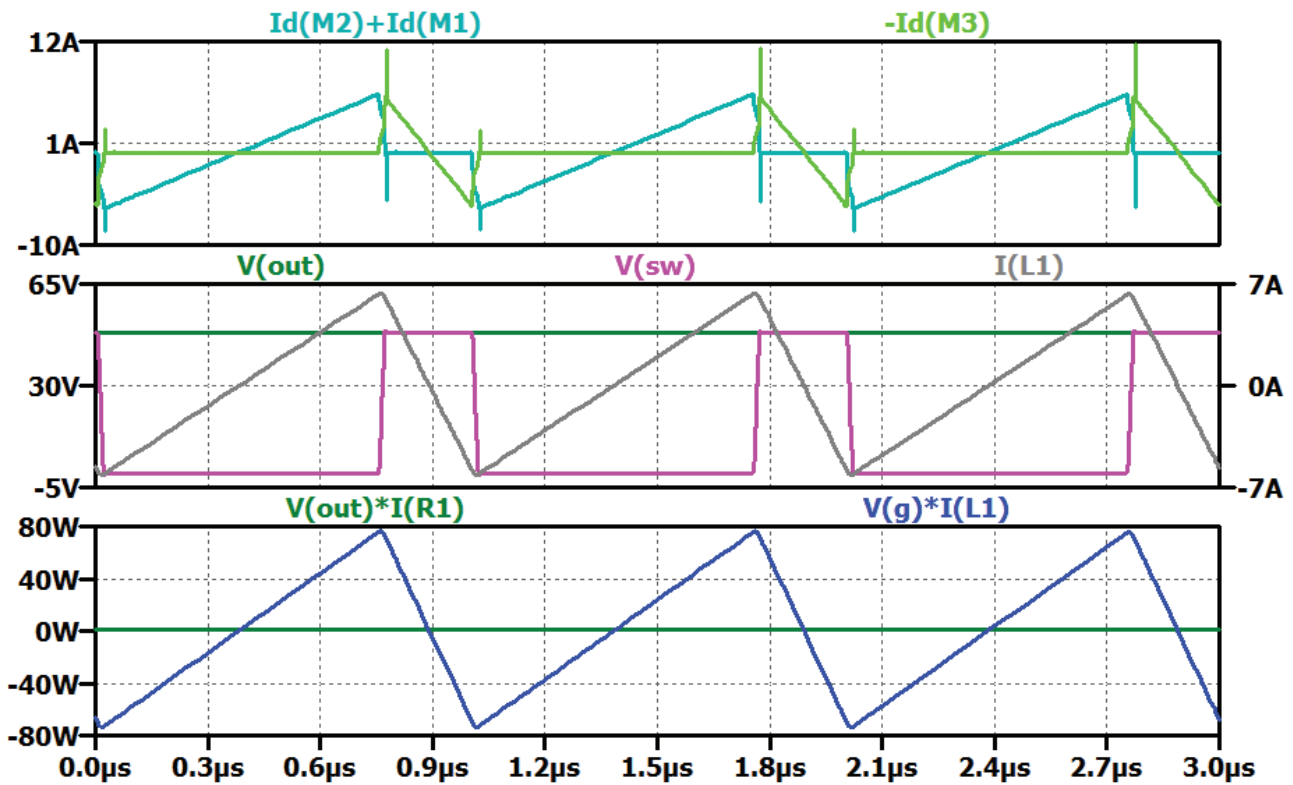
Synchronous Simulation



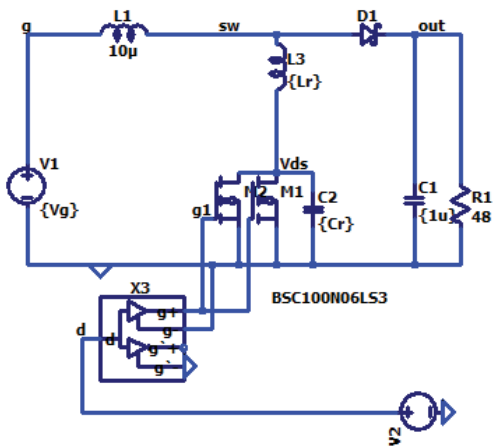
Switching Transitions



Low Power Operation

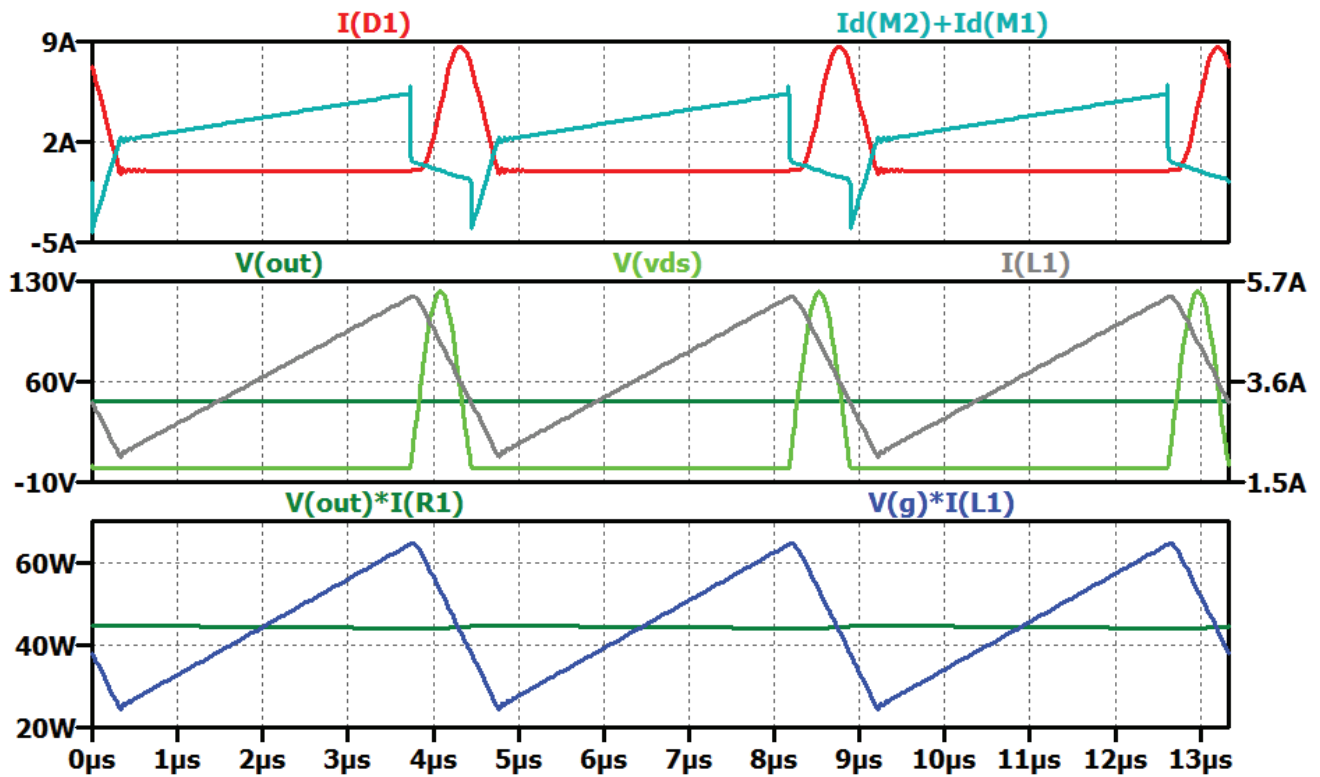


Resonant Operation

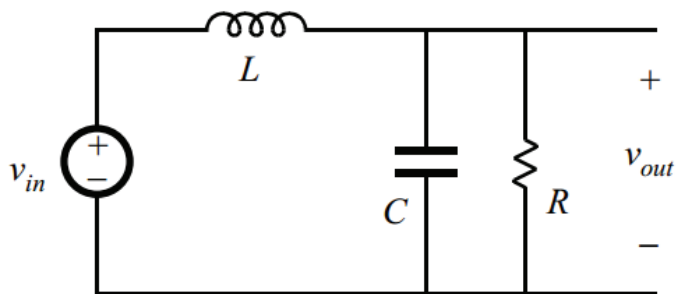


Switching	L	C_{out}	f_s	Diode	η (Sim)
Hard	22uH	22uF	202k	Si (FR)	93.9%
Hard	22uH	22uF	202k	Si Schottky	95.8%
Soft	4.65uH	22uF	202k	Si Schottky	98.4%
Soft	710nH	4.4uF	1 MHz	Si Schottky	98.2%
Soft	710nH	4.4uF	1 MHz	MOSFET	99.6%
Resonant	10uH + 2.4uH	1uF + 10nF	225 kHz	Si Schottky	98.6%
Resonant	10uH + 2.4uH	1uF + 10nF	225 kHz	MOSFET	99.96%

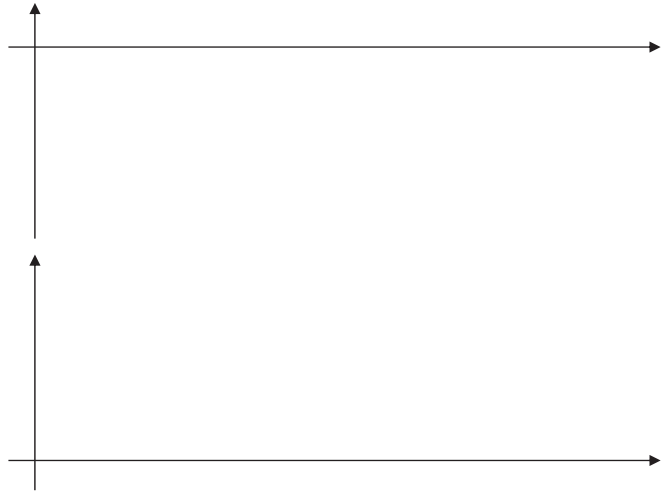
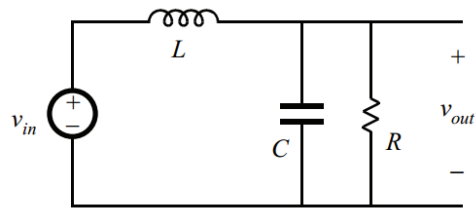
Resonant Boost Converter



Resonant Circuits



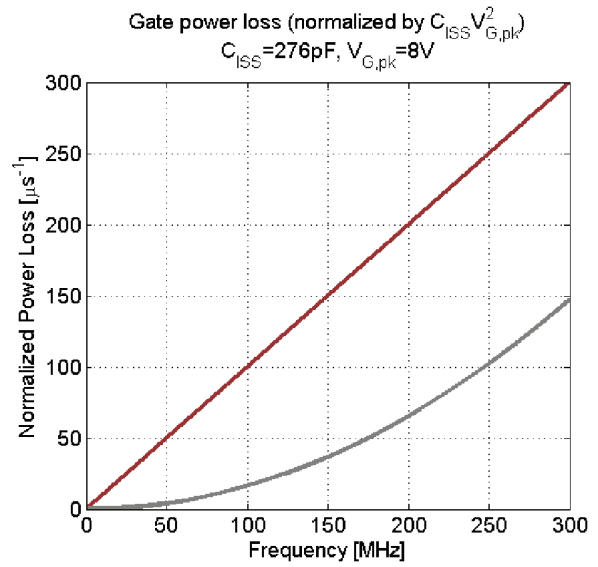
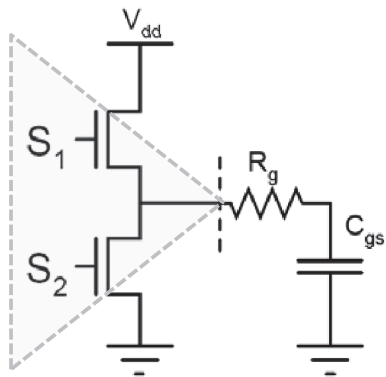
Resonant Circuit Analysis



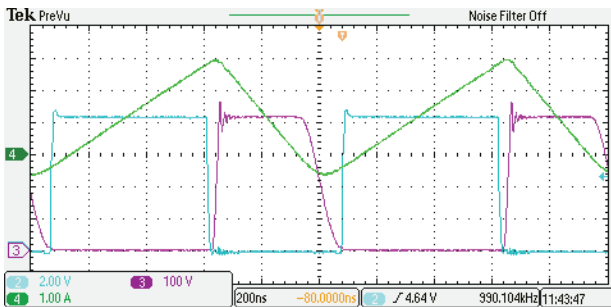
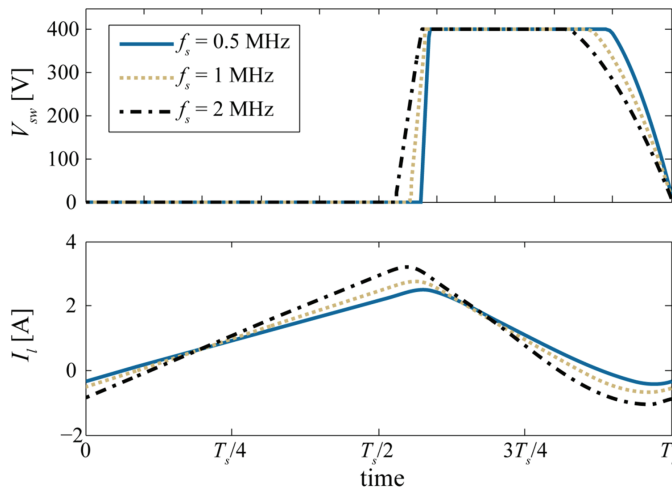
Soft Switching

- Advantages
 - Reduced switching loss
 - Possible operation at higher switching frequency
 - Lower EMI
- Disadvantages
 - Increased current and/or voltage stresses due to circulating current
 - Higher peak and rms current values
 - Complexity of analysis and modeling

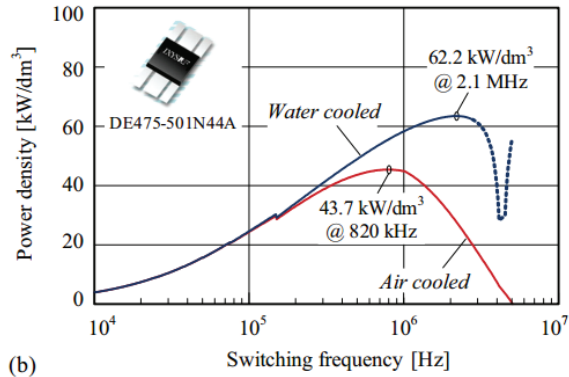
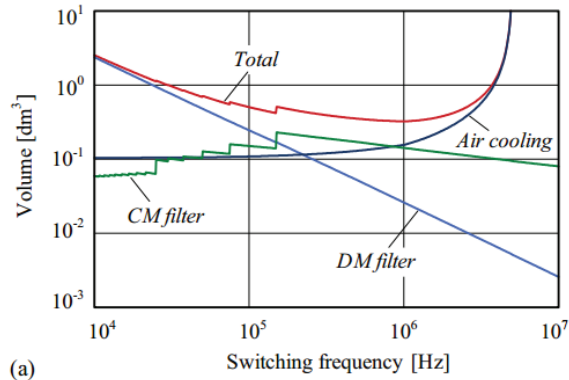
Limitations: Gate Drive



Limitations: t_d/T_s



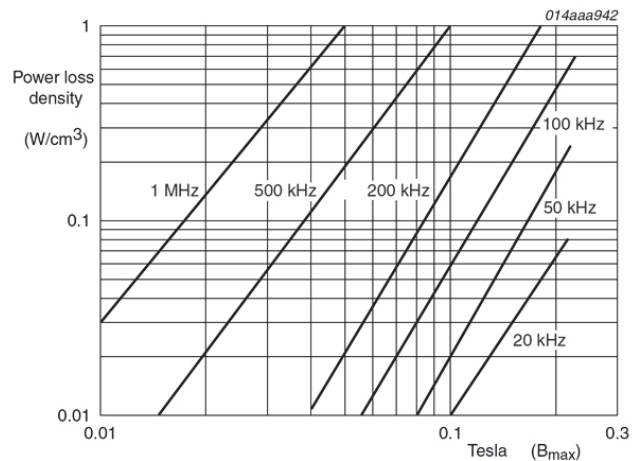
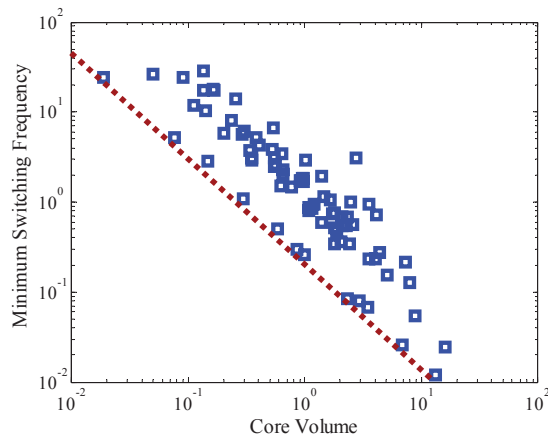
Limitations: Thermal



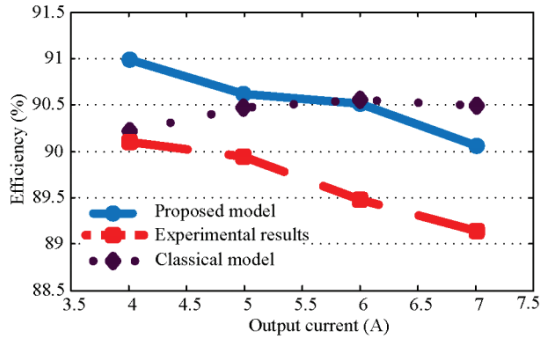
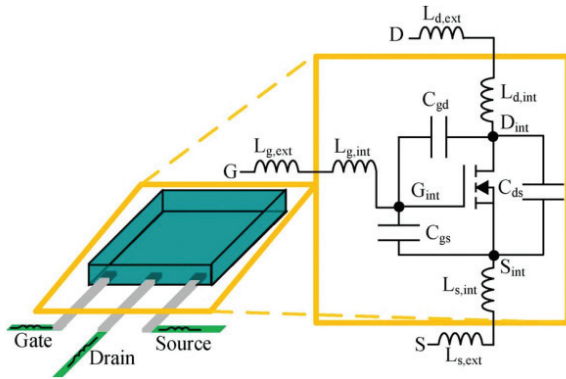
Kolar, J.W.; Drofenik, U.; Biela, J.; Heldwein, M.L.; Ertl, H.; Friedli, T.; Round, S.G.; Wenz, M. Converter Power Density Barriers," *Power Conversion Conference - IPEC 2007*, vol., no., pp.P-9,P-29, 2-5 April 2007



Limitations: Magnetics Design



Limitations: Circuit Modeling



Rodríguez, M.; Rodríguez, A; Mlaja, P.F.; Lamar, D.G.; Zúniga, J.S., "An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model," *Power Electronics, IEEE Transactions on*, vol.25, no.6, pp.1626,1640, June 2010