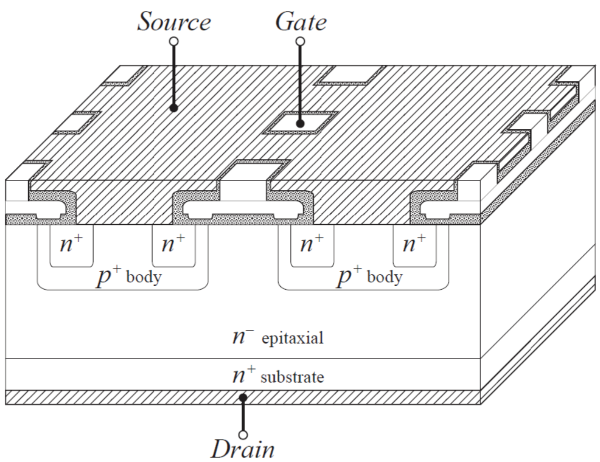
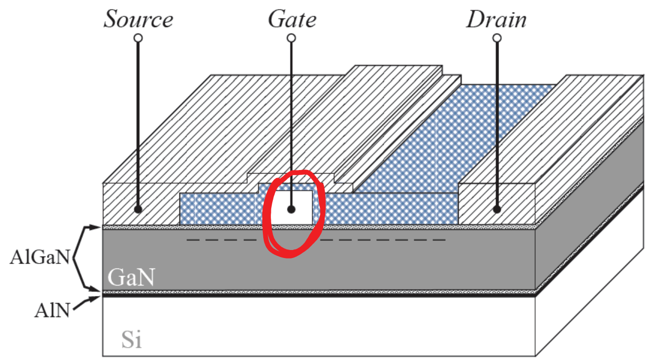
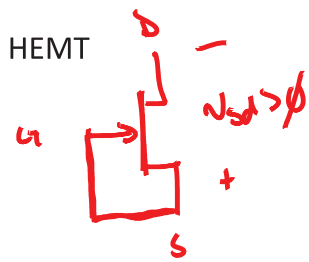
GaN Devices



Vertical Silicon Power MOSFET



Lateral GaN HEMT



- No body diode (reverse conduction due to $V_{gd} > V_{gd,th} \approx 2V$)
  - Use antiparallel (schottky) diode or precise dead time
- Significantly faster switching

Designing with GaN

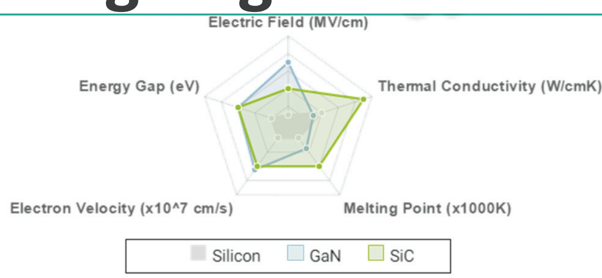
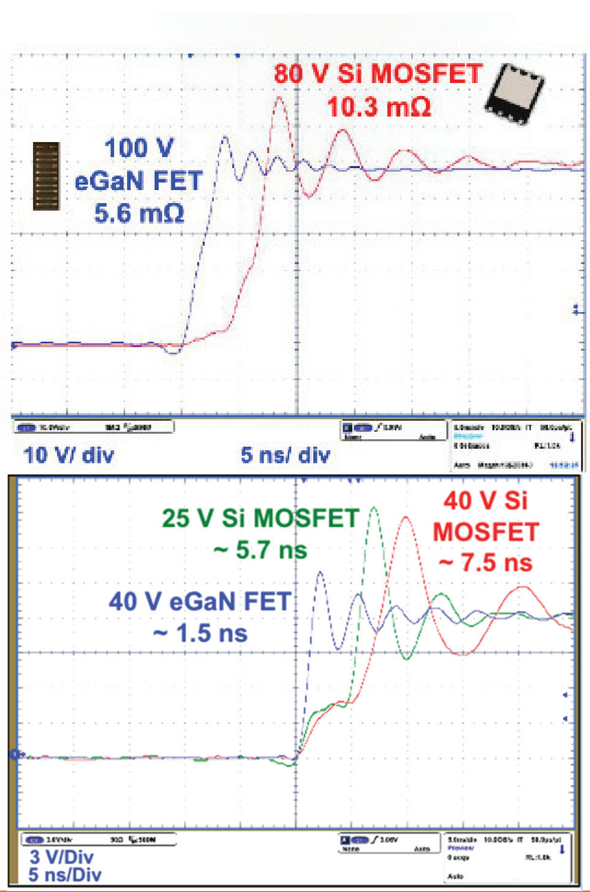


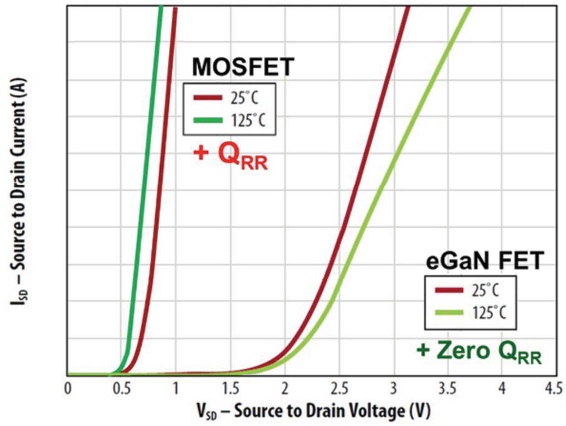
Fig. 1: Material properties of silicon, silicon carbide, and gallium nitride.

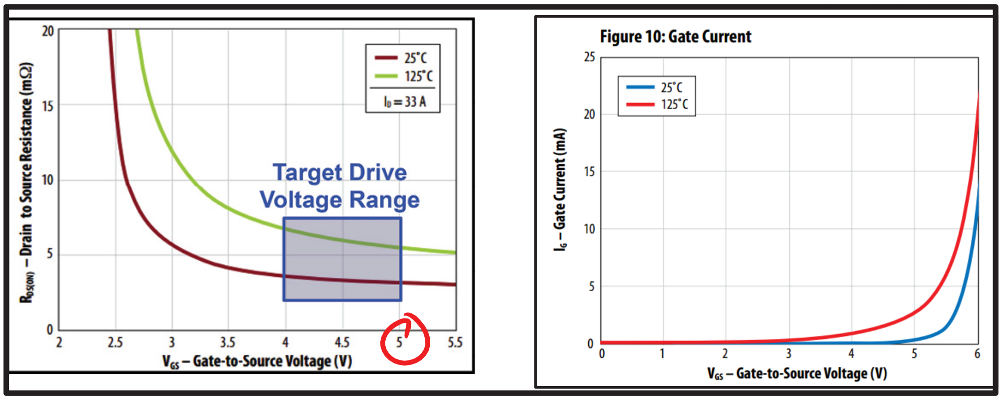


- Because of high electric breakdown field and high electron velocity, GaN devices with comparable R_{on} can be significantly smaller and switch must faster.
- Need **very** good layout to prevent ringing from causing overvoltage and device failure.
- More information:
  - http://potenntial.eecs.utk.edu/About.php?topic=PowerSemiconductors

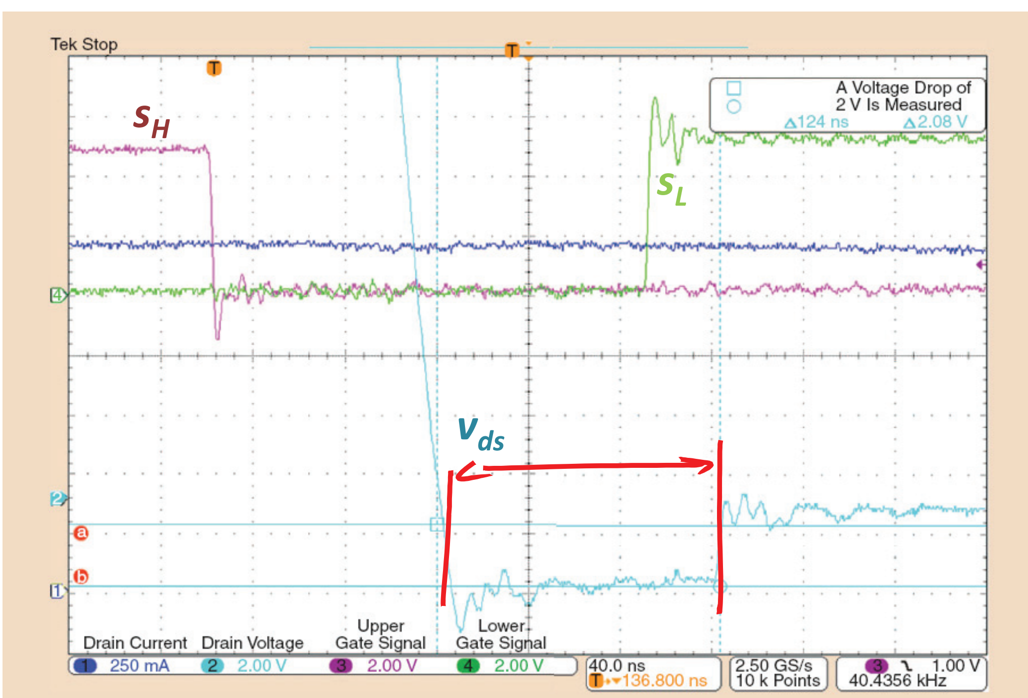
GaN Design Issues

1. Reverse conduction mechanism
2. Sensitivity to parasitics
3. Gate robustness
4. Small size -> Thermal, soldering difficult

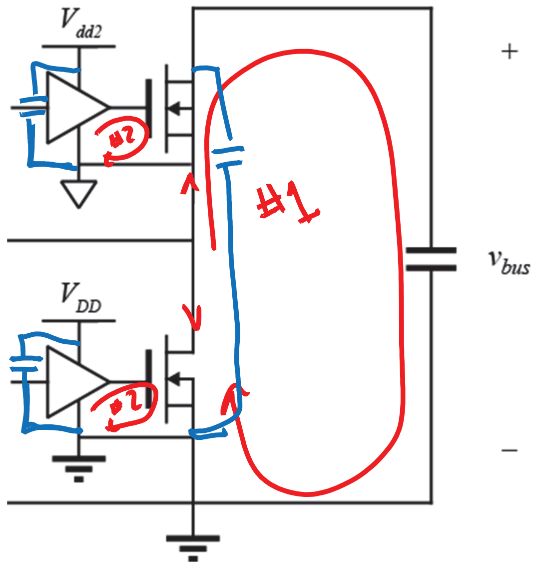




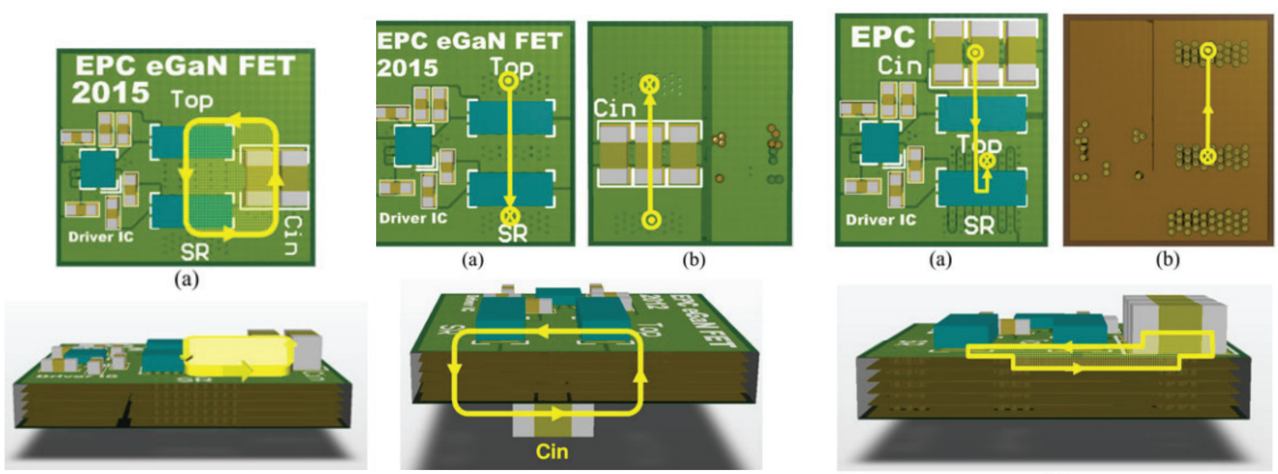
Reverse Conduction



Bridge Layout

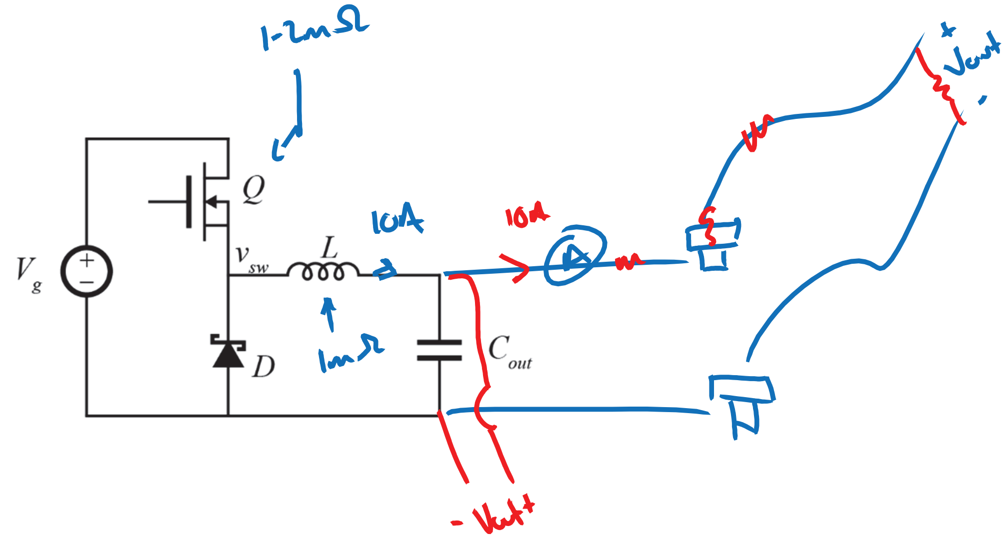


Half Bridge Layout: Example

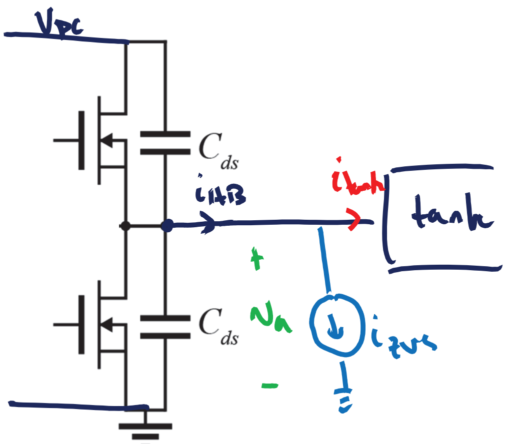


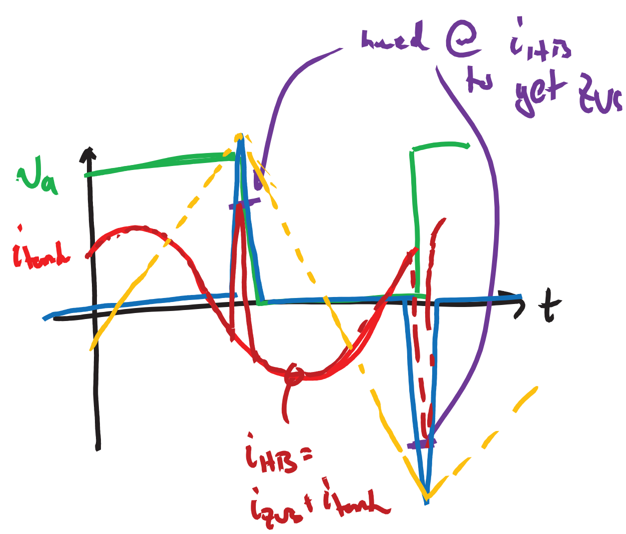
Lateral Vertical "Optimal"

Kelvin Measurement

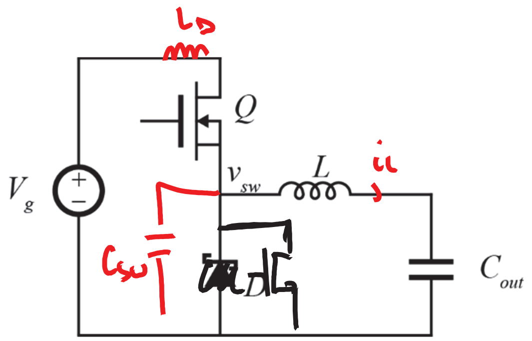


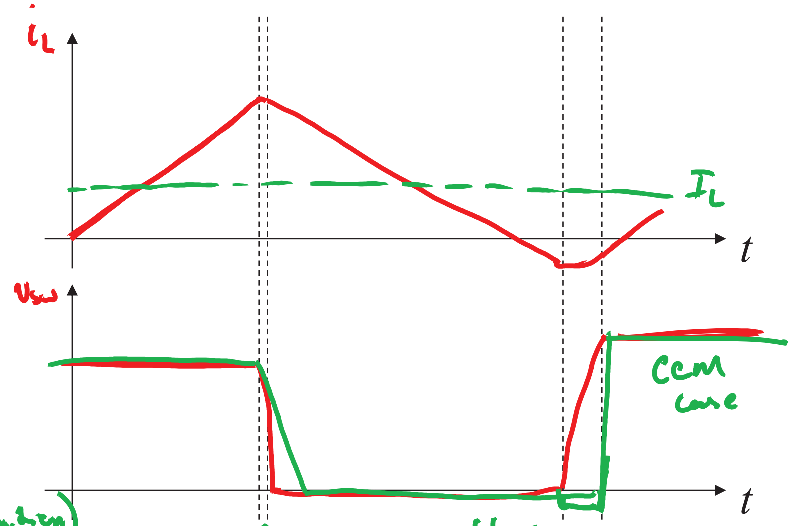
ZVS Assist Circuits





Remaining Switching Losses

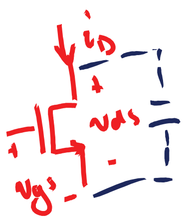


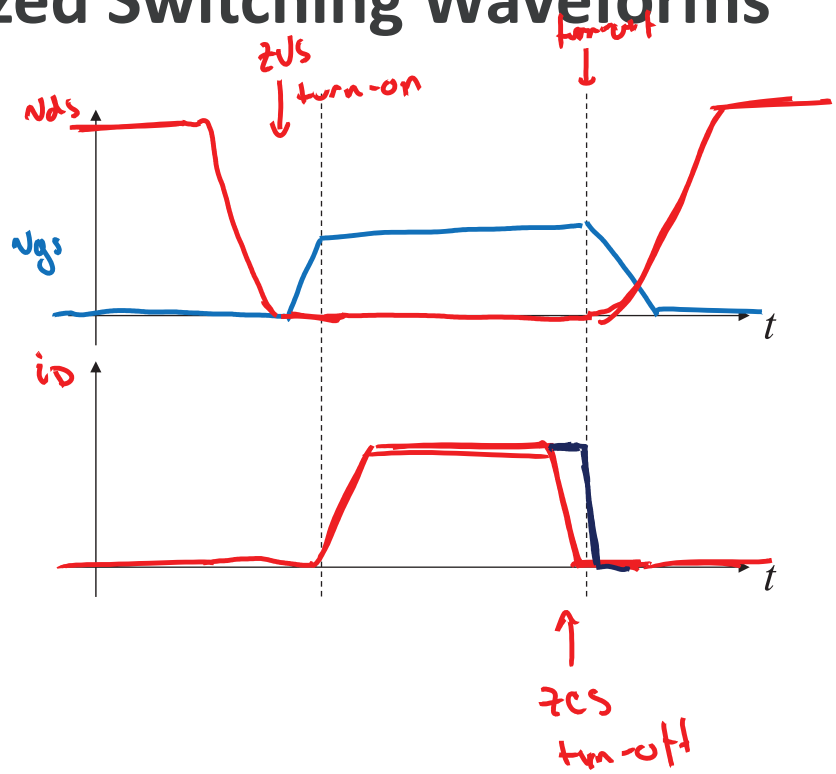


Switching-related Losses

1. C_{sw} → reduced (2nd transition)
2. Overlap → { turn-on → reduced; turn-off → ($\frac{I_L}{C_{sw}} \ll \frac{i_g}{C_{gd}}$) L_D may increase (!) }
3. Reverse Recovery → eliminated
4. Q_g → no effect
5. Body diode conduction → reduce (dt setting)
6. Shoot-through → aleviated
7. Additional parasitics (L_D) ?

Idealized Switching Waveforms





Class-E Amplifier

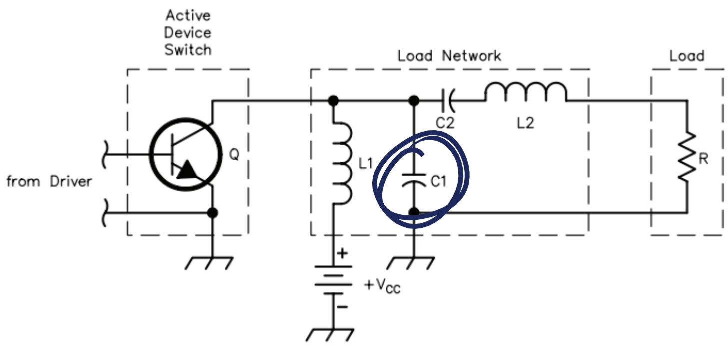


Fig 2—Schematic of a low-order Class-E amplifier.

$V_{ds,pk} > 3 \times V_g$

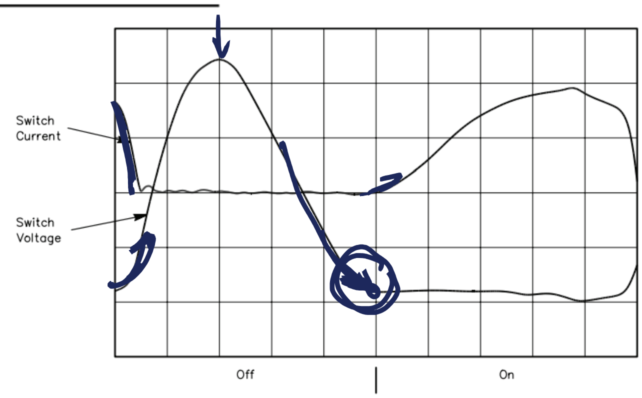
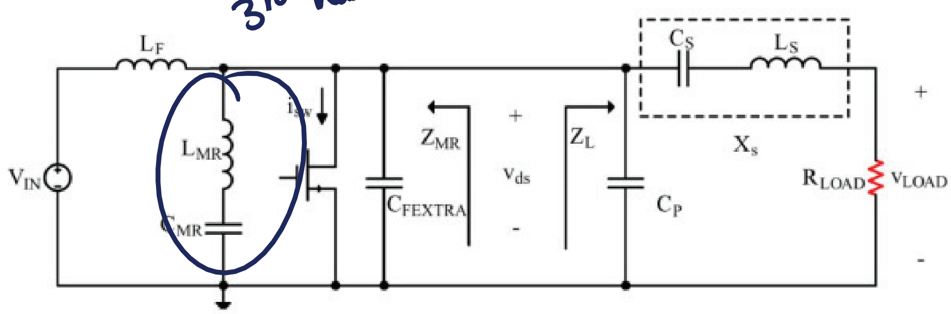
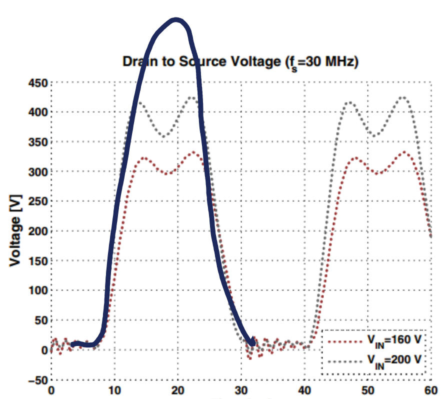


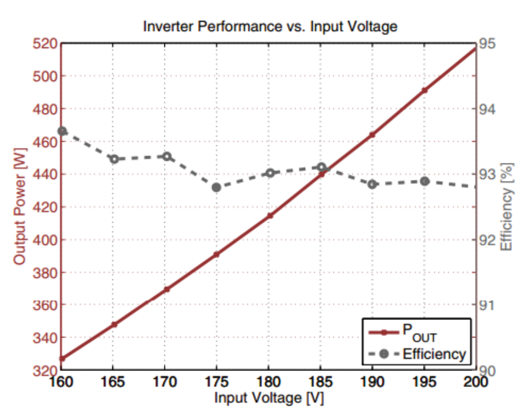
Fig 3—Actual transistor voltage and current waveforms in a low-order Class-E amplifier.

Class Φ_2 Inverter

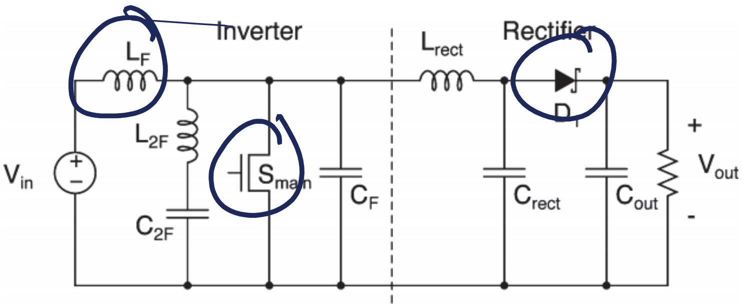
3rd harmonic



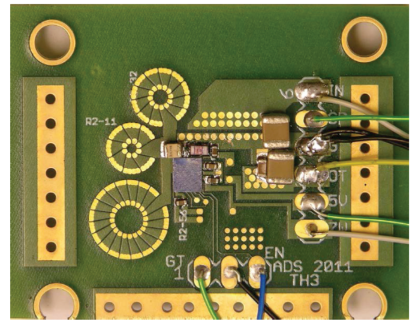




VHF DC-DC Converter



Φ_2 Boost Converter



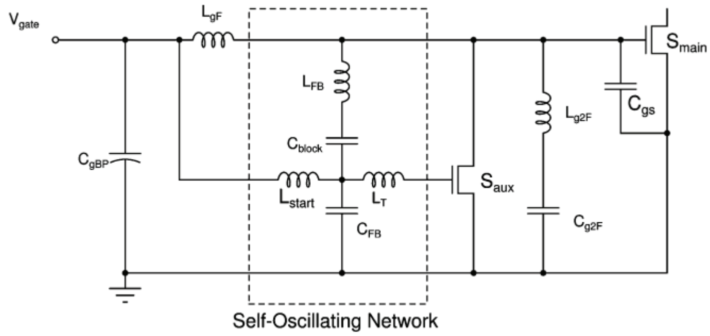


Fig. 5. Trapezoidal resonant gate drive circuit with self-oscillating network. The converter is enabled by applying the voltage V_{gate}, and disabled by setting V_{gate} to zero. This gate driver is employed in the 110-MHz converter (Fig. 9).