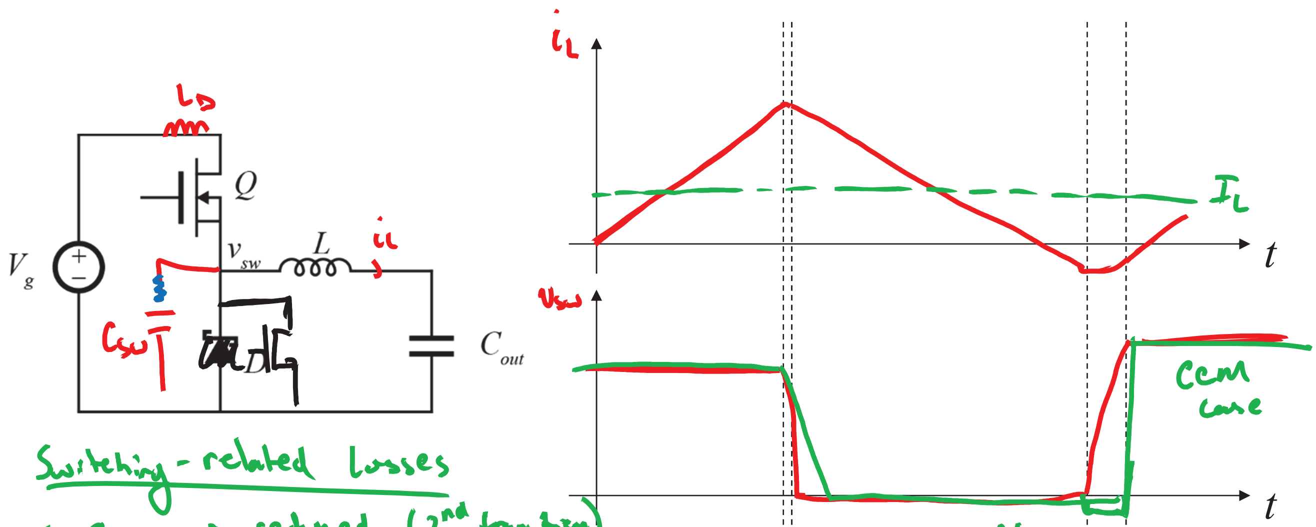
Remaining Switching Losses



Switching-related Losses

1. C_{sw} → reduced (2nd transition)
2. Overlap → { turn-on → reduced; turn-off → $\left(\frac{I_L}{C_{sw}} \ll \frac{i_g}{C_{gd}}\right)$ — L_D may increase (!)
3. Reverse Recovery → eliminated
4. Q_g → no effect
5. Body diode conduction → reduce (dt setting)
6. Shoot-through → aleviated
7. Additional parasitics (L_D) ?

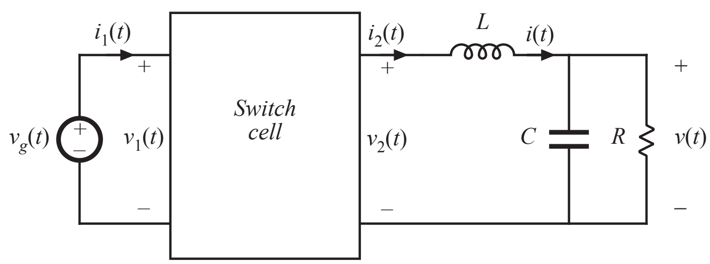
Chapter 20: Resonant Switch Topologies

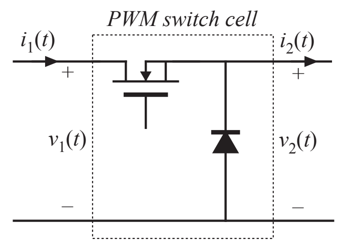
- Introduction
- 20.1 The zero-current-switching quasi-resonant switch cell
  - 20.1.1 Waveforms of the half-wave ZCS quasi-resonant switch cell
  - 20.1.2 The average terminal waveforms
  - 20.1.3 The full-wave ZCS quasi-resonant switch cell
- 20.2 Resonant switch topologies
  - 20.2.1 The zero-voltage-switching quasi-resonant switch
  - 20.2.2 The zero-voltage-switching multiresonant switch
  - 20.2.3 Quasi-square-wave resonant switches
- 20.3 Ac modeling of quasi-resonant converters
- 20.4 Summary of key points

The resonant switch concept

General idea:

- PWM switch network is replaced by a resonant switch network
- This leads to a quasi-resonant or quasi-squarewave version of the original PWM converter

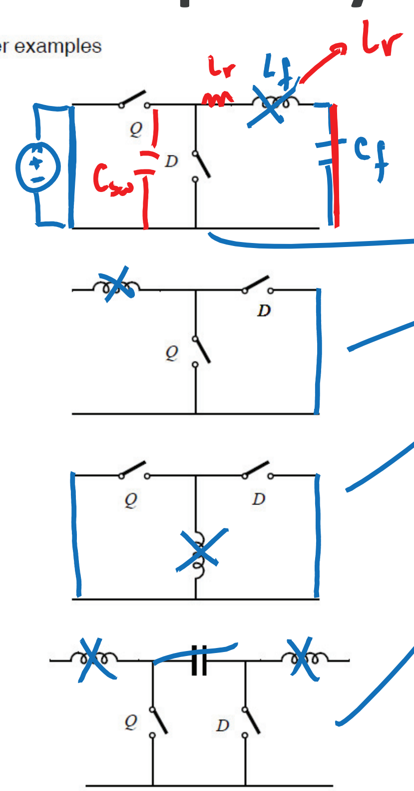




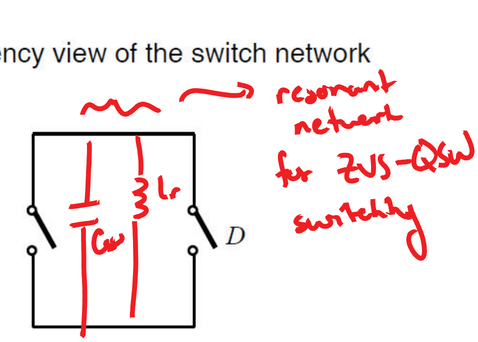
Example: realization of the switch cell in the buck converter

High Frequency Switch Network

Converter examples



High-frequency view of the switch network



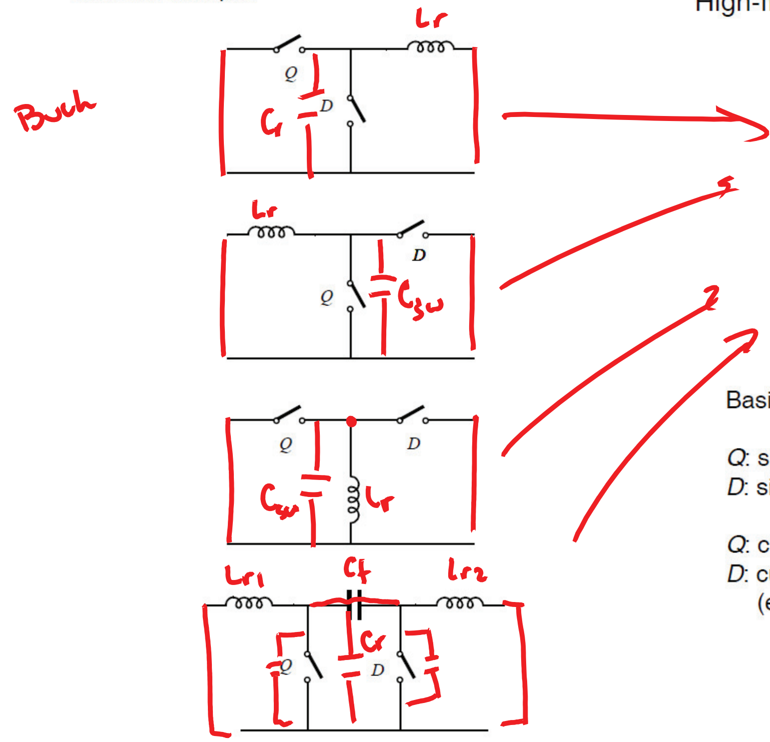
Basic switch implementation options

Q: single-quadrant (transistor)
D: single-quadrant (diode)

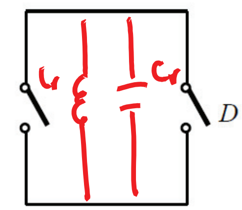
Q: current-bidirectional (e.g. MOSFET)
D: current-bidirectional synchronous rectifier (e.g. MOSFET)

ZVS-QSW: Review

Converter examples



High-frequency view of the switch network

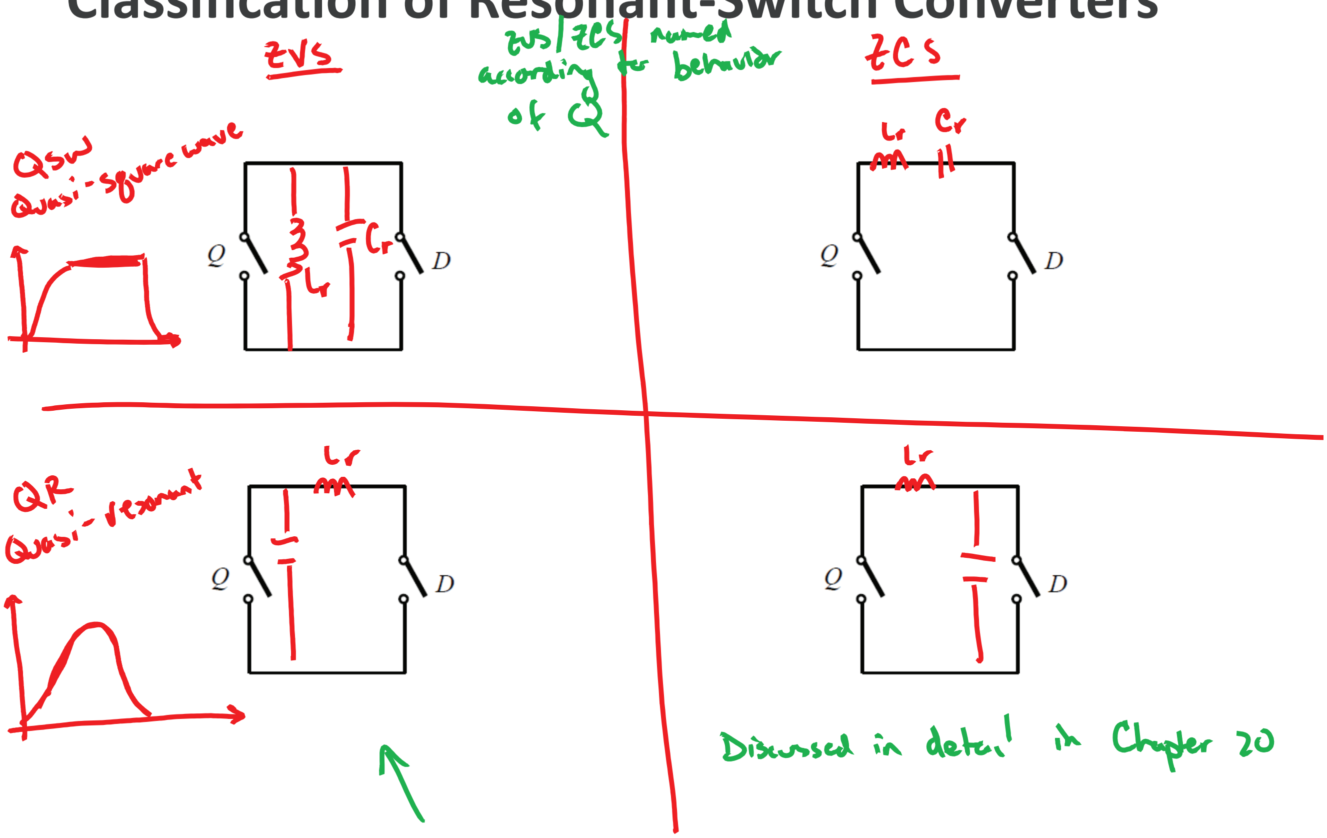


Basic switch implementation options

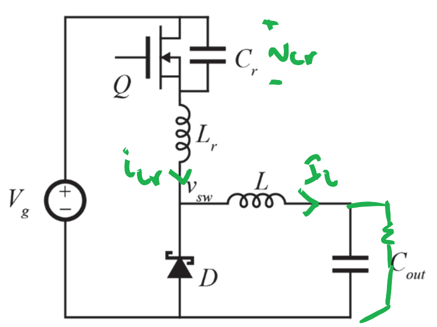
Q: single-quadrant (transistor)
D: single-quadrant (diode)

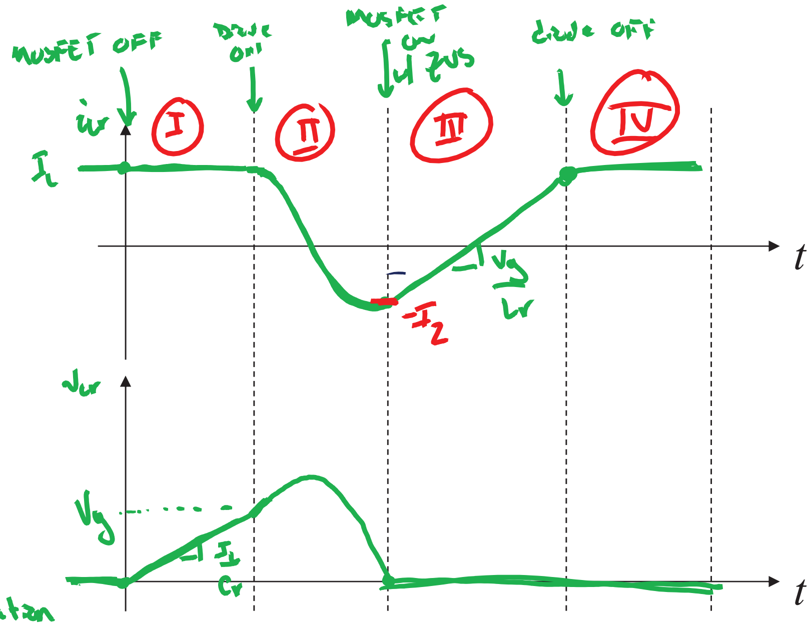
Q: current-bidirectional (e.g. MOSFET)
D: current-bidirectional synchronous rectifier (e.g. MOSFET)

Classification of Resonant-Switch Converters

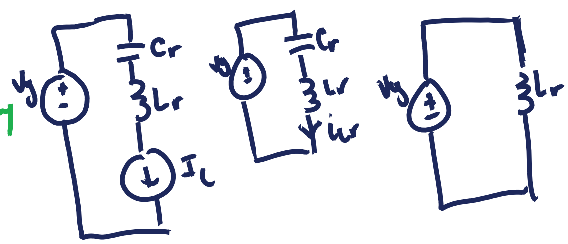


ZVS-QR Buck





+ Incorporates both C_{ds} & L_s of MOSFET into operation
+ $i_{ds,pk} = I_L$
- $V_{ds,pk}$ will increase significantly
- Diode assumed ideal



ZVS-QR State Plane

$V_{base} = V_g \qquad Z_0 = \sqrt{L_r/C_r}$

(I): $\frac{I_1}{C_r} t_1 = V_g \rightarrow \theta_1 = \frac{1}{J_L}$

(II): $r_2^2 = J_L^2 = J_2^2 + 1$

$J_2 = \sqrt{J_L^2 - 1}$

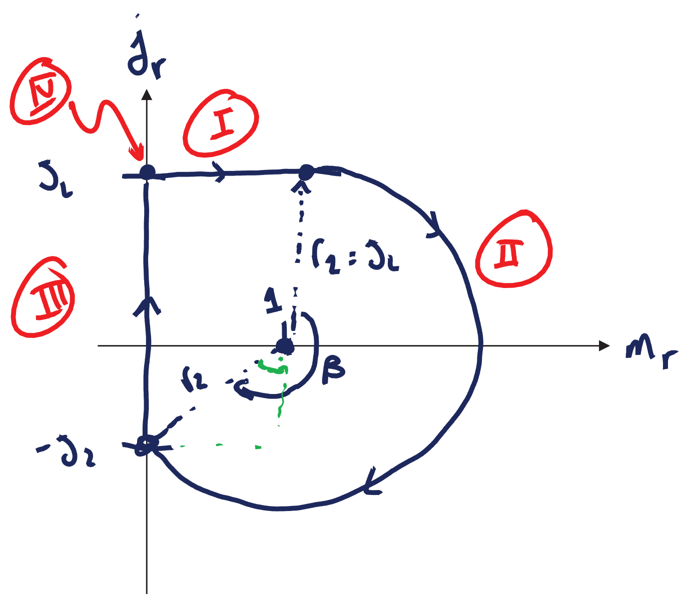
$\beta = \pi + \sin^{-1}\left(\frac{1}{J_L}\right)$

(III): $\frac{V_g}{L_r} t_3 = I_2 + I_L$

$\theta_3 = J_2 + J_L$

(IV): X

$\theta_1 + \beta + \theta_3 + \theta_4 = \frac{2\pi}{F}$



Averaging

Apply volt-second balance on L_f

$$\langle v_{L_f} \rangle = 0 = \langle v_{sw} \rangle - V$$

$$0 = V_g - \langle v_{cr} \rangle - \cancel{\langle v_{Lr} \rangle}^{\,0} - V$$

$$V = V_g - \langle v_{cr} \rangle$$