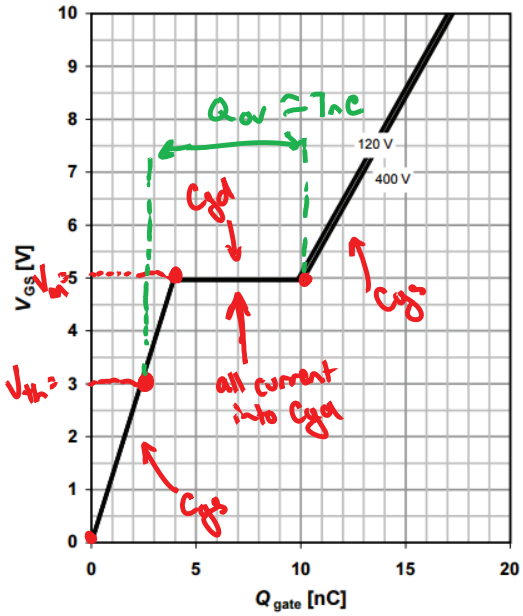
Overlap Time

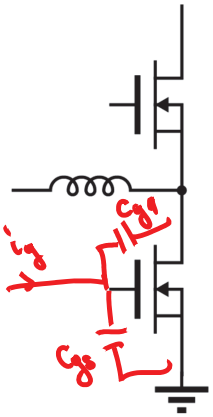
9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=5.2 A pulsed

parameter: V_{DD}

Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.34 mA	2.5	3	3.5	
Gate resistance	R_G	f=1 MHz, open drain	-	1.8	-	Ω





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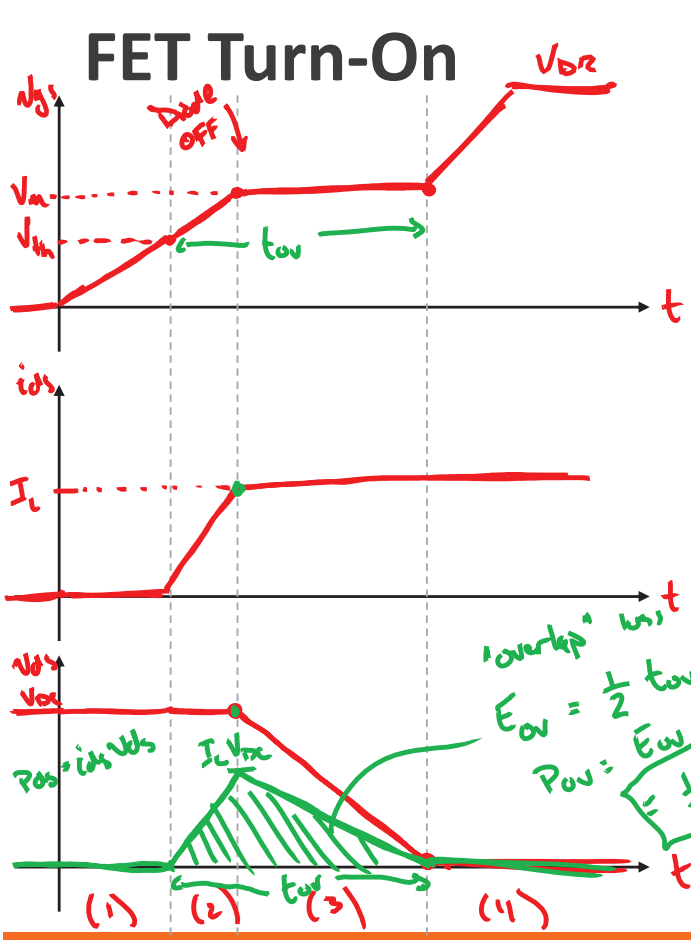
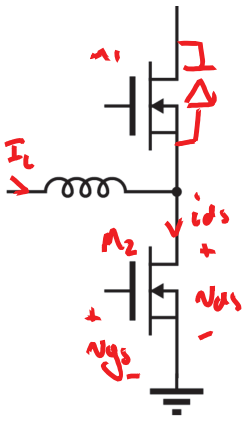
FET Turn-On



in act/sat

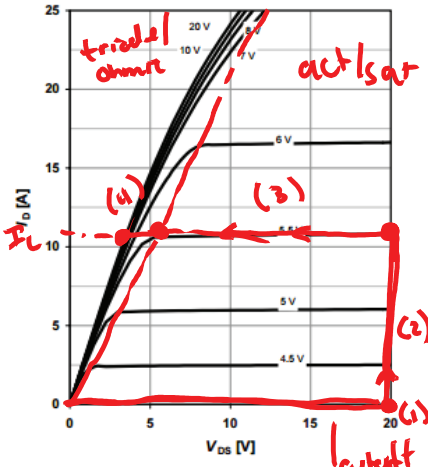
$i_{ds} \simeq g_{fs}(v_{gs} - V_{th})$



"overlap" loss, t_{ov}

$E_{ov} = \frac{1}{2} t_{ov} I_L V_{DC}$

$P_{ov} = E_{ov} f_s = \frac{1}{2} I_L V_{DC} t_{ov} f_s$



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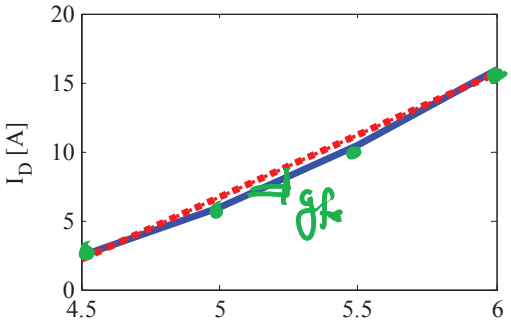
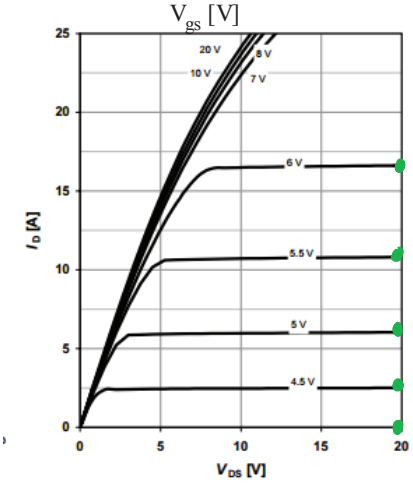
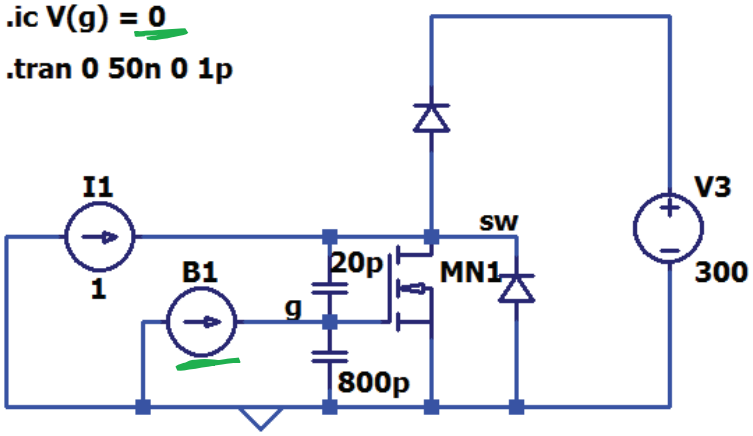
Device Transconductance



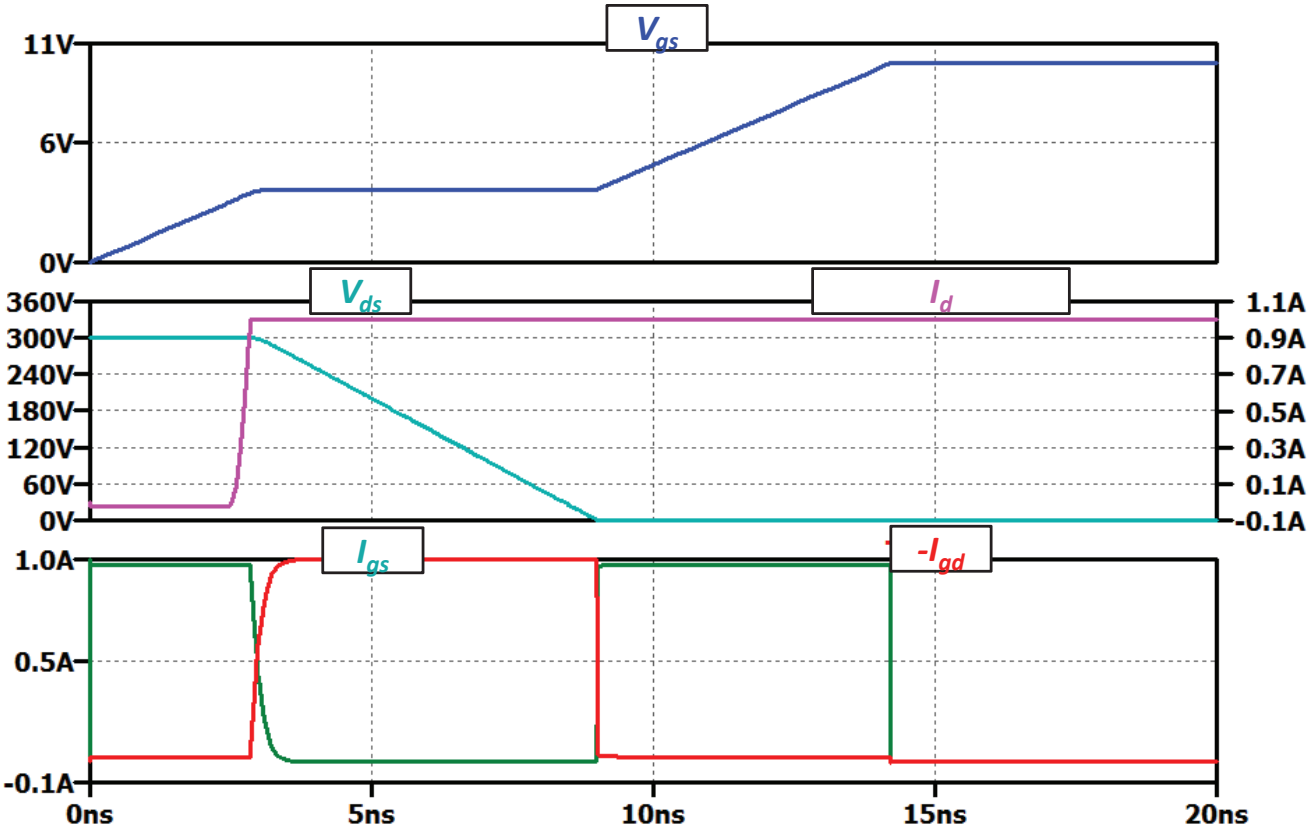


Example Simulation

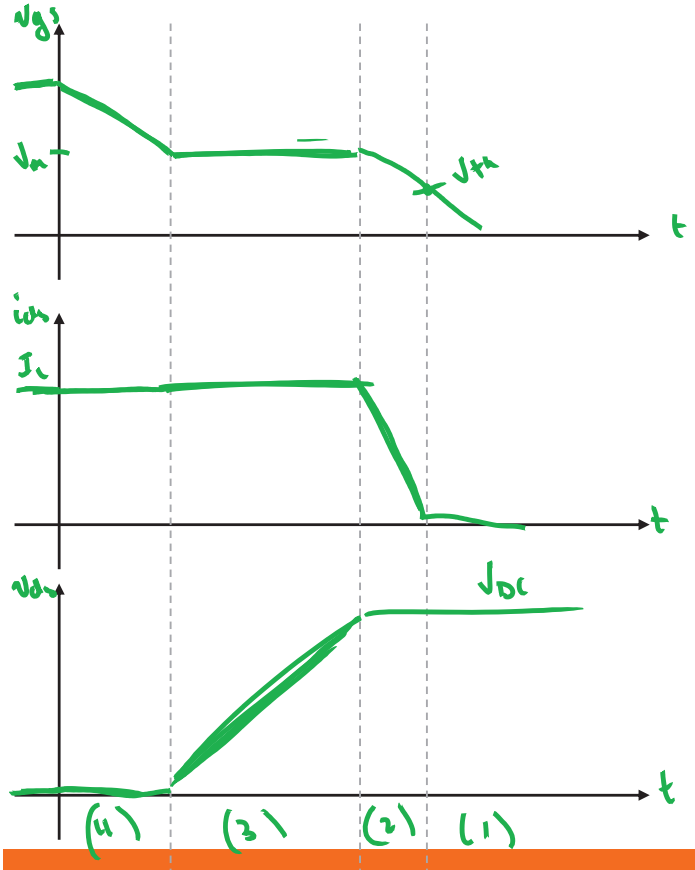



```
.ic V(g) = 0
.tran 0 50n 0 1p

I=IF(V(g)<10,1,0)

.model myD D(n=.01)

.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m  Vds=600 Ron=385m Qg=0n)
```

Simulation Waveforms – Turn On

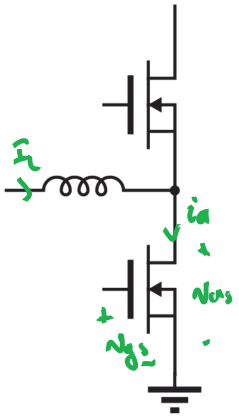


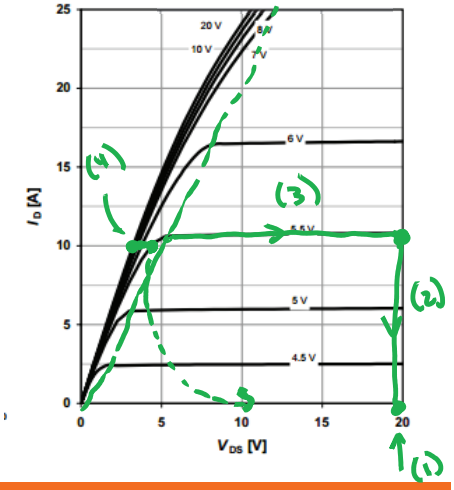
Turn-Off Transition



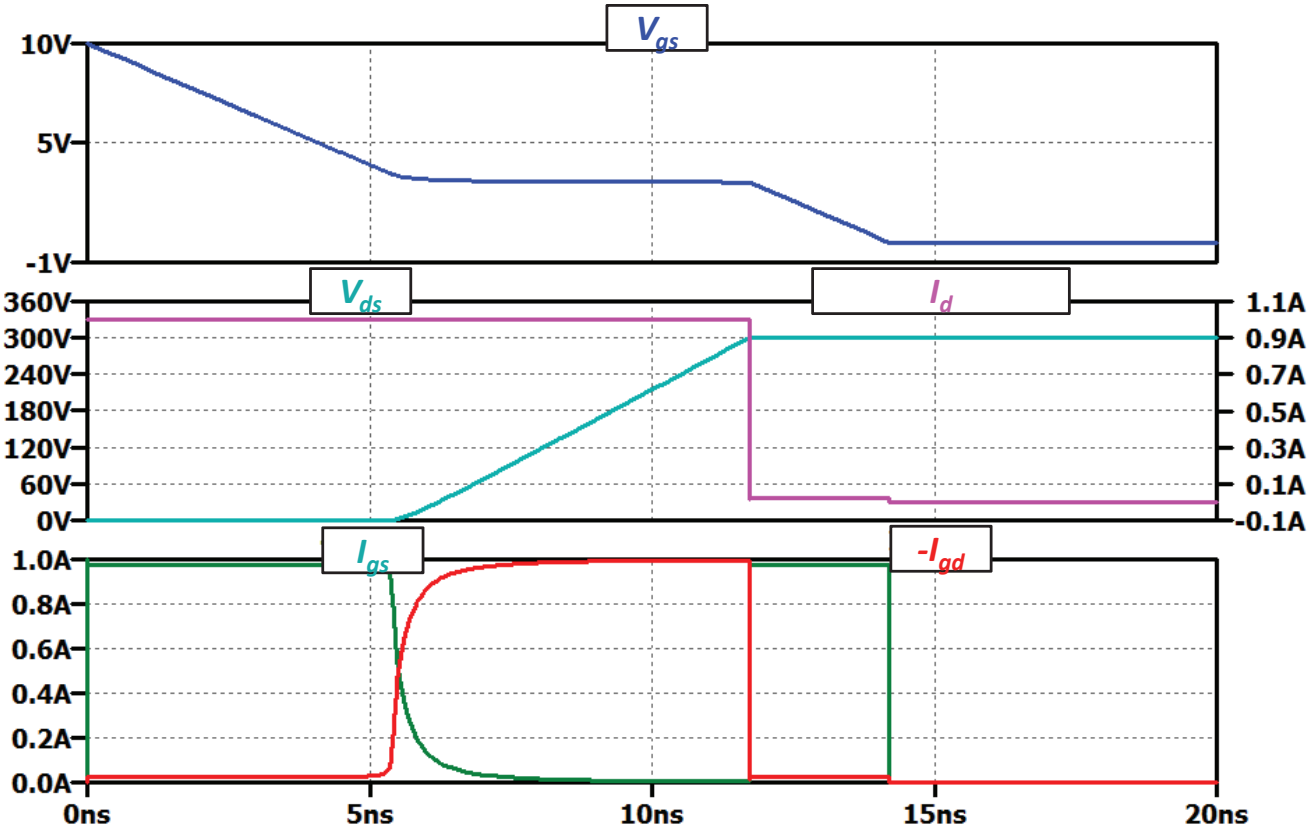
$P_{ov(off)} = P_{ov(on)}$

$= \frac{1}{2} V_{DS} I_L \frac{t_{sw}}{T_s}$



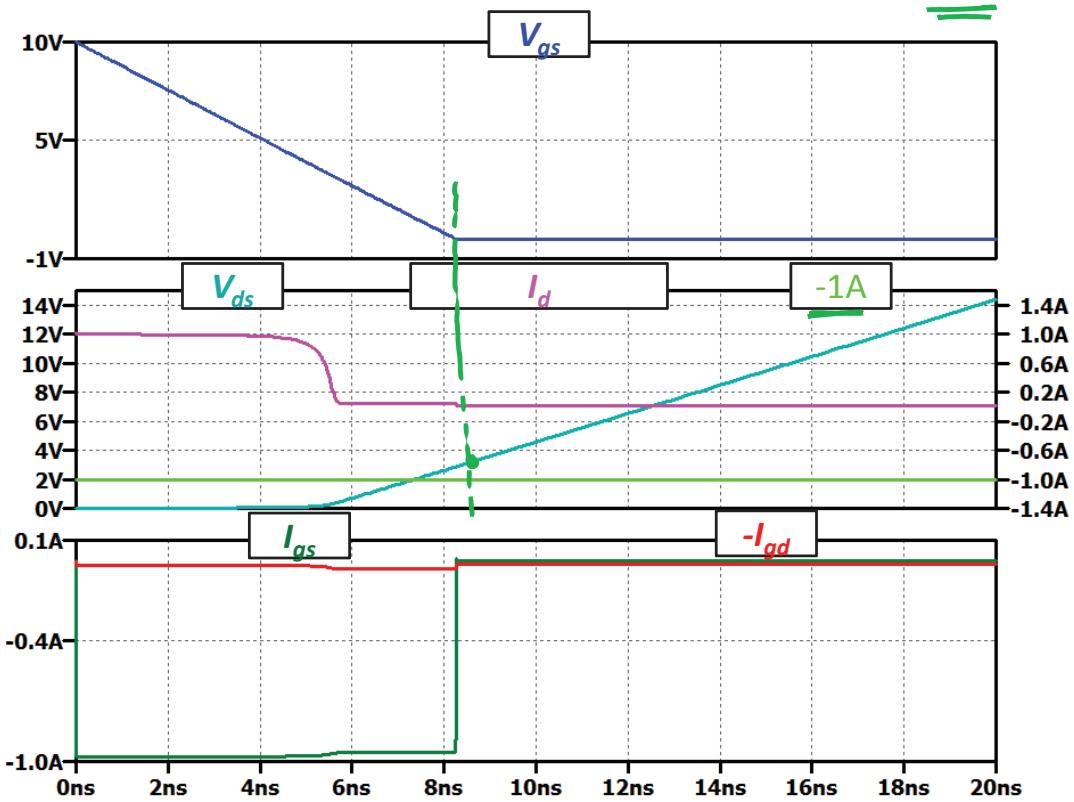


Turn-off



Turn-Off (Drain Dominated)

Add C_{ds}

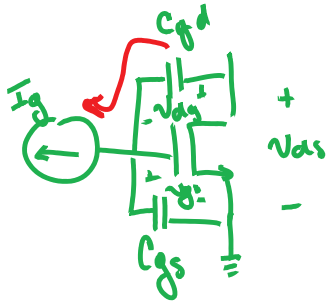


Gate- vs. Drain-Limited Switching

Ideally, FET turns off completely before V_{ds} begins to rise

$$\frac{dV_{ds}}{dt} = \frac{I_L}{C_{ds}}$$

if FET in cutoff



$$V_{ds} = V_{gs} + V_{dg}$$

during $\frac{dv}{dt}$ interval $\rightarrow V_{gs} = V_m$

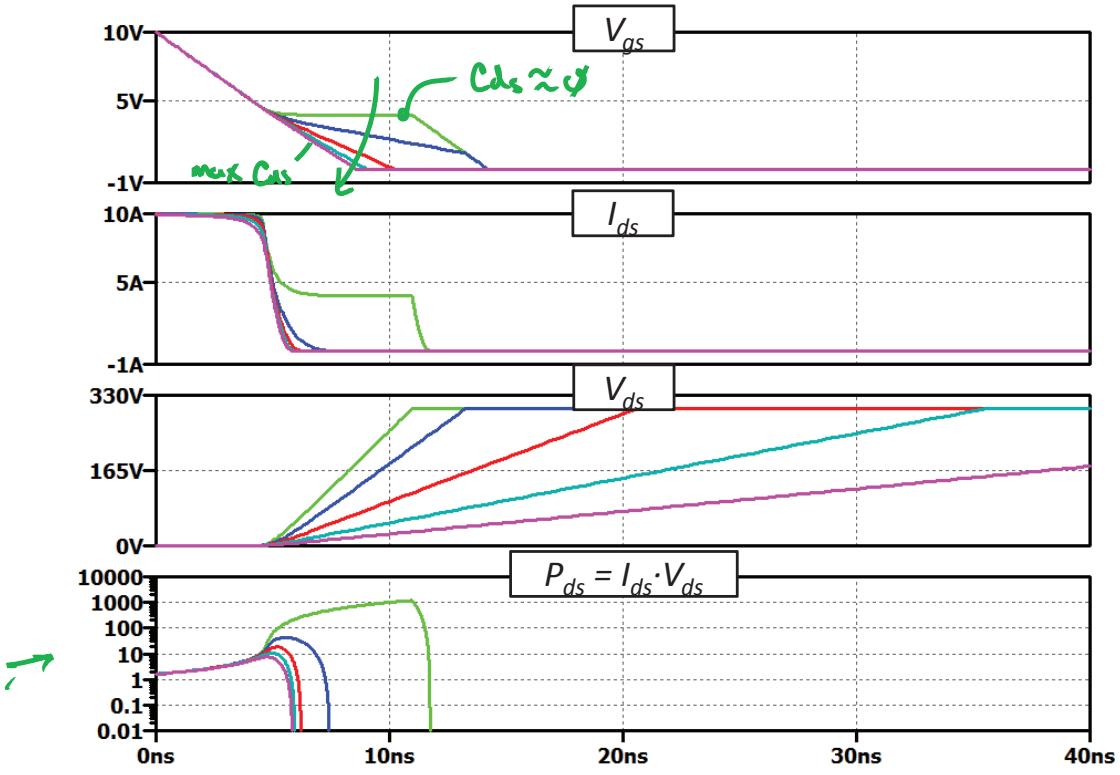
$$\frac{dV_{ds}}{dt} = \frac{dV_{dg}}{dt} = \frac{I_g}{C_{gd}}$$

$$\frac{I_g}{C_{gd}} >> \frac{I_L}{C_{ds}}$$

↳ $P_{ov(off)} \approx \emptyset$

if opposite is true, $P_{ov(off)} = P_{ov(on)}$

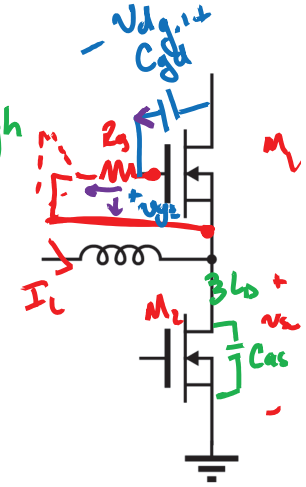
Simulation Results: Cds Sweep

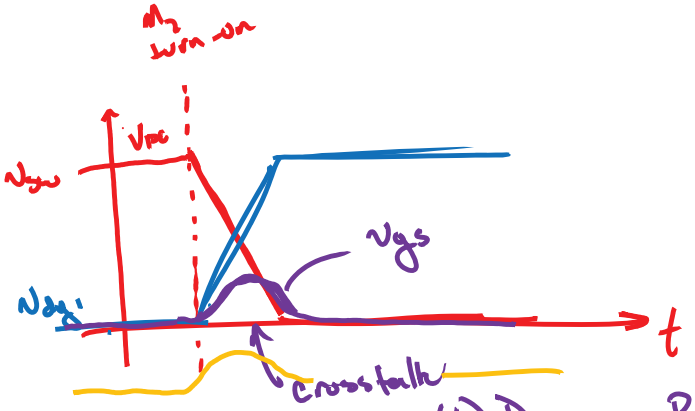


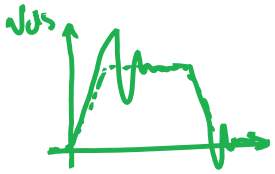
Limitations on Switching Speed

(1) Overshoot / ringing

(2) Crosstalk / shoot-through







Remedies for cross-talk:

(1) Decrease $R_{g,L}$ on M_1

(2) Turn on M_2 more slowly (increase $R_{g,H}$ on M_2)

(3) Use negative v_{gs} for turn-off