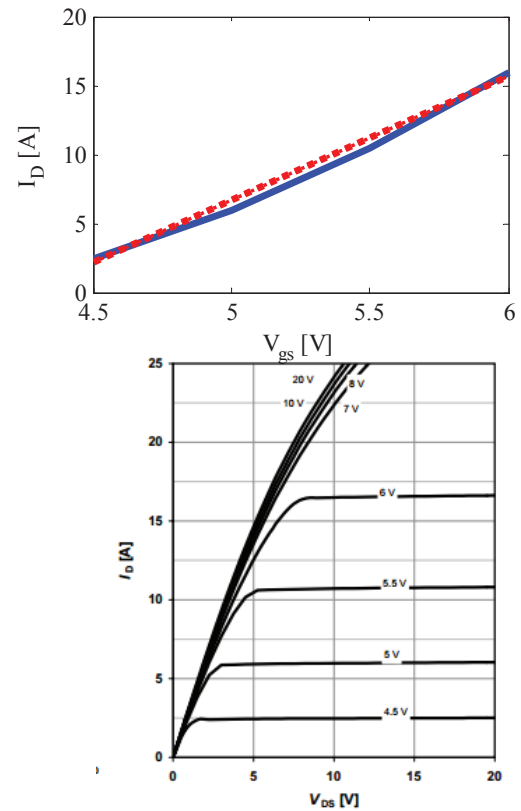
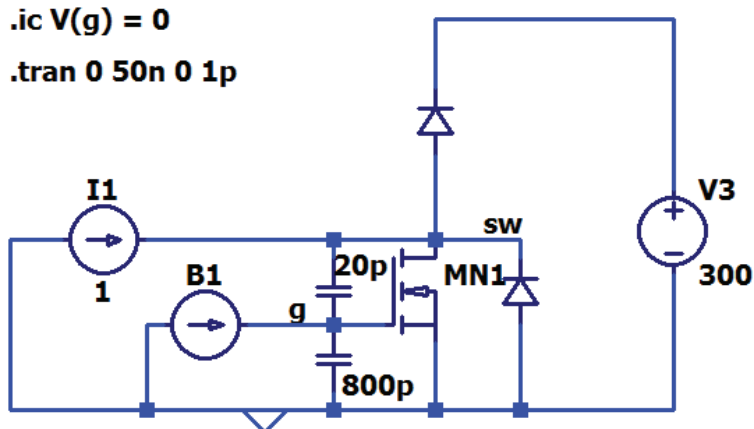


Device Transconductance



Example Simulation

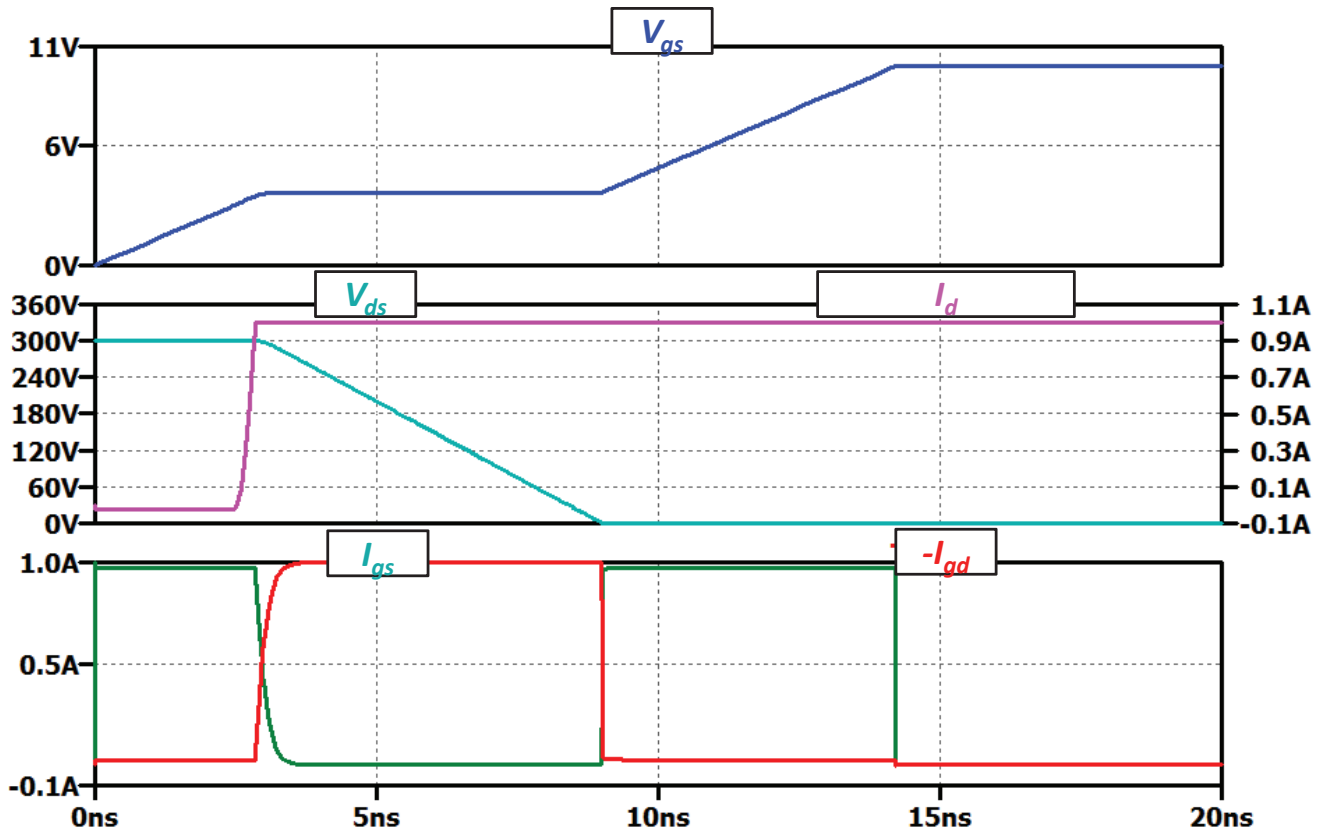


I=IF(V(g)<10,1,0)

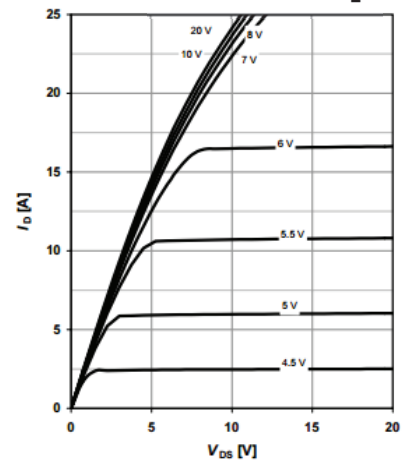
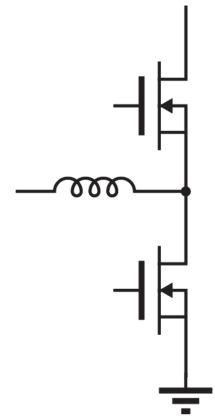
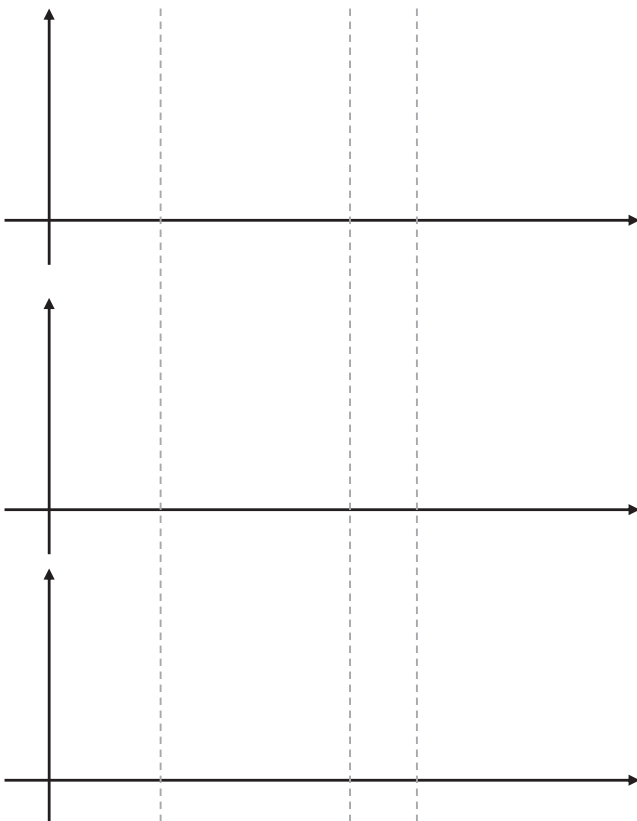
.model myD D(n=.01)

**.model testFET VDMOS(Rg=.1 Rd=0 Rs=0 Vto=3 Kp=9 Cgdmax=0p
+ Cgdmin=0p Cgs=0p Cjo=1.5f Is=26p Rb=0m Vds=600 Ron=385m Qg=0n)**

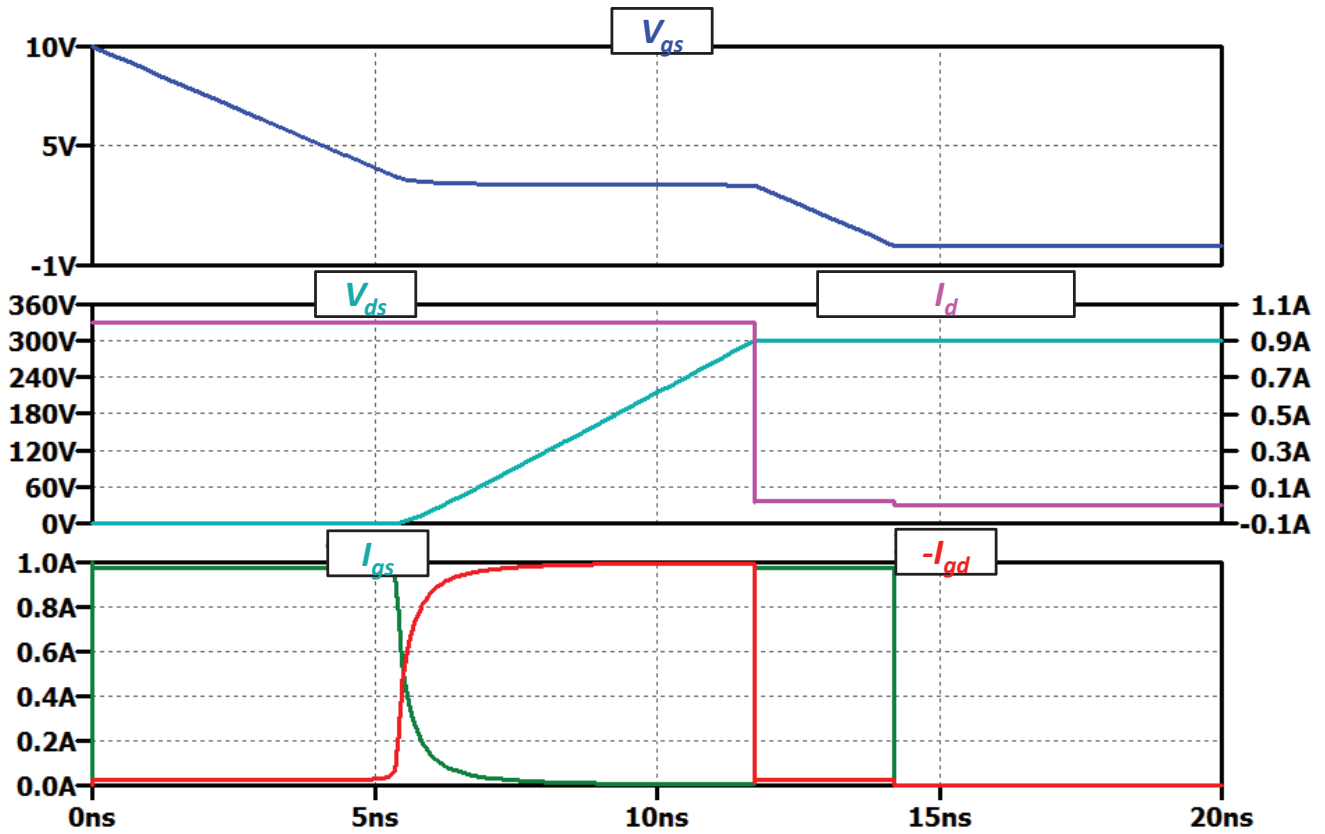
Simulation Waveforms – Turn On



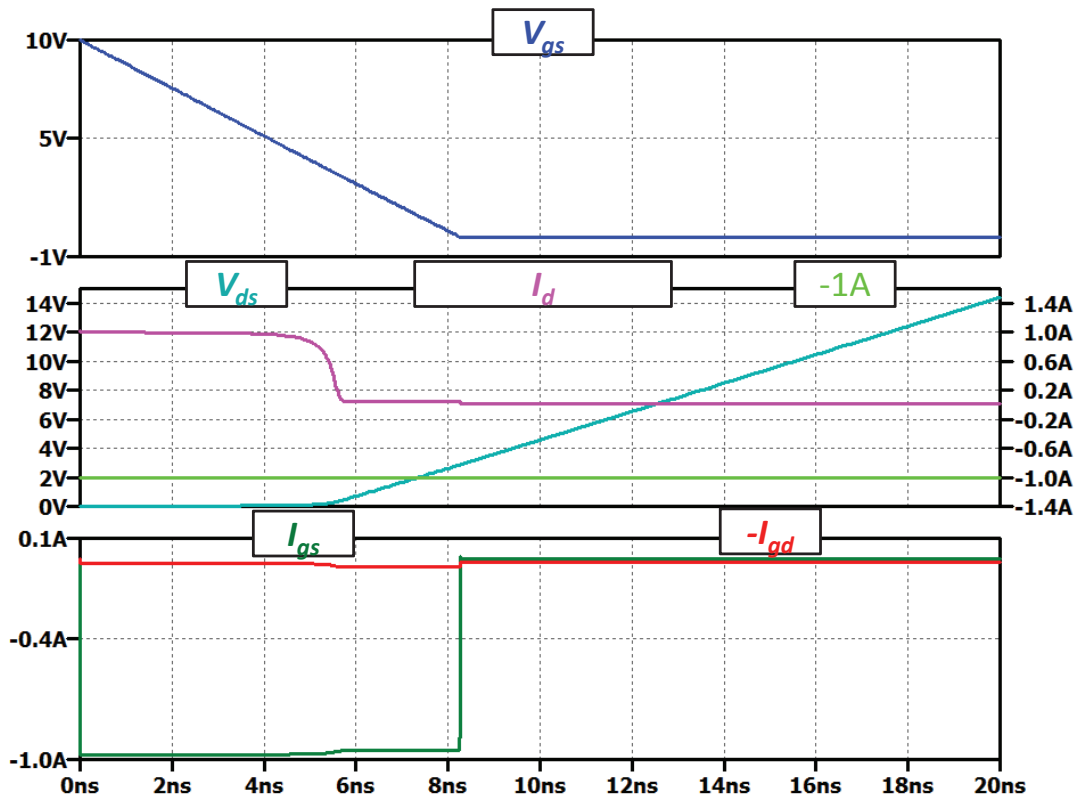
Turn-Off Transition



Turn-off

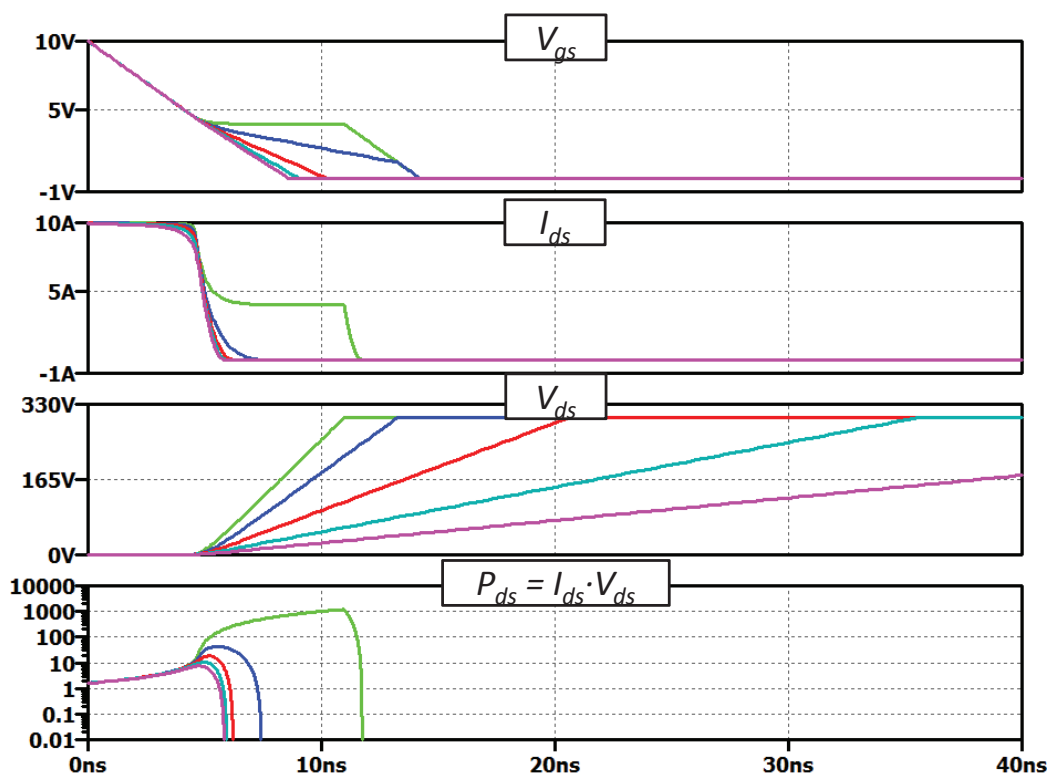


Turn-Off (Drain Dominated)



Gate- vs. Drain-Limited Switching

Simulation Results: Cds Sweep



Limitations on Switching Speed

