Department of Electrical Engineering and Computer Science, The University of Tennessee
ECE551 – System on Chip Design, Fall 2018

This course provides background and hands-on experience with top-down VLSI design flows where custom design techniques are married with HDL synthesis to produce complex digital systems. Topics covered include HDL coding techniques for system-on-chip (SOC) design, standard cell library development and use, synthesis techniques, algorithms for placement and routing, floorplanning, FPGA-based design and prototyping, timing analysis, and power-aware design techniques. Students will gain experience applying top-down VLSI design techniques in the implementation of SOCs, FPGA-based implementations and advanced microprocessors.

Teaching Staff:

Professor: Garrett S. Rose: garose@utk.edu, 865-974-3132, **MK308**

Schedule
Lecture: Monday, Wednesday, Friday 11:15AM – 12:05PM, **MK406**

Office Hours
Professor Rose: Monday and Wednesday 2:00PM – 3:00PM

No Required Textbook
Suggested Texts

1. S. Sutherland, *RTL Modeling with SystemVerilog for Simulation and Synthesis: Using SystemVerilog for ASIC and FPGA Design*, CreateSpace Independent Publishing, 2017. (ISBN: 978-1546776345)
2. C. Spear, *SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*, Springer, 2012. (ISBN: 978-1461407140)
3. D. Thomas, *Logic Design and Verification Using SystemVerilog*, CreateSpace Independent Publishing, 2016. (ISBN: 978-1523364022)

Grading

Homework/Labs:	25%
Quizzes/Participation:	10%
Mid-Term:	15%
Final Project:	35%
Final Exam:	15%

Assignment Policy
Homework assignments are to be completed on your own time – professor will be available to help. Depending on class size and FPGA board availability, lab assignments ***might*** be completed in teams if we must share FPGA boards. All homework and lab assignments are to be handed in at beginning of class on due date unless told otherwise. ***If there is a reasonable excuse, you will get one week after original due date to submit only if you notify the professor at the earliest possible time.*** One week after due date solutions will be posted on Canvas and no excuses will be accepted for late assignments. In *extreme* situations, you may be accommodated by other substitute assignments (alt. homework, extra credit, etc.).

A major component of this course is a group project where you will implement a design of your choice. As part of your learning experience, you will discuss ideas, devise a plan, and divide up the work as a team consisting of 2-3 members. Toward the end of class, project presentations will be delivered by each team. It is recommended that you begin forming teams and considering potential projects soon.

Academic Integrity
All homework to be turned in for credit must be each student's own work. Lab assignments must be the work of only the team members (or individual) responsible. Students can discuss problems and general ideas but any code or other deliverable must be written independently by each student and/or team.

Pop quizzes and in-class activities may be given from time to time during the class lecture period. Some in-class activities may allow for or even require collaboration with other students. Quizzes and in-class activities will be graded as part of "Quizzes/Participation." ***Quizzes and both exams will be closed-notes with no discussion allowed***. Any violations can result in a zero on the given quiz or exam.

Electronic Devices
Laptops, smartphones, tablets and other electronic devices are allowed during lectures in as much as such devices are used with discretion and proper respect is given to the professor and other students. If the use of any electronic device is found to be a distraction then said device must be turned off and put away immediately.

A major component of this course consists of learning to code with VHDL. As such, some in-class activities may benefit from the use of a laptop or tablet. However, in general, no activity will be given which requires the use of such devices.

Project Expectations
A major component of this course is a group project where students will implement a design of their choice. As part of the learning experience, students will discuss ideas, devise a plan, and divide up the work as a team consisting of 2-3 members. Toward the end of class, project presentations will be delivered by each team. It is recommended that students begin forming teams and considering potential projects as soon as possible.

Disability Statement
Any student requiring an accommodation based on the impact of a disability should contact the Office of Disability Services at 865-974-6087 to coordinate reasonable accommodations for documented disabilities.

Some Topics Covered
- Introduction: Bottom-Up versus Top-Down Design Styles
- Top-Down Design Approach with SystemVerilog
- Top-Down Design using Standard Cells
- ASIC/SoC Design Flows and Methodology
- SystemVerilog Design for FPGA Implementations
- FPGA-based Prototyping of ASIC Designs
- On-Chip Interconnect: Buses and Networks-on-Chip
- Integration and Optimization of On-Chip Processor Cores
- Seamless Integration of IP Blocks
- Verification and Testing
- Timing Analysis and Power Analysis
- Optimizing FPGA-based Designs
- Digital Systems in Practical Applications