GARRETT S. ROSE

University of Tennessee, Knoxville
Department of Electrical Engineering & Computer Science
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EDUCATION

Ph.D., Electrical Engineering, August 2006
University of Virginia, Charlottesville, VA
Dissertation: Design Approaches for Nanoscale Circuits and Architectures

M.S., Electrical Engineering, May 2003
University of Virginia, Charlottesville, VA
Thesis: Nanoelectronic Device Modeling for Robust Circuit Design and Analysis

B.S., Computer Engineering, May 2001
Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, VA

EXPERIENCE

University of Tennessee, Knoxville, TN (August 2014 – Present)

Associate Professor, Electrical Engineering and Computer Science, August 2014 – Present

- Research in VLSI circuit design, including nanoelectronic computer architectures, neuromorphic computing and the design of hardware security primitives.
- Teach courses (undergraduate and graduate) in computer engineering and VLSI.

Air Force Research Laboratory, Information Directorate, Rome, NY (July 2011 – July 2014)

Senior Electronics Engineer, Computing & Communications Division, January 2013 – July 2014
Electronics Engineer, Computing & Communications Division, July 2011 – December 2012

- Aid in the design and development of a multi-core processor for Air Force applications.
- Research in areas of nanoscale architectures, neuromorphic hardware and hardware securit

SUNY Institute of Technology (SUNYIT), Marcy, NY (January 2014 – May 2014)

Adjunct Professor (AFRL Affiliated), January 2014 – May 2014

- Develop and teach courses related to nanoelectronic systems.
- Foster collaborations between SUNYIT and AFRL/RI.

Polytechnic Institute of New York University, Brooklyn, NY (August 2006 – May 2011)

Assistant Professor, Electrical and Computer Engineering, August 2006 – May 2011

- Research in VLSI circuit design, including chip multiprocessors and nanoelectronics.
- Taught several courses (undergraduate and graduate), primarily in the area of VLSI circuits.

University of Virginia, Charlottesville, VA (August 2001 – July 2006)

Graduate Teaching & Research Assistant, August 2001 – July 2006

- Lab instructor/grader for Intro. to Electrical Circuit Analysis and Electrical Circuits I.
- Grader and Teaching Assistant for Introduction to VLSI.

The MITRE Corp., McLean, VA (May 2004 – August 2005)

Multidiscipline Systems Engineer, May 2004 – August 2005 (part-time employee)

- Assessed nanoscale memory and computer systems through the use of SPICE simulation.
- Conducted research toward designing and realizing a digital processor on the nanoscale.

CPFilms, Inc., Martinsville, VA (May 2000 – August 2002)

Engineering Summer Internship, May – August 2000, 2001 and 2002

- Programmed a system for controlling an automated crane system used in the warehouse.

DESCRIPTIVE BIOGRAPHY

Garrett S. Rose received the B.S. degree in computer engineering from Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, in 2001 and the M.S. and Ph.D. degrees in electrical engineering from the University of Virginia, Charlottesville, in 2003 and 2006, respectively. His Ph.D. dissertation was on the topic of circuit design methodologies for molecular electronic circuits and computing architectures.

Presently, he is an Associate Professor in the Department of Electrical Engineering and Computer Science at the University of Tennessee, Knoxville where his work is focused on research in the areas of nanoelectronic circuit design, neuromorphic computing and hardware security. Prior to that, from June 2011 to July 2014, he was with the Air Force Research Laboratory, Information Directorate, Rome, NY. From August 2006 to May 2011, he was an Assistant Professor in the Department of Electrical and Computer Engineering at the Polytechnic Institute of New York University, Brooklyn, NY. From May 2004 to August 2005 he was with the MITRE Corporation, McLean, VA, involved in the design and simulation of nanoscale circuits and systems. His research interests include low-power circuits, system-on-chip design, trusted hardware, and developing VLSI design methodologies for novel nanoelectronic technologies.

Dr. Rose is a member of the Association of Computing Machinery, IEEE Circuits and Systems Society and IEEE Computer Society. He serves and has served on Technical Program Committees for several IEEE conferences (including ISCAS, GLSVLSI, NANOARCH) and workshops in the area of VLSI design. In 2010, he was a guest editor for a special issue of the ACM Journal of Emerging Technologies in Computing Systems that presented key papers from the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH'09). Since April 2014 he is an associate editor for IEEE Transactions on Nanotechnology.

SKILLS

- Application of circuit design techniques to novel technologies such as molecular electronics.
- Use of hardware description languages (VHDL & Verilog) for system design and analysis.
- Software development using C/C++, Python, Perl, MATLAB and SKILL.
- Utilization of CAD tools for circuit design and simulation (e.g., Cadence, Synopsys, SPICE, etc.).

HONORS, ACCOMPLISHMENTS & AWARDS

- 2014 AFRL/RI Research and Technology Team Award
- Nominee: 2014 AFRL Early Career Award
- Notable Achievement Award – Invention, U.S. Air Force, for patent application 13/506,856 "Electronic Charge Sharing CMOS-Memristor Neural Circuit," June 2012.
- Best Student Paper Award (with Jeyavijayan Rajendran), 24th International Conference on VLSI Design, Indian Institute of Technology Madras, Chennai, India, 2011
- Best Senior Poster Presentation, 2009 NANO-DDS Conference, Ft. Lauderdale, FL, 2009
- Best Student Paper Award, ACM Great Lakes Symposium on VLSI, Philadelphia, PA, 2006
- Winner of First Phase and 2nd place in Second Phase in SRC SoC Design Challenge 2005-2006, Designed an ultrasound image processor to be fabricated as a system-on-chip in Spring 2006
- Honorable mention in DAC (Design Automation Conference) Student Design Contest, 40th DAC, Anaheim, CA 2003 (for analog turbo decoder design)

- Second Phase participant in SRC SiGe Design Challenge 2002-2003,
  Designed and implemented analog turbo decoder using IBM SiGe process
- Graduate Assistantship, University of Virginia, August 2001-2006
- Passed the Fundamentals of Engineering Exam (EIT), Spring 2001

ACTIVITIES

Funded Research Projects at the University of Tennessee

- Title: "NCS-FO: Biomimetic Membrane Networks as Adaptable Neuromorphic Computation Circuits"
  Sponsor: **NSF**
  PI: Garrett S. Rose
  Co-PI: Charles P. Collier
  Duration: September 2016 – August 2019
  Amount: $669,763
- Title: "MRI: Development of iSNARLD (Instrument for Situational Network Awareness for Real-time and Long-term Data)"
  Sponsor: **NSF**
  PI: Gregory D. Peterson
  Co-PIs: Hairong Qi, Garrett S. Rose, Victor G. Hazelwood
  Duration: September 2016 – August 2019
  Amount: $822,120
- Title: "Foundations of Nanoelectronic Physically Unclonable Computing Systems"
  Sponsor: **AFOSR**
  PI: Garrett S. Rose
  Duration: June 2016 – June 2021
  Amount: $1,512,846
- Title: "Design of a Memristive Dynamic Adaptive Neural Network Array (mrDANNA)"
  Sponsor: **AFRL/RI**
  PI: Garrett S. Rose
  Co-PIs: Mark E. Dean, James Plank
  Duration: December 2015 – December 2018
  Amount: $1,217,929
- Title: "Deep Learning Approach on HPC, Neuromorphic, and Quantum Computing"
  Sponsor: **DOE Office of Science, ASCR**
  PI: Thomas E. Potok (ORNL)
  Collaborators: Robert M. Patton (ORNL), Travis Humble (ORNL), Steven Young (ORNL), Robert F. Lucas (USC-ISI), Federico M. Spedalieri (USC-ISI), Garrett S. Rose
  Duration: November 1, 2015 – October 31, 2018
  UTK Amount: $128,783

Funded Research Projects Prior to Joining the University of Tennessee

- Title: "Methods for Developing Secure Nonlinear Computer Architectures"
  Sponsor: **AFOSR (LRIR/AFRL Intramural)**
  PI: Garrett S. Rose
  Duration: October 2012 – September 2015
  Amount: $908,000

- Title: “Exploiting Nonlinear Evolutionary Logic for Secure Computing”
  Sponsor: **AFOSR/RI (Mini-Grant)**
  PI: Garrett S. Rose
  Duration: May – September 2012
  Amount: $25,000
- Title: “Circuit Level Design for Emerging Memristive Neuromorphic Systems”
  Sponsor: **AFRL (Contract)**
  Contractor: Garrett S. Rose
  Duration: September 3 – December 31, 2010
  Amount: $10,000
- Title: “Hybrid CMOS-Nano-CMOS Architectures and CAD Tools for Nanoelectronic and Bio-Inspired Electronic Applications”
  Sponsor: **NSF (EMT)**
  PI: Garrett S. Rose
  Co-PIs: Ramesh Karri, Wei Wang
  Duration: September 15, 2008 – August 31, 2009
  Amount: $100,000
- Title: “Development and Demonstration of a High Performance Computing System Based on a Modern High Speed Switch Fabric”
  Sponsor: **Department of Defense - Army**
  PI: Garrett S. Rose
  Co-PIs: H. Jonathan Chao, Kang Xi
  Duration: September 15, 2008 – April 30, 2011
  Amount: $1,000,000
- Title: “Scalable Reconfigurable High Performance Computing”
  Sponsor: **Polytechnic University (Angel Fund)**
  PI: H. Jonathan Chao
  Co-PI: Garrett S. Rose
  Duration: July 1, 2007 – June 30, 2008
  Amount: $150,000

Summer Research Activities

- Title: “Design, Modeling and Simulation of Memristor Based Circuits and Systems”
  Sponsor: **AFRL (Visiting Faculty Research Program)**
  PI: Garrett S. Rose
  Duration: June – August 2010
  Status: On-site work at AFRL (Rome, NY), June – August 2010

Professional Affiliations and Societies

- Member of the Institute of Electrical and Electronics Engineers (IEEE).
- Member of the IEEE Computer Society.
- Member of the IEEE Circuits and Systems (CAS) Society.
- Member of the American Society for Engineering Education (ASEE).
- Member of the Association for Computing Machinery (ACM).
- Member of Eta Kappa Nu; Recording Secretary, Virginia Tech, Fall 2000.

Professional Activities

- Associate Editor, IEEE Transactions on Nanotechnology, since 2014
- Track Co-Chair, Emerging and Post-CMOS Technologies Track,
  IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2016
- TPC Member/Reviewer, IEEE HOST Symposium, 2013 – 2016
- TPC Member/Reviewer, Design Automation Conference (DAC), 2014 – 2016
- TPC Member/Reviewer, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2008 – 2016
- TPC Member/Reviewer, IEEE/ACM NANOARCH, 2015 – 2016
- Poster Session Chair, IEEE HOST 2015
- Track Co-Chair, System Design and Security (SDS) Track,
  IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2015
- Publication Co-Chair, IEEE CISDA Conference, 2015
- Session Chair, IEEE MWSCAS, 2015
- TPC Member/Reviewer, IEEE IJCNN, 2013
- Track Co-Chair, Emerging Technologies Track,
  Great Lakes Symposium on VLSI (GLSVLSI), 2012
- Poster Session Chair, IEEE/ACM NANOARCH 2012
- TPC Member/Reviewer, International Conference on Nano-Networks, 2007, 2011
- Session Chair & Poster Session Chair for IEEE ISCAS 2011
- Guest Editor, ACM Journal of Emerging Technology in Computing, 2010,
  Special Issue for NANOARCH 2009
- Session Chair, Design Automation Conference (DAC), 2010
- Special session organizer and co-chair for IEEE ISCAS 2010:
  Memristors and Memristive Systems – From Devices to Applications
- Track Co-Chair, Quantum and Nanoscale Circuits Track,
  European Conference on Circuit Theory and Design, 2009
- Panel Chair, IEEE/ACM NANOARCH, 2009 & 2010
- Session Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009
- TPC Member/Reviewer, Design, Automation and Test in Europe (DATE), 2009
- Publicity Chair, IEEE/ACM NANOARCH, 2007 & 2008
- Session Chair, IEEE/ACM NANOARCH, 2007, 2008 & 2009
- Session Chair, IEEE Conference on Nanotechnology, 2007

Paper Reviewer

- IET Computers and Digital Techniques
- IEEE Transactions on Computer Aided Design (TCAD)
- IEEE Transactions on Circuits and Systems I (TCAS-I)
- IEEE Computer
- IEEE Transactions on Nanotechnology
- IEEE Computer Architecture Letters
- Electronics Letters
- ACM Journal of Emerging Technologies in Computing
- IEEE Transactions on Multi-Scale Computing Systems (TMSCS)

Have also reviewed several papers for VLSI related conferences.

Research Proposal Evaluation & Project Review

- Panel Participation/Evaluator: NSF, Secure & Trustworthy Computing (SaTC), 2015
- Advisory Board Member: DOD/AFOSR MURI Project: Security Theory of Nanoscale Devices, Project at University of Florida, Lead PI: Mark Tehranipoor, 2014-present
- Proposal Review (Non-Panel): DOE Office of Science, 2015
- Proposal Review (Non-Panel): Army Research Office (ARO), 2015
- Panel Participation/Evaluator: DOE Office of Science, ASCR, 2014, 2015

Service to the University (University of Tennessee)

- Serve on Department of EECS Undergraduate Curriculum Committee, 2016-present
- High School Introduction to Engineering Systems for Twelfth Graders (HITES12), Summer 2016 Faculty Mentor, lead 4 students in side-channel analysis mitigation for FPGA-based encryption
- High School Introduction to Engineering Systems for Twelfth Graders (HITES12), Summer 2015 Faculty Mentor, lead 4 students in developing SIMON encryption/decryption engine on FPGA
- Mentored team submission to Embedded Systems Challenge at "Cybersecurity Awareness Week" (CSAW) at NYU – Submitted First Phase design; did not advance to Second Phase, Fall 2014

Service to the University (Polytechnic Institute of NYU)

- 2009-2010 Member of NYU-Abu Dhabi Faculty Search Committee (Computer Engineering)
- Advised a summer CATT undergraduate intern from IIT, Kharagpur, India, Summer 2009
- NYU-Abu Dhabi Affiliated Faculty
- Serve on Computer Engineering Undergraduate Steering Committee
- Program Coordinator and Advisor for Master of Science in Computer Engineering
- Program Coordinator and Advisor for Computer Engineering Graduate Certificate
- Serve on ECE Department Graduate Curriculum and Standards Committee
- 2008-2009 Member of the ECE Faculty Search Committee; search to fill three positions, two in wireless communications and one in computer engineering
- Open House / Lab showcase coordinator, 2007-2008
- 2007-2008 Member of the ECE Faculty Search Committee
- Freshmen Mentor 2007-2008 (10 CompE students mentored)
- Course Director for graduate and undergraduate courses
- Undergraduate recruiting; have met with admitted but still uncommitted students
- Participation in summer YES program in 2007 and 2008; have mentored 5 high school students; one student, Josh Schwartz, 4th place in 2007 Intel International Science & Engineering Fair

COURSES TAUGHT

- ECE 551 (UT): Digital System Design – Spring 2015, Fall 2016
- ECE 599 (UT): Special Topics: Nanoelectronic Systems Design – Summer 2016
- ECE 459/559 (UT): Secure & Trustworthy Computer Hardware Design – Spring 2016
- ECE 351 (UT): Digital Systems Design – Fall 2014, Fall 2015
- ECE 490 (SUNYIT): Introduction to Nanoelectronic Systems – Spring 2014
- EE 3193 (NYU-Poly): Introduction to VLSI Design – Spring 2007 – Spring 2011
- EE 4144 (NYU-Poly): Introduction to Embedded Systems Design – Fall 2010
- EL 9413 (NYU-Poly): Advanced VLSI Design Techniques – Fall 2008, Fall 2010
- EL 6443 (NYU-Poly): VLSI Systems and Architectures – Spring 2007 – Spring 2011
- EL 5473 (NYU-Poly): Introduction to VLSI Circuit Design – Fall 2006 – Fall 2010

ADVISING – Since Joining the University of Tennessee

PhD Students

- **Md Musabbir Adnan**, PhD Student in Computer Engineering, 2016-present
- **Sherif Amer**, PhD Student in Computer Engineerint, 2016-present
- **Sagarvarma Sayyaparaju**, PhD Student in Electrical Engineering, 2016-present
- **Gangotree Chakma**, PhD Student in Electrical Engineering, 2015-present
  Dissertation Research: Memristive Neuromorphic Computing
- **Md Badruddoja Majumder**, PhD Student in Electrical Engineering, 2015-present
  Dissertation Research: Security Techniques for Nanoelectronic Memory and Logic
- **Mesbah Uddin**, PhD Student in Computer Engineering, 2015-present
  Dissertation Research: Nanoelectronic Hardware Security Primitives

MS Students

- **Austin Wyer**, MS Student in Computer Science, 2016-present
- **Ryan Weiss**, MS Student in Electrical Engineering, 2016-present

Undergraduate Student Researchers

- **Michael Wilder**, BS Student in Computer Engineering, Mentored 2016-present
- **Clarence Wong**, BS Student in Electrical Engineering, Mentored 2016-present
- **Elvis Offor,** BS Student in Computer Science, Mentored 2015-present
- **Daniel Caballero**, BS Student in Computer Engineering, Mentored 2015-present
- **Miles N. Gepner**, BS Student in Computer Science, Mentored 2015-present
- **Samuel Brown**, BS Student in Electrical Engineering, Mentored 2015-present
- **Austin Wyer**, BS Student in Computer Science; Mentored 2015-2016
- **Harry N. Hughes**, BS Student in Computer Engineering, Mentored 2015-2016
- **Caleb Williamson**, BS Student in Computer Engineering, Mentored Summer 2015
- **Chauncey Meade**, BS Student in Computer Engineering; Mentored 2014-2015

ADVISING – Prior to Joining the University of Tennessee

Post-Doctoral Research Assistant (Polytechnic Institute of NYU)

- **Aamir Zia**, Research: 3D Networks-on-Chip for Chip Multiprocessors
  November 2009 – June 2010; PhD from Rensellar Polytechnic Institute, 2009
  Now with Intel, Hillsboro, OR

PhD Students (Polytechnic Institute of NYU)

- **Harika Manem**, PhD in Electrical Engineering received December 2011
  Dissertation: "Design Approaches for Nanoscale Logic and Memory Architectures"
  Now a Research Scientist at College of Nanoscale Science and Engineering, Albany, NY
- **Sachhidh Kannan,** Dissertation Research: 2D and 3D NoC for Chip Multiprocessors
  PhD Advisor September 2009 – May 2011.
  Now a Security Researcher at Intel Corporation, Hillsboro, Oregon.
- **Jeyavijayan Rajendran**, Dissertation Research: Nanoscale Circuits and Hardware Security
  Co-Advised with Ramesh Karri, Spring 2011.
  Now an Assistant Professor in Electrical Engineering at the University of Texas at Dallas.

MS Students (Polytechnic Institute of NYU)

- **Yang Yang**, MS Student in Electrical Engineering; Advised 2009-2010
- **Nischay Tata**, MS Student in Electrical Engineering; Advised 2009-2010

- **Dan Wang**, Masters in Electrical Engineering received December 2010
- **Shaojun Ma**, Masters in Computer Engineering received May 2010
  Thesis: "An Energy-Efficient Network-on-Chip"
- **Xiaohua Xu**, Masters in Computer Engineering received May 2010
- **Ramya Geetha Yellamsetty**, Masters in Electrical Engineering received December 2009
  Thesis: "Floorplan Based Path Length Optimization for Clos Network on Chip"
- **Sachhidh Kannan**, Masters in Electrical Engineering received December 2008
  Thesis: "Design of a Run-Time Reconfigurable Random Access FPGA"
- **Wael Refai**, Masters in Electrical Engineering received December 2008
  Received PhD from Virginia Tech, 2015.
  Now an Assistant Professor in Engineering and Technology at Western Carolina University.
- **Shunting Lin**, Masters in Electrical Engineering received December 2008
- **Yongji (Mario) Jiang**, Masters in Electrical Engineering received August 2008
  Thesis: "Dynamic On-Chip Temperature Management Based on Dual-MOSFET Equivalent Resistor Thermal Sensor"
- **Harika Manem**, Masters in Electrical Engineering received May 2008
  Thesis: "A Hybrid CMOS-Nano FPGA Architecture Built from Programmable Logic Arrays"
- **Harish Chandra**, Masters in Electrical Engineering received December 2007

Summer Intern Mentoring at AFRL

- **Saxxon Gonzalez**, BS Student from SUNYIT; Mentored 2014
- **Cory E. Merkel**, PhD Student from Rochestor Institute of Technology; Mentored 2013
- **Jillian M. Hallak**, MS Student from University of Rochester; Mentored 2013 & 2014
- **James W. Bohl**, MS Student from Rennselaer Polytechnic Institute; Mentored 2013
- **Jun Jie Huang**, BS/MS Student from Rochestor Institute of Technology; Mentored 2013
- **Huan Zhang**, MS Student from Polytechnic Institute of NYU; Mentored 2012

PUBLICATIONS

Patents

4. Q. Wu, R. Linderman, **G. Rose**, H. Li, Y. Chen, and M. Hu, "Method and Apparatus for Performing Close-Loop Programming of Resistive Memory Devices in Crossbar Array based Hardware Circuits and Systems," U.S. Patent Application Number 14/328,043, filed July 10, 2014.

3. **G. Rose**, N. McDonald, L.-K. Yan, and B. Wysocki, "Write-Time Based Memristive Physical Unclonable Function," U.S. Patent Application Number 13/868,529, filed April 23, 2013.

2. R. Linderman, Q. Wu, **G. Rose**, H. Li, Y. Chen, and M. Hu, "Apparatus for Performing Matrix-Vector Multiplication Approximation Using Crossbar Arrays of Resistive Memory Devices," U.S. Patent Application Number 13/965,495, filed August 13, 2013. Patent granted October 6, 2015, U.S. Patent Number US 9152827 B2.

1. **G.S. Rose**, R. Pino, and Q. Wu, "Electronic Charge Sharing CMOS-Memristor Neural Circuit," U.S. Patent Application Number 13/506,856, filed May 15, 2012. Patent granted September 9, 2014, U.S. Patent Number US 8832009 B2.

Book Chapters

7. B. Wysocki, N. McDonald, C. Thiem, and **G.S. Rose**, "Hardware-Based Computational Intelligence for Size, Weight, and Power Constrained Environments," in *Network Science and Cybersecurity*, R. Pino, Ed., Springer, 2013.

6. **G.S. Rose**, D. Kudithipudi, G. Khedkar, N. McDonald, B. Wysocki, and L.-K. Yan, "Nanoelectronics and Hardware Security," in *Network Science and Cybersecurity*, R. Pino, Ed., Springer, 2013.
5. D. Kudithipudi, C. Merkel, M. Soltiz, **G.S. Rose**, and R.E. Pino, "Design of Neuromorphic Architectures with Memristors," in *Network Science and Cybersecurity*, R. Pino, Ed., Springer, 2013.
4. **G.S. Rose** and H. Manem, "A Hybrid CMOS-Nano FPGA Based on Majority Logic: From Devices to Architectures," in *CMOS Processors and Memories, Springer Series: Analog Circuits and Signal Processing*, K. Iniewski, Ed., Springer, 2010.
3. M.R. Stan, **G.S. Rose**, and M.M. Ziegler, "Hybrid CMOS/Molecular Integrated Circuits," in *Moore's Law: Beyond Planar Silicon CMOS and into the Nano Era, Springer Series in Material Science*, vol. 106, H. Huff, Ed., Springer, 2009.
2. S. Das, C.A. Picconatto, **G.S. Rose**, M.M. Ziegler, and J.C. Ellenbogen, "System-Level Design and Simulation of Nanomemories and Nanoprocessors," in *Nano and Molecular Electronics Handbook*, S. Lyshevski, Ed., CRC, May 2007.
1. S. Das, **G.S. Rose**, M.M. Ziegler, C.A. Picconatto, and J.C. Ellenbogen, "Architectures and Simulations for Nanoprocessor Systems Integrated on the Molecular Scale," in *Introducing Molecular Electronics*, G. Cuniberti, G. Fagas, and K. Richter, Eds. Berlin: Springer, 2005.

Journal Papers

16. J. Rajendran, R. Karri, J.B. Wendt, M. Potkonjak, N. McDonald, **G.S. Rose**, and B. Wysocki, "Nano Meets Security: Exploring Nanoelectronic Devices for Security Applications," *Proceedings of the IEEE*, vol. 103, no. 5, pp. 829—849, May 2015.
15. J. Rajendran, R. Karri, and **G.S. Rose**, "Improving Tolerance to Variations in Memristor-based Applications Using Parallel Memristors," *IEEE Transactions on Computers*, vol. 64, no. 3, pp. 733—746, March 2015.
14. J. Rajendran, H. Zhang, C. Zhang, **G.S. Rose**, Y. Pino, O. Sinanoglu, and R. Karri, "Fault Analysis-Based Logic Encryption," *IEEE Transactions on Computers*, vol. 64, no. 2, pp. 410—424, February 2015.
13. G. Khedkar, D. Kudithipudi, and **G.S. Rose**, "Power Profile Obfuscation using Nanoscale Memristive Devices to Counter DPA Attacks," *IEEE Transactions on Nanotechnology*, vol. 14, no. 1, pp. 26 – 35, January 2015.
12. M. Hu, H. Li, Y. Chen, Q. Wu, **G.S. Rose**, and R. Linderman, "Memristor Crossbar-Based Neuromorphic Computing System: A Case Study," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 25, no. 10, pp. 1864—1878, October 2014.
11. M. Soltiz, D. Kudithipudi, C. Merkel, **G.S. Rose**, and R. E. Pino, "Memristor-Based Neural Logic Blocks for Nonlinearly Separable Functions," *IEEE Transactions on Computers*, vol. 62, no. 8, pp. 1597—1606, August 2013.
10. **G.S. Rose**, J. Rajendran, H. Manem, R. Karri, and R. Pino, "Leveraging Memristive Systems in the Construction of Digital Logic Circuits," *Proceedings of the IEEE*, vol. 100, no. 6, June 2012.
9. H. Manem, J. Rajendran, and **G.S. Rose**, "Stochastic Gradient Descent Inspired Training Technique for a CMOS/Nano Memristive Trainable Threshold Gate Array," *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 5, pp. 1051—1060, May 2012.
8. J. Rajendran, H. Manem, R. Karri, and **G.S. Rose**, "An Energy-Efficient Memristive Threshold Logic Circuit," *IEEE Transactions on Computers*, vol. 61, no. 4, pp. 474—487, April 2012.

7. H. Manem, J. Rajendran, and **G.S. Rose**, "Design Considerations for Multi-Level CMOS/Nano Memristive Memory," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 8, no. 1, Feb. 2012.
6. A. Zia, S. Kannan, H.J. Chao, and **G.S. Rose**, "3D NOC for Many-Core Processors," *Microelectronics Journal*, vol. 42, no. 12, pp. 1380—1390, Dec. 2011.
5. B. Gojman, H. Manem, **G.S. Rose**, and A. DeHon, "Inversion Schemes for Sublithographic Programmable Logic Arrays," *IET Computers & Digital Techniques*, vol. 3, no. 6, pp. 625—642, Nov. 2009.
4. **G.S. Rose** and M.R. Stan, "A Programmable Majority Logic Array using Molecular Scale Electronics," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 11, pp. 2380–2390, Nov. 2007.
3. S. Das, A.J. Gates, H.A. Abdu, **G.S. Rose**, C.A. Picconatto and J.C. Ellenbogen, "Designs for Ultra-Tiny, Special-Purpose Nanoelectronic Circuits," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 11, pp. 2528–2540, Nov. 2007.
2. **G.S. Rose**, Y. Yao, J.M. Tour, A.C. Cabe, N. Gergel-Hackett, N. Majumdar, J.C. Bean, L.R. Harriott, and M.R. Stan, "Designing CMOS/Molecular Memories while Considering Device Parameter Variations," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 3, no. 1, April 2007.
1. **G.S. Rose**, M.M. Ziegler, and M.R. Stan, "A Large-Signal Universal Device Model for Nanoelectronic Circuit Simulation," *IEEE Transactions on Very Large Scale Integration*, vol. 12, no. 11, pp. 1201—1208, Nov. 2004.

Conference Papers

47. C. Schuman, J.D. Birdwell, M. Dean, J. Plank, and **G. Rose**, "Neuromorphic Computing: A Post-Moore's Law Complementary Architecture," to appear in *International Workshop on Post-Moore's Era Supercomputing (PMES)*, Salt Lake City, UT, November 2016.
46. G. Chakma, M.E. Dean, **G.S. Rose**, K. Beckman, H. Manem, and N. Cady, "A Hafnium-Oxide Memristive Dynamic Adaptive Neural Network Array," to appear in *International Workshop on Post-Moore's Era Supercomputing (PMES)*, Salt Lake City, UT, November 2016.
45. M. Uddin, M.B. Majumder, **G.S. Rose**, H. Manem, K. Beckmann, Z. Alamgir, and N. Cady, "Techniques for Improved Reliability in Memristive Crossbar PUF Circuits," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pittsburgh, PA, July 2016.
44. **G.S. Rose**, M. Uddin, and M.B. Majumder, "A Designer's Rationale for Nanoelectronic Hardware Security Primitives," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pittsburgh, PA, July 2016. (special session)
43. M.E. Dean, J. Chan, C. Daffron, A. Disney, J Reynolds, J.S. Plank, **G.S. Rose**, J.D. Birdwell, and C.D. Schuman, "An Application Development Platform for Neuromorphic Computing," in *Proceedings of IEEE International Joint Conference on Neural Networks (IJCNN)*, Vancouver, Canada, July 2016.
42. **G.S. Rose**, "Security Meets Nanoelectronics for Internet of Things Applications," in *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Boston, MA, May 2016. (special session)
41. C. Daffron, J. Chan, A. Disney, L. Bechtel, R. Wagner, M.E. Dean, **G.S. Rose**, J.S. Plank, J.D. Birdwell, and C.D. Schuman, "Extensions and Enhancements for the DANNA Neuromorphic Architecture," in *Proceedings of IEEE SoutheastCon*, Norfolk, Virginia, March 2016.
40. N. Cady, K. Beckmann, H. Manem, M.E. Dean, **G.S. Rose**, and J. Van Nostrand, "Towards Memristive Dynamic Adaptive Neural Network Arrays," in *Proceedings of the Government*

Microcircuit Applications and Critical Technology Conference (GOMACTech), Orlando, FL, March 2016.

39. J. Bohl, L.-K. Yan, and **G.S. Rose**, "A Two-Dimensional Chaotic Logic Gate for Improved Computer Security," in *Proceedings of Midwest Symposium on Circuits and Systems* (*MWSCAS*), Fort Collins, CO, August 2015.

38. **G.S. Rose** and C.A. Meade, "Performance Analysis of a Memristive Crossbar PUF Design," in *Proceedings of Design Automation Conference* (*DAC*), San Francisco, CA, June 2015.

37. D. Kudithipudi, C. Merkel, Y.K. Ooi, and **G.S. Rose**, "On Designing Primitives for Cortical Processors with Memristive Hardware," in *Proceedings of the International IEEE System-on-Chip Conference* (*SOCC*), Las Vegas, NV, September 2014.

36. **G.S. Rose**, "A Chaos-based Arithmetic Logic Unit and Implications for Obfuscation," in *Proceedings of the IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI*), Tampa, FL, July 2014.

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33. M. Hu, H. Li, Q. Wu, **G.S. Rose**, and Y. Chen, "BSB Training Scheme Implementation on Memristor-Based Circuit," in *Proceedings of the IEEE Symposium on Computational Intelligence for Security and Defence Applications (CISDA)*, Singapore, April 2013.

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29. M. Soltiz, C. Merkel, D. Kudithipudi, and **G.S. Rose**, "RRAM-Based Adaptive Neural Logic Block for Implementing Non-Linearly Separable Functions," in *Proceedings of IEEE/ACM International Symposium on Nanoscale Architectures* (*NANOARCH*), Amsterdam, Netherlands, July 2012.

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25. **G.S. Rose**, R. Pino, and Q. Wu, "Exploiting Memristance for Low-Energy Neuromorphic Computing Hardware," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, May 2011.
24. J. Rajendran, R. Karri, and **G.S. Rose**, "Parallel Memristors Improve Variation Tolerance in Memristive Digital Circuits," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, May 2011.
23. H. Manem and **G.S. Rose**, "A Read-Monitored Write Circuit for 1T1M Memristor Memories," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, May 2011.
22. S. Kannan and **G.S. Rose**, "A Hierarchical 3-D Floorplanning Algorithm for Many-core CMPs," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, May 2011.
21. J. Rajendran, H. Manem, R. Karri, and **G.S. Rose**, "An Approach to Tolerate Variations for Memristor Based Applications," in *Proceedings of International Conference on VLSI Design*, Chennai, India, January 2011. (**Best Paper Award**)
20. A. Zia, S. Kannan, H.J. Chao, and **G.S. Rose**, "Highly-Scalable 3D Clos NOC for Many-Core CMPs," in *Proceedings of IEEE International NEWCAS Conference*, Montreal, Canada, June 2010.
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18. H. Manem, **G.S. Rose**, X. He, and W. Wang, "Design Considerations for Variation Tolerant Multilevel CMOS/Nano Memristor Memory," in *Proceedings of the ACM Great Lakes Symposium on VLSI*, Providence, Rhode Island, May 2010.
17. **G.S. Rose**, "Overview: Memristive Devices, Circuits and Systems," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, Paris, France, June 2010. (special session)
16. X. Guo, S. Lin, W. Refai, and **G.S. Rose**, "Non-Overlapping Transition Encoding for Global On-Chip Interconnect," in *Proceedings of the 2009 IEEE International SOC Conference*, Belfast, Northern Ireland, United Kingdom, September 2009.
15. J. Rajendran, H. Manem, and **G.S. Rose**, "NDR Based Threshold Logic with Memristive Synapses," in *Proceedings of the IEEE Conference on Nanotechnology*, Genoa, Italy, July 2009.
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13. Y. Jiang and **G.S. Rose**, "A Dual-MOSFET Equivalent Resistor Thermal Sensor," in *Proceedings of the ACM Great Lakes Symposium on VLSI*, Boston, Massachusetts, May 2009.
12. H. Manem and **G.S. Rose**, "The Effects of Logic Partitioning in a Majority Logic Based CMOS-Nano FPGA," in *Proceedings of the ACM Great Lakes Symposium on VLSI*, Boston, Massachusetts, May 2009.
11. H. Manem and **G.S. Rose**, "The Effect of Device Parameter Variation on Programmable Majority Logic Arrays," in *Proceedings of the IEEE Conference on Nanotechnology*, Arlington, Texas, August 2008.
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8. A.C. Cabe, **G.S. Rose**, and M.R. Stan "Data Encoding Eliminates Parasitic Current Paths in Molecular Memory," in *Proceedings of the IEEE Conference on Nanotechnology*, Hong Kong, China, August 2007, pp. 70-75.
7. N. Gergel-Hackett, **G.S. Rose**, P. Paliwoda, C.A. Hacker, and C.A. Richter, "On-Chip Characterization of Molecular Electronic Devices: The Design and Simulation of a Hybrid Circuit Based on Experimental Molecular Electronic Device Results," in *Proceedings of the ACM Great Lakes Symposium on VLSI*, Stresa, Italy, March 2007.
6. Z. Qi, W. Huang, A. Cabe, W. Wu, Y. Zhang, **G. Rose**, and M.R. Stan, "A Design Methodology for a Low-Power, Temperature-Aware SoC Developed for Medical Image Processors," in *Proceedings of the 2006 IEEE International SOC Conference*, Austin, TX, September 2006.
5. A.C. Cabe, Z. Qi, W. Huang, Y. Zhang, M.R. Stan, and **G.S. Rose**, "A Flexible, Technology Adaptive Memory Generation Tool," in *CDNLive! Silicon Valley 2006 Conference Proceedings*, San Jose, CA, September 2006.
4. **G.S. Rose**, A.C. Cabe, N. Gergel-Hackett, N. Majumdar, M.R. Stan, J.C. Bean, L.R. Harriott, Y. Yao, and J.M. Tour, "Design Approaches for Hybrid CMOS/Molecular Memory Based on Experimental Device Data," in *Proceedings of the ACM Great Lakes Symposium on VLSI*, Philadelphia, PA, May 2006, pp. 2-7. (**Best Paper Award**)
3. M.R. Stan, **G.S. Rose**, and M.M. Ziegler, "Hybrid CMOS/molecular Electronic Circuits," in *Proceedings of the International Conference on VLSI Design*, Hyderabad, India, Jan. 2006.
2. **G.S. Rose** and M.R. Stan, "Memory Arrays Based on Molecular RTD Devices," in *Proceedings of the 3rd IEEE Conference on Nanotechnology*, San Francisco, CA, August 2003.
1. M.M. Ziegler, **G.S. Rose**, and M.R. Stan, "A Universal Device Model for Nanoelectronic Circuit Simulation," in *Proceedings of the 2nd IEEE Conference on Nanotechnology*, Washington, D.C., August 2002, pp. 83–88.

Technical Reports and Preprint Papers

2. J. Rajendran, R. Karri, J. B. Wendt, M. Potkonjak, N. McDonald, **G.S. Rose**, and B. Wysocki, "Nanoelectronic Solutions for Hardware Security," *Cryptology ePrint Archive*, Report 2012/575.
1. Y. Pino and **G. S. Rose**, "Secure Hardware Design for Trust – Interim Report."

Refereed or Invited Abstracts & Presentations

22. G. Chakma, E. Offor, M. Dean, and **G. Rose**, "A Reconfigurable Memristive DANNA Circuit with Implementations in Pattern Recognition," at *Neuromorphic Computing Workshop: Architectures, Models, and Applications (NCAMA)*, Oak Ridge, TN, June 2016.
21. **G. Rose** et al. (Panelists), Panel Session: "IOT Security: Issues, Innovations, and Interplays," at *ACM Great Lakes Symposium on VLSI*, Session Chair: S. Bhunia, Boston, MA, May 2016. (invited)
20. **G.S. Rose**, "Memristive Dynamic Adaptive Neural Network Arrays," *Neuro-Inspired Computational Elements (NICE) Workshop*, Berkeley, California, March 2016.
19. C. Hurst, M. Tehranipoor, L. Yan, **G. Rose** (Panelists), Panel Session: "Security and Privacy," at *Florida International University Workshop on Trends in Cybersecurity: Security of Smart Things*, Session Chair: S. S. Iyengar, Miami, Florida, October 2015.
18. **G.S. Rose**, "Assessing the Security Strengths and Vulnerabilities of Emerging Nanoelectronic Computing Systems," *CMOS Emerging Technologies Research*, Vancouver, British Columbia, Canada, May 2015. (invited)

17. **G.S. Rose**, "Construction Considerations for Memristive Physical Unclonable Functions," *ARO Workshop on Trustworthy Hardware*, New York, NY, November 2014. (invited)
16. **G.S. Rose**, "Nanoelectronics and Hardware Security," *ARO Workshop on Trustworthy Hardware*, New York, NY, November 2013. (invited)
15. R. Howe, H. Hunter, P. Kim, J.-O. Klein, and **G. Rose (**Panelists), Panel Session: "What Lies in Our (Nanoelectronic) Future?," at *IEEE/ACM International Symposium on Nanoscale Architectures* (*NANOARCH*), Session Chair: A. Raychowdhury, New York, NY, July 2013. (invited)
14. **G.S. Rose**, "Exploiting Memristive Device Behavior for Emerging Digital Logic and Memory Applications," tutorial, *IEEE SOC Conference*, Niagara Falls, NY, September 2012.
13. **G.S. Rose**, "Nanoelectronics and Hardware Security," *Network Science and Reconfigurable Systems for Cybersecurity Conference*, Beltsville, MD, August 2012.
12. **G.S. Rose**, "Exploration of CMOS-Memristive Neuromorphic Circuits," to appear at *AIAA Infotech@Aerospace*, St. Louis, Missouri, March 2011. (invited)
11. **G.S. Rose**, H. Manem, and J. Rajendran, "Memristor Based Nanoelectronic Architectures for Emerging Sensor Applications," *Nanoelectronic Devices for Defense and Security Conference*, Ft. Lauderdale, FL, September 2009. (**Best Senior Poster Award**)
10. **G.S. Rose**, "Hybrid CMOS-Nano Architectures: A Circuits Perspective," *CMOS Emerging Technologies*, Banff, Alberta, Canada, February 2009. (invited)
9. **G. Rose**, V. Gorelik, S.-C. Liu, and M. Hynd **(**Panelists), Panel Session: "Using Advanced Micro/Nano-electronic Technology to Establish Neuromorphic Systems," at *International Conference on Nano-Networks* (*Nano-Net*), Session Chair: W. Wang, Boston, MA, September 2008. (invited)
8. H. Manem and **G.S. Rose**, "The Effects of Logic Partitioning in a Majority Logic Based CMOS-Nano FPGA," poster, *IEEE/ACM International Symposium on Nanoscale Architectures* (*NANOARCH*), Anaheim, CA, June 2008.
7. **G.S. Rose**, "Hybrid CMOS-nano Architectures from a Circuits Perspective," tutorial, *International Symposium on Circuits and Systems*, Seattle, WA, May 2008.
6. N. Gergel-Hackett, A.A. Hill, C.A. Hacker, C.A. Richter, P. Paliwoda, and **G.S. Rose**, "The Design, Simulation, and Fabrication of a Hybrid Molecular Electronic Device/CMOS Circuit," *Materials Research Society Spring Meeting*, San Francisco, CA, March, 2008.
5. **G.S. Rose**, "Versatile Multiprocessing: HPC Systems & Chip Multiprocessors," *2007 Chinese Institute of Engineers Annual Convention*, Newark, NJ, November 2007. (invited)
4. **G.S. Rose** and P.C. Paliwoda, "Modeling and Design Approaches of Emerging Nanoelectronic Circuits and Systems," *Molecular Cond. Workshop*, West Lafayette, IN, July 2007. (invited)
3. **G.S. Rose**, "Digital Memory and Logic from Hybrid CMOS/Molecular Electronics," *Virginia Nanotech 2006*, Newport News, VA, June 2006.
2. **G.S. Rose** and M.R. Stan, "A Programmable Majority Logic Array using Molecular Scale Electronics," poster, *Fourteenth ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 2006.
1. **G.S. Rose** and M.R. Stan, "Programmable Logic Using Molecular Devices in a Three Dimensional Architecture," *Molecular-Scale Electronics VII*, San Diego, CA, January 2005.

Other Presentations

9. **G.S. Rose**, "mrDANNA: Memristive Dynamic Adaptive Neural Network Array," UTK EECS Industrial Advisory Board (IAB) Dinner, University of Tennessee, Knoxville, TN, April 2016.

8. **G.S. Rose**, "Memristive Neuromorphic Computer Architectures," SUNY Polytechnic Institute – Colleges of Nanoscale Science and Engineering, Albany, NY, March 2016.
7. **G.S. Rose**, "Exploiting Memristive Device Behavior for Emerging Digital Logic and Memory Applications," Rochester Institute of Technology, Rochester, NY, September 2011.
6. **G.S. Rose**, "Communication Solutions for Emerging Chip Multiprocessor Architectures," National Tsing-Hua Univerisity, Hsinchu, Taiwan, June 2009.
5. **G.S. Rose**, "The Professional Engineer in the 21st Century," *IEEE Spectrum Tech Insider: Navigating your Career in Science and Technology*, Webinar, June 2007.
4. P.C. Paliwoda, H. Chandra, K. Dadhirao, and **G.S. Rose**, "CMOS/Nano Integrated Circuit Design," *From the Lab to the Marketplace: Nanotechnology Symposium*, Brooklyn, NY, April 2007. (poster)
3. **G.S. Rose**, M.R. Stan, W. Huang, Y. Zhang, W. Wu, A.C. Cabe, and Z. Qi, "An SRAD Image Processor as a Reconfigurable, Temperature-Aware SoC Designed for Low-Power Operation," *TECHCON*, Portland, OR, October 2005.
2. J.C. Ellenbogen, C.A. Picconatto, **G.S. Rose**, S. Das, and M.M. Ziegler, "System Simulations and Analyses for MoleApps Nanoprocessors and Nanosensor Systems," *DARPA Moletronics PI Meeting*, Fair Lakes, VA, June 2004.
1. W. Huang, V. Igure, **G. Rose**, Y. Zhang, and M. Stan, "Analog Turbo Decoder Implemented in SiGe BiCMOS Technology," University Booth Poster, *Design Automation Conference (DAC)*, Anaheim, CA, June 2003.