Design Techniques for in-Field Memristor Forming Circuits

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Design Techniques for In-Field Memristor Forming Circuits

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***Abstract*—This work presents circuit design techniques for in-field forming of metal-oxide memristor-based systems. While several works have addressed forming from a device characterization stand point, to the best of the authors' knowledge, the integration of a forming circuit in a memristor-based application hasn't been thoroughly studied. Two challenges exist for in-field forming which are the high forming voltages required and SPICE level modeling of the forming process. Both challenges are addressed in this work and circuit level solutions are provided. A method for incorporating forming in memristor models is proposed via increasing the high resistance state (HRS) value to mimic the pre-forming resistance of the device and simulating the design for a wide range of pre-forming resistances. Also, a circuit design is presented for proper isolation of peripheral circuitry during forming to avoid any malfunction. It is shown that forming is executed successfully without disrupting the CMOS peripheral circuitry. It is important to highlight the need for developing a concise physical model for forming in SPICE environment. Also, device designers should work on lowering the forming voltage in order to ease the integration of forming circuits in memristor based applications.**

I. Introduction

The peculiar characteristics of the memristor [1] device are thought to be immensely promising in applications such as nonvolatile memories and neuromorphic circuits. While several materials can exhibit memristive properties, metal-Oxide based memristors (i.e. RRAM) are predominantly used in most applications in which the conductivity of the device is modulated based on oxygen vacancy creation/annihilation mechanism [2]. Fresh Metal Oxide memristor samples cannot exhibit resistive switching before a forming (i.e. electroforming) process which is interpreted as a Time Dependent Dielectric Breakdown (TDDB) [3]. While it is an indispensable step that needs to be performed irrespective of the application, to the best of the authors knowledge, in-field electroforming has been widely overlooked in the literature. While electroforming has been extensively studied from the stand point of device characterization via the 1T1R structure [4], memristor-based applications don't account for the forming step which requires dedicated circuitry different from the 1T1R stucture since forming is executed in-field (i.e. the memristor device will be surrounded by other CMOS circuitry)

To this end, this work presents the design of an in-field forming circuit integrated within a general neuromorphic architecture. The memristive device employed in this work is based on HfO_2 process manufactured in-house by SUNY Polytechnic Institute [4]. However, the proposed design can be readily extended to any memristor application or material. First, we provide a circuit oriented approach to model electroforming in a SPICE environment highlighting the main attributes governing it. Then, the proposed forming circuit is presented and design decisions are investigated. Section II describes the 1T1R structure used for device characterization and the model used in this work. Section III analyzes electrforming and describes the proposed circuit. Conclusions and future prospects are presented in section IV.

II. Background

A. Memristor Model

The memristor model used in this work is an empirical model [5] experimentally fitted to the HfO_2 manufactured at SUNY Polytechnic Institute integrated with the IBM 65nm 10LPe process. Equations (1) and (2) describe the model:

$$\frac{dM}{dt} = \begin{cases} -C_{LRS}(\frac{V(t)-V_{tp}}{V_{tp}})^{P_{LRS}} f_{LRS}(M(t)), & V(t) > V_{tp} \\ C_{HRS}(\frac{V(t)-V_{tn}}{V_{tn}})^{P_{HRS}} f_{HRS}(M(t)), & V(t) < V_{tn} \\ 0, & \text{otherwise,} \end{cases} \tag{1}$$

where C is a fitting coefficient, V_{tp} and V_{tn} are the positive and negative thresholds, respectively, and P_{HRS} and P_{LRS} are control parameters that govern the nonlinearity of the model. Functions f_{HRS} and f_{LRS} capture the resistance saturation (commonly referred to as window functions). Equation (2) presents the window function:

$$f(M(t)) = \begin{cases} \frac{1}{1+e^{\frac{M(t)-\theta_{HRS}HRS}{\beta_{HRS}\Delta r}}}, V(t) < V_{tn} \\ \frac{1}{1+e^{\frac{\theta_{LRS}LRS-M(t)}{\beta_{LRS}\Delta r}}}, V(t) > V_{tp} \end{cases} \tag{2}$$

where β and θ are fitting parameters. The advantage of this model over the other models in the literature is that it can be easily fitted to experimental data and is based on measurable parameters. Fig 1 depicts the I-V sweeps for both simulation and experimental data.

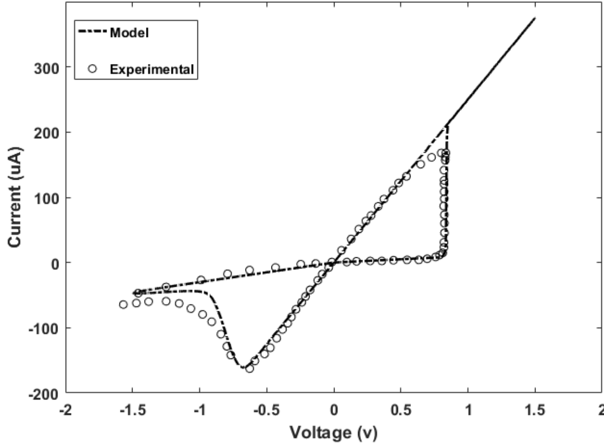

Fig. 1: I-V plots of the proposed model against experimental data.

B. 1T1R structure used for characterizing the forming process

The conventional 1T1R structure used in RRAM characterization is depicted in Fig 2. VF is swept and the quiescent current is monitored until a sudden increase in the current is observed indicating that a forming event has occurred. Once forming is initiated, the resistance of the memristor switches to LRS which, depending on the forming conditions and material stack, might gravitate to a very low value. This results in a relatively high quiescent current, which needs to be controlled by a current compliance in order to avoid any damage to the surrounding circuitry. The current compliance mechanism is implemented via the series transistor biased in pinch off saturation by means of VG.

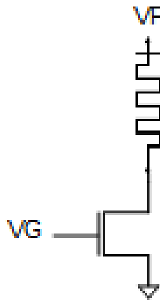

Fig. 2: 1T1R structure.

III. Proposed Design

A. Electroforming Modeling

From a circuit's designer perspective, three quantities need to be modeled during electroforming, namely: device resistance in its pristine state (oxide resistance prior to forming), the current compliance and VF for they directly impact the design of the forming circuit.

Fresh metal oxide memristor samples typically have no oxygen vacancies present in the oxide (except very few due to deficiencies in the material). As VF is ramped up, the induced stress on device results in a dielectric break down in which some of the Oxygen atoms are knocked out of their original locations leaving behind Oxygen vacancies that constitute a conductive path (also known as conductive filament) for the electrons. The state with maximum oxygen vacancies corresponds to the least resistance state: LRS. When a voltage of opposite polarity is applied across the device, some vacancies are recovered (annihilated), but not all of them, which results in the high resistance state: HRS. Because not all vacancies are recovered, HRS is typically less than the resistance of the fresh sample prior to forming [2]. In order to model the pre-forming resistance in the memrsitor Verilog-A model used in this work, HRS was increased above the typical HRS and the circuit was simulated with a wide range of pre-forming resistance values.

Once forming is initiated, the device switches to LRS. Since, LRS is the least resistance state, it governs the maximum current that flows through the memristor. Thus, the current compliance should be set at a specific level such that the memristor forms properly (i.e. avoid huge cycle-to-cycle variation or complete failure of the device). This information is often provided by the device manufacturer.

VF is ideally the voltage across the memristor device at which forming occurs. However, due to necessity of the current compliance mechanism, VF is typically, the voltage across the series combination of the memristor and the series FET device. Hence, during in-field forming, the circuit should realize the 1T1R structure in order to ensure applying the same conditions during characterization .

B. The proposed in-field forming circuit

The 1T1R structure used during characterization of the HfO_2 yielded VF=$2.3V$ and a stress duration of $5ms$ (the time required to effect forming while $2.3V$ is applied).

A high forming voltage that exceeds 2.3V in this work presents a major design challenge for CMOS integration [6]. Peripheral circuitry typically operate at voltages around 1V (1.2V in IBM 65nm 10LPe process) and, accordingly, the transistors used cannot tolerate such high forming voltages. Hence, during forming, the peripheral circuitry should be properly isolated in order to avoid any damage. Fig 3 depicts the proposed circuit.

The circuit operates in two phases: (1) forming phase and (2) operation phase.

1) **Forming Phase ($\phi1 = \phi2 = 0V$):** In this phase, the transmission gates are turned OFF to isolate pre-neuron and the post-neuron from the forming circuitry. The pre-neuron can be floating at this phase depending on the signals feeding it. On the other side, the post-neuron's input is typically a capacitor that can charge even though the transmission gate is switched off given the long forming duration (it is an RC network that might charge the capacitor depending on the relative values of the time constant and the forming duration). Hence, during forming, all nodes that are in contact with the pre-neuron and the post-neuron have to be protected. Therefore, pull down

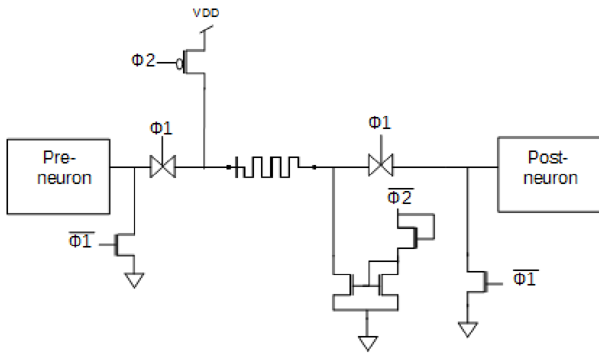

Fig. 3: Proposed On-chip forming circuit

transistors MN1 and MN2 are switched ON to pull these nodes to ground. This way, the proposed solution can also be applied to any general circuit. Finally, during forming, the current mirror represented by M1, M2 and M3 is activated to provide a current limit (current compliance) to the circuit. The current compliance is set to $72\mu A$ in this work based on manufacturer data. Also, the current compliance value plays an important role in determining the LRS as shown in fig 4.

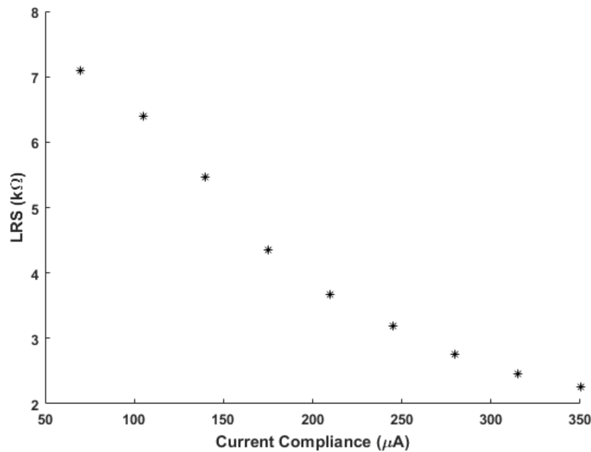

Fig. 4: LRS vs. the current compliance

The VDD used for formation is 3.3V in order to provide voltage higher than 2.3V at node VF and all transistors depicted in the figure are DGXFET transistors available in the 65nm 10LPe process which can operate at 3.3V.

2) Operation Phase **($\phi1 = \phi2 = 3.3V$):** In this phase, The forming transistor MP is turned OFF thereby isolating the 3.3V from the circuit. The current compliance is turned OFF as well as the pull down transistors. Transmission gates are turned ON providing a connection between the pre-neuron, the memristor and the post-neuron.

While transitioning between phases, both the forming circuitry and the transmission gates are ON for a small period of time. While this duration is short, it still results in voltage spikes that might damage the peripheral circuitry. Hence, a non-overlapping clock module is implemented that generates both $\phi1$ and $\phi2$. Fig 5 depicts the non-overlapping clock generator.

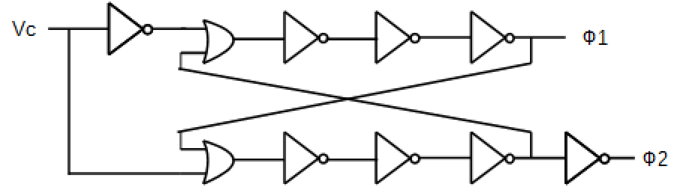

Fig. 5: Non-overlapping clock generator

The number of inverter stages are chosen according to the required non-overlapping time window. Vc is the control signal used for initiating forming.

The proposed design was simulated using Cadence Spectre. Fig 6 depicts the non-overlapping clock signals representing $\phi1$ and $\phi1$.

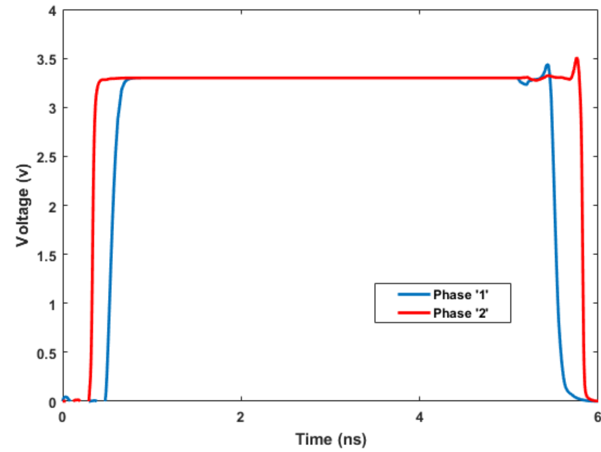

Fig. 6: Non-overlapping clock signals

Fig 7 shows how the VF and the node voltages on the peripheral circuitry behave. The forming phase is the second half cycle where the Vc drops to 0V. It is readily shown that VF well exceeds the 2.3V which provides sufficient voltage for forming while both nodes touching the synaptic buffer and the neuron are pulled down to ground. When Vc is high, the forming circuit is turned OFF and all nodes pick 0.6V which is a floating voltage. Fig 8 depicts the current through the mirror during forming. The current compliance is set at $72\mu A$ and drops to almost zero when the forming is turned OFF. It is readily shown that both currents in M1 and M2 follow each other during the forming phase. The mirror voltage is also plotted which is around $1.27V$.

In order to account for a wide range of pre-forming resistance of the device, a parametric sweep was run over a wide range of resistances ranging from $50k\Omega$ to $5M\Omega$. Fig 9 presents the results of the analysis. It is shown that forming occurs irrespective of the pre-forming resitance and the memristor resistance drops to LRS.

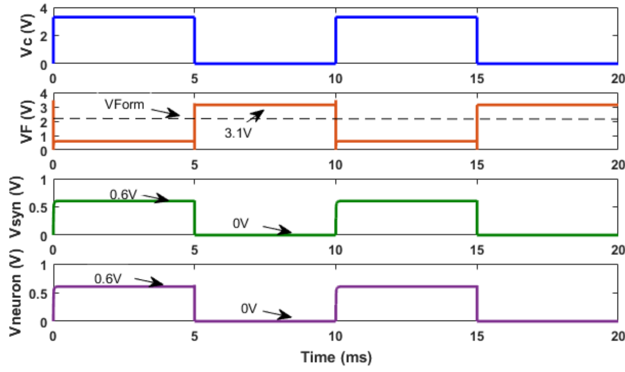

Fig. 7: Critical Voltage nodes during forming

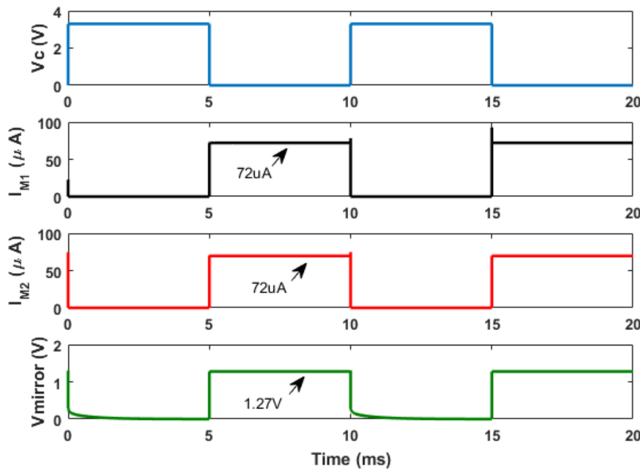

Fig. 8: Current Compliance

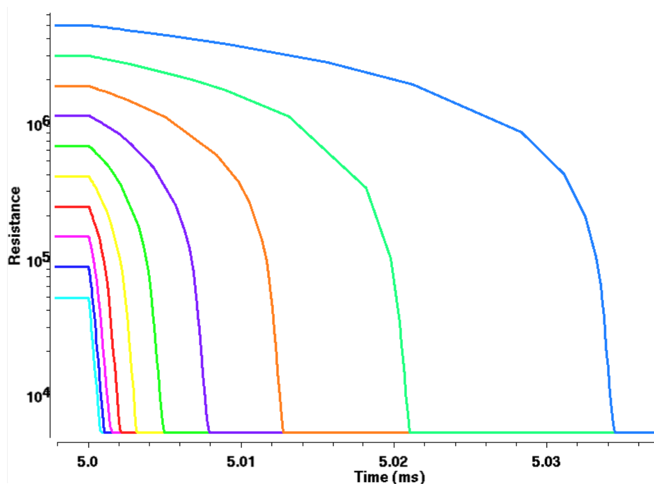

Fig. 9: Parametric analysis run over a wide range of pre-forming resistance values

IV. Conclusions and Discussions

This work highlighted the challenges associated with the design of in-field forming circuits. A method to model forming in Verilog-A was presented through increasing the HRS of the device and simulating for a wide range of resistance values. This method is inspired by the physics of electro-forming that follows a TDDB mechanism. Also, circuit level solutions for in-field forming were provided and simulated with experimentally verified memristor model. It is shown that the high forming voltages of metal-oxide memristor devices requires properly isolating the peripheral circuitry during the forming phase since peripheral circuitry typically operate at relatively lower voltage levels. Design techniques to combat such challenges were presented. Future work should address how to lower forming voltages and develop a more concise and detailed model for electroforming.

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