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Analysis and Modeling of Electroforming in Transition Metal Oxide-based Memristors and its Impact on Crossbar Array Density

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***Abstract*—This work proposes a compact physical model for electroforming in Transition Metal Oxide memristors. The proposed model is based on oxide breakdown statistics and validated against experimental data and Monte Carlo simulations. The model is applied to the problem of area optimization of memristive crossbar array. It is shown that a trade-off exists between the area of the cross-point and the area of the forming circuit. Reduction of the switching layer thickness and/or varying the local field enhancement may result in an appreciable reduction of the forming voltage which, in turn, alleviates the need for forming transistors and yields significant area reduction. On the other hand, these gains might be subdued by scaling the crossbar array itself. The proposed compact model can be used by circuit designers who wish to explore the impact of forming on their crossbar designs and helps with projecting device requirements that are best suited for a particular circuit of interest.**

***Index Terms*—Memristors, ReRAM, Transition Metal Oxide, Forming, Area, Crossbar.**

I. Introduction

TRANSITION Metal Oxide (TMO) memristors [1] have been widely used in memrsitor-based structures such as crossbar arrays. A major challenge in TMOs is the requirement of a one time forming process (also known as electroforming). Electroforming typically requires higher than nominal voltages which bring about significant design challenges [2] and area constraints due to the introduction of in-field forming circuitry which ultimately degrades the density advantage of crossbars. Efforts have been undertaken to lower the forming voltages down to the level of operation voltages. Experimental data has shown successful reduction in the forming voltage with device scaling and/or process parameters such as local field enhancement [3]–[5]. Yet, to the best of the authors' knowledge, little has been done towards modeling the dynamics of this relationship. In [6], the impact of area and thickness scaling of the device switching layer on the forming voltage was studied based on cell based models [7]. In order to provide means for the fast assessment of the impact of forming on memristor-based structures such as crossbar arrays, a compact model for the forming voltage is necessary. In this work, a physical compact model of electroforming in TMOs is proposed. To showcase the utility of the proposed model, the derived model is applied to memristive crossbar arrays.

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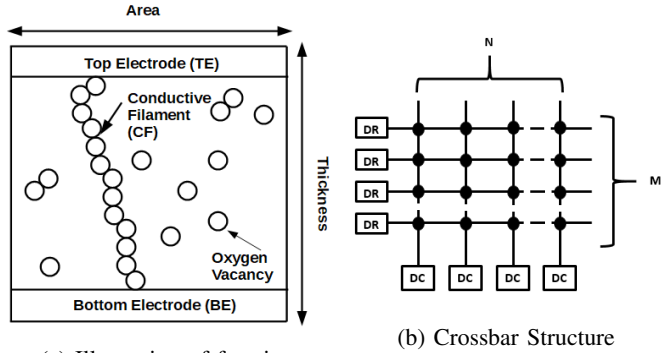

(a) Illustration of forming

(b) Crossbar Structure

Fig. 1: Schematic illustration of forming in (a) and crossbar structure including the forming circuit represented by DR and DC in (b)

II. Forming Voltage model derivation

It was shown in [8] that area dependence of electroforming can be modeled similar to gate oxide breakdown [9] using Poisson statistics as follows:

$$P(k, A) = \frac{(DA)^k}{k!} e^{-DA}, \tag{1}$$

where k is the number of breakdown paths, A is the area of the oxide and D is the density of the breakdown paths. Electroforming follows the weakest link character where formation is accomplished once a single filament is formed between both electrodes [6], [8] as shown in Fig 1a. Hence, prior to forming, no path has yet been formed and, accordingly, one can write:

$$P(D, A) = e^{-DA}, \tag{2}$$

where (2) can be interpreted as the probability of having no percolating path between both electrodes. This picture reinforces the Poisson nature of the breakdown process where if (1) represents the probability that k breakdown paths exist in an area A, then (2) models the area it takes for breakdown to occur which complies with the picture of electroforming where forming is accomplished once a single filament shunts both electrodes. From a reliability modeling stand point, (2) can be interpreted as oxide reliability as a function of area $R(A)$ with parameter D. Hence, one can define Mean Area To Failure (MATF) as the average area it takes for the oxide to break down formally derived as follows:

$$A_f = \int_0^\infty R(A)dA = \int_0^\infty e^{-DA}dA = \frac{1}{D}, \quad (3)$$

where A_f is the MATF. During electroforming, defects are induced based on the applied electric field which can be described according to the following equation [10]–[12]:

$$r = \nu e^{-\frac{(E_A - \alpha E)}{k_b T}} = r_0 e^{K\alpha \frac{V_F}{t_{ox}}}, \quad (4)$$

where K is $1/k_bT$, r is the probability of defect generation, ν is a characteristic probability of generation, E_A is the average activation energy of oxygen vacancy generation, α is a barrier lowering coefficient representing the local field enhancement, E is the applied electric field across the oxide which can be described as the forming voltage divided by the oxide thickness such that $E = V_F/t_{ox}$, k_b and T are the Boltzmann constant and temperature, respectively.

By definition, D is the density of breakdown paths. Hence, D can be viewed as a chain of oxygen vacancies from the top to the bottom electrode whose length is proportional to the oxide thickness and, accordingly, D can be approximated as follows $D \approx r^{t_{ox}}$. The aforementioned picture can be formally described according to Poisson statistics as follows:

$$P(k, dA) \approx \begin{cases} 1 - DdA, & k = 0 \\ DdA, & k = 1 \\ 0, & k > 1 \end{cases} \quad (5)$$

where in any arbitrary area ΔA, multiple paths to ground can exist. However, as ΔA becomes infinitesimally small such that ΔA approaches dA, one path can exist and the Poisson distribution can be approximated according to the above equation. From (3) and (4), one can arrive at the following forming voltage model:

$$A_f = {r_0}^{-t_{ox}} e^{-K\alpha V_F}, \quad (6)$$

or equivalently, $V_F = \frac{ln(1/r_0)}{K\alpha} t_{ox} - \frac{ln(A_f)}{K\alpha}$.

III. Model Validation

In order to verify the validity of the derived model, the proposed model was compared against experimental data drawn from multiple sources in the literature. It is readily shown that the proposed model agrees with the experimental data. Fig 2a validates the model against experimental data in [5] where the linear dependence of the forming voltage on oxide thickness is demonstrated. Fig 2b is based on data drawn from [3] and shows the effect of local enhancement on the forming voltage. Higher local enhancement (often accomplished by structural modification and/or addition of impurities) makes the forming voltage less sensitive to area scaling which is manifested in a flatter V_F vs. A_f relationship. This is captured by the model where boosting the local enhancement reduces the coefficient next to $ln(A_f)$. In Fig 2c, based on [4], model parameters ($1/K\alpha$ and $ln(1/r_0)$) were extracted from $5.2nm$, applied to two other devices with thicknesses $4.4nm$ and $3.4nm$, and compared to experimental observations. A Close match was observed between the proposed model and experimental data.

A Monte Carlo simulation framework was also developed to further validate the derived analytical model. The advantage of numerical simulations is that model parameters are more easily controlled where the impact of each parameter can be evaluated separately holding all other parameters constant. Fig. 4 depicts the Monte Carlo simulation flow. The device is represented by a 2D grid where each location can be either conductive or non-conductive depending on whether a random test number is greater or smaller than the voltage dependent switching probability [10]. In Fig 3a and b, Only device area and thickness were varied. Hence, no change in the slope is observed as predicted by the model. Reduction in the forming voltage is observed with increasing/decreasing device area/thickness. In Fig 3c, only local enhancement was varied. Higher local enhancement makes the forming voltage less sensitive to device area (note that here the curve is steeper for higher local field enhancement because the axes are flipped if compared to the Fig 2).

IV. Effect of forming on the crossbar density

A crossbar structure with M rows and N columns is depicted in Fig 1b where every row and column require a driver DR and DC, respectively. The major challenge with high forming voltage is the requirement of dedicated circuitry during electroforming that is capable of isolating the peripheral circuitry to protect it from high forming voltages and executes forming in-field. This circuitry is represented here via DR and DC. A detailed explanation of the forming circuit can be found in [2]. Also, such devices are typically large compared to the regular devices in order to accommodate high forming voltages. In this case study, we use transistors provided by the 65nm Process Design Kit (PDK) from IBM [13], [14] where DR and DC are DGXFET with minimum length of $0.5\mu m$ so they can tolerate voltages up to $3.3V$. On the other hand, regular FET devices are used for peripheral circuitry with nominal voltage $1.2V$ and minimum length $60nm$. Hence, a forming voltage less than or equal to $1.2V$ can eliminate the need for the sizable DR and DC. The total area of the crossbar is $A_{XBar} = A_{forming} + A_{active}$ such that:

$$A_{forming} = (M + N)A_{DR,DC}U(V_F - 1.2), \quad (7)$$

where $A_{forming}$ is the total area of the forming circuitry, $A_{DR,DC}$ is the area of a single forming driver for every row and column which are assumed equal here for simplicity and $U(V - 1.2)$ is a unit step function to model the fact that the forming circuitry is only required when the forming voltage is higher than the nominal voltage which is $1.2V$ in this study. The values used for $A_{DR,DC}$ are $L = 0.5\mu m$ and $W = 4\mu m$ to provide low series resistance with the memristor device during regular operation since DR and DC are mainly transmission gates with some supporting circuitry. In this estimate, only transmission gates were considered since they scale with the crossbar. The total area of the memristors A_{active} can be modeled as follows:

$$A_{active} = (MN){r_0}^{-t_{ox}} e^{-K\alpha V_F}, \quad (8)$$

It is shown in Fig 5 that using a device with $t_{ox} = 10nm$ might not help reducing the crossbar area since reducing the forming voltage to the level of operation voltages where the

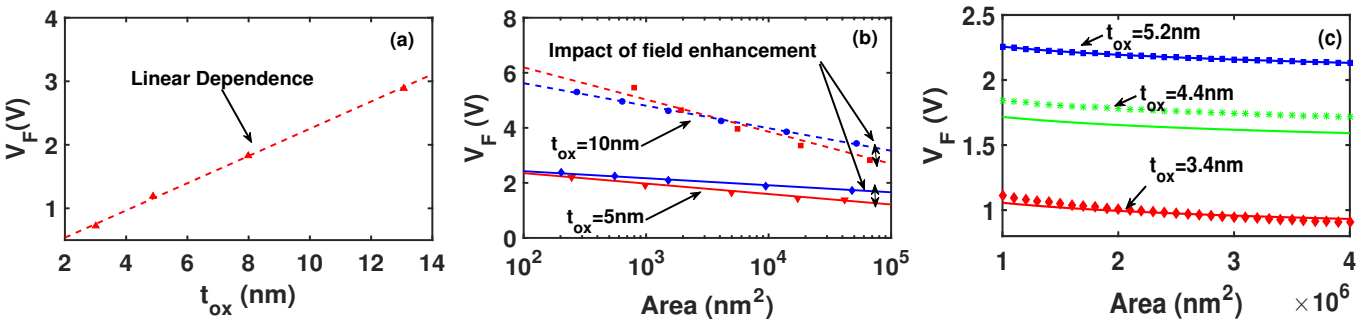

Fig. 2: Model validation against experimental data. (a) shows the linear dependence of the forming voltage on oxide thickness [5].(b) demonstrates the impact of field enhancement [3].(c) compares the model (solid) to experimental data (shapes) [4].

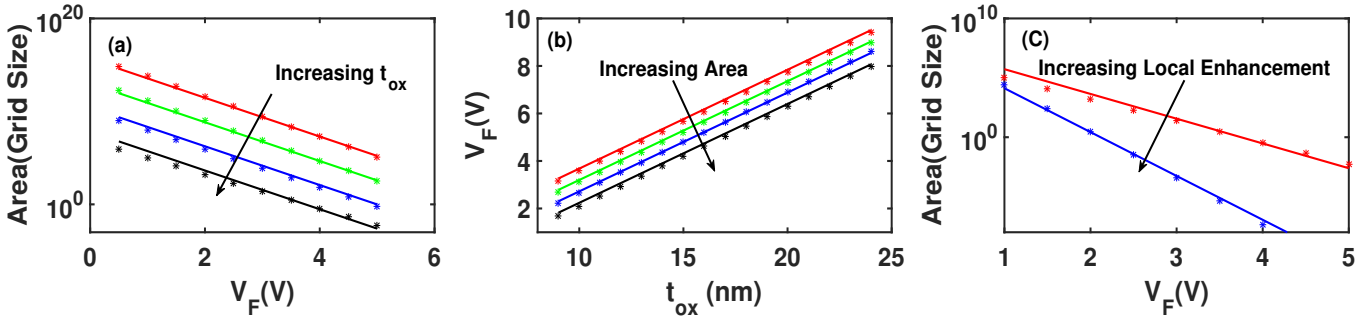

Fig. 3: Model validation (solid) against Monte Carlo simulations (shapes).(a) depicts an exponential decrease in the device area with increasing the forming voltage for various device thicknesses. (b) depicts a linear increase of the forming voltage with device thickness for various areas. (c) shows the impact of field enhancement. Area and thickness are measured by grid size.

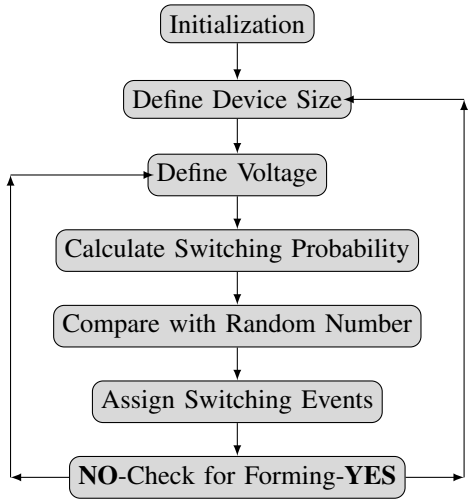

Fig. 4: Monte Carlo Simulation framework.

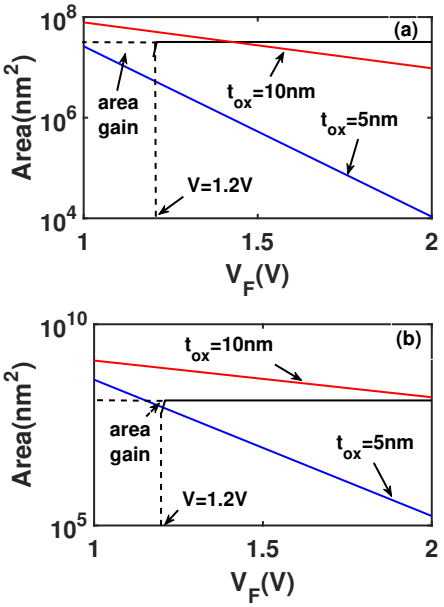

Fig. 5: Impact of thickness on area of the crossbar structure for (a) 4X4 array (b) 16X16 array. The black solid line represents the area of the forming circuit.

forming circuit is not needed requires memristive devices that already consume larger area than the forming circuit. In fact, in this case, it might be better to live with high forming votlages and include a forming circuit. On the other hand, decreasing the device thickness down to $t_{ox} = 5nm$ may result in appreciable area reduction if the forming circuit is removed altogether represented by *area gain* in Fig 5a which can be thought of as the optimum design region for a crossbar with such device parameters. Scaling the crossbar size, however, may subdue these gains since A_{active} scales as MN while $A_{forming}$ scales as $M + N$. This analysis emphasizes the utility of such a closed form model for it can be used to project device requirements for optimum crossbar size.

V. Conclusion

This letter proposes a physical forming model for TMO-based memristors . The model is applied to crossbar arrays and it is shown that there exists a trade-off between the area of the crosspoint and the area of the forming circuit. Thickness scaling may reduce the area of the crossbar array while their effect might be subdued by scaling the crossbar array.

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