A Novel Architecture for Digital Pulse Height Analysis with Application to Radiation Spectroscopy

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Abstract

A novel digital approach to real-time, high-throughput, low-cost pulse height analysis (PHA) for radiation spectroscopy is presented. The analog nuclear signal is sampled at a high rate using an analog-to-digital converter (ADC), and analyzed by a state-of-the-art field programmable gate array (FPGA). A customized fixed-point polynomial fitting algorithm is utilized for pulse-height estimation. Other pulse parameters, such as width and asymmetry, are attainable for pulse shape analysis (PSA) purposes, such as particle identification. The mathematical complexity of the algorithm is strongly reduced by applying parallel arithmetic, resulting in complete elimination of processing dead-time. The proposed scheme is easily scalable by substituting the FPGA and ADC with more advanced integrated circuits as they appear.

1. Introduction

Recent research in the field of digital signal processing for nuclear spectroscopy has yielded various pulse height analysis (PHA) techniques (Jordanov *et al.*, 1993; Simoes *et al.*, 1995). Despite many advantages of using fully digital systems, frequently the high processing requirements bound overall performance in terms of counting rate and effective resolution. Most suggested solutions utilize expensive floating-point digital signal processors (DSP) to overcome these limitations (Simoes *et al.*, 1995; Simoes *et al.*, 1996).

Improvements in analog-to-digital converters along with advances in programmable logic integrated circuits allow for new real-time digital pulse processing techniques to be introduced. In this paper we describe such a technique, based on a state-of-the-art field programmable gate array (FPGA) as the main processing unit performing high-speed arithmetic calculations. The pulse height is estimated using polynomial fitting optimized to exploit the advantages of customized logic design. Utilization of the customized logic renders a real-time, no dead-time, high performance and highly scalable solution for PHA, without the requirement of an expensive DSP. The method can easily be exercised in other nuclear spectroscopy applications.

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2. The proposed system

The proposed board houses a 12-bit high-sampling-rate analog-to-digital converter (ADC), a field programmable gate array (FPGA), peripheral analog components, an embedded micro-controller with external memory and connection to a desktop PC. Accounting the specifications of currently available components, and assuming pulse-width of 5 μsec, a global system clock of 16 MHz is suggested. VHDL (VHSIC hardware description language) code was written and optimized for the characteristic features of the FPGA architecture. Using the VHDL code, logic-level simulation and gate-level synthesis were performed for determining the estimated performance and hardware required. Figure 1 depicts a block diagram of the suggested setup.

The analog signal is continuously sampled by the ADC with an effective resolution of 10 bits per sample. The same clock also drives the FPGA, which directly receives the samples and performs real-time peak detection followed by fitting of the pulse peak with a second order polynomial expression. Calculations are carried out by customized logic executing parallel fixed-point arithmetic operations. The estimated pulse heights are transferred to the micro-controller, which in-turn accumulates and transfers the data to a PC station for further analysis and graphical display.
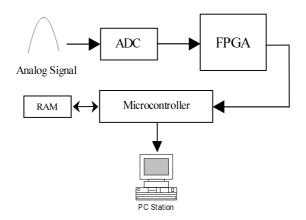

Fig. 1: Simplified diagram of the pulse height analysis system.

3. Fitting model arithmetic calculations

In order to estimate the pulse height we need to correctly model the pulse peak. A second order polynomial expression provides a good approximation to the peak of a Gaussian function. Resulting from empirical study, which took into account the system characteristics mentioned above, a set of 28 samples surrounding the pulse-peak was found optimal.

Let us express the pulse peak model as:

$$f(x) = ax^2 + bx + c, \qquad (1)$$

where x is the discrete time variable. The goal is to determine the model parameters a, b and c from which the pulse height may be estimated.

Applying a least-square-error technique, we are interested in minimizing the error,

$$\varepsilon = \sum_{i=-L}^{H} \left[f(x_i) - y_i \right]^2 \qquad (2)$$

where L and H define the lower and upper index values, respectively and y_i represents the ith sample, by solving the following equations:

$$\frac{\partial \varepsilon}{\partial a} = 0, \quad \frac{\partial \varepsilon}{\partial b} = 0, \quad \frac{\partial \varepsilon}{\partial c} = 0 \qquad (3)$$

which, expressed in matrix form, yields the following linear set of equations:

$$\begin{bmatrix} m_{2,1} \\ m_{1,1} \\ m_{0,1} \end{bmatrix} = \begin{bmatrix} m_{4,0} & m_{3,0} & m_{2,0} \\ m_{3,0} & m_{2,0} & m_{1,0} \\ m_{2,0} & m_{1,0} & m_{0,0} \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix} \qquad (4)$$

A moment is defined as:

$$m_{i,j} = \sum_{k=-L}^{H} x_k^i y_k^j \qquad (5)$$

Moments $m_{i,0}$ depend only on the sample time-locations, hence they are determined beforehand and stored in the FPGA memory. The rest of the moments, which depend on the sample values as well as their locations, are calculated each clock cycle. The liberty of choosing a time scale x_k was taken in order to simplify the implementation. By selecting summation limits that are symmetrical with respect to $t=0$, we derive that $L=H$ and consequently $m_{i,0}=0$, for odd i values. Let us define $m^+_{i,j}$ as the moment sequentially following $m_{i,j}$. Calculating $m^+_{i,j}$ is achieved by using the following recursive relation:

$$\begin{aligned} m_{i,1}^+ &= \sum_{k=-L}^{H} k^i y_{k+1} \\ &= \sum_{k=-L+1}^{H+1} (k-1)^i y_k = \\ &= \sum_{k=0}^{i} \binom{i}{k} (-1)^k m_{i,1} + y_{H+1} H^i - y_{-L} (-L-1)^i \end{aligned} \qquad (6)$$

For ease of implementation, and as an outcome of experimental study, we choose $H=L=14$. Consequently, two goals are achieved: (1) coefficients of the summation operation are factors of 2 that may be easily calculated and (2) moments with an odd i index nullify due to the symmetry. By substituting the above definitions in expression (4) we are left with the following equation for the maximal value of $f(x)$:

$$y_{peak} = C_1 \frac{m_{1,1}^{2}}{m_{2,1} - C_4 m_{0,1}} + C_3 m_{0,1} - C_2 m_{2,1} \qquad (7)$$

where the constants are defined as:

$$n = L + H + 1 = 29$$

$$C_1 = \frac{m_{4,0} n - m_{2,0}^2}{4 m_{2,0}^2 \cdot n} \tag{8}$$

$$C_2 = \frac{m_{2,0}}{m_{4,0} n - m_{2,0}^2}$$

$$C_3 = \frac{m_{4,0}}{m_{4,0} n - m_{2,0}^2}$$

$$C_4 = \frac{m_{2,0}}{n}$$

As can be seen in equation (7), calculating the pulse height requires only 5 multiplication operations and a single division, since the constants are calculated *a-priori*. We utilized a division operator and two concurrent multiplication operators in order to obtain real-time processing. Table 1 describes a scheduling diagram of the peak height calculations (equation 6) utilizing these resources. Common techniques for reducing the differential non-linearity effects of the ADC may be applied prior to the fitting algorithm described in this paper.

<div align="center">Time Step</div>

	t_0	t_1	t_2
1st Multiplier	$m_{1,1}^2$	$C_1 m_{1,1}^2$	$C_2 m_{2,1}$
2nd Multiplier	$C_4 m_{0,1}$	$C_3 m_{0,1}$	No Operation
Divider	No Operation	No Operation	$\dfrac{C_1 m_{1,1}^2}{m_{2,1} - C_4 m_{0,1}}$

<div align="center">Table 1: Peak height arithmetic calculations schedule.</div>

4. The pulse analysis architecture

As illustrated in Figure 2, tracking the signal behavior is comprised of the following four phases:
1. Detecting initial crossing of a predefined threshold that indicates the existence of a pulse.
2. Determining the location of the pulse peak.
3. Detecting pulse end point by a crossing of the predefined threshold.
4. Measuring the time interval between the beginning and end points of the pulse and confirming it is within the anticipated boundaries.

Processing the sampled pulse consists of several concurrently executed stages as shown schematically in Figure 3.
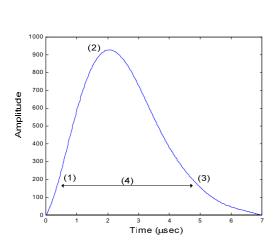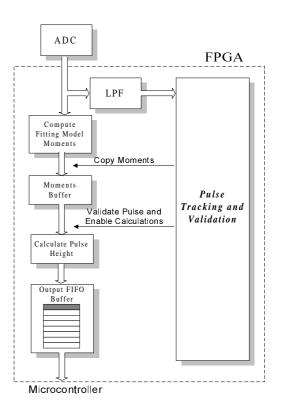

Fig. 2: Pulse tracking and validation phases

Fig. 3: Block diagram of the pulse processing architecture

A primary module is responsible for correct detection, tracking and validation of the pulse. As a result, processing of noise and corrupted pulses is avoided. Consequently, it is the responsibility of this module to manage other modules via designated control lines. A flowchart describing the primary model is given in Figure 4.

The ADC and FPGA are synchronized using a local oscillator operating at 16 MHz. With each clock cycle the ADC produces a new sample. A digital low-pass infinite impulse response (IIR) filter is applied to the signal before it is transferred to the pulse tracking and detection module. The filter coefficients were restrained to simple binary shifting arithmetic operations requiring only 5 adders and 4 registers.
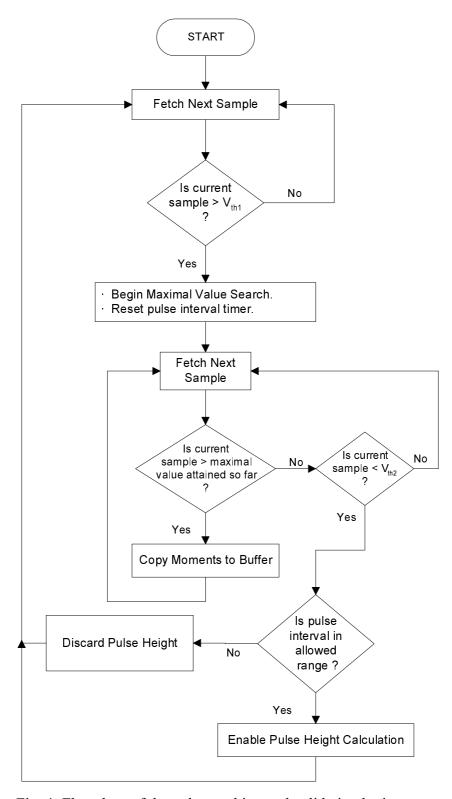
Fig. 4: Flowchart of the pulse tracking and validation logic

The transfer function of the digital low-pass filter applied is:

$$H(z) = \frac{\frac{1}{8} + \frac{1}{4}z^{-1} + \frac{1}{8}z^{-2}}{1 - \frac{3}{4}z^{-1} + \frac{1}{4}z^{-2}} \tag{9}$$

The frequency domain characteristics of this filter are an approximation to those of a second order Butterworth low-pass filter with a cut-off frequency at 2.5 MHz (Ifeachor *et al.,* 1993). Using simple *O(n)* shift-and-add type multipliers and *O(n)* subtractive binary division operator (Waser *et al.*, 1982). Applying this filter removes high-frequency noise and renders more robust decision-making. Figure 5 depicts the frequency-domain response of the filter.
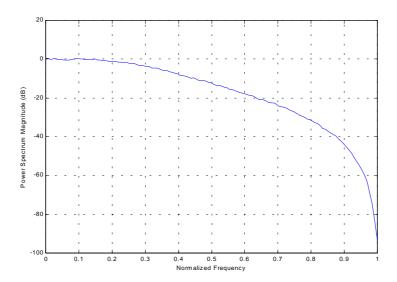

Fig. 5: Frequency response of the digital low-pass filter.

For each incoming sample, a module calculates the fitting model moments using the recursive formula (equation 6) described earlier. At the point where a new maximal value is detected a duplicate of the moments is made in a designated buffer. Upon detecting a sample smaller than the predefined threshold pulse termination is assumed. Providing the pulse is within the expected time interval, a signal is enabled and height calculation commences after which the estimated height is transferred to the output buffer. If the pulse interval is shorter or longer than expected, the estimated height is discarded. This criterion functions as a simple pile-up rejection mechanism.

Since the pulse height calculation module operates independently, processing of the next pulse may begin prior to the completion of calculation, thus eliminating potential dead time. This way, pulse height calculations may last the duration of an entire pulse before dead time circumstances occur. The estimated pulse height is passed on to the output buffer, which collects values and delivers them to the micro-controller. Utilizing a buffer eases the timing requirements from the micro-controller.

5. Simulation results

The nuclear pulses assumed are shaped with a width of approximately 5.5 µsec as illustrated in Figure 2. Using the arithmetics discussed earlier, complete peak height calculation was achieved in 54 clock cycles, which is approximately 3.2 µsec. It is possible to further reduce calculation time by applying more efficient arithmetic techniques that typically require additional memory. Since pulse width is roughly 5 µsec, we found no need to utilize such techniques.

Using a mathematical model for nuclear pulses, a broad range of peaks has been synthesized. In order to make the simulations as accurate as possible, typical white Gaussian noise has been added to each synthesized pulse, free running clock was exercised and quantization error was applied. Three alternative pulse height estimation techniques were examined using Monte Carlo simulation: (a) simple maximal value search, (b) digital low-pass filtering followed by maximal value search and (c) the proposed polynomial fitting technique. Table 2 summarizes the peak estimation accuracy attained using each the three methods, where the error is expressed in terms of the mean square error (in channels).

PHA Method	Simple Max Search	Max Search with LPF	Polynomial Fitting
Error Variance (Channels)	6.05	4.18	1.82

Table 2: Peak height estimation error using simple max search, max search with digital filtering and polynomial fitting

The simple maximal value search method is highly sensitive to additive noise, which accounts for the relatively poor performance of this method. Suppressing the effect of noise by applying the low-pass filter improved the results by over 35 percent. It should be noted that the digital filter is intended to suppress interference contributed by the digital circuitry. Using analog low-pass filter prior to entering the ADC eliminates analog noise, since the ability to digitally filter this noise is limited by the ADC's sampling frequency. As expected, the polynomial fitting technique further improved the estimation results.

6. Conclusions

A fully digital, high-throughput, no calculation dead-time PHA technique has been presented. An FPGA has been considered for performing hardware-efficient pulse height estimation. The low-cost, high-scalability and low-complexity resulting from the customized hardware design, maintains a substantial advantage over more expensive DSP-based solutions. Analog preprocessing including amplifying, shaping and discrimination of the signal may be combined with the suggested technique to render a complete PHA system. Faster ADC and FPGA devices will allow for improvement of resolution and enhance the ability to capture shorter pulses without the need to modify

the PHA algorithm. Current study focuses on combining noise suppression and more efficient pile-up rejection techniques with the proposed PHA method, as well as applying the method to multi-width nuclear pulses. We anticipate extensive utilization of custom solutions in the field of digital nuclear spectroscopy.

References

Ifeachor, E. C., and B. W. Jervis (1993). *Digital Signal Processing: A Practical Approach*, Addison-Wesley, New York.

Jordanov, V., and G. F. Knoll (1993). "Digital Pulse Processor Using A Moving Average Technique," *IEEE Trans. Nucl. Sci.*, **40**, no. 4, pp. 764-769.

Simoes, J. B., P. C. P. S. Simoes, and C. M. B. A. Correia (1995). "Nuclear Spectroscopy Pulse Height Analysis Based on Digital Signal Processing Techniques," *IEEE Trans. Nucl. Sci.,* **42**, no. 4, pp. 700-704.

Simoes, P. C. P. S., J. C. Martins, and C. M. B. A. Correia (1996). "A New Digital Signal Processing Technique for Applications in Nuclear Spectroscopy," *IEEE Trans. Nucl. Sci.*, **43**, no. 3, pp. 1804-1809.

Waser, S., and M. J. Flynn (1982). *Introduction to Arithmetic for Digital Systems Designers*, Holt, Rinehart and Winston, New York.