A FLEXIBLE ATM TRAFFIC SYNTHESIZER FOR EVALUATING HIGH-PERFORMANCE PACKET-SWITCHED NETWORKS

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Abstract: *High-speed routers and switches are required to support both high throughput as well as provision of quality-of-service (QoS) requirements. The diversified characteristics of Internet traffic complicates the process of efficiently modeling the flow statistics and evaluating the performance of scheduling algorithms, which are at the core of switches and routers. In this paper an ATM analyzer, which supports data rates of oc-12 (622 Mbps), is presented. The system allows a wide range of traffic flows to be synthesized, transmitted to an optical switching fabric and analyzed upon reception. Utilizing a combined hardware and software custom design, several key network parameters are obtained including mean cell delay, cell delay variation and cell loss rate. A prototype system has been designed, built and successfully tested.*

KEYWORDS: ATM Traffic Modeling, Traffic Engineering, Switching Performance

INTRODUCTION

Analyzing and quantifying the performance of high-speed switches and routers is becoming a paramount issue, particularly in the context of the rapidly growing Internet infrastructure. Regardless of the switching technology and switch fabric there is a necessity for tools that can determine the traffic flow statistical parameters to evaluate the switches and routers performance. Such metrics include the maximal throughput, the mean cell delay, cell delay variance and cell loss rate. Advanced communications protocols, such as ATM and IPv6, support a wide range of quality-of-service (QoS) parameters that are predefined over an allocated channel. Determining switch performance becomes more significant with the growing demand for guaranteed QoS [1], [2] in applications such as voice and video.

Wavelength division multiplexing (WDM) is widely accepted as the physical-layer solutions for future broadband networks. While reliable WDM-based Tbit/sec point-to-point communication has been demonstrated, switch architectures that can efficiently manage the extensive amounts of diversely characterized traffic loads are still investigated. In this paper a real-time ATM Analyzer system designed and built for synthesizing ATM traffic at rates of up to 622 Mb/sec and measuring QoS performance of such high-performance switches and routers is presented. The system is based on a state-of-the-art FPGA performing real-time traffic synthesis and statistical data collection. By modeling off-line and processing the modeled information through the system, a large degree of flexibility is offered yielding credible examination of modern switching devices.

1. SYSTEM ARCHITECTURE

1.1 Hardware layout

As depicted in figure 1, the traffic analysis system consists of a PC workstation running dedicated software, 4 ATM traffic processor cards (ATPC) and a Utopia-II/SONET conversion card with bi-directional links to the switch fabric. Dedicated PC software allows a wide range of traffic characteristics to be defined for synthesis at the ATPC. Upon establishing the required traffic, commands are sent to the ATPC via dedicated high-speed serial links. Each ATPC has the following three objectives which are performed in real-time:

(1) Receive traffic synthesis commands issued by the PC
(2) Traffic synthesis – generate ATM traffic at rates of up to 622 Mbps in accordance with prescribed commands originating from the PC software.
(3) Analyze traffic statistics, by examining data received from the other ATPC, and generate and transmit to the PC switching performance metrics.

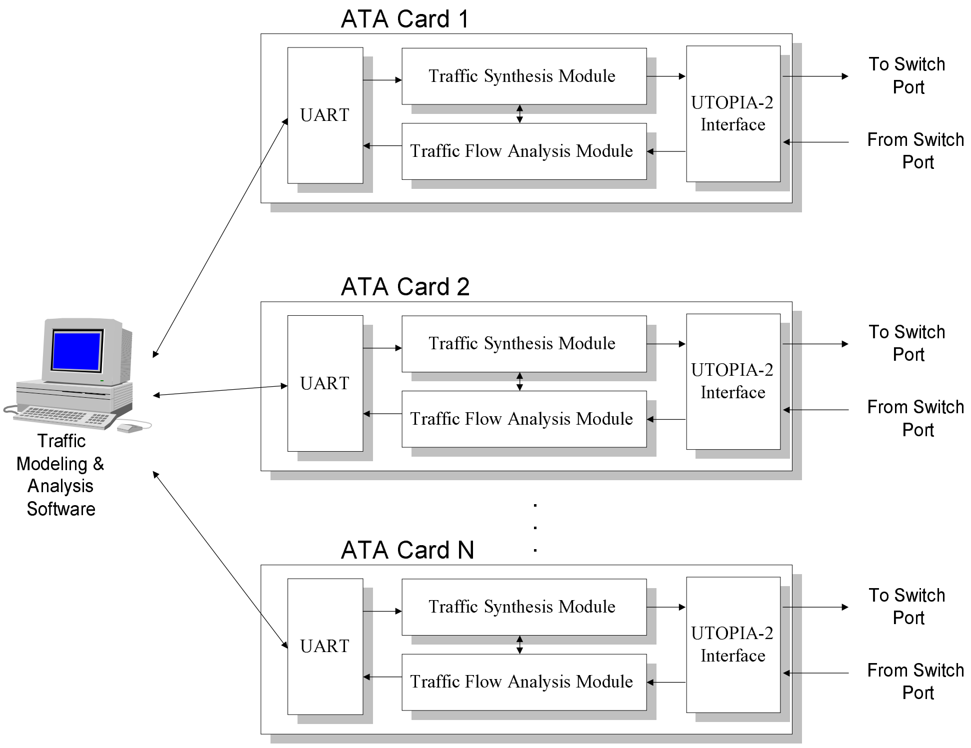

Figure 1: ATM Analyzer System Layout

Figure 2 shows a picture of the ATPC. The functionality of the ATPC is performed by a custom logic design implemented on a state-of-the-art Field Programmable Gate Array (FPGA) running at 50 MHz. Dedicated input and output lines were incorporated to support the Utopia-2 interface and other required signals. The logic design was written in VHDL and synthesized for the specific FPGA.

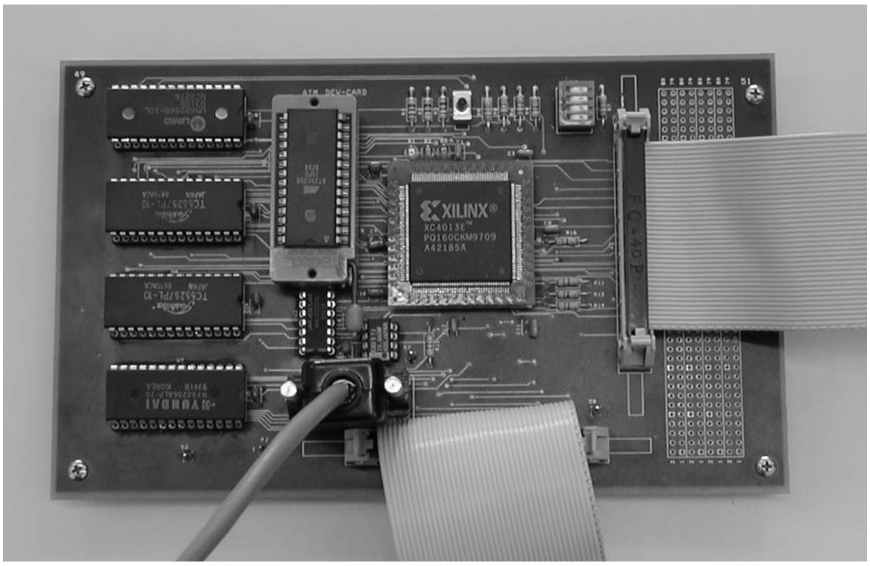

Figure 2: The ATM Traffic Processor Card (ATPC)

1.2 Traffic Synthesis Engine

In order to maximize the flexibility and diversity in generating ATM traffic cells, the PC issues the ATPC, via the high-speed serial link, a high rate of traffic synthesis commands. Each command consists of three fields: bitrate, destination probability distribution and cell arrival process. Traffic synthesis commands are issued in time slots of 1 msec in duration. Time slot resolution directly affects the cell flow granularity. The bitrate parameter determines the aggregated load that is generated during a time slot, while the destination probability distribution describes the relative share of traffic each destination receives. By selecting different bitrate and destination distributions a wide range of traffic models, such as aggregated MPEG video flows, can be generated.

In addition, the two primary criteria that strongly affect switching performance are the packet arrival statistics and destinations distribution. Typically, it is assumed that arriving packets obey a binomial process and are uniformly distributed to all destinations. Since current high-speed routers and switches are limited to an aggregated capacity of two hundred Gbit/sec, it is difficult to predict how valid will these assumptions be in future multi-Tbit/sec interconnections. The simplest traffic load model consists of a Bernoulli i.i.d.

(independent identical distribution) arrival pattern whereby cell destinations are uniformly distributed. According to the Binomial distribution model, the probability of k packets arriving during n cell slots is given by:

$$P\{k\} = \frac{n!}{k!(n-k)!} p^k q^{n-k} \qquad (1)$$

where at each cell time there is a probability p that a cell will arrive, and a probability q=1-p that no cell arrives. It is well known that real-life traffic tends to burstiness due to the prevalence of modern multi-media applications such as compressed video and sound. Many models of bursty traffic have been proposed. In our synthesizer, a cell arrival process parameter is used, which allows for either Bernoulli process or an on-off arrival process modulated by a two-state Markov chain to characterize traffic generation. The result is a train of bursty cell arrivals, each containing cells with identical destination, followed by periods of empty cell slots. The expression for the mean offered load under such bursty traffic is:

$$\text{O}\mathit{fferd\ Load} = \frac{q}{p+q} \qquad (2)$$

where p and q are the transition probabilities with regard to the active and idle periods, respectively. Due to the geometric distribution of the duration of active and idle periods, the mean burst length is $1/p$.

Besides the bursty arrival characteristics, real-life traffic destinations are not uniformly distributed; traffic tends to be focused on “preferred” or “popular” destinations. Unfortunately, the performance of many scheduling algorithms degrades under non-uniform traffic conditions, where not all queues are evenly and heavily loaded. Maximum matching algorithms are known to perform poorly and cause queue starvation under these conditions. We introduce here a destination distribution model named Zipf's law. The Zipf law was proposed by G. K. Zipf [3]-[5]. The Zipf law states that frequency of occurrence of some events (P), as a function of the rank (i), where the rank is determined by the above frequency of occurrence, is a power-law function: $P_i \sim 1/i^k$, with the exponent k close to unity.

The most famous example of Zipf's law is the frequency of English words in a given text. Most common is the word "the", then "of", "to" etc. When the number of occurrence is plotted as the function of the rank (i=1 most common, i=2 second most common, etc.), the functional form is a power-law function with exponent close to 1. It was shown that many natural and human phenomena such as Web access statistics, company size and biomolecular sequences all obey the Zipf law with k close to 1. We use the Zipf distribution to model packet destination distribution. The probability that an arriving packet is heading destination i is given by:

$$Zipf(i) = \frac{\frac{1}{i^k}}{\sum_{j=0}^{N} \frac{1}{j^k}} \quad (3)$$

where i is the packet destination, k is the Zipf order and N is the system order, i.e., the number of switch ports.

While $k = 0$ represents uniform distribution, as k increases the distribution becomes more biased towards preferred destinations. In order to generate a stable and realistic traffic model, the average steady-state load at each input port must not exceed 100%. Similarly, the average steady-state aggregated traffic flows arriving from all input ports to any destination port must not exceed 100%. Random traffic is synthesized based on internal pseudo-random generators running at the system clock rate. Cells received at each ATPC are analyzed. Statistical metrics such as the mean cell delay and cell delay variation are obtained by comparing synchronized time stamps issued by the transmitting ATPC.

2. CORE ANALYSIS SOFTWARE

The software running on the PC station provides a graphical user interface for issuing traffic synthesis commands and receiving statistical data regarding performance. Two types of messages are periodically sent from the ATPCs: traffic synthesis messages and traffic analysis messages. The traffic synthesis messages embody information regarding the number of cells transmitted to each of the destinations (ATPCs) during each time slot. Traffic analysis messages summarize the mean cell delay, cell delay variance and cell loss. Data collected during a simulation interval can be stored for further off-line analysis. Figures 3 presents the ATM analyzer software user interface, including the parameter values of the received as compared to the transmitted ATM data. The QoS parameters are derived accordingly. Figure 4 presents an example of a bursty synthesized messages versus time as transmitted to four different destinations.

Employing off-line traffic modeling, which can incorporate various multi-media and other QoS demanding applications, and translating these models to 1 msec “bins” yields a powerful traffic synthesis engine. In fact, any traffic model that can efficiently be partitioned into 1 msec segments without significantly impairing modeling information may be employed. The software allows for the definition of CBR, VBR and UBR traffic of various characteristics to be appended at any instance during the simulation. Incoming traffic flows are visually displayed next to the associated QoS switching statistics.

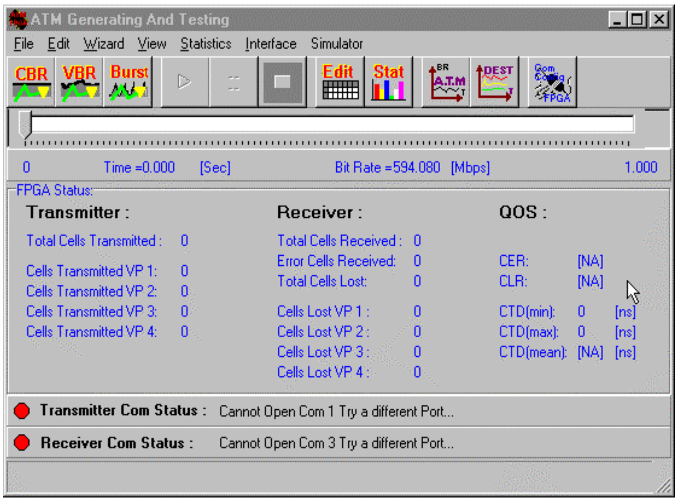

Figure 3. ATM analyzer software user interface

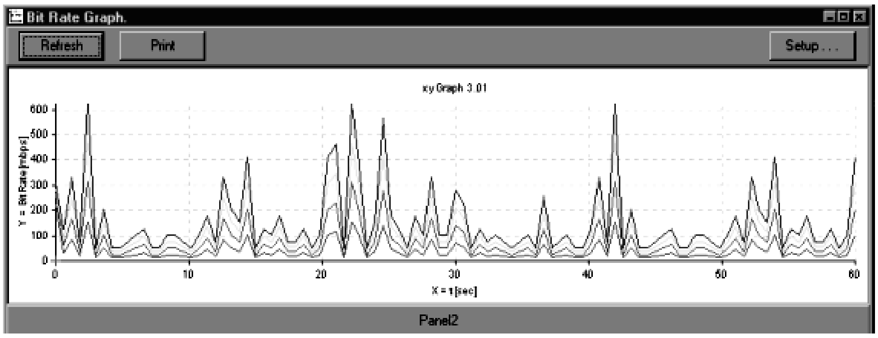

Figure 4. Example of synthesized traffic; instantaneous bit-rate (Mbit/sec) versus time for four different destinations

3. SUMMARY

A flexible hardware and software system for generating diverse ATM traffic flows and measuring the switching performance of an examined switch architecture has been presented. By defining the offered load, destination distribution and cell arrival process in each 1 msec period, a wide range of complex traffic flows, such as aggregate multi-media traffic, can be generated in real-time. Utopia-2 interface is employed for conformance with standard ATM switch components. Based on the proposed system, switches and routers accommodating large port densities may be examined as means of evaluating performance of the switching fabric.

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